



2Ω, Quad, SPST, CMOS Analog Switches

MAX4677/MAX4678/MAX4679

General Description

The MAX4677/MAX4678/MAX4679 quad analog switches feature 1.6Ω max on-resistance (RON) when operating from a dual ±5V supply. RON is matched between channels to 0.3Ω max and is flat (0.4Ω max) over the specified signal range. Each switch can handle Rail-to-Rail® analog signals. Off-leakage current is 0.1nA at +25°C. These switches are ideal in low-distortion applications and are the preferred solution over mechanical relays in automated test equipment. They have low power requirements, require less board space, and are more reliable than mechanical relays.

The MAX4677 has four normally closed (NC) switches, and the MAX4678 has four normally open (NO) switches. The MAX4679 has two NC and two NO switches and features guaranteed break-before-make switching.

The MAX4677/MAX4678/MAX4679 operate from either a single +2.7V to +11V or dual ±2.7V to ±5.5V supplies, making them ideal for use in digital card applications and single-ended 75Ω systems.

These devices feature a separate logic supply input that operates from +2.7V to V+, allowing independent logic and analog supplies.

Applications

Reed Relay Replacement	Avionics
Test Equipment	ADC Systems
Communications Systems	Data-Acquisition Systems
Audio Signal Routing	PBX/PABX Systems

Features

- ◆ On-Resistance 1.6Ω max
- ◆ On-Resistance Flatness 0.4Ω max
- ◆ On-Resistance Matching 0.3Ω max
- ◆ Dual ±2.7V to ±5.5V or Single +2.7V to +11V Supply Range
- ◆ TTL/CMOS-Logic Compatible
- ◆ Crosstalk -84dB at 1MHz
- ◆ Off-Isolation -65dB at 1MHz
- ◆ -3dB Bandwidth: 66MHz
- ◆ Rail-to-Rail Signal Range

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4677EUE	-40°C to +85°C	16 TSSOP
MAX4677EPE	-40°C to +85°C	16 DIP
MAX4678EUE	-40°C to +85°C	16 TSSOP
MAX4678EPE	-40°C to +85°C	16 DIP
MAX4679EUE	-40°C to +85°C	16 TSSOP
MAX4679EPE	-40°C to +85°C	16 DIP

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW

DIP/TSSOP MAX4677	
LOGIC	SWITCH
0	ON
1	OFF

DIP/TSSOP MAX4678	
LOGIC	SWITCH
0	OFF
1	ON

DIP/TSSOP MAX4679		
LOGIC	SWITCHES 1, 4	SWITCHES 2, 3
0	OFF	ON
1	ON	OFF

SWITCHES SHOWN FOR LOGIC "0" INPUT



2Ω, Quad, SPST, CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

V+ to GND	-0.3V to +12V	Continuous Power Dissipation (T _A = +70°C) 16-Pin Plastic DIP (derate 10.5mW/°C above +70°C)..842mW 16-Pin TSSOP (derate 5.7mW/°C above +70°C).....457mW
V- to GND	+0.3V to -12V	
V+ to V-	+12V	Operating Temperature Range
V _L , IN ₋ to GND (Note 1)	-0.3V to (V+ + 0.3V)	-40°C to +85°C
V _{COM-} , V _{NC-} , V _{NO-} (Note 1)	V- to V+	Storage Temperature Range
Current (any terminal)	±50mA	-65°C to +150°C
Continuous Current (COM ₋ , NC ₋ , NO ₋)	±100mA	Junction Temperature
Peak Current (COM ₋ , NC ₋ , NO ₋ pulsed at 1ms 10% duty cycle)	±200mA	+150°C
		Lead Temperature (soldering, 10s)
		+300°C

Note 1: Signals on NC₋, NO₋, COM₋, or IN₋ exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +5V ±10%, V- = -5V ±10%, V_L = +2.7V to V+, GND = 0, V_{IH} = +2.4V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
ANALOG SWITCH							
Input Voltage Range	V _{COM-} , V _{NO-} , V _{NC-}		V-		V+	V	
On-Resistance	R _{ON}	V+ = 4.5V, V- = -4.5V, I _{COM-} = 50mA, V _{NO-} or V _{NC-} = ±3.3V	T _A = +25°C	1.2	1.6	Ω	
			T _A = T _{MIN} to T _{MAX}		2		
On-Resistance Match Between Channels (Note 3)	ΔR _{ON}	V+ = 4.5V, V- = -4.5V, I _{COM-} = 50mA, V _{NO-} or V _{NC-} = ±3.3V	T _A = +25°C	0.2	0.3	Ω	
			T _A = T _{MIN} to T _{MAX}		0.5		
On-Resistance Flatness (Note 4)	R _{FLAT}	V+ = 4.5V, V- = -4.5V, I _{COM-} = 50mA, V _{NO-} or V _{NC-} = ±3.3V, 0	T _A = +25°C	0.2	0.4	Ω	
			T _A = T _{MIN} to T _{MAX}		0.5		
NC ₋ or NO ₋ Off-Leakage Current (Note 5)	I _{N(OFF)}	V+ = +5.5V, V- = -5.5V, V _{NO-} or V _{NC-} = ±4.5V, V _{COM-} = ∓4.5V	T _A = +25°C	-1	0.1	1	nA
			T _A = T _{MIN} to T _{MAX}	-10		10	
COM ₋ Off-Leakage Current (Note 5)	I _{COM(OFF)}	V+ = +5.5V, V- = -5.5V, V _{NO-} or V _{NC-} = ±4.5V, V _{COM-} = ∓4.5V	T _A = +25°C	-1	0.1	1	nA
			T _A = T _{MIN} to T _{MAX}	-10		10	
COM ₋ On-Leakage Current (Note 5)	I _{COM(ON)}	V+ = +5.5V, V- = -5.5V, V _{COM-} = ±4.5V, V _{NO-} or V _{NC-} = ±4.5V or floating	T _A = +25°C	-2	0.2	2	nA
			T _A = T _{MIN} to T _{MAX}	-25		25	
LOGIC INPUT							
Input Logic High	V _{IH}	V _L = V+		2.4		V	
Input Logic Low	V _{IL}	V _L = V+			0.8	V	
Input Leakage Current	I _{IN}	V _L = V+		-1	0.005	1	μA

2Ω, Quad, SPST, CMOS Analog Switches

MAX4677/MAX4678/MAX4679

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +5V ±10%, V- = -5V ±10%, VL = +2.7V to V+, GND = 0, VIH = +2.4V, VIL = +0.8V, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Positive Supply Voltage	V+		+2.7		+5.5	V
Negative Supply Voltage	V-		-2.7		-5.5	V
Logic Supply Voltage	VL		2.7		V+	V
Positive Supply Current	I+	IN_ = GND or VL		0.001	1	μA
Negative Supply Current	I-	IN_ = GND or VL			-1	μA
Logic Supply Current	IL	IN_ = GND or VL			1	μA
Ground Current	IGND	IN_ = 0 or V+, V+ = 5.5V, V- = -5.5V			1	μA
DYNAMIC						
Turn-On Time	tON	V+ = +4.5V, V- = -4.5V, VNC_ or VNO_ = ±3.3V, VL = V+, Figure 2	TA = +25°C	200	350	ns
			TA = TMIN to TMAX		500	
Turn-Off Time	tOFF	V+ = +4.5V, V- = -4.5V, VNC_ or VNO_ = ±3.3V, VL = V+, Figure 2	TA = +25°C	110	150	ns
			TA = TMIN to TMAX		350	
Break-Before-Make Delay	tBBM	Figure 3, MAX4679 only, RL = 300Ω, CL = 35pF	5			ns
Charge Injection	Q	RGEN = 0, CL = 1nF, VGEN = 0, Figure 4		85		pC
Off-Isolation	VISO	RL = 50Ω, CL = 5pF, f = 1MHz, Figure 5a		-65		dB
Crosstalk		RL = 50Ω, CL = 5pF, f = 1MHz, Figure 6a		-84		dB
-3dB Bandwidth	BW	RS = 50Ω, RL = 50Ω, Figure 7a		66		MHz
NC or NO Off-Capacitance	C(N_OFF)	f = 1MHz, Figure 8		85		pF
COM Off-Capacitance	C(COMOFF)	f = 1MHz, Figure 8		85		pF
On-Capacitance	C(ON)	f = 1MHz, Figure 8		350		pF

2Ω, Quad, SPST, CMOS Analog Switches

MAX4677/MAX4678/MAX4679

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = +5V ±10%, V- = 0, VL = +2.7V to V+, GND = 0, VIH = +2.4V, VIL = +0.8V, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
ANALOG SWITCH							
Input Voltage Range	VCOM-, VNO-, VNC-		0		V+	V	
On-Resistance	RON	V+ = +4.5V, ICOM_ = 50mA, VNO_ or VNC_ = 3.3V		1.8	2.7	Ω	
		TA = TMIN to TMAX			3.5		
On-Resistance Match Between Channels (Note 3)	ΔRON	V+ = +4.5V, ICOM_ = 50mA, VNO_ or VNC_ = 3.3V		0.05	0.15	Ω	
		TA = TMIN to TMAX			0.3		
On-Resistance Flatness (Note 4)	RFLAT	V+ = +4.5V, ICOM_ = 50mA, VNO_ or VNC_ = 3.3V, 1.5V		0.15	0.25	Ω	
		TA = TMIN to TMAX			0.4		
NC_ or NO_ Off-Leakage Current (Note 5)	IN_(OFF)	V+ = +5.5V; VNO_ or VNC_ = 4.5V, 1V; VCOM_ = 1V, 4.5V		-1	0.1	1	nA
		TA = TMIN to TMAX		-10		10	
COM_ Off-Leakage Current (Note 5)	ICOM_(OFF)	V+ = +5.5V; VNO_ or VNC_ = 4.5V, 1V; VCOM_ = 1V, 4.5V		-1	0.1	1	nA
		TA = TMIN to TMAX		-10		10	
COM_ On-Leakage Current (Note 5)	ICOM_(ON)	V+ = +5.5V; VCOM_ = 1V, 4.5V; VNO_ or VNC_ = 1V, 4.5V, or floating		-2	0.2	2	nA
		TA = TMIN to TMAX		-25		25	
LOGIC INPUT							
Input Low Voltage	VIL	VL = V+			0.8	V	
Input High Voltage	VIH	VL = V+	2.4			V	
Input Leakage Current	IIN	VL = V+	-1	0.005	1	μA	
POWER SUPPLY							
Positive Supply Voltage	V+		2.7		6	V	
Logic Supply Voltage	VL		2.7		V+	V	
Positive Supply Current	I+	VIN_ = 0 or VL, VL = V+		1	1	μA	
Logic Supply Current	IL	VIN_ = 0 or VL, V+ = 5.5V			1	μA	
Ground Current	IGND	VIN_ = 0 or VL, V+ = 5.5V		1	10	μA	
DYNAMIC							
Turn-On Time	ton	VL = V+, V+ = +4.5V; VNC_ or VNO_ = 3.3V, RL = 300Ω, CL = 35pF, Figure 2		600	1000	ns	
		TA = TMIN to TMAX			1400		
Turn-Off Time	toff	VL = V+, V+ = +4.5V; VNC_ or VNO_ = 3.3V, RL = 300Ω, CL = 35pF, Figure 2		120	165	ns	
		TA = TMIN to TMAX			400		

2Ω, Quad, SPST, CMOS Analog Switches

MAX4677/MAX4678/MAX4679

ELECTRICAL CHARACTERISTICS—Single Supply (continued)

($V_+ = +5V \pm 10\%$, $V_- = 0$, $V_L = +2.7V$ to V_+ , $GND = 0$, $V_{IH} = +2.4V$, $V_{IL} = +0.8V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Break-Before- Make Delay	t_{BBM}	MAX4679 only, $R_L = 300\Omega$, $C_L = 35pF$, Figure 3	5			ns
Charge Injection	Q	$R_{GEN} = 0$, $C_L = 1nF$, $V_{GEN} = 0$, Figure 4		9		pC
Off-Isolation	V_{ISO}	$R_L = 50\Omega$, $C_L = 5pF$, $f = 1MHz$, Figure 5b		-65		dB
Crosstalk		$R_L = 50\Omega$, $C_L = 5pF$, $f = 1MHz$, Figure 6b		-84		dB
-3dB Bandwidth	BW	$R_S = 50\Omega$, $R_L = 50\Omega$, Figure 7b		63		MHz
NC or NO Off-Capacitance	$C_{(N_OFF)}$	$f = 1MHz$, Figure 8		85		pF
COM Off-Capacitance	$C_{(COMOFF)}$	$f = 1MHz$, Figure 8		85		pF
On-Capacitance	$C_{(ON)}$	$f = 1MHz$, Figure 8		350		pF

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

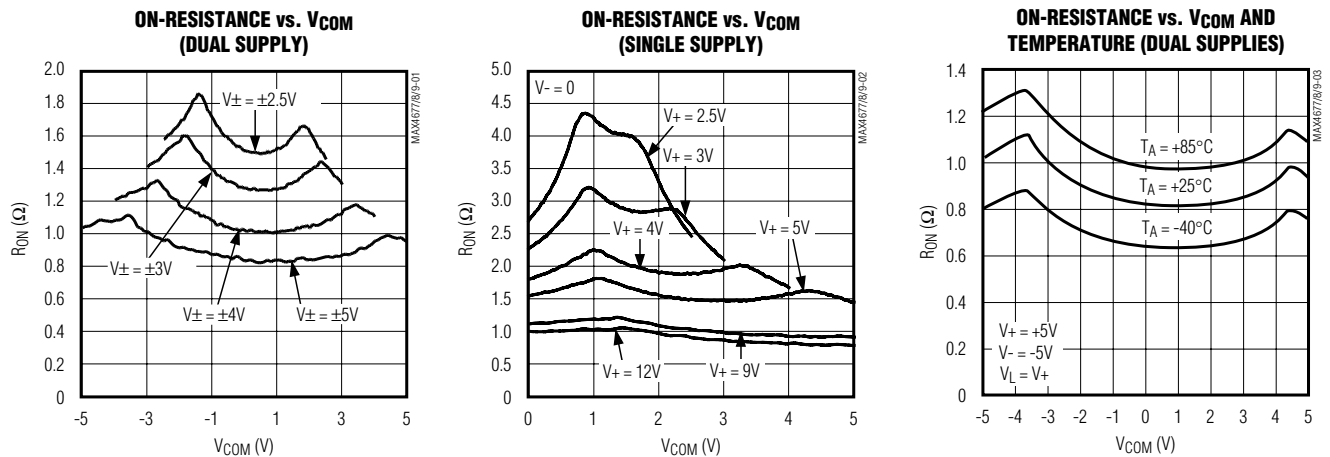
Note 3: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 5: Leakage parameters are 100% tested at maximum-rated hot operating temperature and the highest supply voltage, and guaranteed by correlation at $+25^\circ C$.

Typical Operating Characteristics

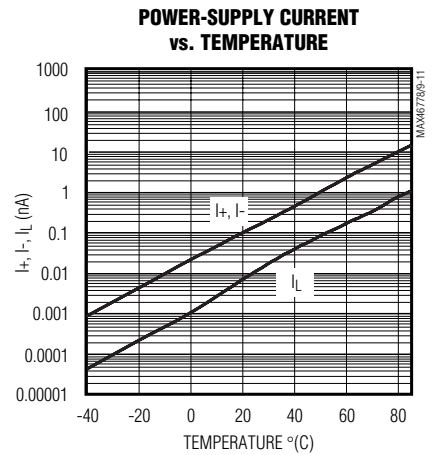
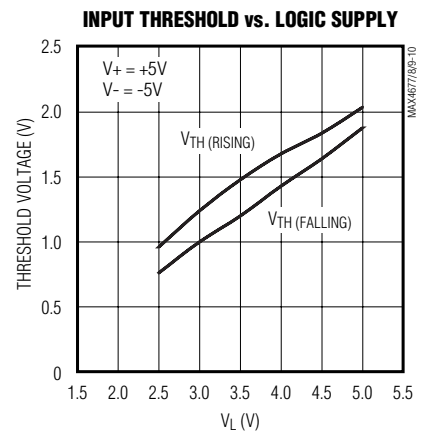
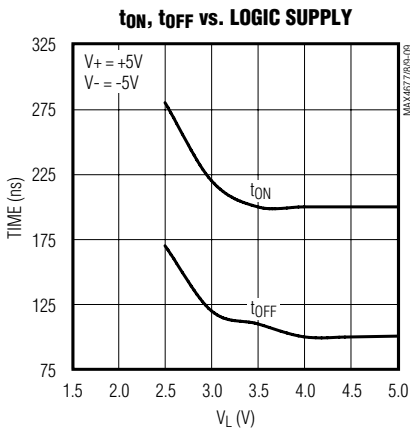
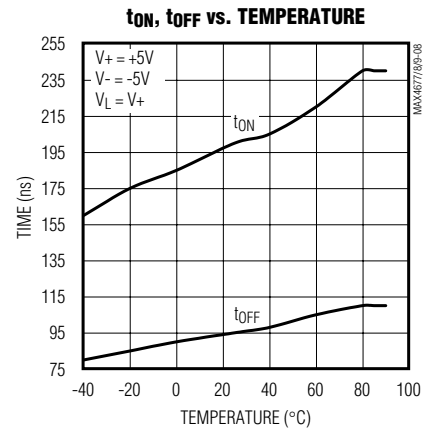
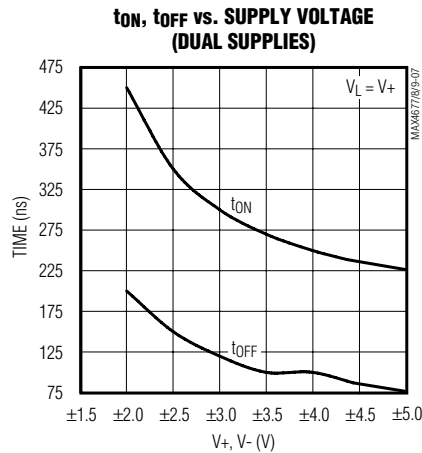
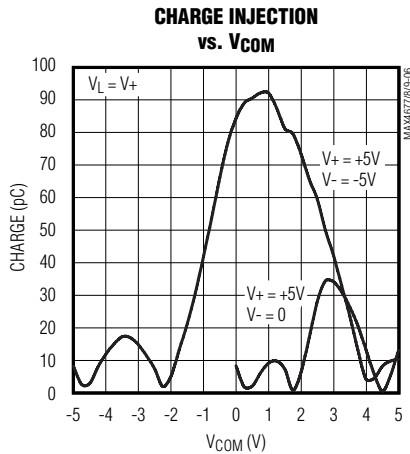
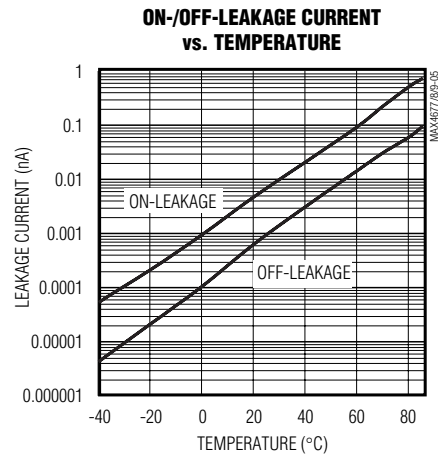
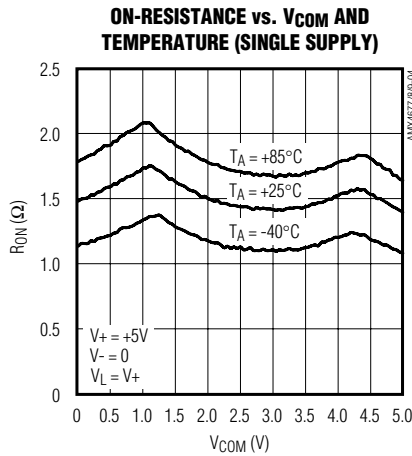
($T_A = +25^\circ C$, unless otherwise noted.)



2Ω, Quad, SPST, CMOS Analog Switches

Typical Operating Characteristics (continued)

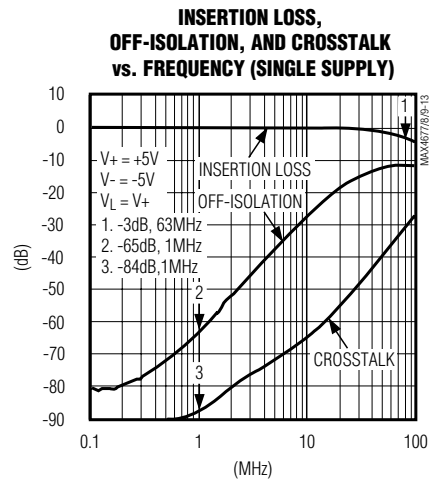
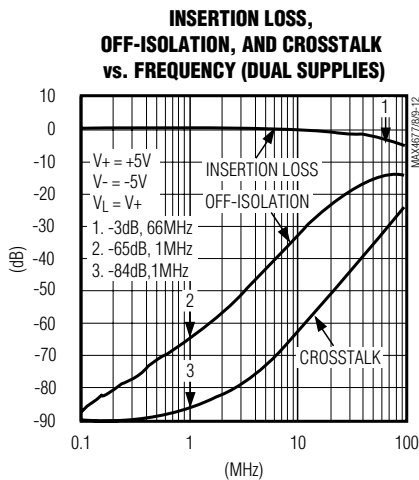
($T_A = +25^\circ\text{C}$, unless otherwise noted.)



2Ω, Quad, SPST, CMOS Analog Switches

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)



Pin Description

PIN			NAME	FUNCTION
MAX4677	MAX4678	MAX4679		
1, 8, 9, 16	1, 8, 9, 16	1, 8, 9, 16	IN1, IN2, IN3, IN4	Logic Inputs
2, 7, 10, 15	2, 7, 10, 15	2, 7, 10, 15	COM1, COM2, COM3, COM4	Analog Switch Common Terminals
3, 6, 11, 14	—	—	NC1, NC2, NC3, NC4	Analog Switch Normally Closed Terminals
—	3, 6, 11, 14	—	NO1, NO2, NO3, NO4	Analog Switch Normally Open Terminals
—	—	3, 6	NO1, NO4	Analog Switch Normally Open Terminals
—	—	11, 14	NC2, NC3	Analog Switch Normally Closed Terminals
4	4	4	V-	Negative Supply-Voltage Input. Connect to GND for single-supply operation.
5	5	5	GND	Ground
12	12	12	V _L	Logic Supply Input
13	13	13	V ₊	Positive Supply Input

MAX4677/MAX4678/MAX4679

2Ω, Quad, SPST, CMOS Analog Switches

Applications Information

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V+ on first, then V-, then VL followed by the logic inputs, NO-, NC-, or COM. If proper power-supply sequencing is not possible, add two small signal diodes (D1, D2) in series with the supply pins, and a Schottky diode between V+ and VL for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to one diode drop below V+ and one diode drop above V-, but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed 11V.

Power-supply bypassing improves noise margin and prevents switching noise from propagating from the V+ supply to other components. A 0.1μF capacitor connected from V+ to GND is adequate for most applications.

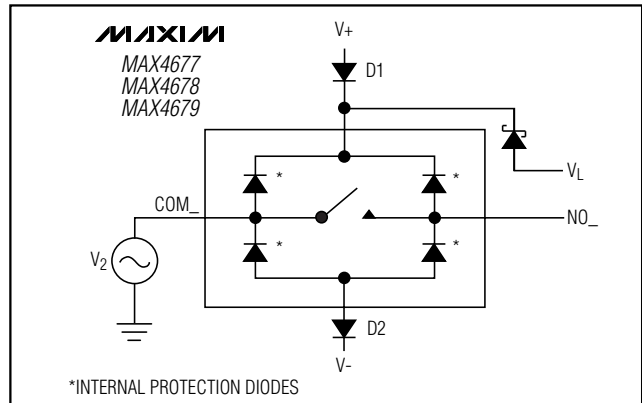


Figure 1. Overvoltage Protection Using External Blocking Diodes

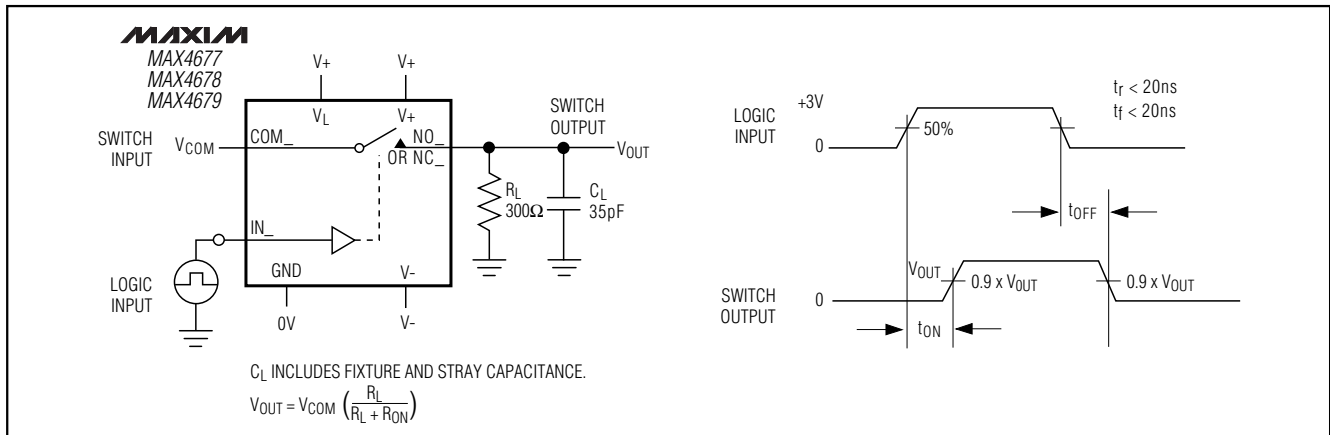


Figure 2. Switching Time

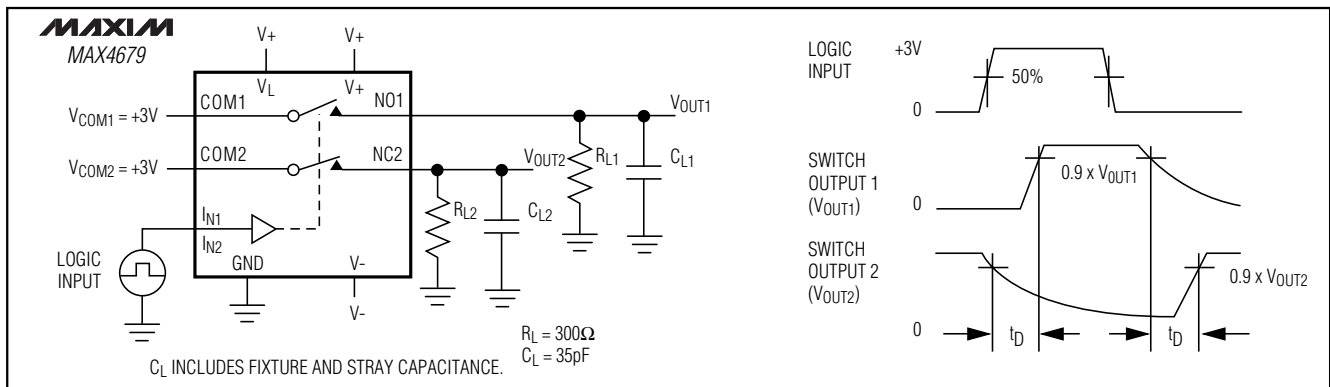


Figure 3. Break-Before-Make Interval (MAX4679 Only)

2Ω, Quad, SPST, CMOS Analog Switches

MAX4677/MAX4678/MAX4679

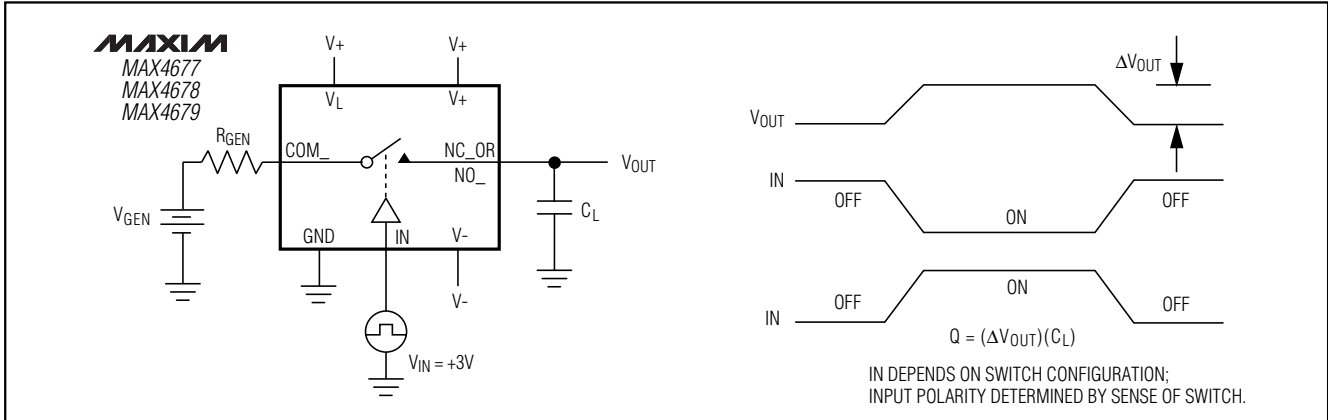


Figure 4. Charge Injection

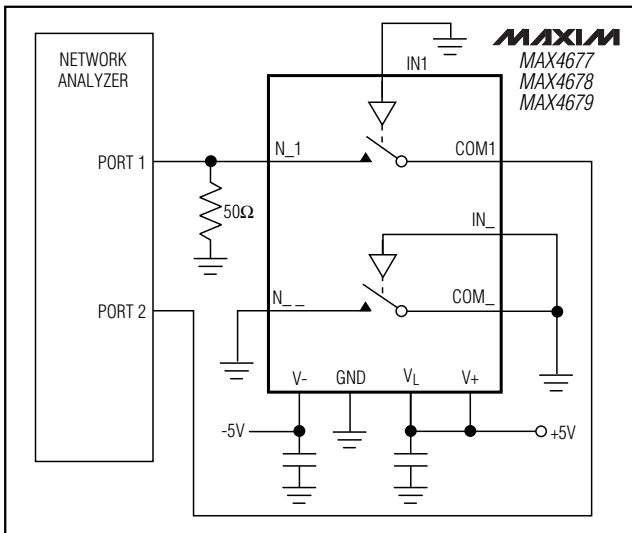


Figure 5a. Off-Isolation Test Circuit, Dual Supplies

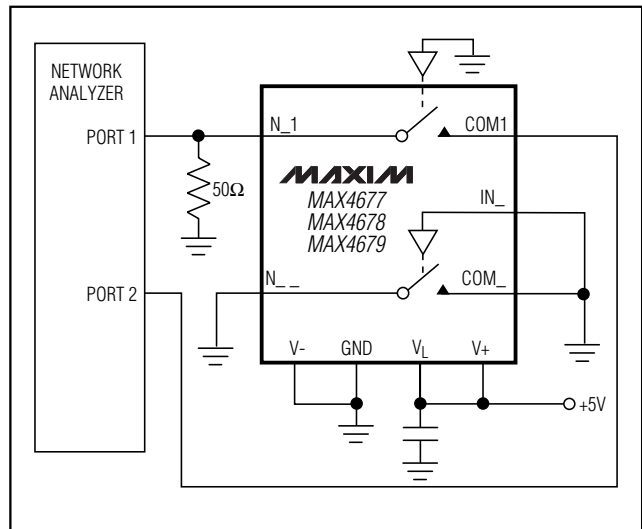


Figure 5b. Off-Isolation Test Circuit, Single Supply

2Ω, Quad, SPST, CMOS Analog Switches

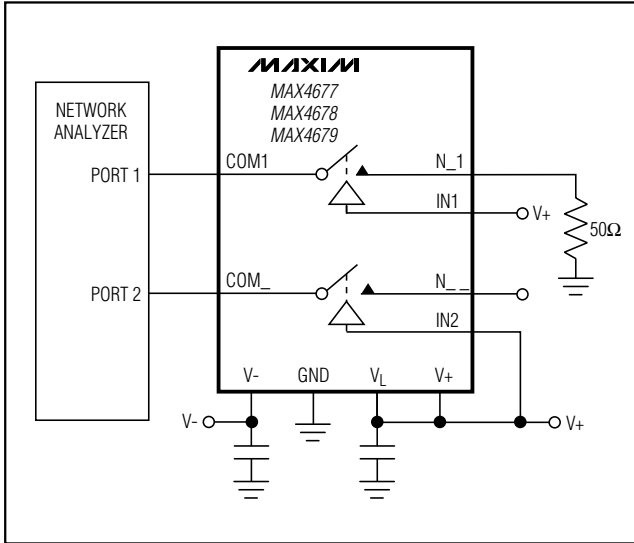


Figure 6a. Crosstalk Test Circuit, Dual Supplies

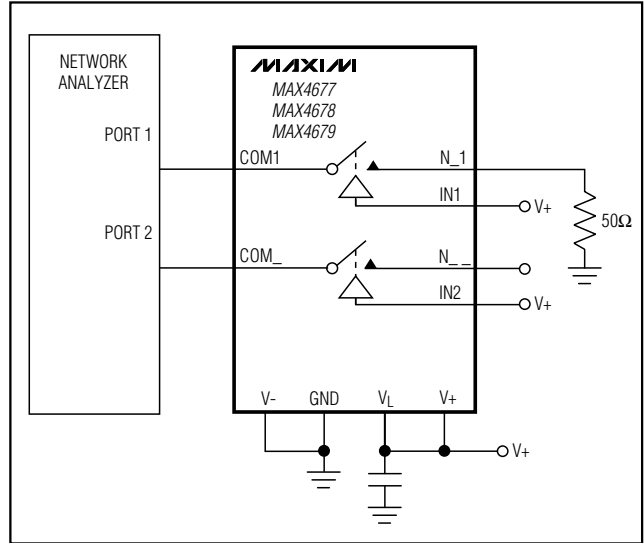


Figure 6b. Crosstalk Test Circuit, Single Supply

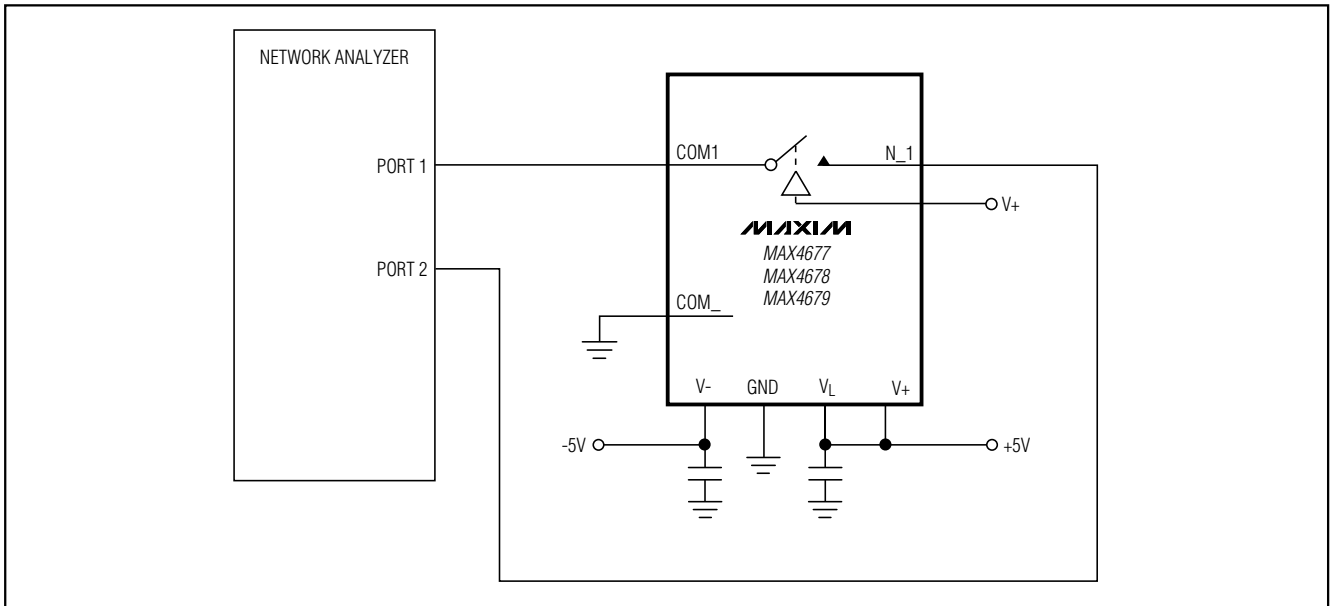


Figure 7a. Insertion Loss Test Circuit, Dual Supplies

2Ω, Quad, SPST, CMOS Analog Switches

MAX4677/MAX4678/MAX4679

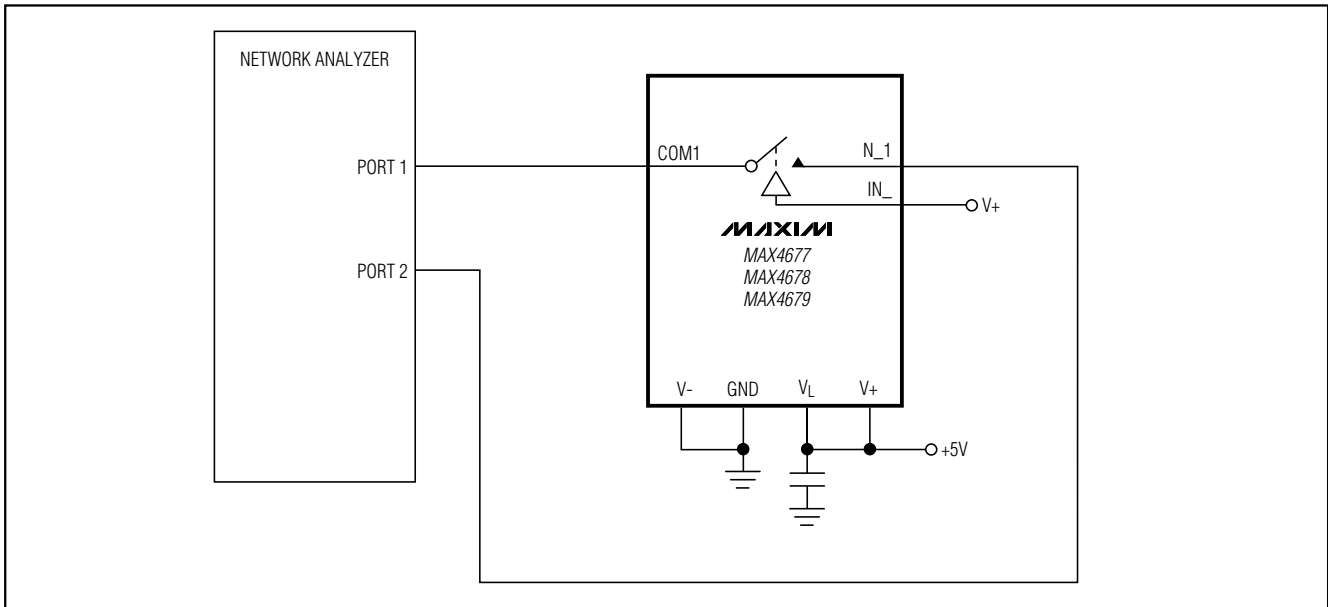


Figure 7b. Insertion Loss Test Circuit, Single Supply

Chip Information

TRANSISTOR COUNT: 240
PROCESS: CMOS

2Ω, Quad, SPST, CMOS Analog Switches

Package Information

COMMON DIMENSIONS

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	1.10	—	.043
A ₁	0.05	0.15	.002	.006
A ₂	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b ₁	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c ₁	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		0.26 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
Ø	0*	8*	0*	8*

JEDEC	N	VARIATIONS			
		MILLIMETERS		INCHES	
MD-153	N	MIN	MAX	MIN	MAX
AB	14	4.50	5.10	.193	.201
AC	16	4.90	5.10	.193	.201
AC-FP	16	4.90	5.10	.193	.201
AD	20	2.85	3.15	.112	.124
AD-FP	20	6.40	6.60	.252	.260
AE	20	6.40	6.60	.252	.260
AF	X	4.00	4.34	.157	.171
AF	24	7.70	7.90	.303	.311
AF	28	9.60	9.80	.378	.386
AF-FP	D	9.60	9.80	.378	.386
AF-FP	X	5.35	5.65	.211	.222

NOTES:
 1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 mm PER SIDE.
 3. CONTROLLING DIMENSION: MILLIMETER.
 4. MEETS JEDEC OUTLINE MD-153 VARIATIONS AB, AC, AD, AE, AF.
 5. DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY.
 6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

MAXIM
 PROPRIETARY INFORMATION
 TITLE: PACKAGE OUTLINE, TSSOP, 4.40mm BODY, 0.65mm PITCH
 APPROVAL: _____ DOCUMENT CONTROL NO: 21-0066 REV: C 1/1

PACKAGE FAMILY OUTLINE: PDIP .300"

INCHES				MILLIMETERS				N	MS001		
MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX				
A	—	0.180	—	4.572	D	0.348	0.390	8.84	9.91	8	AB
A ₁	0.020	—	0.508	—	D	0.735	0.765	18.67	19.43	14	AC
A ₂	0.125	0.175	3.18	4.45	D	0.745	0.765	18.92	19.43	16	AA
A ₃	0.055	0.080	1.40	2.03	D	0.885	0.915	22.48	23.24	18	AD
B	0.015	0.021	0.381	0.533	D	1.015	1.045	25.78	26.54	20	AE
B ₁	0.045	0.060	1.14	1.524	D	1.14	1.265	28.96	32.13	24	AF
C	0.009	0.014	0.229	0.355	D	1.360	1.380	34.54	35.05	28	AF
D ₁	0.005	0.080	0.13	2.03							
E	0.300	0.325	7.62	8.255							
E ₁	0.275	0.295	6.985	7.493							
e	0.100	—	2.54	—							
eA	0.300	—	7.62	—							
eB	—	0.400	—	10.16							
L	0.115	0.150	2.921	3.81							

NOTES:
 1. D₁ DO NOT INCLUDE MOLD FLASH
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
 3. CONTROLLING DIMENSION: MILLIMETER
 4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
 5. SIMILAR TO JEDEC MS-095-AH
 6. N = NUMBER OF PINS

MAXIM
 PROPRIETARY INFORMATION
 TITLE: PACKAGE FAMILY OUTLINE: PDIP .300"
 APPROVAL: _____ DOCUMENT CONTROL NO: 21-0043 B REV: 1/1

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