ISL55100A/BEVAL3/3Z

Evaluation Board User's Guide

AN1217
Rev 1.00
Sep 12, 2008

ISL55100 Device Application Overview

The ISL55100 is a Quad Driver/Receiver device that is typically utilized in bi-directional testing applications where formatted timing sets "write data to" and "read data back" from digital devices.

Examples of bi-directional bus based devices are UARTs, Real Time Clocks, Interrupt Controllers, Parallel I/O devices, FPGA's and others. Memory devices are also bi-directional in that data can be stored in them and then retrieved at a later time.

The ISL55100 provides four driver/receiver pairs (DOUT0-3/VINP0-3) that are usually tied together in order to support bi-directional communications (bus cycle emulation). HIZ control of the drivers enables this configuration.

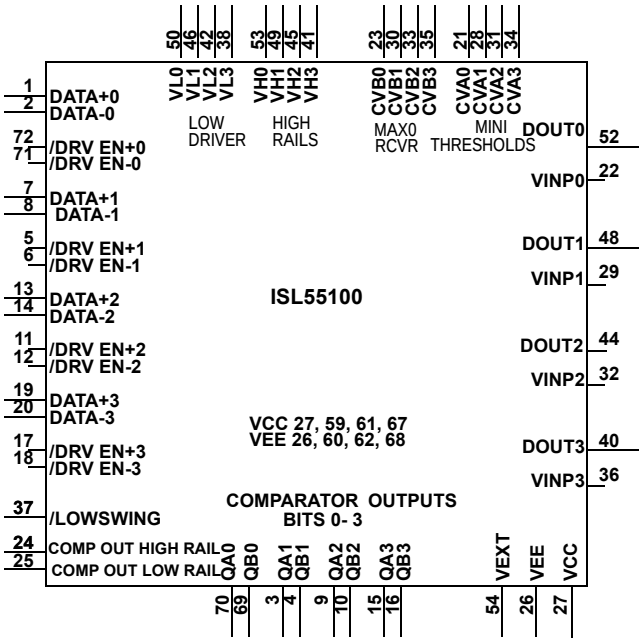


FIGURE 1. FUNCTIONAL ISL55100A/BEVAL3/3Z PINOUT

The ISL55100 provides the means of "translating" the DUT's bus levels for a test system (Figure 3). Level translation on "Write Operations" is accomplished with the drivers. "Read Operation" level translation is done via the receiver/comparators. Comparator QA/QB outputs adjust their levels to the tester side logic levels by way of the COMP-HIGH and COMP-LOW levels. Comparators in the receivers set the DUT side level thresholds. Further the Window Comparators (Dual Threshold Receivers) enable received data to be verified for proper levels (Valid1, Valid 0). Level translation enables the Pin Electronics Pattern Devices to write data to and read data back from different types of logic families.

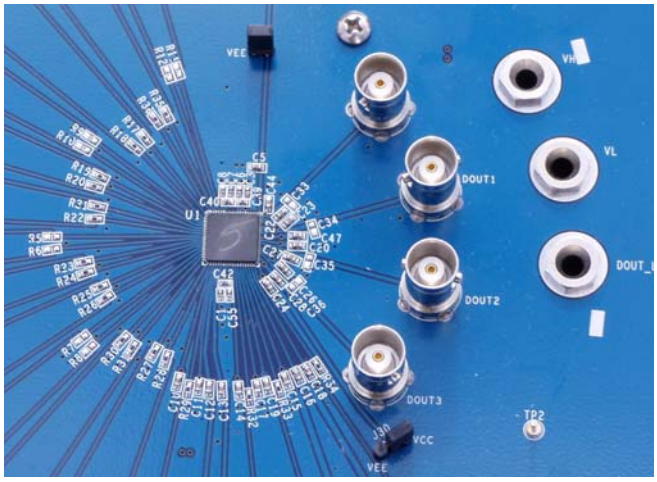
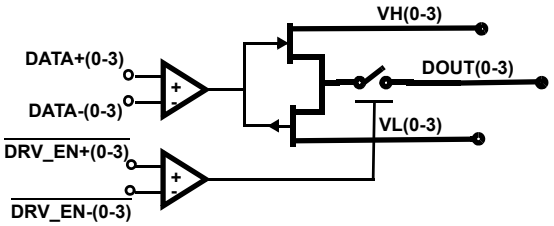


FIGURE 2. DEVICE AREA, ISL55100A/BEVAL3/3Z EVALUATION BOARD

The ISL55100A/BEVAL3/3Z Evaluation Board enables easy access to the various ISL55100 connections. All inputs and outputs are matched for signal path length.

QUAD - WIDE RANGE, LOW ROUT, TRI-STATABLE - DRIVERS



QUAD - DUAL LEVEL COMPARATOR - RECEIVERS

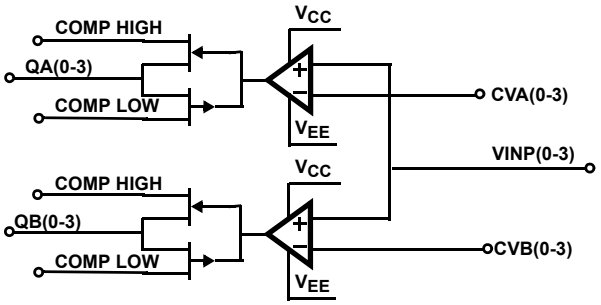


FIGURE 3. DIAGRAM OF ISL55100A/BEVAL3/3Z DRIVERS AND RECEIVERS

The ISL55100A/BEVAL3/3Z is made up of four drivers and four dual level receivers. Drivers provide voltage level translation for "Write" operations while the Dual Level Comparators translate voltage levels for "Read" operations.

ISL55100A/BEVAL3/3Z Evaluation Board

The ISL55100A/BEVAL3/3Z Evaluation board provides the means to experiment with an Intersil ISL55100A/BEVAL3/3Z Quad Driver Receiver. Experiments typically include Driver Waveform analysis based on the user's load. Driver analysis may also include waveforms at various voltage rails and also include data propagation and HIZ transition timing.

The user can also collect information related to receiver comparator characteristics, device dynamic power consumption and the timing of comparator outputs. In addition, the evaluation board accommodates loop-back testing and exercising of the LowSwing and VEXT modes of operation.

The DOUT_LOAD and VDIGC/D busses on the ISL55100A/BEVAL3/3Z Evaluation board provide the user with flexibility to initiate special analysis. This document sets up the ISL55100A/BEVAL3/3Z in a typical usage/configuration. As the user progresses in knowledge, the concept behind the analysis capability of the DOUT_LOAD, VDIGC and VDIGD should become evident.

FIGURE 4. ISL55100A/BEVAL3/3Z EVALUATION BOARD

BNC's are used for high frequency connections. Banana plugs and jumpers are used for low frequency/power supply connections.

Basic Design Fundamentals Include:

- Matched circuit lengths on DATA inputs, Driver Outputs and Comparator measurement points.
- Banana jack terminals used for low frequency connections. (Power supplies, VDIGC/D Bias Busses)
- BNC connectors for high frequency connections. (Driver data and enable inputs, driver outputs, receiver inputs, comparator outputs)
- Jumpers for static mode selections. (LowSwing, Differential Biasing, VEXT)
- All DATA, DRV_EN and VINP signals have 50Ω loads to ground and may be jumpered to test busses via jumpers.

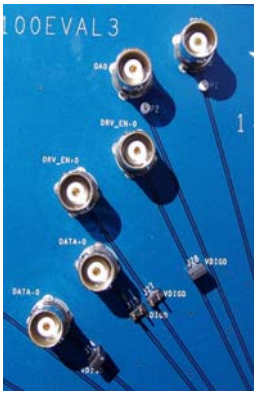


FIGURE 5. HIGH SPEED, TESTER SIDE, DRIVER CONNECTIONS

There are six high speed BNC tester side connections for each of the four channels: DATA± control the high/low activity. DRV_EN± enable/disable the driver outputs and QA/QB are receiver/window comparator outputs.

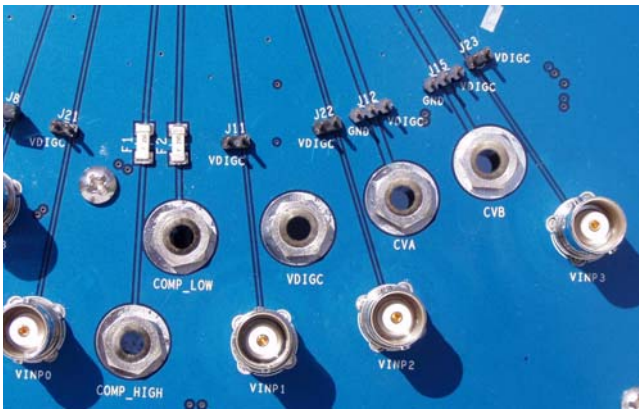


FIGURE 6. LOW FREQUENCY CONNECTORS

COMP_HIGH and LOW, CVA, CVB, V_{EE}, V_{CC}, GND and VDIGC/D are low frequency power supply banana jack connections.

Driver Data and Driver Enable Differential Inputs Overview

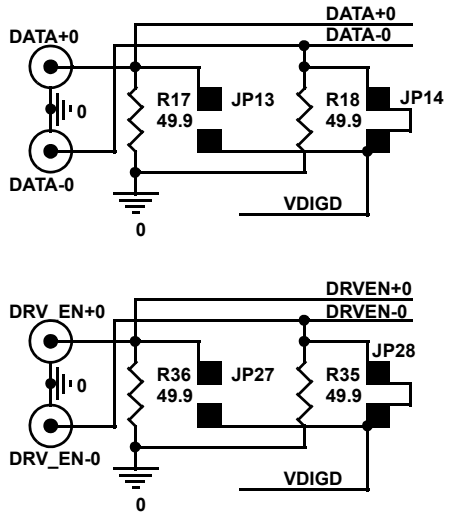


FIGURE 7. EACH DRIVER HAS FOUR INPUT CONTROL LINES

The user may wish to remove the 49.9Ω resistors and terminate the inputs differently to ground. For series termination, all resistors and jumpers would be removed. The user can then install resistors across the differential inputs by connecting a resistor from the signal side of JP13/JP27 (+ inputs) to the signal side of JP14/JP28 (- inputs).

DIFFERENTIAL INPUTS

DATA± and DRV_EN± are differential inputs. For each of the four drivers, there are four input signals. DATA+, DATA- and DRV_EN+, DRV_EN-. The DATA+ and DATA- inputs will control if the Driver Output is driven to the High Driver Rail (VH) or the Low Driver Rail (VL). The DRV_EN+ and DRV_EN-inputs enable or disable the Driver Output. When enabled, the Driver Output will be driven either to the Driver High Rail or the Driver Low Rail. When disabled, the Driver Output floats to a High Impedance condition (HIZ). The ability to “Float” the Drivers enables bi-directional operations, or shared bus line utilization.

Caution: These paired inputs: DATA+, DATA- and DRV_EN+, DRV_EN- must NOT be driven to the same voltage level. DATA+ and DATA- must be at least 200mV apart in voltage level. DRV_EN+ and DRV_EN- must also be at least 200mV apart in voltage level. The differential receivers within the ISL55100 can exhibit high speed chatter if their inputs are at the same voltage level. The user will notice an increase in ISL55100's ICC if the chatter condition exists.

The differential inputs need to transition quickly (<5ns) with respect to each other. When DATA+ is 200mV (or more) higher than DATA-, the associated driver output will be driven to the High Driver Rail/Supply (VH). When DATA+ is lower than DATA- by 200mV or more, the associated driver output will be driven to the Low Driver Rail/Supply (VL).

SINGLE-ENDED CONTROL

An important note to remember is the user must **NOT** tie one of the inputs to ground. Often this is mistakenly done to enable “Single-Ended” control. However, connecting one input to ground and toggling the other input usually results in both inputs being at the same voltage level (Ground) when the driven signal is low.

The proper remedy to obtain Single-Ended control is to bias one of the inputs to the “mid-level” of the other inputs planned voltage swing. Example; a TTL driver is 2.8V when high and 0.4V when low. The preferred bias level of the paired differential input will be 1.4V.

Preparation for Power-up

JUMPER DISCUSSION

Note: A Jumper Placement Summary is located on page page 4.

The ISL55100 Evaluation board enables single-ended input via two design attributes. First, jumpers are provided on all DATA+(0-3), DATA-(0-3), DRV_EN+(0-3), DRV_EN-(0-3) inputs. These jumpers enable the selected inputs to be connected to a Bias Bus on the Evaluation board. Second, this bias bus VDIGD is connected to a banana jack for connection to a DC bias voltage. The ISL55100 Evaluation board is typically shipped with the jumpers set to connect DATA-(0-3) and DRV_EN-(0-3) to the bias bus VDIGD.

During initial setup of the board, it is recommended the VDIGD Banana Jack be connected to a 0.5V DC supply. The reason for the low voltage level relates to the 50Ω load resistors on all inputs. Keeping the bias low reduces the current requirements of the bias supply. This enables the user to become familiar with the ISL55100 until such time as experiments possibly lead to the removal of the 50Ω resistors and the addition of series termination across the + and - differential inputs.

As a result, in the early experiment stages, it is recommended that Jumpers 14, 28, 01, 03, 10, 07, 08 and 25 be installed. Jumpers 13, 27, 02, 04, 09, 05, 06, 26 should be removed. In this configuration, VDIGD banana jack will need to be connected to a 0.5V DC Power Supply at the proper time in the power-up sequence (see Table 1).

/Lowswing and VEXT Mode Jumpers

There are two mode jumpers on the ISL55100 Eval board. First, the /LowSwing (Pin 37 of the 55100) JP30 should be placed in the V_{CC} position. Second, the V5V banana jack (Pin 54 of the ISL55100) JP29 should be placed in the V_{EE} position.

Comparator Threshold Jumpers

Both CVA Input - JP12 and CVB Input - JP15 should be removed.

Receiver Input Bias Jumpers

The four receivers (VINP0-3) should have the bias Jumpers removed. JP21, 11, 22, 23 should not be installed. These jumpers enable the connection of the four receivers to a bias bus “VDIGC” on the ISL55100A/BEVAL3/3Z Evaluation Board. This feature will not be used during early experiments with the ISL55100 but may be of use to the user in later experiments.

JUMPER SETUP SUMMARY

Note: Detailed discussion on Jumper Placement is given on page 3.

Jumpers Installed

Negative Differential Input connections to the VDIGD (0.5V) Bias Bus.

- DATA-0 JP14
- DATA-1 JP01
- DATA-2 JP10
- DATA-3 JP08
- DRV_EN-0 JP28
- DRV_EN-1 JP03
- DRV_EN-2 JP07
- DRV_EN-3 JP25

Jumpers Removed

Positive Differential Inputs, No VDIGD bias connection

- DATA+0 JP13
- DATA+1 JP02
- DATA+2 JP09
- DATA+3 JP06
- DRV_EN+0 JP27
- DRV_EN+1 JP04
- DRV_EN+2 JP05
- DRV_EN+3 JP26

CVA Input - JP12 and CVB Input - JP15

VINP, no bias (VDIGC not connected)

- VINP0 JP21
- VINP1 JP11
- VINP2 JP22
- VINP3 JP23

Jumpers Positioned

/LowSwing Mode Off..... JP30 in V_{CC} Position

VEXT not in use.....JP29 in V_{EE} Position

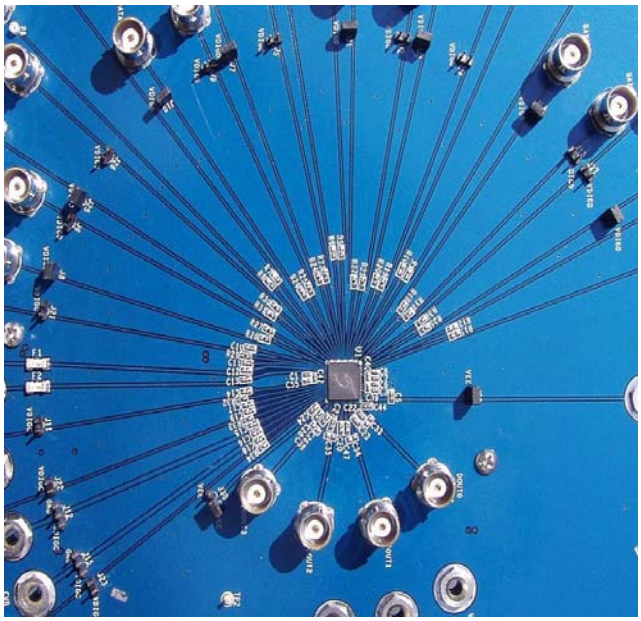


FIGURE 8. EVALUATION BOARD JUMPERS AND LOADS

Jumpers are placed in a circle around the ISL55100. Please note that all inputs have 50Ω resistors to ground. Configuring the jumpers as shown will place the drivers in “driven - low” output, enabled, and compatible with single ended operation.

Power Supply Connections

Power Supply Sequence, Quick Overview

TABLE 1. ISL55100A/BEVAL3/3Z POWER SUPPLY SEQUENCE/SETUP OVERVIEW

SEQ#	SUPPLY DESC	BANANA1 LABEL	BANANA2 LABEL	VOLTAGE	NOTE	
1	V_{EE} - Device Power	V_{EE}	GND	-3.0	70mA quiescent to 450mA	
2	V_{CC} - Device Power	V_{CC}	GND	12.0	70mA quiescent to 450mA	
3	Vbias - Single Ended	VDIGD	GND	0.5	80mA	If missing, drivers will chatter*
4	COMP-HIGH and COMP-LOW	COMP-HIGH	COMP-LOW, GND	3.0	COMP-HIGH must be > COMP-LOW	
5	Rcvr Threshold #1	CVA	GND	2.0	If missing, Comparator Outputs may chatter*	
6	Rcvr Threshold #2	CVB	GND	1.0	If missing, Comparator Outputs may chatter*	
7	Driver High Rail	VH	GND	3.0	10-800mA	Determined by driver load, driver rails and frequency
8	Driver Low Rail	VL	GND	-1.0	10-800mA	

Seq 1 to 6 should be applied in as little time as possible. Remove in reverse order. If supply current exceeds quiescent values, power-down immediately. Supply 7 to 8 can be applied at leisure.

No supply should exceed V_{EE} on the negative side or V_{CC} on the positive side.

* Chatter - Condition where driver or receiver is in an indeterminate state, toggling between high and low. Chatter can cause excessive current drain and possible damage to the ISL55100.

POWER SUPPLY DISCUSSION

All power supplies should be referenced to the “GND” Ground Banana Jack at the corner of the board. Please consult the data sheet for recommended and max voltages used with the ISL55100A/B. In this document we will supply “typical” settings as a starting point for the user.

An ideal quantity of power supplies would be 8 supplies, all with voltage/current displays. In addition, two variable DC sources will be used for various experiments. Another 5.5V/100mA supply will be needed if you with to try the VEXT mode. The supplies operate in the 1V to 20V range and should be rated for ~1A.

At no time should any of the other supplies exceed the V_{CC} voltage or be less than the V_{EE} voltage. Note that internal protection circuits assume VH > VL and COMP_HIGH > COMP_LOW.

Main Device Power

For a typical setup the main supplies are:

Device Logic V_{EE} -3.0V to ground (GND), 70mA with the drivers/receivers in a static condition, to up to 450mA at high frequency.

Device Logic V_{CC} +12.0V to ground (GND), 70mA with the drivers/receivers in a static condition, to up to 450mA at high frequency.

VDIGD Bias Bus should be set to + 0.5V to ground (GND), 80mA (Due to 50Ω loads on differential inputs).

These are the three main supplies that need to come up quickly for the ISL55100 to work properly. Check the current drains of V_{EE}/V_{CC} to see if they are ~70mA. (DATA±, DRV_EN± at static levels, no toggling). If the currents are not in this range, power down the board and check the differential bias connections.

Next power-up the Comparator Output Rails (COMP_HIGH and COMP_LOW) and the Comparator Threshold Inputs CVA’s and CVB’s.

Comparator Output Rails

Connect +3.0V across the COMP_HIGH and COMP_LOW banana jacks. Also, connect the COMP_LOW banana jack to the GND banana jack on the board. Current will be <20mA.

Comparator Thresholds

Connect CVA to +2.0V, Reference to ground (GND)

Connect CVB to +1.0V, Reference to ground (GND)

Current on the CVA and CVB inputs <20mA

Driver Rails

Connect VH to +3.0V, current will be <10mA*

Connect VL to -1.0V, current will be <10mA*. Wire this supply as a negative supply.

* VH/VL Current depends on the User's Driver Load (C33 to 36) and frequency of operation. The <10mA current is based on quiescent operating conditions and no resistive load on the driver outputs.

Note: If supplies are limited, CVA/CVB can be tied to the same supply. Do not leave either one floating or connected to ground as this will cause the comparator output to chatter.

Chattering occurs if the input to a comparator is equal to the threshold voltage. If the receiver input is connected to ground via the 50Ω resistor and 0.0V is applied to CVA or CVB then both the input and the threshold will be at 0.0V. Any noise coupling will cause the comparator outputs QA/QB to “Chatter” high and low with the system noise.

COMPARATOR DISCUSSION

Most computer busses deal with one of two states during active bus transactions. They are high, usually considered a digital 1, or low, usually considered a digital 0.

But digital 1’s and 0’s must operate in an analog world so a tolerance is assigned. The minimum voltage a digital pin can be and still be considered a valid 1 is the V_{IH} level. Likewise, the maximum voltage a digital pin can be and still be considered a valid 0 is the V_{IL} level.

VOH/VOL AND VIH/VIL DISCUSSION

TTL logic levels are assigned these levels:

(VOH, VOL define the Driver Output Rails (VH/VL))

- VOH: A driver driving a digital 1 must assert a minimum of 2.8V to be valid.
- VOL: A driver driving a digital 0 must assert a maximum of 0.4V to be valid.

These voltages are specified at the Driver (High 2.8V, Low 0.4V). However there is an allowance between drive levels and receive thresholds. This allowance is for loss through the circuit paths. A TTL Digital Receiver must be designed such that:

(VIH, VIL define the Receiver Comparator Thresholds)

- VIL: Any received voltage of <0.8V is considered a valid digital 0.
- VIH: Any received voltage of >2.4V is considered a valid digital 1.

Window Comparators go beyond the ability to merely detect 1 and 0 voltage levels. Window Comparators can detect indeterminate pin states (often slow transition pins in the real world).

Window comparators have 2 bits of information for each digital receiver under test. With 2 bits, the tester side logic can determine if the pin under test is a valid digital 1/0 or an illegal voltage level.

In our example, TTL Test Application, we will use the CVA voltage to set the Min1 (V_{IH}) Threshold and the CVB voltage to set the Max1 (V_{IL}) Threshold.

CVA would be set to 2.4V. CVA comparator drives the QA Outputs.

CVB would be set to 0.8V. CVB comparator drives the QB Outputs.

Here are examples of QA/QB levels based on various VINP voltages. (Examples include 50mV Offset per ISL55100 Data Sheet)

1. If VINP = 0.0V then QA = 0, QB = 0

VINP is less than both thresholds, a valid digital 0.

2. If VINP = 0.75V then QA = 0, QB = 0

VINP is still less than both thresholds and still a valid digital 0.

3. If VINP = 0.85V then QA = 0, QB = 1

VINP is > CVB threshold of.8V but less than the CVA threshold of 2.4V.

4. If VINP = 2.35V then QA = 0, QB = 1

VINP is > CVB threshold of.8V but less than the CVA threshold of 2.4V.

5. If VINP = 2.45V then QA = 1, QB = 1

VINP is > both CVA and CVB thresholds, A valid digital 1.

6. If VINP = 2.80V then QA = 1, QB = 1

VINP is > both CVA and CVB thresholds, Still valid digital 1.

Window Comparators Bring Real World Benefits in the Test World

First, the dual thresholds normally detect “slow” pins. Therefore, they provide insight into weak devices. Window comparators detect the fact that the pin is changing, just not quickly enough.

WINDOW COMPARATOR UTILIZATION

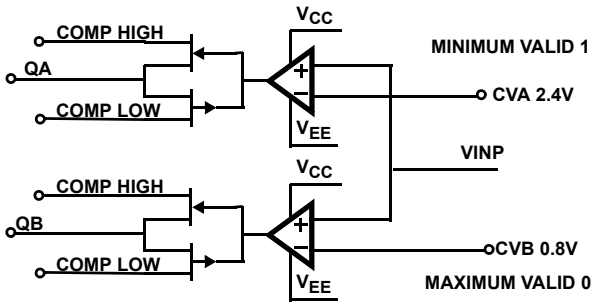


FIGURE 9. WINDOW COMPARATOR USING TTL THRESHOLDS

TABLE 2. WINDOW COMPARATOR TRUTH TABLE

CVA	CVB	VINP	QA	QB
2.4V	0.8V	<0.75V	0	0
2.4V	0.8V	0.85V to 2.35V	0	1
2.4V	0.8V	>2.45V	1	1

Secondly, since the user is testing unknowns, verifying pin activity during write cycles detects shorts in the device under

test. Often these are high-impedance shorts. Detecting these types of failures helps in reducing troubleshooting time. This is one reason why all drivers should be looped-back to receivers even when the pin is being used in a driver only situation (typical example is the Address bus). Looping drivers back for verification is a good test design/development practice.

TABLE 3. BASIC EXAMPLES OF V_{IH}, V_{IL} VOLTAGE LEVELS

LOGIC FAMILY	SUB FAMILIES	V_{IL} VOLTS	V_{IH} VOLTS
CMOS	AC-HC-AHC-C	1.30	3.70
TTL/CMOS	ACT-HCT-AHCT-FCT	0.8	2.40
TTL	F-S-AS-LS-ALS	0.8	2.40

NOTE: Window comparators are used to verify receiver inputs meet V_{IL}, V_{IH} requirements.

SLOW SPEED COMPARATOR OBSERVATIONS

With the board powered up as detailed in Table 1 and jumpers set as previously defined, connect a DC source to the VINP0 BNC. Keep the voltage low, as there is a 50Ω load resistor to ground (R_{29}). Place a scope or a couple of voltmeters on QA0 and QB0. Assuming CVA is set to 2.4V and CVB is set to 0.8V, slowly vary the power supply up and down. You should be able to verify Table 2.

As long as the input voltage is <0.8V, both QA and QB will be at low levels. Once you move the supply above 0.8V QB will become a 1 but QA will remain a 0 until the volt exceeds 2.4V at which point the QA comparator will switch to a one and both QA and QB will be a high.

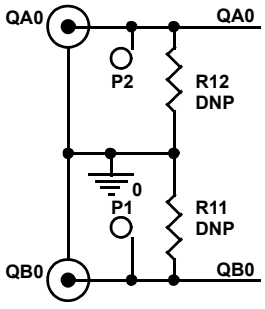


FIGURE 10. QA/QB BNC COMPARATOR OUTPUTS

There are locations on the evaluation board for load resistors on the comparator outputs. However, they are not populated. (DNP = Do not populate.)

The QA/QB high and low voltage levels are determined by the COMP supply. The comparators will drive the QA/QB to the COMP-HIGH level whenever VINP exceeds the CVA /CVB threshold levels. When VINP is less than the CVA/CVB levels, the comparators drive the QA/QB signals to the COMP-LOW signal. The voltage you connect across COMP-HIGH and COMP-LOW determines the amount of voltage swing the Comparator Outputs QA/QB will put out. There is only one COMP_HIGH/COMP_LOW connection for all four receivers.

SLOW SPEED DRIVER DATA OBSERVATIONS

Data Control (Digital 1, Digital 0)

With the board powered up as detailed in Table 1 and jumpers set as previously defined, place a scope on DOUT0 BNC. The DOUT0 should be sitting at VL voltage. Connect a power supply to the DATA+0 BNC. Set the voltage to 1.0V. The DOUT pin should transition to the VH voltage. Moving the supply >200mV above and below the 0.5 bias voltage will cause the output to toggle between VH and VL.

SLOW SPEED DRIVER HIZ OBSERVATIONS

Driver Enable Control (Enabled, HIZ)

With the 1.0V still applied to DATA+0 BNC (DOUT should be at VH Voltage), use another jumper and connect the 1.0V to the DRV_EN+0 BNC. This “disables” the DOUT0 Output. The Output will float slowly downward. Connect the DOUT Pin to ground through a 1kΩ resistor. When DRV_EN+0 is set high the DOUT 0 will be pulled to ground.

Remove the DRV_EN+0 jumper. Set the VL voltage to -3V. Verify that DOUT now transitions from +3 to -3V as you toggle the DATA+0 BNC between ground and 1.0V. You can verify that the driver is always enabled because the DOUT is either +3 to -3V.

Re-apply the 1.0V to the DRV_EN +0 BNC. Notice the DOUT floats down to 0V because of the 1k DOUT load. This verifies the driver is not connected to either VH or VL rail. The driver output is in a HIZ state. In this state other devices can now drive the DOUT pin and not conflict with the ISL55100 Driver.

With the driver disabled, the DOUT bus connection can be driven by another device. The HIZ function enables computer busses to multiplex common bus pins among several computer subsystems.

DYNAMIC DRIVER OBSERVATIONS

Connect the DATA+ inputs to a pattern or pulse generator. Start by setting up a 10MHz square wave into DATA+0 and place a scope on DOUT0. Remember, the generator will be driving a 50Ω load and must be of sufficient amplitude to go > 200mV above the 0.5V bias when high and 200mV below the 0.5V bias when low. Since DRV_EN+0 is low, DOUT0 should be enabled and should be following the generators output. Propagation delay will be about 10ns. Therefore, 10nsec after the generator rises above 0.5V, the DOUT should rise to the VH-Rail value of 3.0V. Likewise it should fall back to VL volts when the generator output falls below 0.5V.

DYNAMIC POWER OBSERVATIONS

As you increase and decrease the frequency of the generator, the ICC current of the V_{CC} and V_{EE} will rise and fall with the pin activity. Remember to keep an eye on the ISL55100 Device Temperature. It is possible to damage the device if it is run at high frequency without proper cooling. Remember also, as you add more channels the power consumption will go up accordingly.

DRIVER LOAD OBSERVATIONS

During these experiments you should check out C_{33} on the evaluation board. In most cases it will be empty when shipped, unless you have requested a specific load installed prior to shipment from the factory. C33 is the location where you can add capacitance and resistors to simulate your desired load.

C_{33}, C_{34}, C_{35}, C_{36} provide load locations for DOUT 0, 1, 2 and 3.

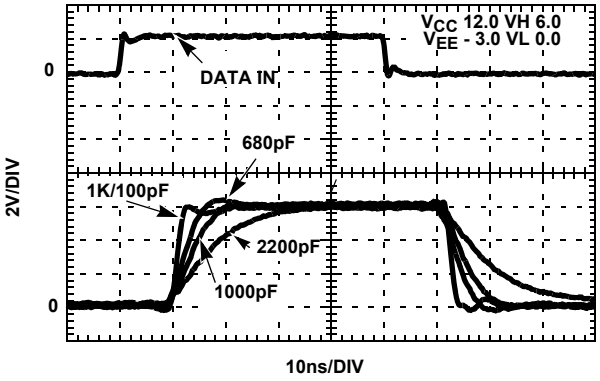


FIGURE 11. DRIVER WAVEFORMS UNDER VARIOUS LOADS

C33-C36 are surface mount locations where user defined driver loads can be installed.

DOUT_LOAD BUS

There is a DOUT_LOAD Banana jack. This bus connects to the DOUT(s) via R13, R14, R15, and R16, which are located on the bottom of the board. This bus enables you to “Bias” the drivers via user selectable resistors so you can either load them to ground or apply a voltage. Normally these load locations (R13 to R16) are not populated when shipped from the factory.

HIZ OBSERVATIONS

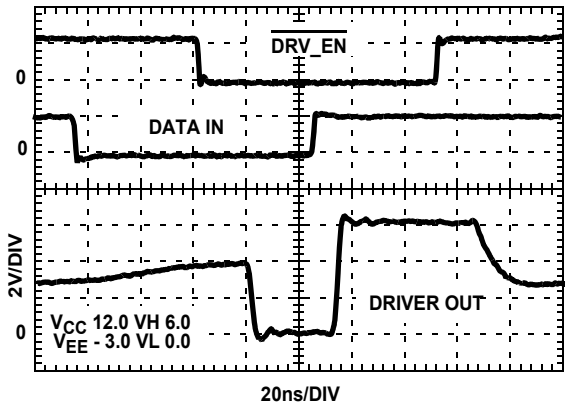


FIGURE 12. DATA AND DRVEN CONTROL OF DRIVER OUT

With HIZ control, driver outputs are only enabled when DRV_EN is in the proper state. If disabled, the DOUT floats. There is ~20ns of propagation delay on the DRV_EN control and ~10ns on the DATA control.

In the above example, the Driver output is tied to a current limited 3.0 voltage source with Drive High Rail of 6.0V and a Low Rail of 0.0V. Your HIZ experiments should include your drive rail voltage values and driver loads

Setting your drive rails to +3 and -3V improves observation of the HIZ operation of the driver. Connect a 1k resistor from DOUT0 to ground. Observe the waveform on DOUT0 with the Generator connected to DATA+0. The DOUT signal should be transitioning from +3 to -3V. This means the driver is always enabled.

Now apply another synchronized pulse to DRV_EN+0. Whenever DRV_EN+0 is low the driver is enabled, and active for either at +3 or -3V. However, when DRV_EN+0 is driven high, the DOUT0 signal goes to HIZ and the 1k DOUT load resistor will pull the output to ground. A 1k load will work when running slow, but as speed increases you have to decrease the value of the load resistor from DOUT0 to ground.

Experiment with the timing of the DATA+0 and DRV_EN+0 while watching the output. Essentially there is ~10ns of propagation delay on the DATA+0 signal, while DRV_EN+0 (HIZ control) takes ~20ns to change the DOUT output. You will also notice that measuring the time to HIZ is a little difficult in that the DOUT floats when in HIZ so the output is slow to reveal that the DOUT drivers are no longer driving the DOUT signal.

ADVANCED HIZ

With the HIZ control you can tie two drivers together. This is often done in memory applications where dual banks are used. Effectively the data is being driven from one driver while the other driver's data is being updated. This enables two drivers/banks of drivers to ping-pong back and forth via the HIZ control. Receivers can also be ganged so the data on one set of receivers is latched and being evaluated while the other receivers are following the inputs waiting for a secondary latching.

The down side of pin muxing is the added capacitance of connecting two drivers together. Added capacitance slows rise and fall times and reduces throughput/bandwidth of the test bus.

DYNAMIC RECEIVER OBSERVATIONS

To observe the receivers at speed, connect a pulse generator directly to the VINP BNCs. Remember there is a 50Ω resistor to ground. R_{29}, R_{32}, R_{33}, and R_{34} are located on the top of the board between the VINP BNC's and the ISL55100.

Essentially you will see the pulse generator signal propagate through to the QA, QB outputs. By changing the amplitude of the pulse generator and the DC Levels on CVA and CVB you can measure the propagation delay through the comparators.

An interesting note is that you can measure rise/fall time with window comparators. Start by setting the pulse generator for 0V to 5V amplitude. You then set the CVB voltage at 0.5V and the CVA voltage at 4.5V. These represent the 10% and 90% amplitude of the 5V pulse.

With QB firing at the 0.5 voltage level and QA firing at the 4.5 voltage level, the difference in the two edges of QA/QB is equal to the 10% to 90% rise/fall time of the pulse.

VDIGC RECEIVER TEST BUS

By using the VDIGC bus you can connect a single source to all four inputs. The VDIGC bus helps with measurements regarding timing and threshold levels. The differences from receiver to receiver can be compared in the configuration. The jumpers that couple the 4 VINP(0 to 3)s to the VDIGC bus are J21, J11, J22 and J23. You can then run a DC level or pulse into the VDIGC banana jack for comparison measurements. When using the VDIGC bus, remember each receiver has a 50Ω load to ground.

Driver to Receiver Loop Back Testing

On most pin electronics designs, there is a user defined series resistor (10Ω to 50Ω) installed between the driver output and the receiver input. This series resistor would be placed between a DOUT BNC and a VINP BNC.You may wish to use various length BNC to BNC cables to provide the loop-back.

Once you've connected a driver to a receiver, you can change the amplitude of the receiver Inputs by changing the VH/VL voltages of the drivers. Remember the 50Ω resistors on the receiver (VINP pins) inputs. You may wish to remove them if you want to run the drivers at higher voltages or with higher load impedance.

ISL55100 UNIQUE FEATURES

/Lowswing Driver Mode

The Lowswing signal improves driver waveforms at low voltages. /Lowswing is available when VH (Driver High Rail) is <5.75V above V_{EE}. You can watch the part automatically change modes as you move the VH voltage above and below 5.75V above V_{EE}. Therefore, connecting /Lowswing to V_{EE} only enables /Lowswing if VH is kept < 5.75V above V_{EE}.

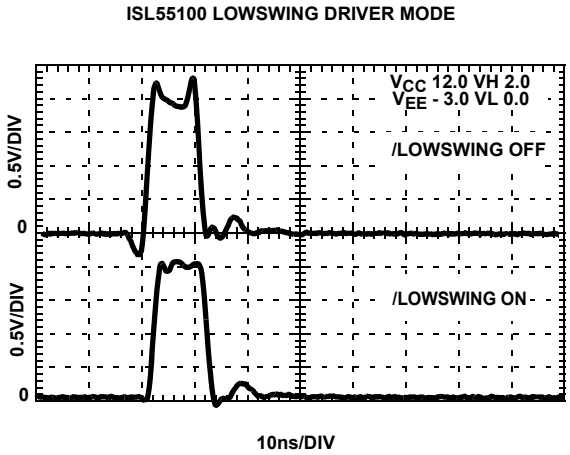


FIGURE 13. LOWSWING CAN BE USEFUL IN SOME APPLICATIONS

/VEXT (V5V Banana Jack) Power Mode

The pin is normally tied to V_{EE} by way of JP29. In this mode, the ISL55100 manufacturers its own internal 5V supply.

However, as speed requirements increase, heat dissipation becomes a problem. Utilizing the VEXT option helps reduce heat dissipation of the ISL55100.

To use the VEXT option, remove JP29 and connect a 5.5V power supply from V_{EE} to V5V banana jack on the evaluation board.

Caution: Do not reference the VEXT power supply to ground. The negative terminal of the external 5.5V supply needs to be connected to V_{EE} so the voltage on VEXT is 5.5V above V_{EE}.

VEXT will require ~25mA quiescent current per ISL55100. However, this requirement will approach 100mA for each device during high frequency operation.

Note: When **not** using VEXT, the minimum voltage from V_{CC} to V_{EE} is 12V. However this drops to 9V when using the VEXT option. Operating at 9.0V reduces power consumption and heat dissipation requirements. But, this also limits the VH drive high rail to the lower V_{CC} potential.

Device Power Observations: VEXT Mode

With a pulse generator connected to DATA+X and the drivers enabled, you will see an increase in power consumption on the VEXT supply along with V_{CC} and V_{EE}. The increase in power will coincide with an increase in frequency. Still, there is an overall heat dissipation savings when using VEXT.

ISL55100A/BEVAL3/3Z Miscellaneous Notes

A complete schematic of the ISL55100A/BEVAL3/3Z Evaluation board is included on the final page of this document.

On the ISL55100A/BEVAL3/3Z Evaluation Board, four voltage busses have been tied across all channels for ease of use. VH(0 to 3), VL(0 to 3), CVA(0 to 3), CVB(0 to 3) signals are all common within themselves. A review of Figure 1 reveals that each channel has separate pin connections for the VH, VL, CVA, CVB functions.

Summary

A typical application for the ISL55100A/BEVAL3/3Z is testing bi-directional bussed based digital devices.

Driver waveforms under user specified loads is one of the first evaluations to be made.

Propagation Delay through the Drivers and Receivers and Time to HIZ are critical timing requirements. Channel-to-channel matching of propagation time is also important.

Power consumption measurements and waveform integrity as Frequency of Operation increases are key in most applications.

The ISL55100A/BEVAL3/3Z Evaluation Board enables the user to view these and other attributes before designing your first ISL55100A/BEVAL3/3Z Pin Electronics Card.

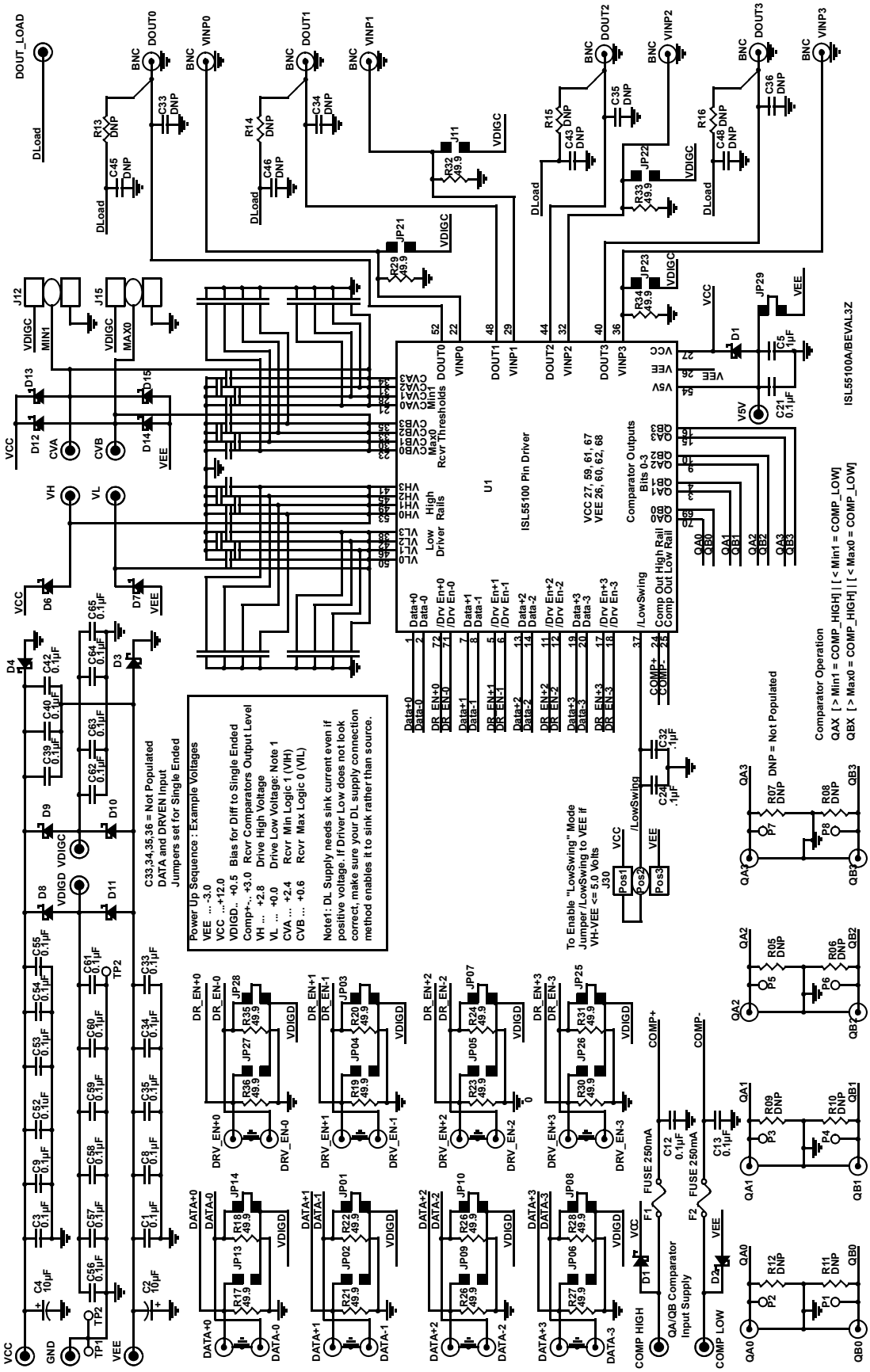


FIGURE 14. ISL55100A/BEVAL3/3Z EVALUATION BOARD SCHEMATIC

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

RENESAS

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 7.0

Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург, Промышленная ул, дом № 19, литера Н, помещение 100-Н Офис 331