MAAP-015036

Power Amplifier, 15 W
8.5 - 10.5 GHz

Rev. V1

Features

- 15 W Power Amplifier
- 42 dBm Saturated Pulsed Output Power
- 17 dB Large Signal Gain
- P_{SAT} >40% Power Added Efficiency
- Dual Sided Bias Architecture
- On Chip Bias Circuit
- 100% On-Wafer DC, RF and Output Power Testing
- 100% Visual Inspection to MIL-STD-883 Method 2010

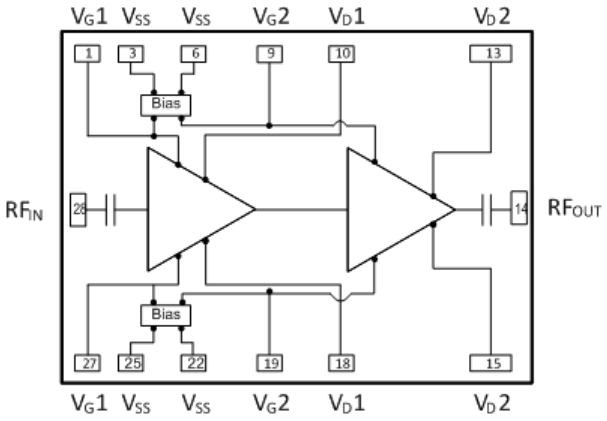
Description

The MAAP-015036 is a two stage GaAs MMIC power amplifier operating from 8.5 - 10.5 GHz, with a saturated pulsed output power of 42 dBm and a large signal gain of 18 dB.

This power amplifier uses GaAs pHEMT device technology and is based upon optical gate lithography to ensure high repeatability and uniformity. The chip has surface passivation for protection and backside via holes and gold metallisation to allow a conductive epoxy die attach process.

This device is well suited for communications, Point to Point radio and radar applications.

Functional Schematic



Pin Configuration[2]

Pad No.	Function	Pad No.	Function
1	V_G1	15	V_D2
2	GND	16	GND
3	$V_{SS}1$	17	GND
4	V_{1_5}	18	V_D1
5	GND	19	V_G2
6	$V_{SS}2$	20	GND
7	V_{2_5}	21	V_{2_5}
8	GND	22	$V_{SS}2$
9	V_G2	23	GND
10	V_D1	24	V_{1_5}
11	GND	25	$V_{SS}1$
12	GND	26	GND
13	V_D2	27	V_G1
14	RF_{OUT}	28	RF_{IN}

2. Backside metal is RF, DC and thermal ground.

Ordering Information

Part Number	Package
MAAP-015036-DIE	Die in Gel Pack[1]
MAAP-015036-DIEEV1	Sample Board Direct Gate Bias
MAAP-015036-DIEEV2	Sample Board On-Chip Gate Bias

1. Die quantity varies.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Power Amplifier, 15 W
8.5 - 10.5 GHz

Electrical Specifications - Pulsed Operation: Duty Cycle = 5%, Pulse = 5 µs, Freq. = 8.5 - 10.5 GHz, T_A = +25°C, Z_0 = 50 Ω, , P_{IN} = 26 dBm, V_G = -0.9 V

Parameter	Units	Min.	Typ.	Max.
Gain (Large Signal)	dB	—	17	—
Gain	dB	—	17	—
Gain Flatness	dB	—	1	—
Input Return Loss	dB	—	-15	—
Output Return Loss	dB	—	-25	—
Saturated Output Power (8.5 - 10.5 GHz) Saturated Output Power (9.0 - 10.0 GHz)	dBm	40.5 41.0	42	—
Power Added Efficiency 8.5 - 9.0 GHz 9.0 - 10.0 GHz 10.0 - 10.5 GHz	%	—	 45 45 43	—
Drain Bias Voltage	V	—	8.0	—
Drain Current	A	3.5	4.8	5.5

Absolute Maximum Ratings[3,4]

Parameter	Absolute Maximum
Input Power	30 dBm
Drain Voltage	+8.5 V
Gate Voltage	-3.0 V < V_G < -0.0 V
Bias Voltage	-6.0 V < V_{SS} < -4.0 V
Drain Current	6 A
Gate Current (Direct Bias)	160 mA
Gate Current (On Chip Bias)	165 mA
Operating Temperature	-40°C to +85°C
Junction Temperature[5,6]	+170°C

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.
5. Operating at nominal conditions with T_J ≤ +160°C will ensure MTTF > 1.0 x 10^6 hours.
6. Typical thermal resistance (Θjc) = 5.7°C/W.

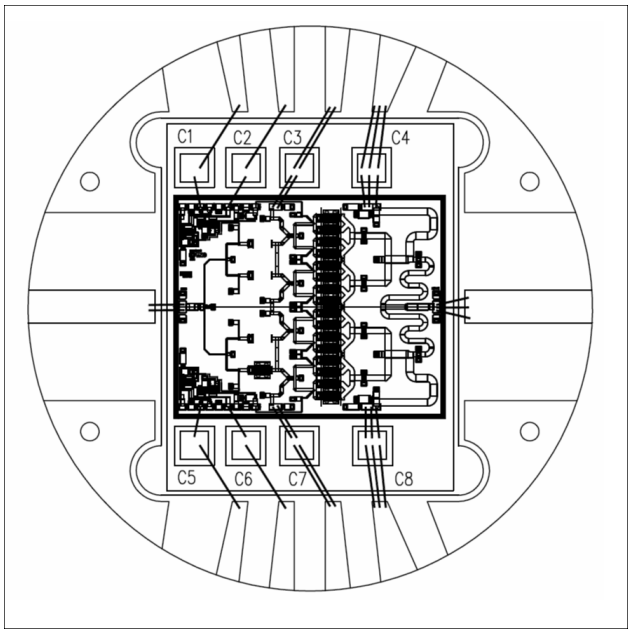
Handling Procedures

Please observe the following precautions to avoid damage:

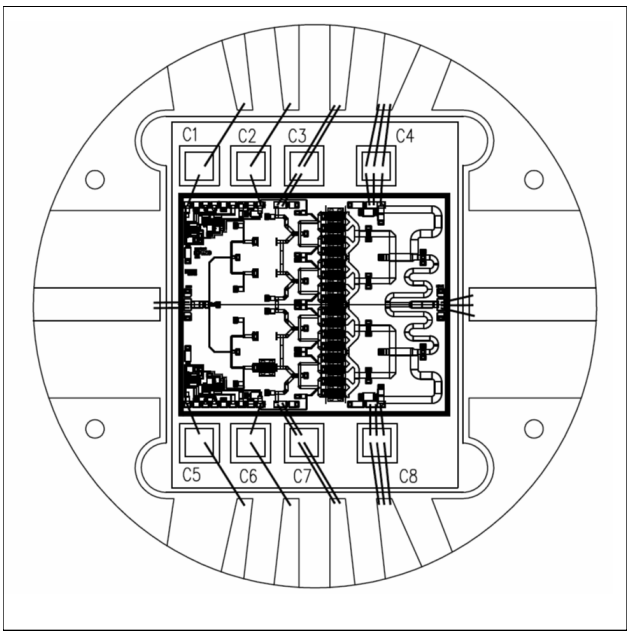
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

Bonding Diagram - On Chip Bias[7]

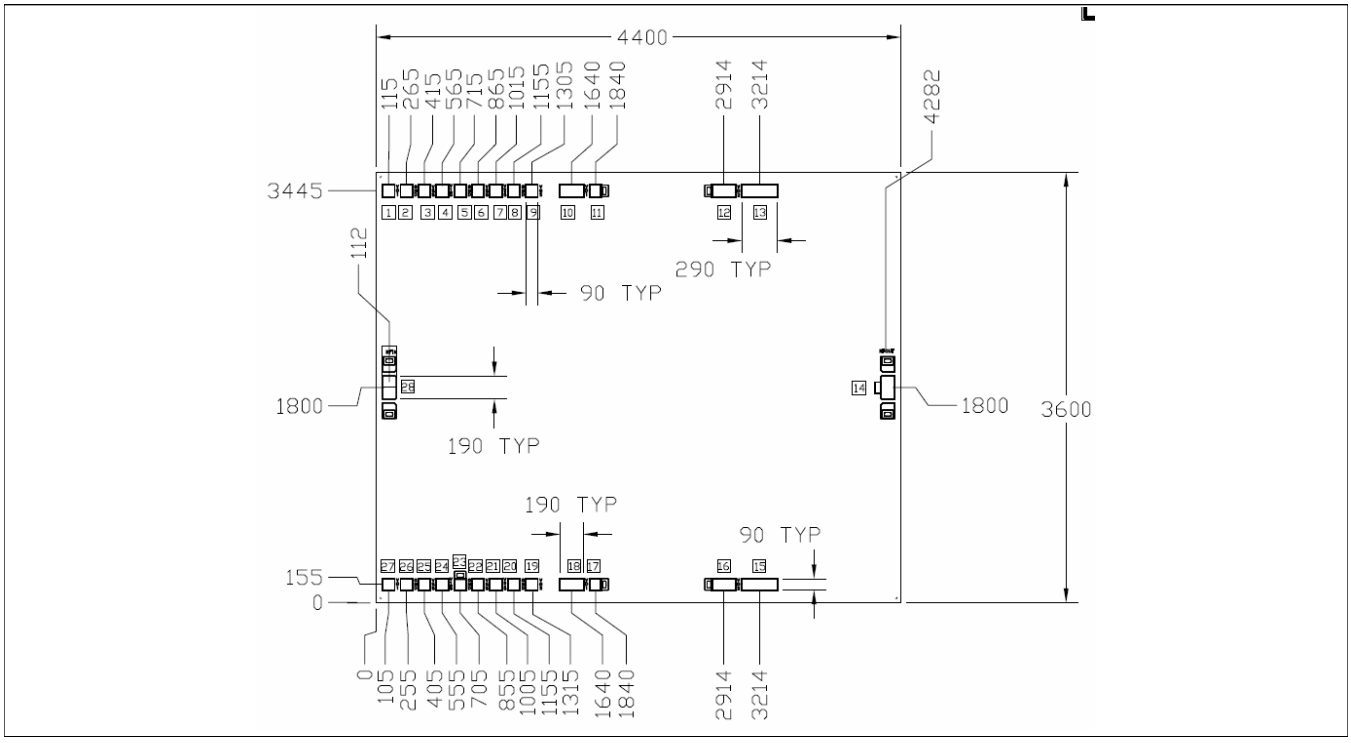


Bonding Diagram - Direct Gate Bias[7]



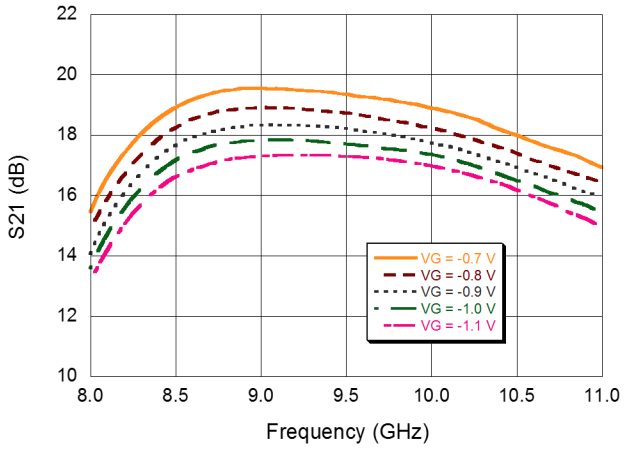
7. Components C1 - C8 are all 120 pF chips.

MMIC Bare Die

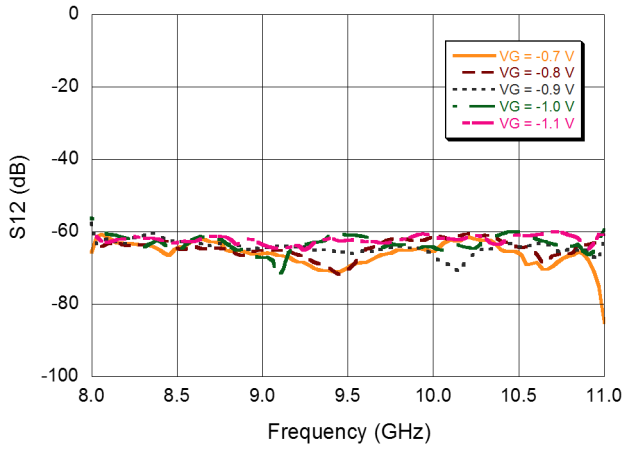


Pulsed Performance Curves over Gate Voltage: V_D = 8 V, Duty Cycle = 5%, Pulse = 5 µs

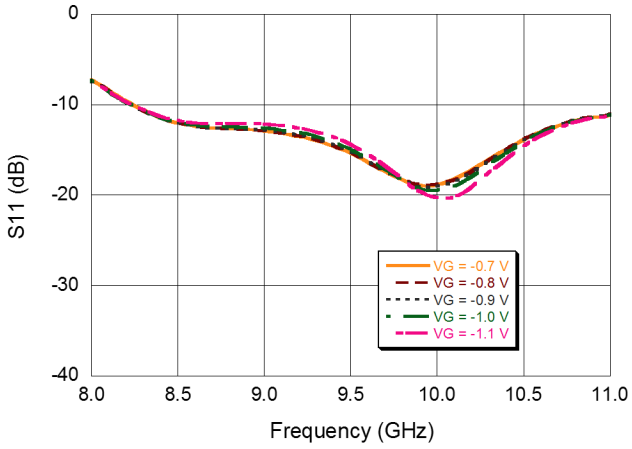
Gain vs. Frequency



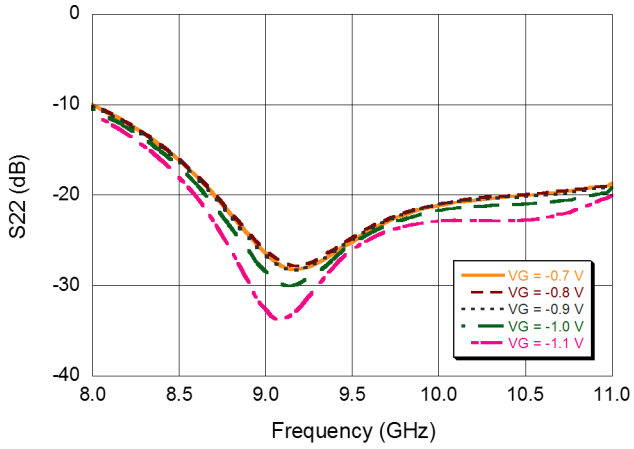
Reverse Isolation vs. Frequency



Input Return Loss vs. Frequency

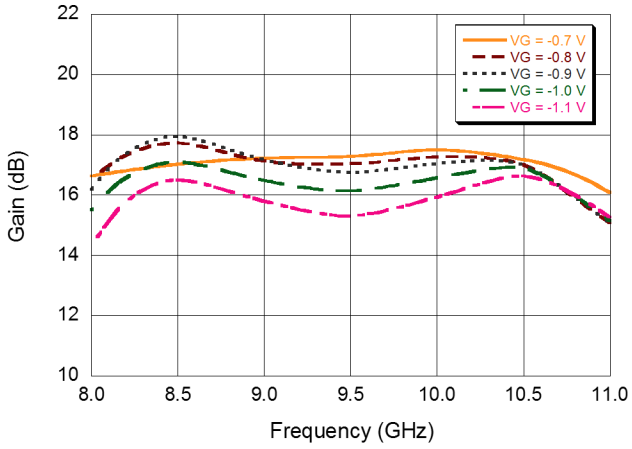


Output Return Loss vs. Frequency

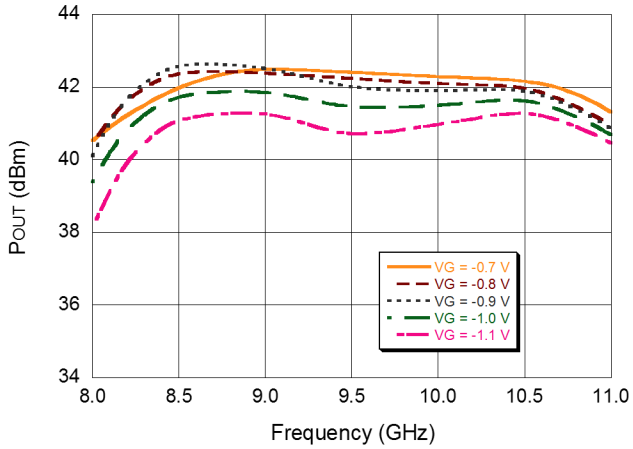


Pulsed Performance Curves over Gate Voltage: P_{IN} = 25 dBm, Duty Cycle = 5%, Pulse = 5 µs

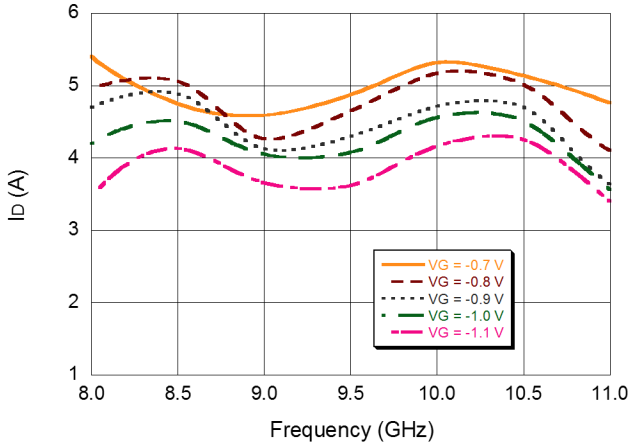
Gain vs. Frequency



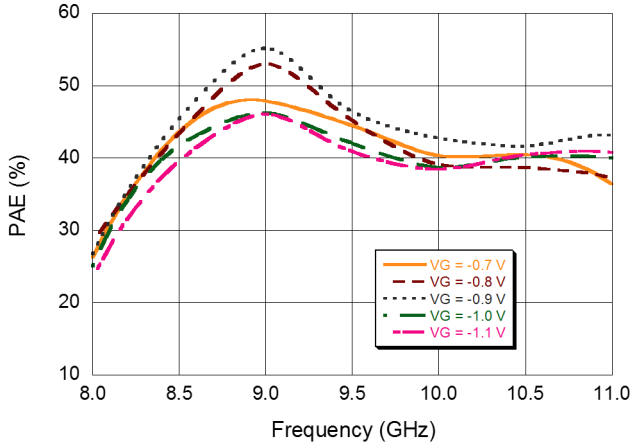
Output Power vs. Frequency



Drain Current vs. Frequency

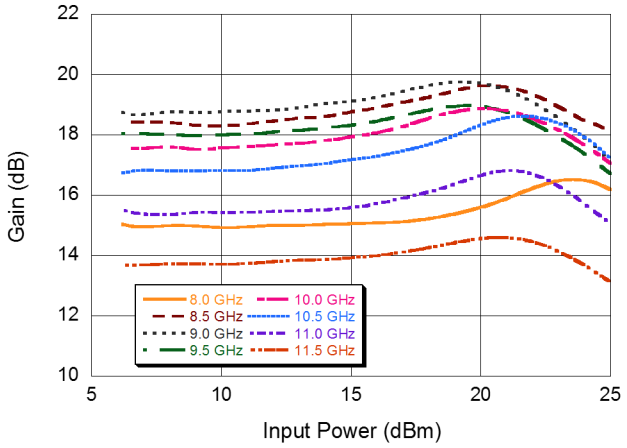


PAE vs. Frequency

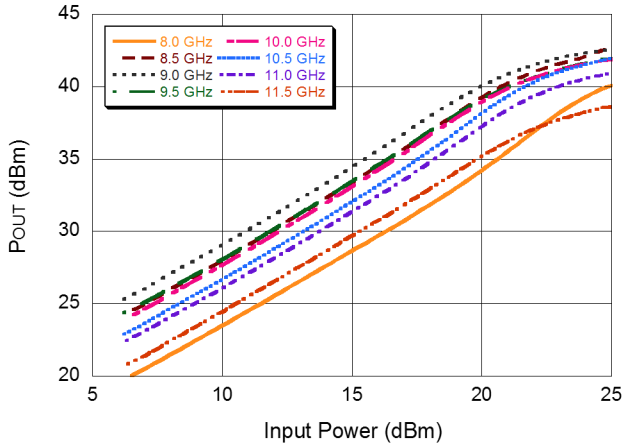


Pulsed Performance Curves over Freq.: V_G = -0.9 V, Duty Cycle = 5%, Pulse = 5 µs

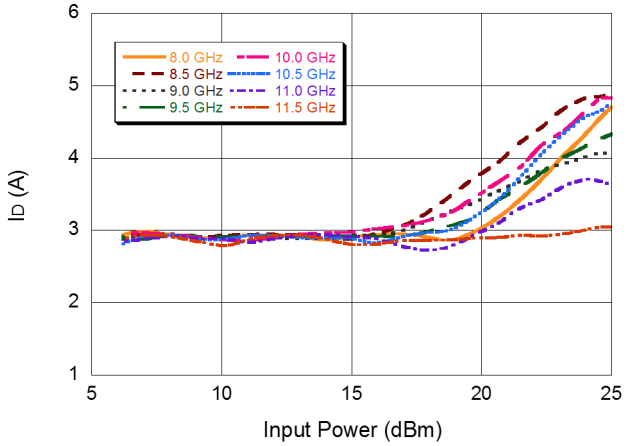
Gain vs. Input Power



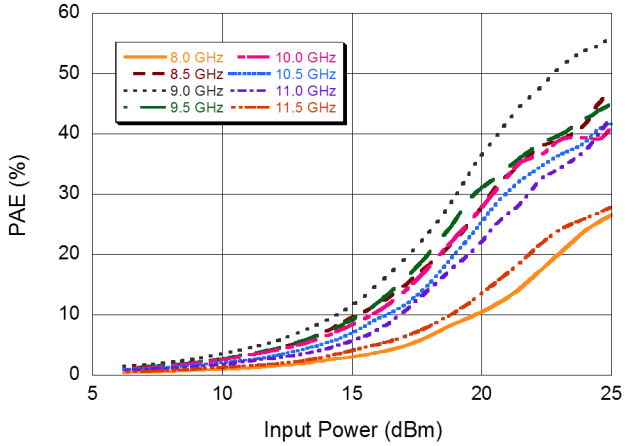
Output Power vs. Input Power



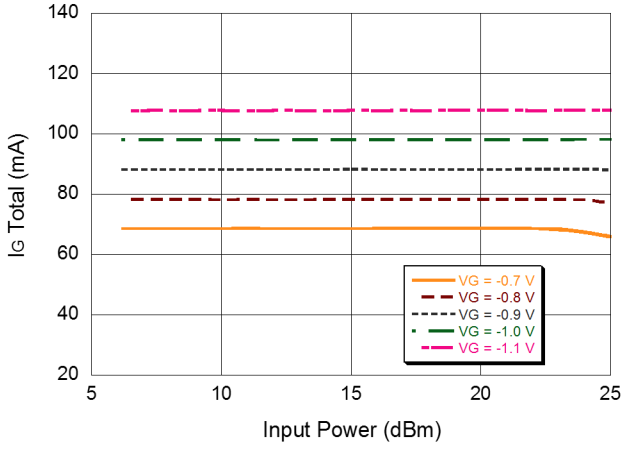
Drain Current vs. Input Power



PAE vs. Input Power

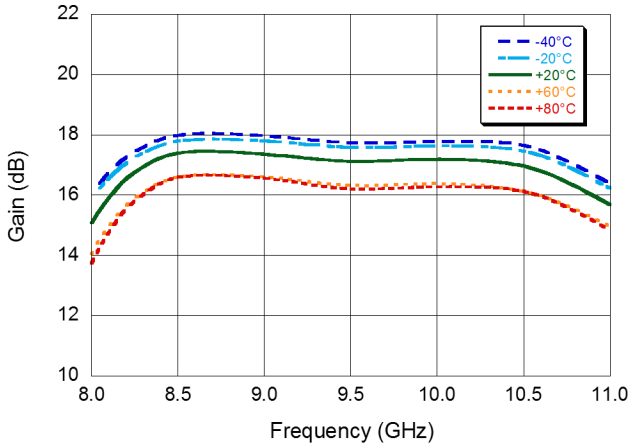


Gate Current vs. Input Power @ 9 GHz

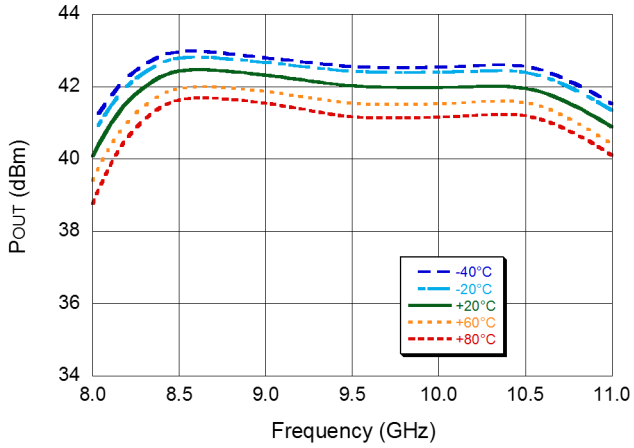


Pulsed Performance Curves over Temperature:
V_G = -0.9 V, P_{IN} = 25 dBm, Duty Cycle = 5%, Pulse = 5 µs

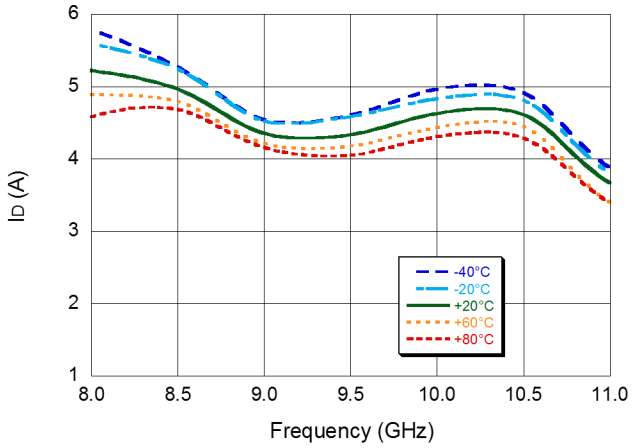
Gain vs. Frequency



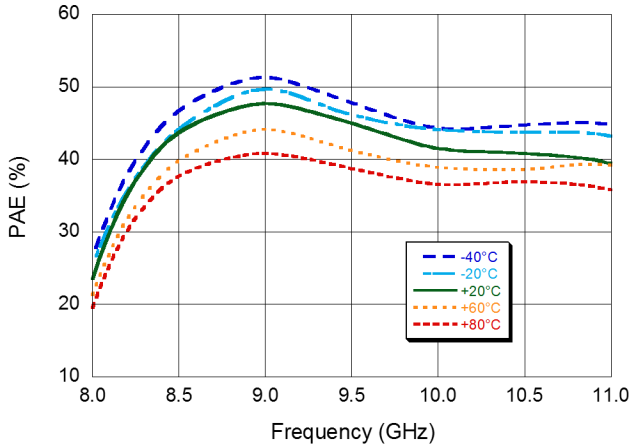
Output Power vs. Frequency



Drain Current vs. Frequency

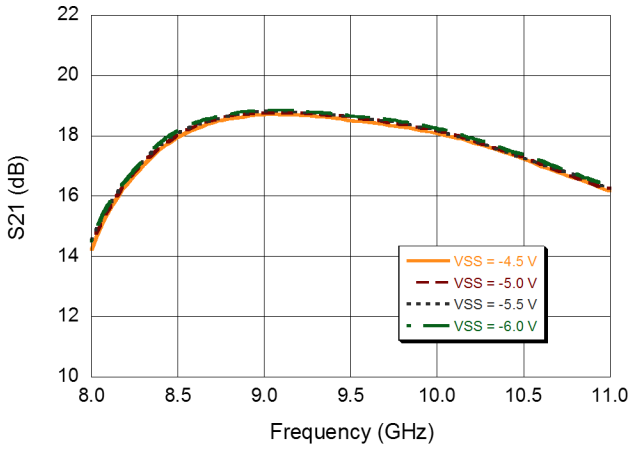


PAE vs. Frequency

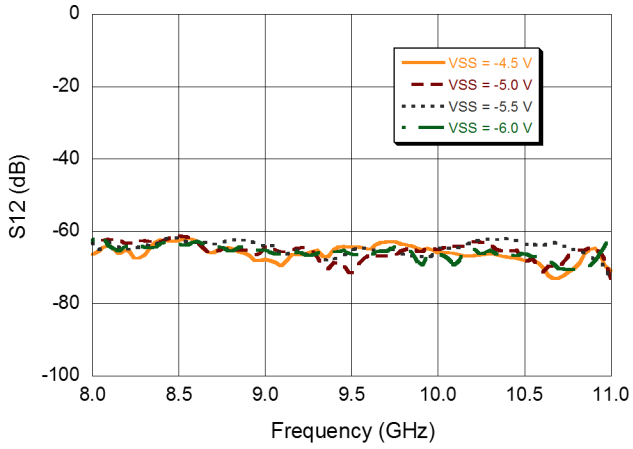


Pulsed Performance Curves over Bias Circuit Voltage, Duty Cycle = 5%, Pulse = 5 µs

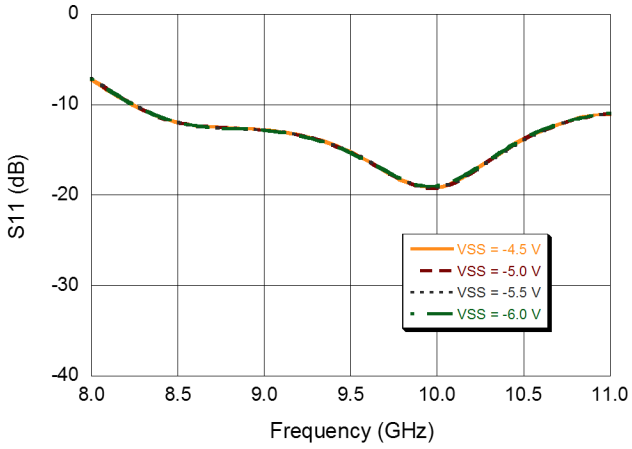
Gain vs. Frequency



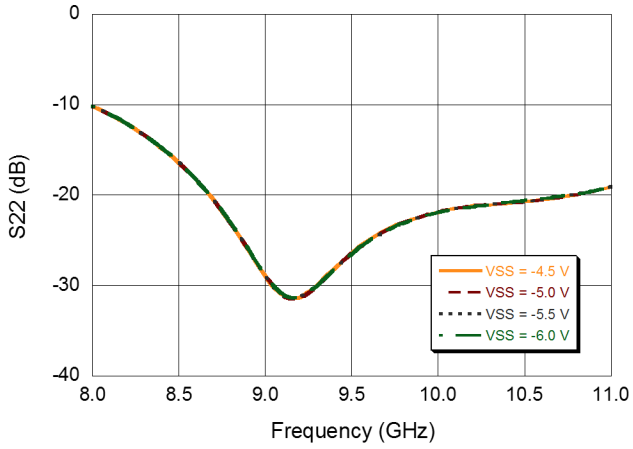
Reverse Isolation vs. Frequency



Input Return Loss vs. Frequency

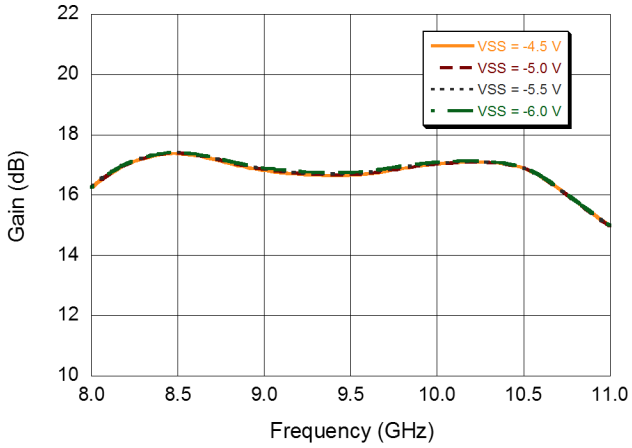


Output Return Loss vs. Frequency

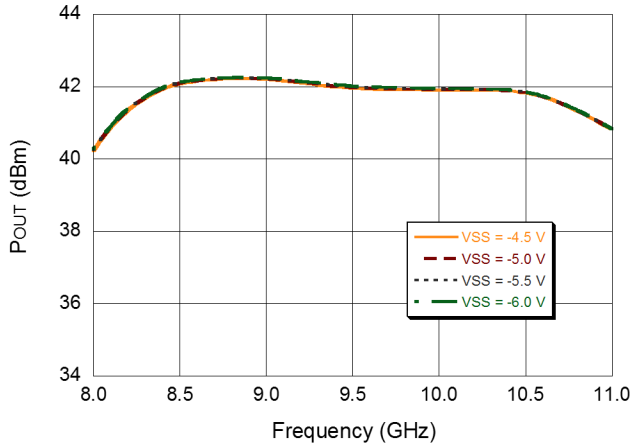


Pulsed Performance Curves over Bias Circuit Voltage :
P_{IN} = 25 dBm, Duty Cycle = 5%, Pulse = 5 µs

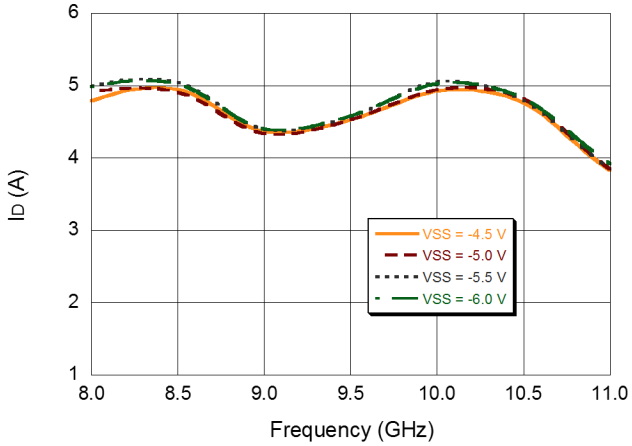
Gain vs. Frequency



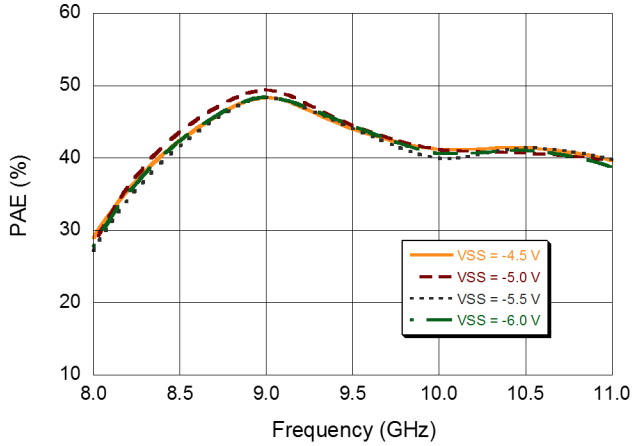
Output Power vs. Frequency



Drain Current vs. Frequency

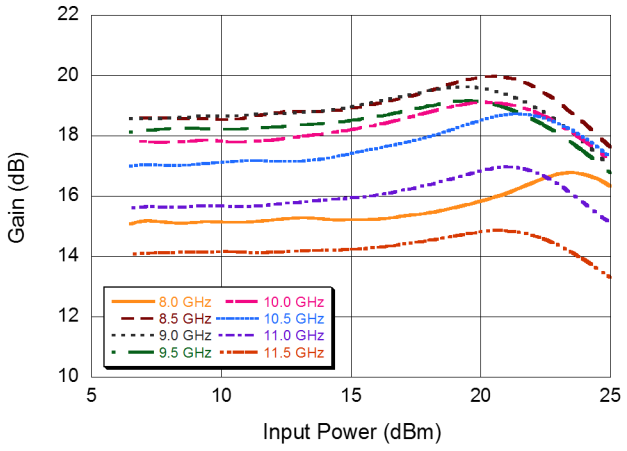


PAE vs. Frequency

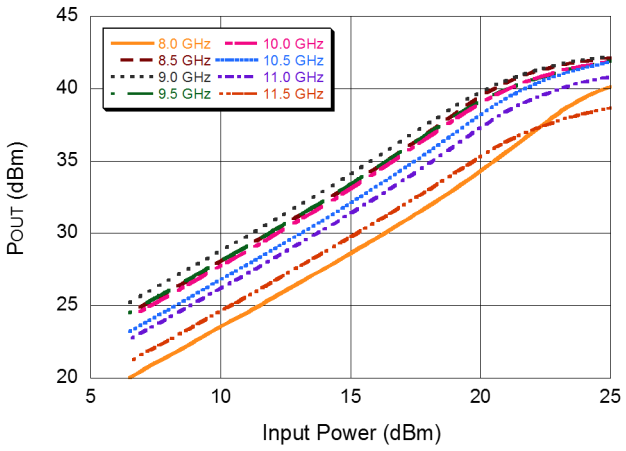


Pulsed Performance Curves over Frequency:
Bias Circuit Voltage = -5 V, Duty Cycle = 5%, Pulse = 5 µs

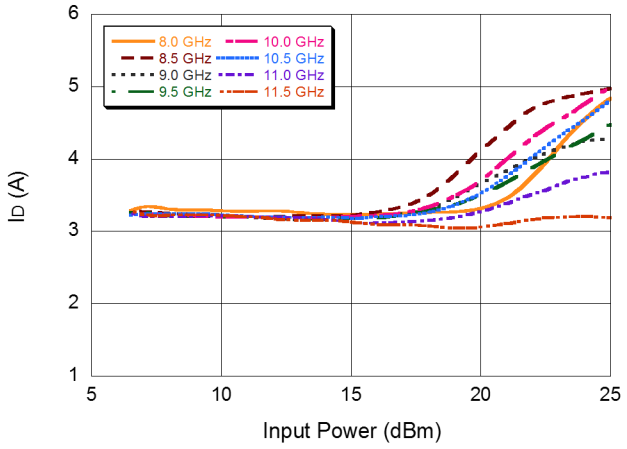
Gain vs. Input Power



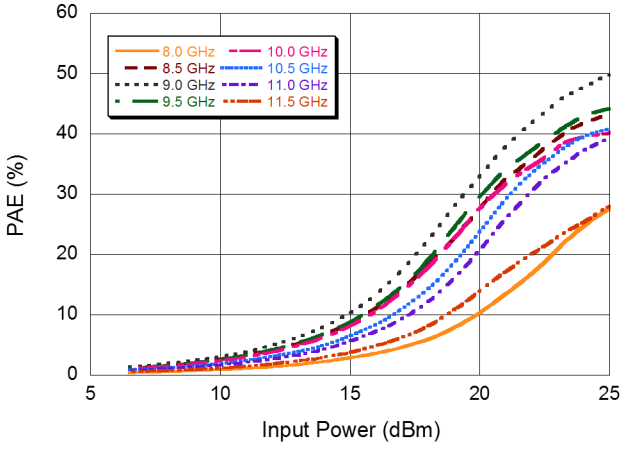
Output Power vs. Input Power



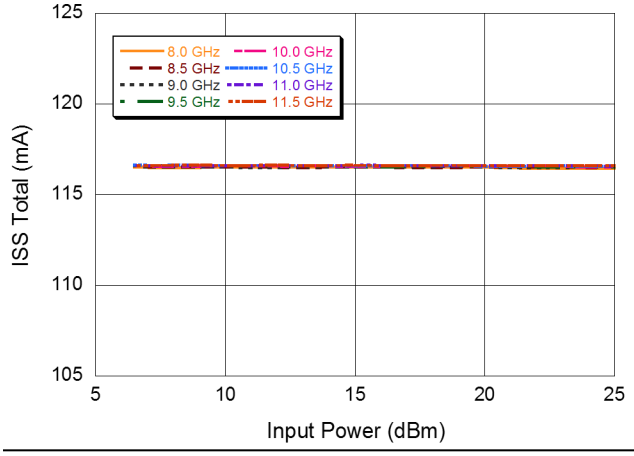
Drain Current vs. Input Power



PAE vs. Input Power



Bias Circuit Current vs. Input Power



Applications Section

Application Notes

Note 1 - Biasing
The gate bias is applied in one of the following:

1. Direct Gate Bias:- V_G1 & V_G2 provide the direct gate bias input to the 2 MMIC stages. This method of biasing allows the user to control the total drain current without the scaling factor provided by the bias circuit . It is recommended that the gate voltage is supplied by both sides of the die. Biasing from one side is optional. Optimum performance can be achieved with a -0.9 V operation.
2. Bias Circuit Biasing:- Applying -5 V to $V_{SS}1$ & $V_{SS}2$, will typically draw 4.5 A with no further adjustment necessary. Wafer lot variation may result in some devices experiencing higher or lower drain currents than the typical 4.5 A. It is recommended that the bias circuits on both sides of the PA are used. Biasing from one side is optional.

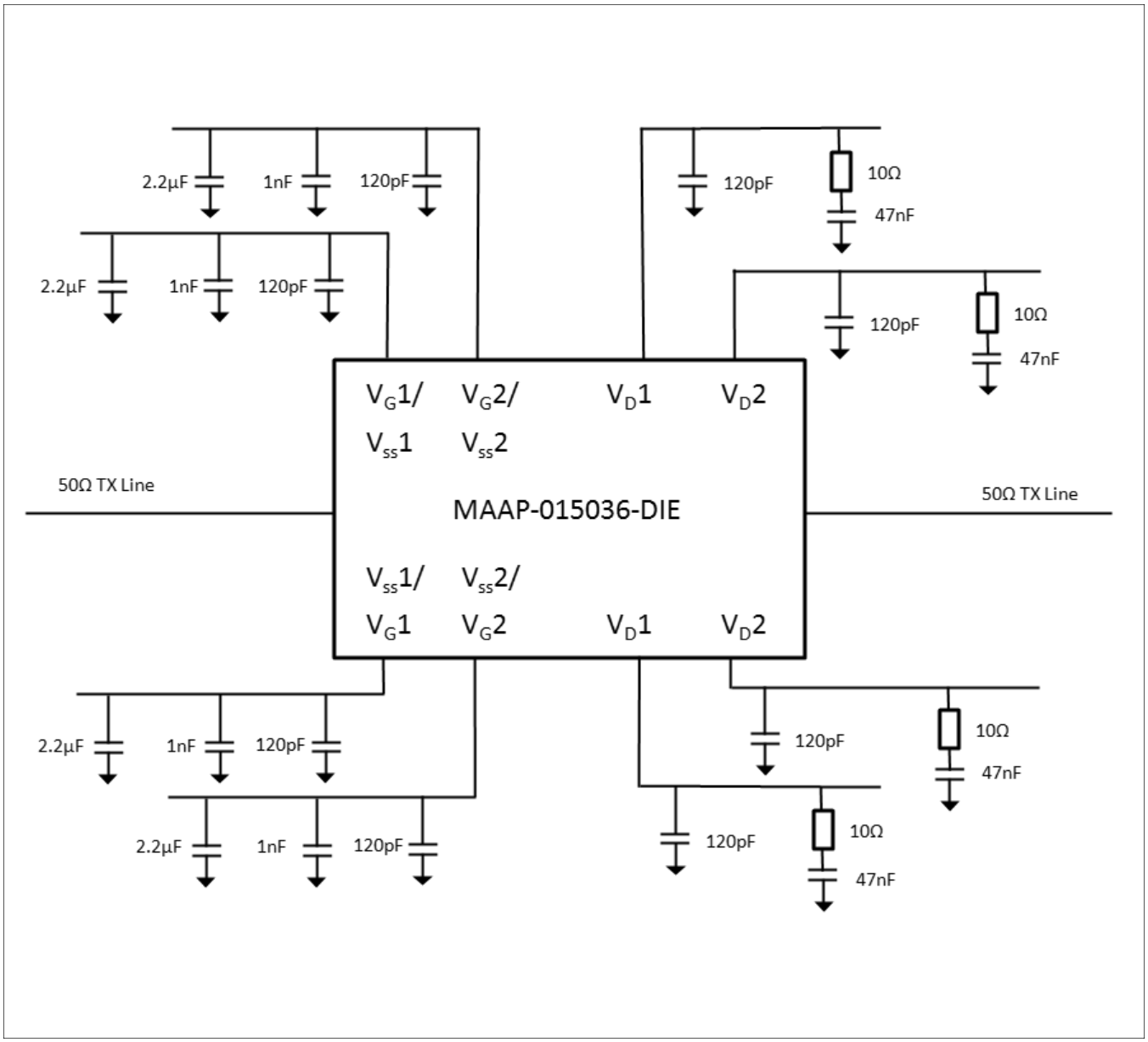
Note 2 - Bias Sequence
When switching on the PA, In each case, the gate bias must be applied before the drain voltage is applied. The drain voltage V_D1 & V_D2 should be biased from the top and bottom sides of the die.

Note 3 - Decoupling Circuits
Each bias pad, V_G, V_{SS} & V_D must have a decoupling capacitor of 120 pF as close to the device as possible, as is shown in the bonding diagrams. Symmetrical decoupling circuits must be maintained on both sides of the die for bias circuit or direct gate bias operation.
Under pulsed operation a large capacitance on the drain will cause a “ringing” effect on the supply voltage. This potentially produces a high voltage at the PA terminals. A recommended decoupling circuit is provided where shunt decoupling capacitors are connected in series with a resistor to minimize this effect.

Note 4 - Pulse Operation
The performance of the MAAP-015036 is characterized under pulsed conditions with a duty cycle of 5% consisting of a pulse width of 5 µS applied to the drain. Under pulsed conditions the gate is constantly biased using either the on chip bias circuit or using a gate voltage directly applied to the PA. It is recommended that the die is mounted with an adequate thermal solution.

Note 5 - Input / Output Transitions
The PA performance must be achieved in a 50 Ω impedance environment on the RF input and output. To maintain performance three bond wires are recommended on the output of the PA each with a maximum length of less than 600 µm. Longer bond wire lengths can be used providing bond pad compensation, in the form of a stub, is used on the application board.

Application Circuit



Applications Section

Handling and Assembly

Die Attachment

This product is manufactured from 0.100 mm (0.004") thick substrate and has vias through to the backside to enable grounding to the circuit. Microstrip substrates should be brought as close to the die as possible and bond wire lengths on the input and output kept as short as possible. The mounting surface should be clean and flat.

If using conductive epoxy, recommended epoxies are Tanaka TS3332LD, Die Mat DM6030HK, Abletherm 2600AT or DM6030HK-Pt cured per the manufacturer's cure schedule. Epoxy should be applied in accordance with the manufacturers specifications and should avoid contact with the top surface of the die. An epoxy fillet should be visible around the total die periphery. For additional information please see the MACOM "Epoxy Specifications for Bare Die" application note.

If eutectic mounting is preferred, then a flux-less gold-tin (AuSn) preform, approximately 0.0012 thick, placed between the die and the attachment surface should be used. A die attach bonder that utilizes a heated collet and provides scrubbing action to ensure total wetting to prevent void formation in a nitrogen atmosphere is recommended. The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280ºC (Note: Gold Germanium should be avoided). The work station temperature should be 310ºC +/-10ºC. Exposure time to these extreme temperatures should be kept to minimum. The die and collet should be pre-heated, to avoid excessive thermal shock during assembly. Avoidance of air bridges and force impact are critical during placement.

Wire Bonding

Windows are provided in the surface passivation above the bond pads to allow wire bonding to the die's gold bond pads. The recommended wire bonding procedure uses 0.076 mm x 0.013 mm (0.003" x 0.0005") 99.99% pure gold ribbon with 0.5-2% elongation to minimize RF port bond inductance. Gold 0.025 mm (0.001") diameter wedge or ball bonds are acceptable for DC Bias connections. Aluminium wire should be avoided. Thermo-compression bonding is recommended though thermo-sonic bonding may be used providing the ultrasonic content of the bond is minimized. Bond force, time and ultrasonic's are all critical parameters. Bonds should be made from the bond pads on the die to the package or substrate. All bonds should be as short as possible.

Стандарт Электрон Связь

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Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

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С нами вы становитесь еще успешнее!

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