

IR21091(S) & (PbF)

HALF-BRIDGE DRIVER

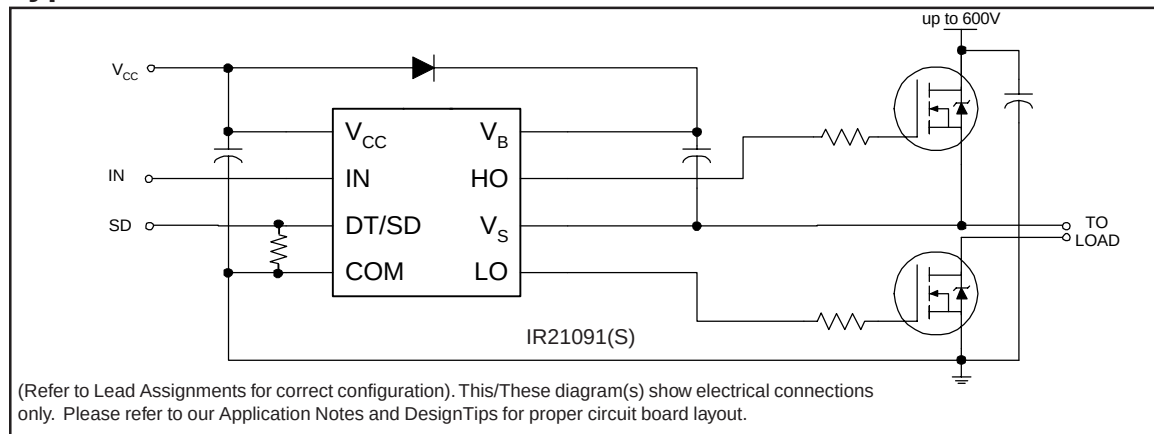
Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High side output in phase with IN input
- Logic and power ground +/- 5V offset.
- Internal 500ns dead-time, and programmable up to 5us with one external R_{DT} resistor
- Lower di/dt gate driver for better noise immunity
- The dual function DT/SD pin input turns off both channels.
- Available in Lead-Free

Description

The IR21091(S) are high voltage, high speed power MOSFET and IGBT drivers with dependant high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

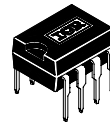
Typical Connection



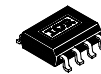
Product Summary

V_{OFFSET}	600V max.
$I_{O+/-}$	120 mA / 250 mA
V_{OUT}	10 - 20V
ton/off (typ.)	680 & 170 ns
Dead time	500 ns
(programmable up to 5us)	

Packages



8 Lead PDIP



8 Lead SOIC

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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating absolute voltage	-0.3	625	V
V _S	High side floating supply offset voltage	V _B - 25	V _B + 0.3	
V _{HO}	High side floating output voltage	V _S - 0.3	V _B + 0.3	
V _{CC}	Low side and logic fixed supply voltage	-0.3	25	
V _{LO}	Low side output voltage	-0.3	V _{CC} + 0.3	
DT/SD	Programmable dead-time and shut-down pin voltage	V _{SS} - 0.3	V _{CC} + 0.3	
V _{IN}	Logic input voltage	V _{SS} - 0.3	V _{CC} + 0.3	
dV _S /dt	Allowable offset supply voltage transient	—	50	V/ns
P _D	Package power dissipation @ T _A ≤ +25°C	—	1.0	W
	(8 Lead PDIP)	—	0.625	
R _{thJA}	Thermal resistance, junction to ambient	—	125	°C/W
	(8 Lead SOIC)	—	200	
T _J	Junction temperature	—	150	°C
T _S	Storage temperature	-50	150	
T _L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply absolute voltage	V _S + 10	V _S + 20	V
V _S	High side floating supply offset voltage	Note 1	600	
V _{HO}	High side floating output voltage	V _S	V _B	
V _{CC}	Low side and logic fixed supply voltage	10	20	
V _{LO}	Low side output voltage	0	V _{CC}	
V _{IN}	Logic input voltage	V _{SS}	V _{CC}	
DT/SD	Programmable dead-time and shut-down pin voltage	V _{SS}	V _{CC}	
T _A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5V to +600V. Logic state held for V_S of -5V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, C_L = 1000 pF, T_A = 25°C, DT = VSS unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	750	950	nsec	$V_S = 0V$
t_{off}	Turn-off propagation delay	—	200	280		$V_S = 0V$ or 600V
MT	Delay matching, HS & LS turn-on/off	—	0	70		
t_r	Turn-on rise time	—	150	220		$V_S = 0V$
t_f	Turn-off fall time	—	50	80		$V_S = 0V$
DT	Deadtime: LO turn-off to HO turn-on(DT _{LO-HO}) & HO turn-off to LO turn-on (DT _{HO-LO})	400	540	680	usec	RDT = 0
		4	5	6		RDT = 200k
MDT	Deadtime matching = DT _{LO} - HO - DT _{HO-LO}	—	0	60	nsec	RDT=0
		—	0	600		RDT = 200k
tsd	Shut down propagation delay	215	—	615		

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, DT= VSS and T_A = 25°C unless otherwise specified. The V_{IL} , V_{IH} and I_{IN} parameters are referenced to V_{SS} /COM and are applicable to the respective input leads: IN and DT. The V_O , I_O and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HO & logic "0" for LO	2.9	—	—	V	$V_{CC} = 10V$ to 20V
V_{IL}	Logic "0" input voltage for HO & logic "1" for LO	—	—	0.8		$V_{CC} = 10V$ to 20V
$V_{SD,TH}$	DT/SD pin shutdown input threshold	11.5	13	14.5		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	0.8	1.4		$I_O = 20$ mA
V_{OL}	Low level output voltage, V_O	—	0.3	0.6		$I_O = 20$ mA
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		$V_{IN} = 0V$ or 5V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	$V_{IN} = 0V$ or 5V RDT = 0
I_{IN+}	Logic "1" input bias current	—	5	20	μA	IN = 5V, SD = 0V
I_{IN-}	Logic "0" input bias current	—	1	2		IN = 0V, SD = 5V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	$V_O = 0V$, PW ≤ 10 μs
I_{O-}	Output low short circuit pulsed current	250	350	—		$V_O = 15V$, PW ≤ 10 μs

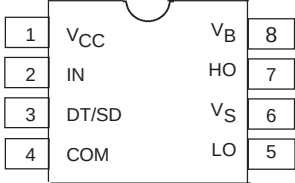
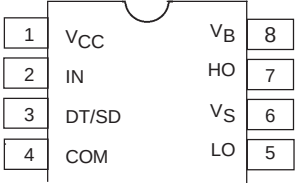
The schematic diagram of the IR21091(S) UV detector circuit is as follows:

- Inputs:** The circuit has two inputs: **IN** and **DT/SD**.
- IN Path:** The **IN** signal passes through a resistor and a buffer (represented by a triangle with a 'u' inside) to the **DEADTIME** block.
- DT/SD Path:** The **DT/SD** signal passes through a resistor to the **DEADTIME** block.
- DEADTIME Block:** This block has two outputs. One output goes to the **VSS/COM LEVEL SHIFT** block, and the other goes to the **UV DETECT** block.
- VSS/COM LEVEL SHIFT Blocks:** There are two such blocks. The first one receives input from the **DEADTIME** block and the **UV DETECT** block. Its output goes to the **PULSE GENERATOR** block. The second **VSS/COM LEVEL SHIFT** block receives input from the **DEADTIME** block and the **UV DETECT** block. Its output goes to the **DELAY** block.
- PULSE GENERATOR:** This block has two outputs. One output goes to the **HV LEVEL SHIFTER** block, and the other goes to the **UV DETECT** block.
- HV LEVEL SHIFTER:** This block has two outputs. One output goes to the **PULSE FILTER** block, and the other goes to the **UV DETECT** block.
- PULSE FILTER:** This block has two outputs. One output goes to the **UV DETECT** block, and the other goes to the **UV DETECT** block.
- UV DETECT Blocks:** There are two **UV DETECT** blocks. The first one receives input from the **PULSE GENERATOR** and the **PULSE FILTER**. Its output goes to the **UV DETECT** block. The second **UV DETECT** block receives input from the **DEADTIME** and the **UV DETECT** block. Its output goes to the **UV DETECT** block.
- Output Stage:** The output of the **UV DETECT** block is connected to the **Q** input of an SR flip-flop. The **R** and **S** inputs of the flip-flop are connected to the **UV DETECT** block. The **Q** output of the flip-flop is connected to the **HO** output. The **Q** output of the flip-flop is also connected to the **UV DETECT** block.
- Power and Ground:** The circuit is powered by **VCC** and **COM**. The **COM** pin is connected to ground. The **VCC** pin is connected to the **UV DETECT** block. The **UV DETECT** block is also connected to ground.

Lead Definitions

Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO
DT/SD	Programmable dead-time lead, referenced to VSS. Disables input/output logic when tied to VCC
V _B	High side floating supply
HO	High side gate drive output
V _S	High side floating supply return
V _{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

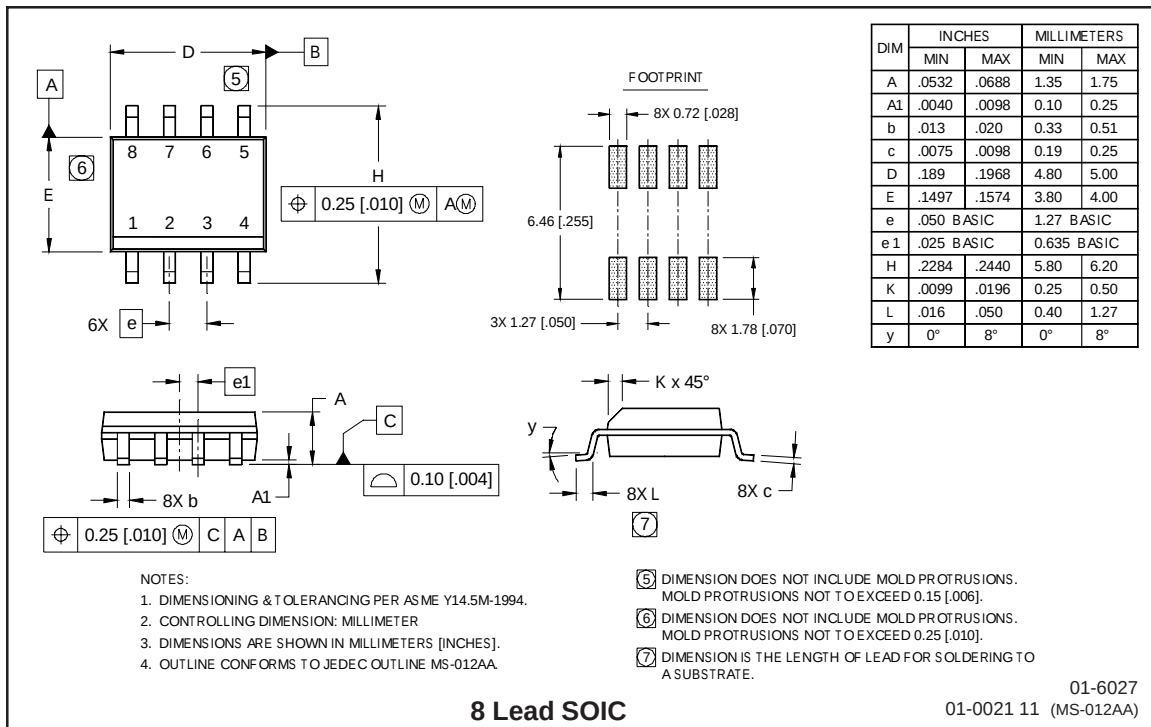
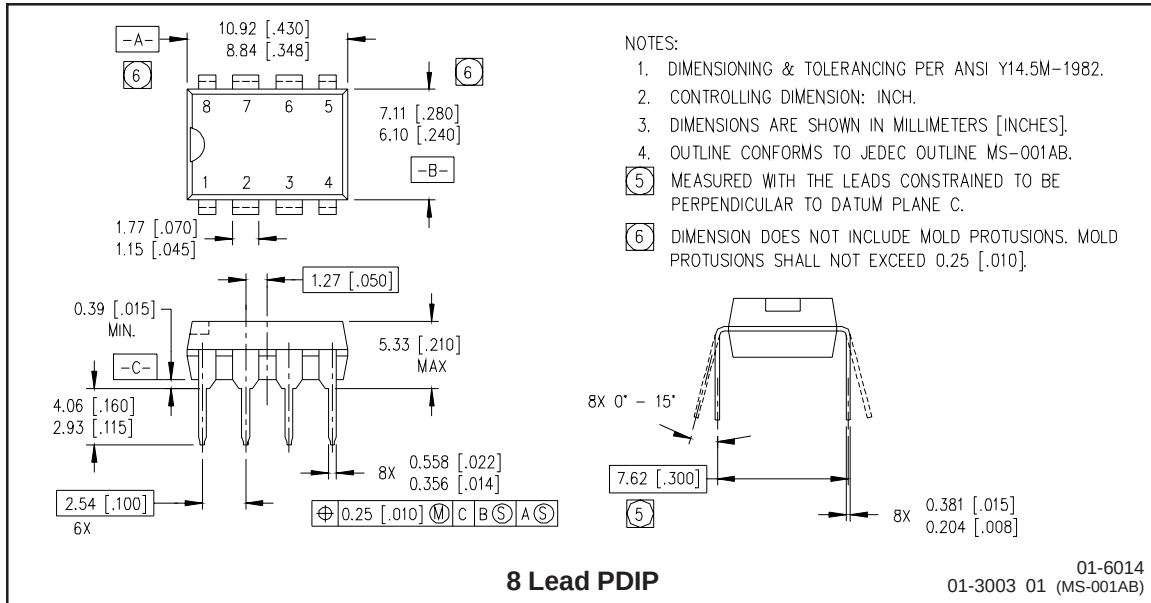
Lead Assignments

 8 Lead PDIP	 8 Lead SOIC
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Case Outlines



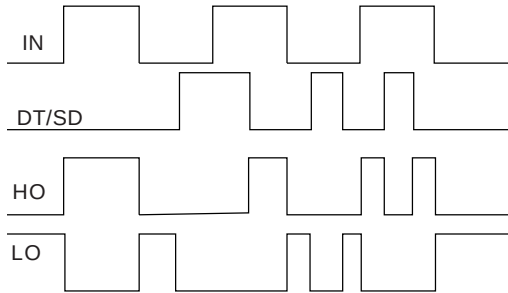


Figure 1. Input/Output Timing Diagram

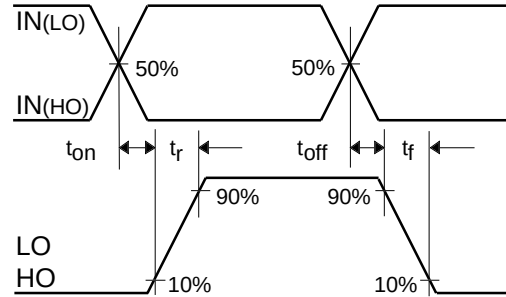


Figure 2. Switching Time Waveform Definitions

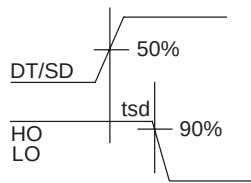


Figure 3. Shutdown Waveform Definitions

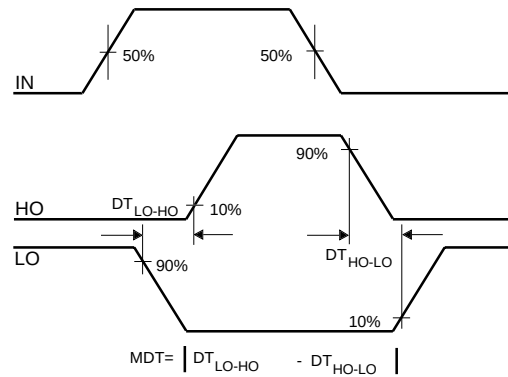


Figure 4. Deadtime Waveform Definitions

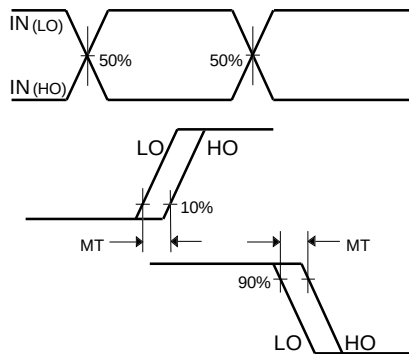
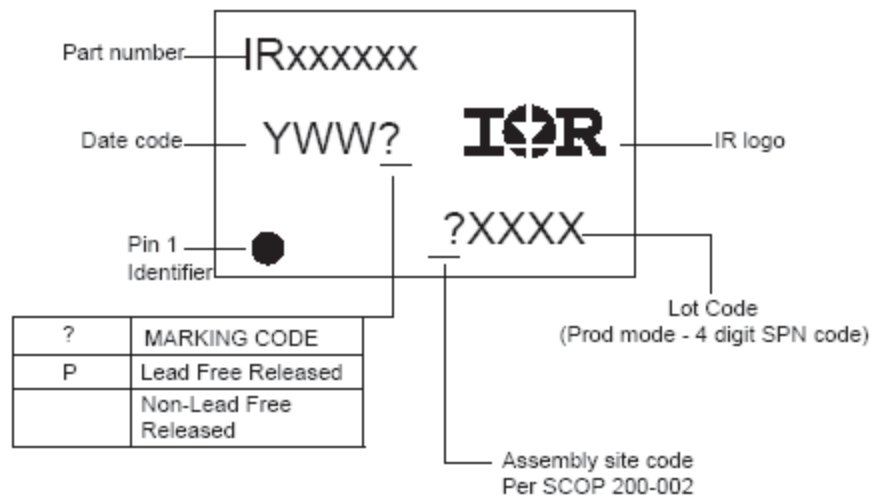


Figure 5. Delay Matching Waveform Definitions

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LEADFREE PART MARKING INFORMATION



Basic Part (Non-Lead Free)

8-Lead PDIP IR21091 order IR21091
8-Lead SOIC IR21091S order IR21091S

Lead-Free Part

8-Lead PDIP IR21091 order IR21091PBF
8-Lead SOIC IR21091S order IR21091SPBF

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This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Website.
Data and specifications subject to change without notice.

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