AP0202AT High-Dynamic Range (HDR) Image Signal Processor (ISP)

AP0202AT Datasheet, Rev. 4

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Features

- Up to 2.0 Mp (1920x1080) ON Semiconductor sensor support
- 30 fps at 1080p, 45 fps at 1.2Mp, 60 fps at 720p (Optimized for operation with HDR sensors)
- Color and gamma correction
- Auto exposure, auto white balance, 50/60 Hz auto flicker detection and avoidance
- Adaptive Local Tone Mapping (ALTM)
- Two-wire serial programming interface (CCIS)
- Parallel output
- Configurable through low-cost SPI Flash and EEPROM devices
- High-level host command interface
- Standalone operation supported
- Up to 7 GPIO
- Fail-safe IO
- Multi-Camera synchronization support

Applications

- Surround, rear and front view cameras
- Blind spot / side mirror replacement cameras
- Automotive viewing/processing fusion cameras

Table 1: Key Performance Parameters

Parameter	Value	
Image sensor interfaces	Parallel and HiSPi	
Input Data FOrmat	Parallel: 12 bit SDR (linear) or 12 bit HDR companded. HiSPI: 12 bit SDR (linear) or 12/14 bit HDR companded	
Output interface	Up to 24-bit parallel[1]	
Output format	RGB888, RGB565, YUV422 8-/10-bit[1]	
Maximum resolution	1920 x 1080 (2.0 Mp)	
Input clock range	10 - 29 MHz	
Output pixel clock maximum	125 MHz[2]	
Supply voltage	V_{DDIO_S}	1.8 or 2.8 V nominal
	V_{DDIO_H}	1.8 or 2.8 or 3.3 V nominal
	V_{DD_REG}	1.8 V nominal
	V_{DD}	1.2 V nominal
	V_{DD_PLL}	1.2 V nominal
	V_{DD_PHY}	2.8 V nominal
	V_{DDIO_OTPM}	2.5 to 3.3 V nominal
Operating temp. (Ambient)	–40°C to +105°C	
Power consumption	250 mW	

Notes: 1. Maximum frame rates depend on output interface and data format configuration used.
2. Maximum pixel clock rates depend on IO voltage.

Ordering Information

Table 2: Available Part Numbers

Part Number	Product Description	**Orderable Product Attribute Description**
AP0202AT2L00XPGA0-DR	Co-Processor, 100-ball VFBGA	Drypack
AP0202AT2L00XPGA0-TR	Co-Processor, 100-ball VFBGA	Tape and Reel
AP0202AT2L00XPGAD3-GEVK	AP0202AT Demo Kit	
AP0202AT2L00XPGAH3-GEVB	AP0202AT Head Board	

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General Description

ON Semiconductor's AP0202AT Image Signal Processor (ISP) is optimized for use with HDR (High Dynamic Range) sensors. The AP0202AT provides full auto-functions support (AWB and AE) and ALTM (Adaptive Local Tone Mapping) to enhance HDR images and advanced noise reduction which enables excellent low-light performance.

Functional Overview

Figure 1 shows the typical configuration of the AP0202AT in a camera system. On the host side, a two-wire serial or SPI interface is used to configure the operation of the AP0202AT, and image data is transferred using the parallel interface between the AP0202AT and the host. The AP0202AT interface to the sensor supports a parallel interface or HiSPi interface.

Figure 1: AP0202AT Connectivity

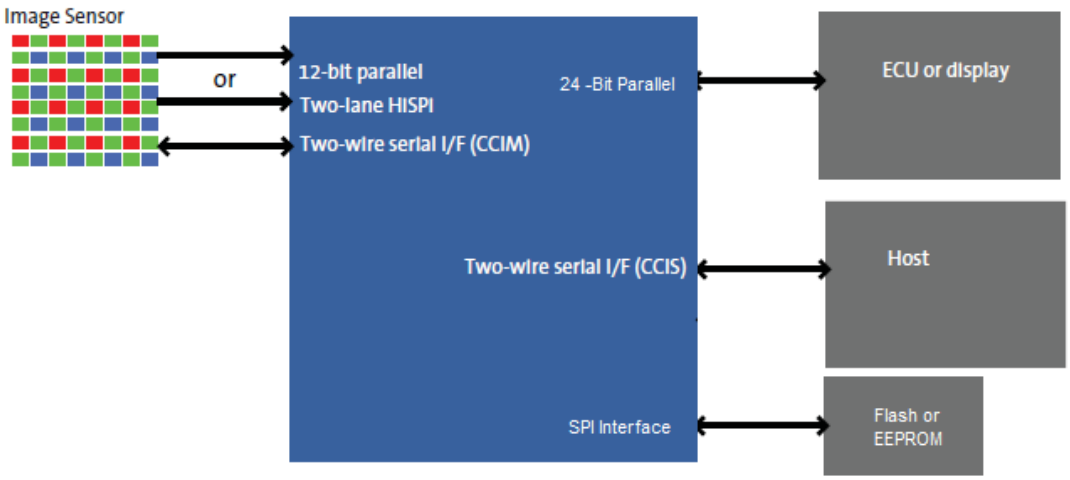
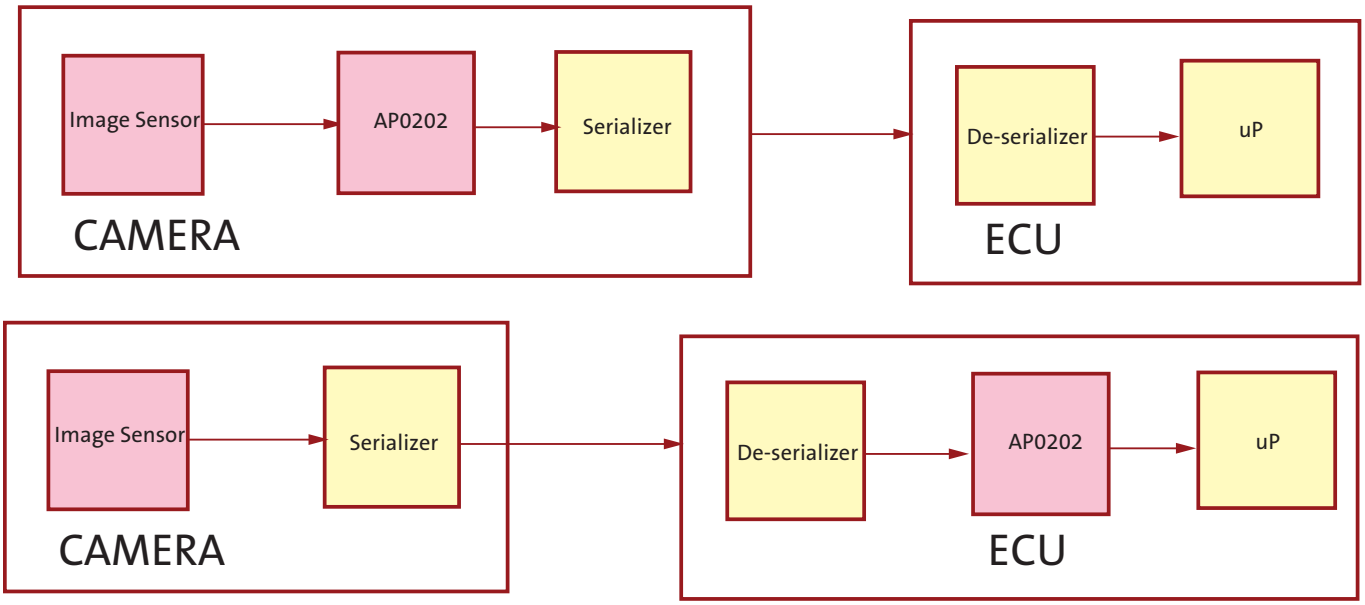


Figure 2: Examples AP0202AT Connectivity



The AP0202AT also supports a Serializer and Deserializer between the sensor and ISP. The AP0202AT supports clock stretching on the slave 2-wire interface.

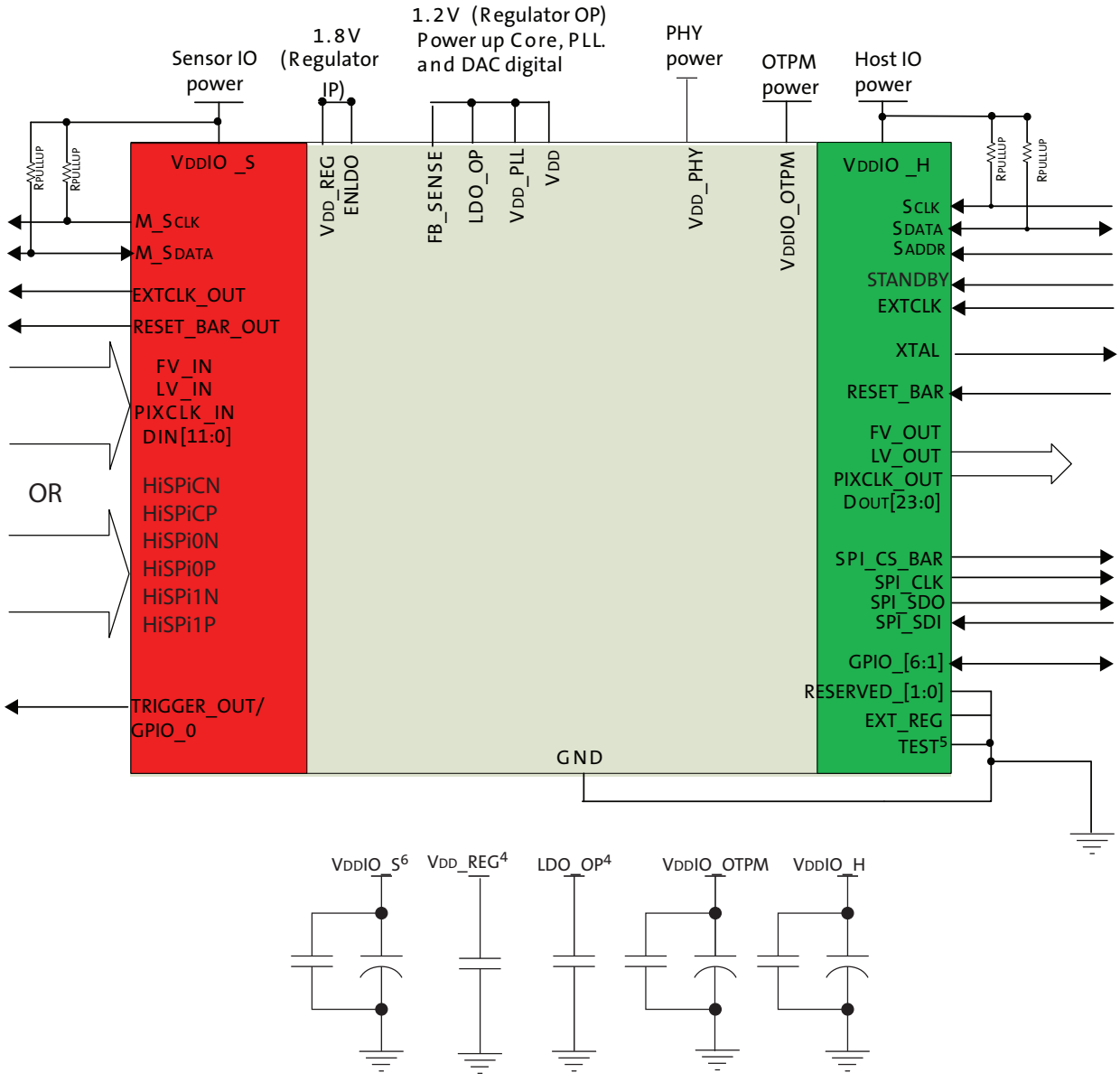
System Interfaces

Figure 3 shows typical AP0202AT device connections.

All power supply rails must be decoupled from ground using capacitors as close as possible to the package.

The AP0202AT signals to the sensor and host interfaces can be at different supply voltage levels to optimize power consumption and maximize flexibility. Table 3 on page 11 provides the signal descriptions for the AP0202AT.

Figure 3: Typical Parallel Configuration - Legacy Mode



Notes: 1. This typical configuration shows only one scenario out of multiple possible variations for this device.

2. ON Semiconductor recommends a 1.5kΩ resistor value for the two-wire serial interface RPULL-UP; however, greater values may be used for slower transmission speed.
3. RESET_BAR has an internal pull-up resistor and can be left floating if not used.
4. The decoupling capacitors for the regulator input and output should have a value of 1.0uF. The capacitors should be ceramic and need to have X5R or X7R dielectric.
5. TEST and RESERVED_[1:0] connect to GND for normal operation.
6. ON Semiconductor recommends that 0.1μF and 1μF decoupling capacitors for each power supply are mounted as close as possible to the pin. Actual values and numbers may vary depending on lay-out and design consideration.
7. The diagram is showing Legacy mode. If Crossbar is used, the 27 parallel outputs can be assigned to any pin. Refer to crossbar section for more details.

HiSPi and Parallel Connection

When using the HiSPi interface, connect the parallel interface to VDDIO_S.

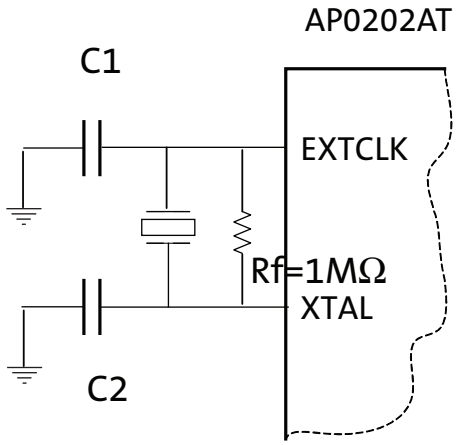
When using the parallel interface, it is recommended for the HiSPi interface to be connected to ground, and the power supply (VDD_PHY) to be connected to +2.8V. Floating these pins is allowed as well.

Crystal Usage

As an alternative to using an external oscillator, a crystal may be connected between EXTCLK and XTAL. Two small loading capacitors and a feedback resistor should be added, as shown in Figure 4.

For applications above 85°C, ON Semiconductor does not recommend using the crystal option. A crystal oscillator with temperature compensation is recommended for applications that require this.

Figure 4: Using a Crystal Instead of an External Oscillator



Rf represents the feedback resistor, an Rf value of 1MΩ is sufficient for AP0202AT. C1 and C2 are decided according to the crystal or resonator CL specification. In the steady state of oscillation, CL is defined as (C1 x C2)/(C1+C2). In fact, the I/O ports, the bond pad, package pin and PCB traces all contribute the parasitic capacitance to C1 and C2. Therefore, CL can be rewritten to be (C1* x C2*)/(C1*+C2*), where C1*=(C1+CIN, STRAY) and

C2*=(C2+$C_{OUT, STRAY}$). The stray capacitance for the IO ports, bond pad and package pin are known which means the formulas can be rewritten as C1*=(C1+1.5pF+$C_{IN, PCB}$) and C2*=(C2+1.3pF+$C_{OUT, PCB}$).

Pin Descriptions

Table 3: Pin Descriptions

Name	Type	Description
EXTCLK	Input	Master input clock. This can either be a square-wave generated from an oscillator (in which case the XTAL input must be left unconnected) or direct connection to a crystal.
XTAL	Output	If EXTCLK is connected to one pin of a crystal, the other pin of the crystal is connected to XTAL pin; otherwise this signal must be left unconnected.
RESET_BAR	Input/PU	Master reset signal, active LOW. This signal has an internal pull up.
SCLK	Input	Two-wire serial interface clock (host interface).
SDATA	I/O	Two-wire serial interface data (host interface).
SADDR	Input	Selects device address for the two-wire slave serial interface. When connected to GND the device ID is 0x90. When wired to VDDIO_H, a device ID of 0xBA is selected.
FRAME_SYNC	Input	Pass through to TRIGGER_OUT. This signal should be connected to GND if not used.
STANDBY	Input	Standby mode control, active HIGH.
EXT_REG	Input	Select external regulator if tied high
ENDLO	Input	Regulator enable (VDD_REG domain)
SPI_SCLK	Output	Clock output for interfacing to an external SPI flash or EEPROM memory.
SPI_SDI	Input	Data in from SPI flash or EEPROM memory. When no SPI device is fitted, this signal is used to determine whether the AP0202AT should auto-configure: 0: Do not auto-configure; Two-wire interface will be used to configure the device (host-config mode) 1: Auto-configure. This signal has an internal pull-up resistor.
SPI_SDO	Output	Data out to SPI flash or EEPROM memory.
SPI_CS_BAR	Output	Chip select out to SPI flash or EEPROM memory.
EXT_CLK_OUT	Output	Clock to external sensor.
RESET_BAR_OUT	Output	Reset signal to external signal.
M_SCLK	Output	Two-wire serial interface clock (Master).
M_SDATA	I/O	Two-wire serial interface clock (Master).
FV_IN	Input	Sensor frame valid input.
LV_IN	Input	Sensor line valid input.
PIXCLK_IN	Input	Sensor pixel clock input.
DIN[11:0]	Input	Sensor pixel data input DIN[11:0]
HiSPiCN	Input	Differential HiSPi clock (negative).
HiSPiCP	Input	Differential HiSPi clock (positive).
HiSPi0N	Input	Differential HiSPi data, lane 0 (negative).
HiSPi0P	Input	Differential HiSPi data, lane 0 (positive).
HiSPi1N	Input	Differential HiSPi data, lane 1 (negative).
HiSPi1P	Input	Differential HiSPi data, lane 1 (positive).
TRIGGER_OUT/GPIO_0	Output	Trigger signal for external sensor.
FV_OUT	Output	Host frame valid output (synchronous to PIXCLK_OUT)
META_LINE_VALID	Output	Line valid signal to indicate when Metadata is valid. In addition, there is a variable option to allow META_LINE_VALID to be reflected in LV_OUT
LV_OUT	Output	Host line valid output (synchronous to PIXCLK_OUT)
PIXCLK_OUT	Output	Host pixel clock output.
DOUT[23:0]	Output	Host pixel data output (synchronous to H_PIXCLK_OUT) .

Table 3: Pin Descriptions

Name	Type	Description
GPIO_[6:1]	I/O	General purpose digital I/O.
TEST	Input	Must be tied to GND in normal operation.
RESERVED_[1:0]	Input	Must be tied to GND in normal operation.
VDDIO_S	Supply	Sensor I/O power supply.
VDDIO_H	Supply	Host I/O power supply.
VDD_PLL	Supply	PLL supply.
VDD	Supply	Core supply.
VDDIO_OTPM	Supply	OTPM power supply.
VDD_PHY	Supply	PHY IO voltage for HiSPi
GND	Supply	Ground
VDD_REG	Supply	Input to on-chip 1.8V to 1.2V regulator.
LDO_OP	Output	Output from on chip 1.8V to 1.2V regulator.
FB_SENSE	Input	On-chip regulator sense signal.

Table 4: Package Pinout

	1	2	3	4	5	6	7	8	9	10
A	RESERVED_0	VDDIO_H	M_SDATA	DIN0	VDD	DIN5	DIN10	LV_IN	VDDIO_S	FV_IN
B	SCLK	GPIO_6	EXTCLK_OUT	M_SCLK	DIN1	DIN4	DIN9	DIN11	HiSPi1N	HiSPi1P
C	SPI_SCLK	RESERVED_1	SDATA	GPIO_5	TRIGGER_OUT/ GPIO_0	DIN3	DIN8	PIXCLK_IN	HiSPiCN	HiSPiCP
D	SPI_SDO	SPI_SDI	SPI_CS_BAR	SADDR	RESET_BAR_OUT	DIN2	DIN7	VDD_PHY	HiSPi0N	HiSPi0P
E	VDD	GPIO_1	STANDBY	GND	GND	GND	DIN6	GND	DGND	VDDIO_H
F	VDDIO_OTPM	GPIO_2	GPIO_3	RESET_BAR	GND	GND	GND	EXTCLK	XTAL	VDD
G	TEST	GPIO_4	FRAME_SYNC	LV_OUT	DOUT16	DOUT12	DOUT5	EXT_REG	ENLDO	VDD_PLL
H	META_LINE_VALID	FV_OUT	DOUT21	DOUT18	DOUT14	DOUT8	DOUT6	DOUT2	FB_SENSE	VDD_REG
J	PIXCLK_OUT	DOUT22	DOUT19	DOUT17	DOUT13	DOUT10	DOUT7	DOUT3	DOUT0	LDO_OP
K	DOUT23	VDDIO_H	DOUT20	DOUT15	VDD	DOUT11	DOUT9	DOUT4	DOUT1	GND

On-Chip Regulator

The AP0202AT has an on-chip regulator, the output from the regulator is 1.2V and should only be used to power up the AP0202AT. It is possible to bypass the regulator and provide power to the relevant pins that need 1.2V. The following table summarizes the key signals when using/bypassing the regulator.

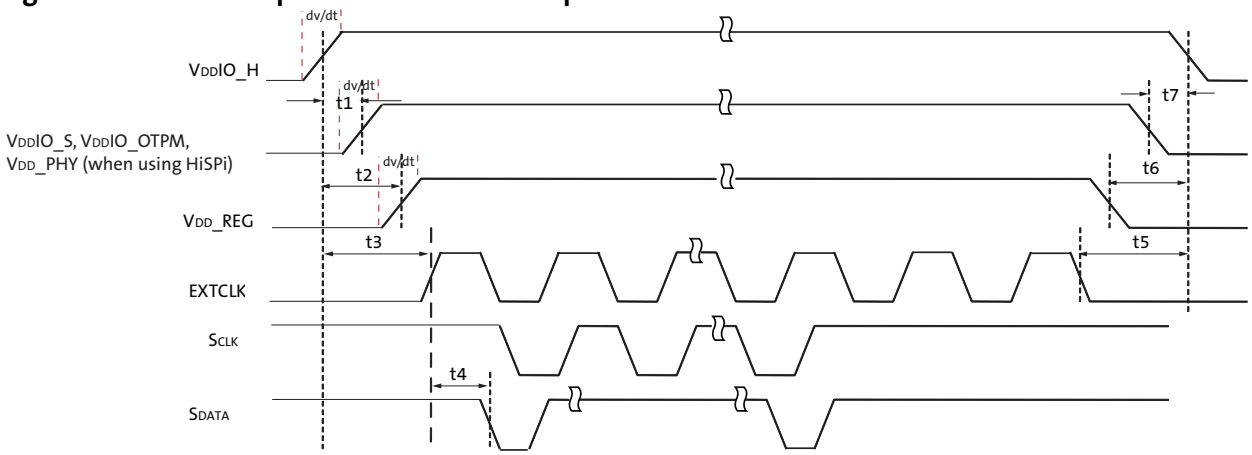
Table 5: Key Signals When Using the Regulator

Signal Name	Internal Regulator	External Regulator
VDD_REG	1.8V	Connect to VDDIO_H
ENLDO	Connect to 1.8V (VDD_REG)	GND
FB_SENSE	1.2V (input)	Float
LDO_OP	1.2V (output)	Float
EXT_REG	GND	Connect to VDDIO_H

Power-Up Sequence

Powering up the AP0202AT requires voltages to be applied in a particular order, as seen in Figure 5. The timing requirements are shown in Table 6. The AP0202AT includes a power-on reset feature that initiates a reset upon power up.

Figure 5: Power-Up and Power-Down Sequence



Note: 1. When using XTAL the settling time should be taken into account.
2. RESET_BAR can be either high or low at power-up

Table 6: Power-Up and Power-Down Signal Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	Delay from VDDIO_H to VDDIO_S, VDDIO_OTPM, VDD_PHY (when using HiSPi)	0	–	50	ms
t2	Delay from VDDIO_H to VDD_REG	0	–	50	ms
t3	EXTCLK activation	t2 + 1	–	–	ms
t4	First serial command[1]	100	–	–	EXTCLK cycles
t5	EXTCLK cutoff	t6	–	–	ms
t6	Delay from VDD_REG to VDDIO_H	0	–	50	ms
t7	Delay from VDDIO_S, VDDIO_OTPM, VDD_PHY (when using HiSPi) to VDDIO_H	0	–	50	ms
dv/dt	Power supply ramp time (slew rate)	–	–	0.1	V/µs

Note: 1. When using XTAL the settling time should be taken into account.

Reset

The AP0202AT has three types of reset available:

- A hard reset is issued by toggling the RESET_BAR signal
- A soft reset is issued by writing commands through the two-wire serial interface
- An internal power-on reset

Table 7 on page 15 shows the output states when the part is in various states.

Table 7: Output States

Name	Hardware States		Firmware States				Notes
	Reset State	Default State	Hard Standby	Soft Standby	Streaming	Idle	
EXTCLK	(clock running or stopped)	(clock running)	(clock running or stopped)	(clock running)	(clock running)	(clock running)	Input
XTAL	n/a	n/a	n/a	n/a	n/a	n/a	Output
RESET_BAR	(asserted)	(negated)	(negated)	(negated)	(negated)	(negated)	Input
SCLK	n/a	n/a	(clock running or stopped)	(clock running or stopped)	(clock running or stopped)	(clock running or stopped)	Input. Must always be driven to a valid logic level
SDATA	High-impedance	High-impedance	High-impedance	High-impedance	High-impedance	High-impedance	Input/Output. A valid logic level should be established by pull-up
SADDR	n/a	n/a	n/a	n/a	n/a	n/a	Input. Must always be driven to a valid logic level
FRAME_SYNC	n/a	n/a	n/a	n/a	n/a	n/a	Input. Must always be driven to a valid logic level
STANDBY	n/a	(negated)	(asserted)	(negated)	(negated)	(negated)	Input. Must always be driven to a valid logic level
EXT_REG	n/a	n/a	n/a	n/a	n/a	n/a	Input. Must always be driven to a valid logic level
ENLDO	n/a	n/a	n/a	n/a	n/a	n/a	Input. Must be tied to VDD_REG or GND
SPI_SCLK	High-impedance	driven, logic 0	driven, logic 0	driven, logic 0			Output
SPI_SDI	Internal pull-up enabled	Internal pull-up enabled	Internal pull-up enabled	internal pull-up enabled			Input. Internal pull-up permanently enabled.
SPI_SDO	High-impedance	driven, logic 0	driven, logic 0	driven, logic 0			Output
SPI_CS_BAR	High-impedance	driven, logic 1	driven, logic 1	driven, logic 1			Output
EXT_CLK_OUT	driven, logic 0	driven, logic 0	driven, logic 0	driven, logic 0			Output
RESET_BAR_OUT	driven, logic 0	driven, logic 0	driven, logic 1	driven, logic 1			Output. Firmware will release sensor reset
M_SCLK	High-impedance	High-impedance	High-impedance	High-impedance			Input/Output. A valid logic level should be established by pull-up
M_SDATA	High-impedance	High-impedance	High-impedance	High-impedance			Input/Output. A valid logic level should be established by pull-up
FV_IN, LV_IN, PIXCLK_IN, DIN[11:0]	n/a	n/a	n/a	n/a	Dependent on interface used	n/a	Input. Must always be driven to a valid logic level

Table 7: Output States (Continued)

Name	Hardware States		Firmware States				Notes
	Reset State	Default State	Hard Standby	Soft Standby	Streaming	Idle	
HiSPiCN	Disabled	Disabled	Dependent on interface used	Dependent on interface used	Dependent on interface used	Dependent on interface used	Input. Will be disabled and can be left floating
HiSPiCP							
HiSPi0N							
HiSPi0P							
HiSPi1N							
HiSPi1P							
FV_OUT, LV_OUT, PIXCLK_OUT	High-impedance	Varied	Driven if used	Driven if used	Driven if used	Driven if used	Output. Default state dependent on configuration
GPIO[6:1]	High-impedance	Input, then high-impedance	Driven if used	Driven if used	Driven if used	Driven if used	Input/Output.
TRIGGER_OUT	High-impedance	High-impedance	Driven if used	Driven if used	Driven if used	Driven if used	
TEST	n/a	n/a	(negated)	(negated)	(negated)	(negated)	Input. Must always be driven to a valid logic level.

Hard Reset

The AP0202AT enters the reset state when the external RESET_BAR signal is asserted LOW, as shown in Figure 6. All the output signals will be in a High-Z state.

Figure 6: Hard Reset Operation

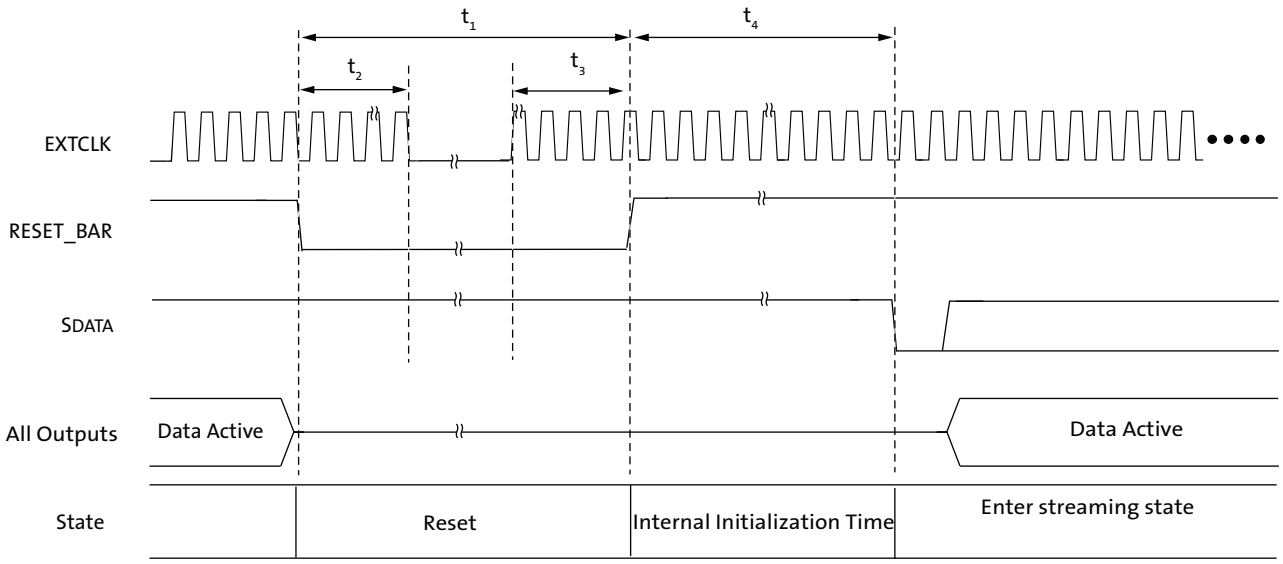


Table 8: Hard Reset

Symbol	Definition	Min	Typ	Max	Unit
t_1	RESET_BAR pulse width	50	–	–	EXTCLK cycles
t_2	Active EXTCLK required after RESET_BAR asserted	10	–	–	
t_3	Active EXTCLK required before RESET_BAR de-asserted	10	–	–	
t_4	First two-wire serial interface communication after RESET is HIGH	100	–	–	

Soft Reset

A soft reset sequence to the AP0202AT can be activated by writing to a register through the two-wire serial interface.

Hard Standby Mode

The AP0202AT can enter hard standby mode by using external STANDBY signal, as shown in Figure 7. In hard standby mode, the total power consumption is reduced. In this mode, the AP0202AT is switched off. A further power reduction can be achieved by turning off the EXTCLK, but this must be restored before de-asserting the STANDBY pin to LOW state to restart the device.

Entering Standby Mode

1. Assert STANDBY signal HIGH.

Exiting Standby Mode

1. De-assert STANDBY signal LOW.

Figure 7: Hard Standby Operation

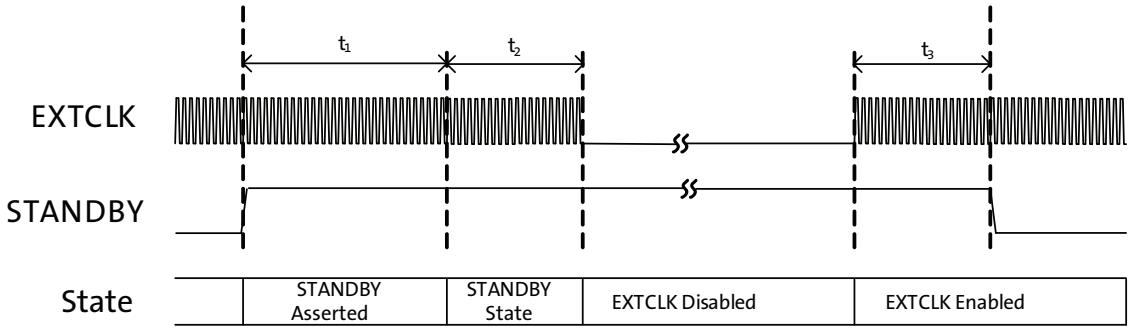


Table 9: Hard Standby Signal Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_1	Standby entry complete	–	–	2	Frames
t_2	Active EXTCLK required after going into STANDBY mode	10	–	–	EXTCLKs
t_3	Active EXTCLK required before STANDBY de-asserted	10	–	–	EXTCLKs

Device Configuration

After power is applied and the device is out of reset (either the power on reset, hard or soft reset), it will enter a boot sequence to configure its operating mode. There are essentially three configuration modes: Flash/EEPROM Config, Auto Config, and Host Config.

The AP0202AT firmware supports a System Configuration phase at start-up. This consists of three sub-phases of execution:

Flash detection, then one of:

a. Flash Config
b. Auto Config
c. Host Config

The System Configuration phase is entered immediately following power-up or reset. Then the firmware performs Flash Detection.

Flash Detection attempts to detect the presence of an SPI Flash or EEPROM device:

- If a device is detected, the firmware switches to the Flash-Config mode.
- If no device is detected, the firmware then samples the SPI_SDI pin state to determine the next mode:
  - If SPI_SDI is low, then it enters the Host-Config mode.
  - If SPI_SDI is high, then it enters the Auto-Config mode.

In the Flash-Config mode, the firmware interrogates the device to determine if it contains valid configuration records:

- If no records are detected, then the firmware enters the Host-Config mode.
- If records are detected, the firmware processes them. By default, when all Flash records are processed the firmware switches to the Host-Config mode. However, the records encoded into the Flash can optionally be used to instruct the firmware to proceed to auto-config, or to start streaming (via a Change-Config).

In the Host-Config mode, the firmware performs no configuration, and remains idle waiting for configuration and commands from the host. The System Configuration phase is effectively complete and the AP0202AT will take no actions until the host issues commands.

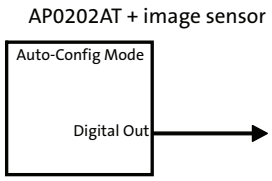
Usage Modes

How a camera based on the AP0202AT will be configured depends on what features are used. In the simplest case, an AP0202AT operating in Auto-Config mode with no customized settings might be sufficient.

A back-up camera with dynamic input from the steering system will require a µC with a system bus interface. Flash sizes up to 2 GB are supported. The two-wire bus is adequate since only high-level commands are used.

In the simplest case no EEPROM or Flash memory or µC is required, as shown in Figure 8 on page 20.

Figure 8: Auto-Config Mode (Not supported for AR0230)



The AP0202AT can be configured by a serial EEPROM or Flash through the SPI Interface.

Figure 9: Flash Mode

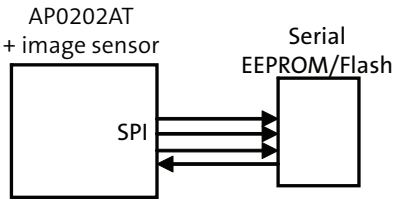
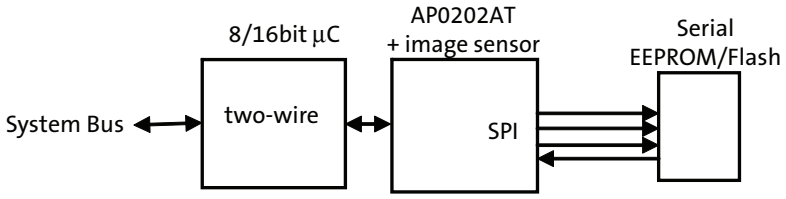


Figure 10: Host Mode with Flash



In this configuration all settings are communicated to the AP0202AT and sensor through the microcontroller.

Figure 11: Host Mode

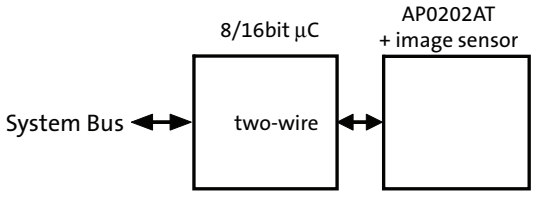


Image Flow Processor

Image and color processing in the AP0202AT is implemented as an image flow processor (IFP) coded in hardware logic. During normal operation, the embedded microcontroller will automatically adjust the operating parameters. For normal operation of the AP0202AT, streams of raw image data from the attached image sensor are fed into the color pipeline. The AP0202AT also has the option to select from a number of test patterns to be input instead of sensor data.

Defect Correction

Image stream processing commences with the defect correction function immediately after data decompanding.

To obtain defect free images, the pixels marked defective during sensor readout and the pixels determined defective by the defect correction algorithms are replaced with values derived from the non-defective neighboring pixels.

AdaCD (Adaptive Color Difference)

The next step in the image stream process is noise reduction. The AP0202AT uses a noise reduction filter called AdaCD which focuses on removing color noise while preserving edge details. Automotive applications require good performance in extremely low light, even at high temperature conditions. In these stringent conditions the image sensor is prone to higher noise levels, and so efficient noise reduction techniques are required to circumvent this sensor limitation and deliver a high quality image.

Black Level Subtraction and Digital Gain

After noise reduction, the pixel data goes through black level subtraction and multiplication by a programmable digital gain. Independent color channel digital gain can be adjusted with registers. Black level subtraction (to compensate for sensor data pedestal) is a single value applied to all color channels. If the black level subtraction produces a negative result for a particular pixel, the value of this pixel is set to 0.

Positional Gain Adjustments (PGA)

Lenses tend to produce images whose brightness is significantly attenuated near the edges. There are also other factors causing fixed pattern signal gradients in images captured by image sensors. The cumulative result of all these factors is known as image shading. The AP0202AT has an embedded shading correction module that can be programmed to counter the shading effects on each individual R, Gb, Gr, and B color signal.

The Correction Function

The correction functions can then be applied to each pixel value to equalize the response across the image as follows:

$$P_{corrected}(row, col) = P_{sensor}(row, col) \times f(row, col) \quad \text{(EQ 1)}$$

where P are the pixel values and f is the color dependent correction functions for each color channel.

Adaptive Local Tone Mapping (ALTM)

Real world scenes often have very high dynamic range (HDR) that far exceeds the electrical dynamic range of the imager. Dynamic range is defined as the luminance ratio between the brightest and the darkest object in a scene. In recent years many technologies have been developed to capture the full dynamic range of real world scenes. For example, the multiple exposure method is widely adopted for capturing high dynamic range images, which combines a series of low dynamic range images of the same scene taken under different exposure times into a single HDR image.

Even though the new digital imaging technology enables the capture of the full dynamic range, low dynamic range display devices are the limiting factor. Today's typical LCD monitor has contrast ratio around 1,000:1; this contrast ratio is not enough for an HDR image (the contrast ratio for an HDR image is around 250,000:1). Therefore, in order to reproduce HDR images on a low dynamic range display device, the captured high dynamic range must be compressed to the available range of the display device. This is commonly called tone mapping.

Tone mapping methods can be classified into global tone mapping and local tone mapping. Global tone mapping methods apply the same mapping function to all pixels. While global tone mapping methods provide computationally simple and easy to use solutions, they often cause loss of contrast and detail. A local tone mapping is thus necessary in addition to global tone mapping for the reproduction of visually more appealing images that also reveal scene details that are important for automotive safety and surveillance applications. Local tone mapping methods use a spatially variable mapping function determined by the neighborhood of a pixel, which allows it to increase the local contrast and the visibility of some details of the image. Local methods usually yield more pleasing results because they exploit the fact that human vision is more sensitive to local contrast.

ON Semiconductor's ALTM solution significantly improves the performance over global tone mapping. ALTM is directly applied to the Bayer domain to compress the dynamic range from 20-bit to 12-bit. This allows the regular color pipeline to be used for HDR image rendering.

Color Interpolation

In the raw data stream fed by the external sensor to the IFP, each pixel is represented by a 20- or 12-bit integer number, which can be considered proportional to the pixel's response to a one-color light stimulus, red, green, or blue, depending on the pixel's position under the color filter array. Initial data processing steps, up to and including ALTM, preserve the one-color-per-pixel nature of the data stream, but after ALTM it must be converted to a three-colors-per-pixel stream appropriate for standard color processing. The conversion is done by an edge-sensitive color interpolation module. The module pads the incomplete color information available for each pixel with information extracted from an appropriate set of neighboring pixels. The algorithm used to select this set and extract the information seeks the best compromise between preserving edges and filtering out high frequency noise in flat field areas. The edge threshold can be set through register settings.

Color Correction and Aperture Correction

To achieve good color fidelity of the IFP output, interpolated RGB values of all pixels are subjected to color correction. The IFP multiplies each vector of three pixel colors by a 3 x 3 color correction matrix (CCM). The three components of the resulting color vector are

all sums of three 10-bit numbers. The color correction matrix can be either programmed by the user or automatically selected by the auto white balance (AWB) algorithm implemented in the IFP. Color correction should ideally produce output colors that are corrected for the spectral sensitivity and color crosstalk characteristics of the image sensor. The optimal values of the color correction matrix elements depend on those sensor characteristics and on the spectrum of light incident on the sensor. The color correction variables can be adjusted through register settings.

The AP0202AT offers a three-CCM solution that will give the user improved color fidelity when under a wide range of lighting.

To increase image sharpness, a programmable 2D aperture correction (sharpening filter) is applied to color-corrected image data. The gain and threshold for 2D correction can be defined through register settings.

Gamma Correction

The gamma correction curve is implemented as a piecewise linear function with 33 knee points, taking 12-bit arguments and mapping them to 10-bit output. The abscissas of the knee points are fixed at 0, 8, 16, 24, 32, 40, 48, 56, 64, 80, 96, 112, 128, 160, 192, 224, 256, 320, 384, 448, 512, 640, 768, 896, 1024, 1280, 1536, 1792, 2048, 2560, 3072, 3584, and 4096. The 10-bit ordinates are programmable through variables.

The AP0202AT has the ability to calculate the 33-point knee points based on the tuning of cam_ll_gamma and cam_ll_contrast_gradient_bright. The other method is for the host to program the 33 knee point curve.

Also included in this block is a Fade-to Black curve which sets all knee points to zero and causes the image to go black in extreme low light conditions.

Color Kill

To remove high-or low-light color artifacts, a color kill circuit is included. It affects only pixels whose luminance exceeds a certain preprogrammed threshold. The U and V values of those pixels are attenuated proportionally to the difference between their luminance and the threshold.

YUV Color Filter

As an optional processing step, noise suppression by one-dimensional low-pass filtering of Y and/or UV signals is possible. A 3- or 5-tap filter can be selected for each signal.

Camera Control and Auto Functions

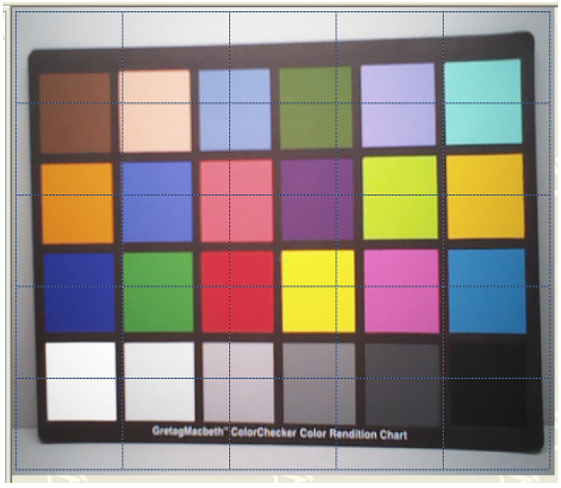
Auto Exposure

The auto exposure algorithm optimizes scene exposure to minimize clipping and saturation in critical areas of the image. This is achieved by controlling exposure time and analog gains of the external sensor as well as digital gains applied to the image.

Auto exposure is implemented by a firmware algorithm that is running on the embedded microcontroller that analyzes image statistics collected by the exposure measurement engine, makes a decision, and programs the sensor and color pipeline to achieve the desired exposure. The measurement engine subdivides the image into 25 windows organized as a 5 x 5 grid.

Figure 12: 5 x 5 Grid

W 0,0	W 0,1	W 0,2	W 0,3	W 0,4
W 1,0	W 1,1	W 1,2	W 1,3	W 1,4
W 2,0	W 2,1	W 2,2	W 2,3	W 2,4
W 3,0	W 3,1	W 3,2	W 3,3	W 3,4
W 4,0	W 4,1	W 4,2	W 4,3	W 4,4



AE Track

Other algorithm features include the rejection of fast fluctuations in illumination (time averaging), control of speed of response, and control of the sensitivity to small changes. While the default settings are adequate in most situations, the user can program target brightness, measurement window, and other parameters described above.

The AE Track changes AE parameters (integration time, gains, and so on) to drive scene brightness to the programmable target.

To avoid unwanted reaction of AE on small fluctuations of scene brightness or momentary scene changes, the AE track uses a temporal filter for luma and a threshold around the AE luma target. The driver changes AE parameters only if the filtered luma is larger than the AE target step and pushes the luma beyond the threshold.

Auto White Balance

The AP0202AT has a built-in AWB algorithm designed to compensate for the effects of changing spectra of the scene illumination on the quality of the color rendition. The algorithm consists of two major parts: a measurement engine performing statistical analysis of the image and a driver performing the selection of the optimal color correction matrix and IFP digital gain. While default settings of these algorithms are adequate

in most situations, the user can reprogram base color correction matrices, place limits on color channel gains, and control the speed of both matrix and gain adjustments. The AP0202AT AWB displays the current AWB position in color temperature, the range of which will be defined when programming the CCM matrices.

The region of interest can be controlled through the combination of an inclusion window and an exclusion window.

Dual Band IRCF

For some applications a day/night filter would be switched in/out, this option is an additional cost to the camera system. The AP0202AT supports the use of dual band IRCF, which removes the need for the switching day/night filter. Tuning support is provided for this usage case. Refer to the AP0202AT developer guide for details.

Exposure and White Balance Modes

The AP0202AT supports auto and manual exposure and white balance modes. In addition, it will operate within synchronized multi-camera systems. In this use case, one camera within the system will be the 'master', and the others 'slaves'. The master is used to calculate the appropriate exposure and white balance. This is then applied to all slaves concurrently under host control.

Auto Mode

In Auto Exposure mode the AE algorithm is responsible for calculating the appropriate exposure to keep the desired scene brightness, and for applying the exposure to the underlying hardware. In Auto White Balance mode the AWB algorithm is responsible for calculating the color temperature of the scene and applying the appropriate red and blue gains to compensate.

Triggered Auto Mode

The Triggered Auto Exposure and Triggered Auto White Balance modes are intended for the multi-camera use cases, where a host is controlling the exposure and white balance of a number of cameras. The idea is that one camera is in triggered-auto mode (the master), and the others in host-controlled mode (slaves). The master camera must calculate the exposure and gains, the host then copies this to the slaves, and all changes are then applied at the same time.

Manual Mode

Manual mode is intended to allow simple manual exposure and white balance control by the host. The host needs to set the CAM_AET_EXPOSURE_TIME_MS, CAM_AET_EXPOSURE_GAIN and CAM_AWB_COLOR_TEMPERATURE controls and trigger an exposure, the camera will calculate the appropriate integration times and gains.

Host Controlled

The Host Controlled mode is intended to give the host full control over exposure and gains

Flicker Avoidance

Flicker is caused by artificial light which is usually generated from incandescent or fluorescent light sources. The frequency of alternating current (AC) power sources in most countries is 50 Hz or 60 Hz, which emit light with alternating inverted positive and nega-

tive voltages. This results in a light source reflecting from an object to have a light intensity change frequency of 100 Hz and 120 Hz respectively. If the integration time is not an integer multiple of the period of AC powered light intensity, flicker can be visible. The AP0202AT can be programmed to avoid flicker for 50 or 60 Hertz. For integration times below the light intensity period (10ms for 50Hz environment, 8.33 ms in 60 Hz environments), flicker cannot be avoided. The AP0202AT supports an indoor AE mode, that will ensure flicker-free operation.

Flicker Detection

The AP0202AT supports flicker detection, the algorithm is designed only to detect a 50Hz or 60Hz flicker source.

Output Formatting

The pixel output data in AP0202AT will be transmitted as an 8- to 24-bit word over one or two clocks.

Uncompressed YCbCr Data Ordering

The AP0202AT supports swapping YCbCr mode, as illustrated in Table 10.

Table 10: YCbCr Output Data Ordering

Mode	Data Sequence			
Default (no swap)	Cbi	Yi	Cri	Yi+1
Swapped CrCb	Cri	Yi	Cbi	Yi+1
Swapped YC	Yi	Cbi	Yi+1	Cri
Swapped CrCb, YC	Yi	Cri	Yi+1	Cbi

The data ordering for the YCbCr output modes for AP0202AT are shown in Table 11 and Table 12:

Table 11: YCbCr Output Modes (Default mode; cam_port_parallel_msb_align=0x1)

Mode	Byte	Pixel i	Pixel i+1	Notes
YCbCr_422_8_8	Odd (DOUT [23:16])	Cbi	Cri	Data range of 0-255 (Y=16-235 and C=16-240)
	Even (DOUT [23:16])	Yi	Yi+1	
YCbCr_422_10_10	Odd (DOUT [23:14])	Cbi	Cri	Data range of 0-1023 (Y=64-940 and C=64-960)
	Even (DOUT [23:14])	Yi	Yi+1	
YCbCr_422_16	Single (DOUT [23:8])	Cbi_Yi	Cri_Yi+1	Data range of 0-255 (Y=16-235 and C=16-240)
YCbCr_422_20	Single (DOUT [23:4])	Cbi_Yi	Cri_Yi+1	Data range of 0-1023 (Y=64-940 and C=64-960)

Note: Odd means first cycle; even means second cycle.

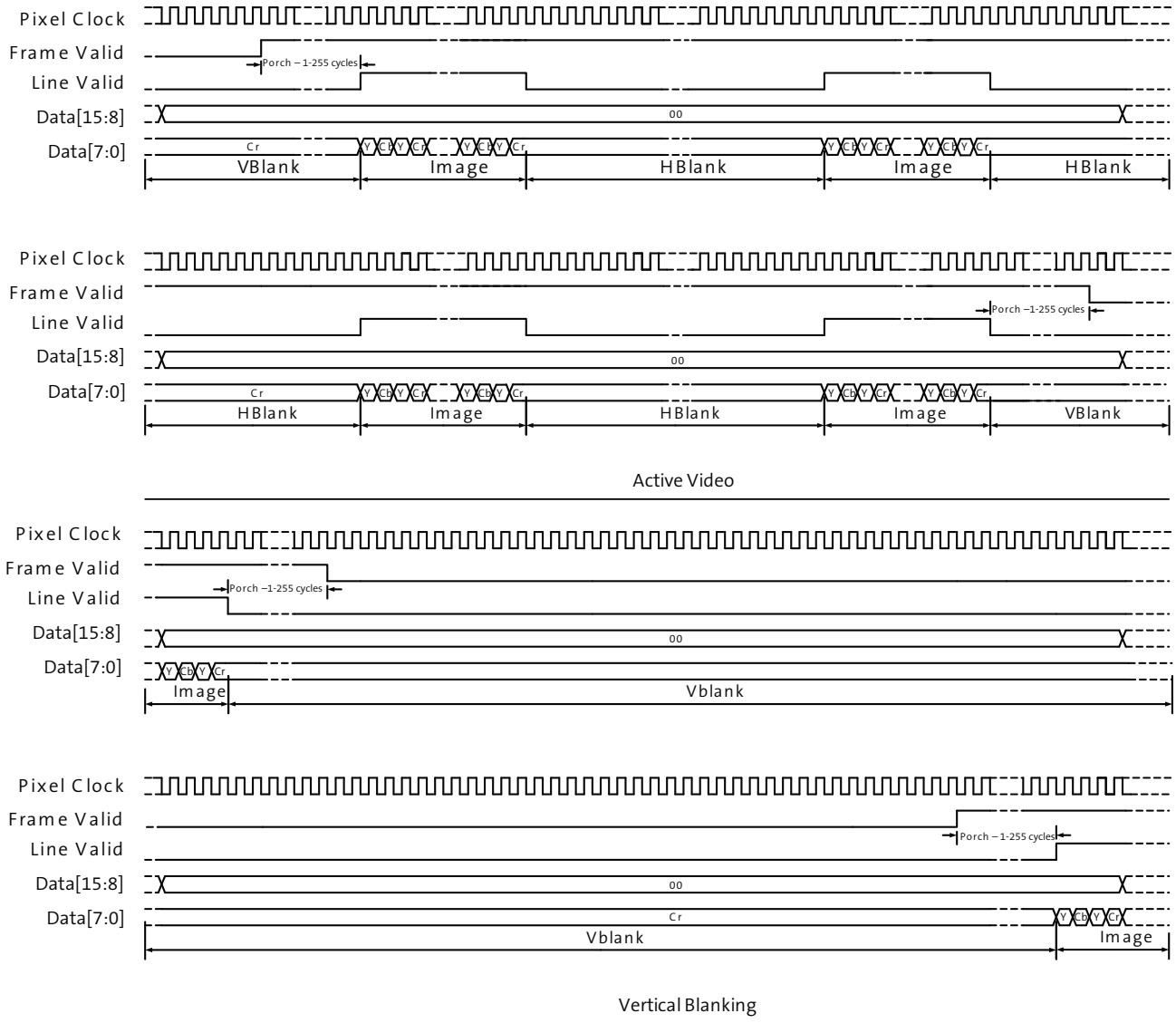
Table 12: YCbCr Output Modes (Default mode; cam_port_parallel_msb_align=0x0)

Mode	Byte	Pixel i	Pixel i+1	Notes
YCbCr_422_8_8	Odd (DOUT[7 :0])	Cbi	Cri	Data range of 0-255 (Y=16-235 and C=16-240)
	Even (DOUT [7:0]	Yi	Yi+1	

Table 12: YCbCr Output Modes (Default mode; cam_port_parallel_msb_align=0x0)

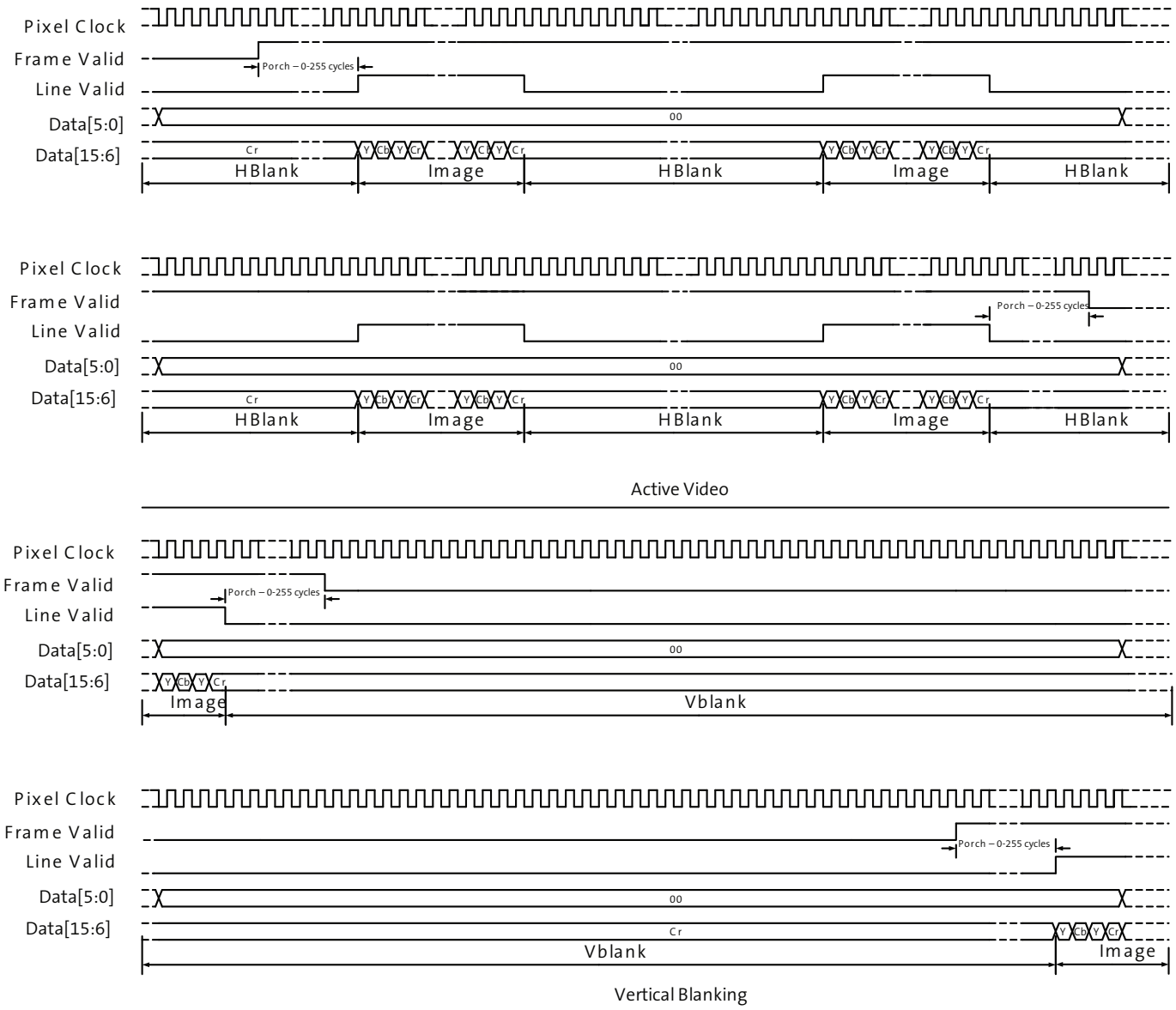
Mode	Byte	Pixel i	Pixel i+1	Notes
YCbCr_422_10_10	Odd (DOUT [9:0])	Cbi	Cri	Data range of 0-1023 (Y=64-940 and C=64-960)"
	Even (DOUT [9:0])	Yi	Yi+1	
YCbCr_422_16	Single (DOUT [15:0])	Cbi_Yi	Cri_Yi+1	Data range of 0-255 (Y=16-235 and C=16-240)
YCbCr_422_20	Single (DOUT [19:0])	Cbi_Yi	Cri_Yi+1	Data range of 0-1023 (Y=64-940 and C=64-960)

Figure 13: 8- bit YCbCr Output (YCbCr_422_8_8)



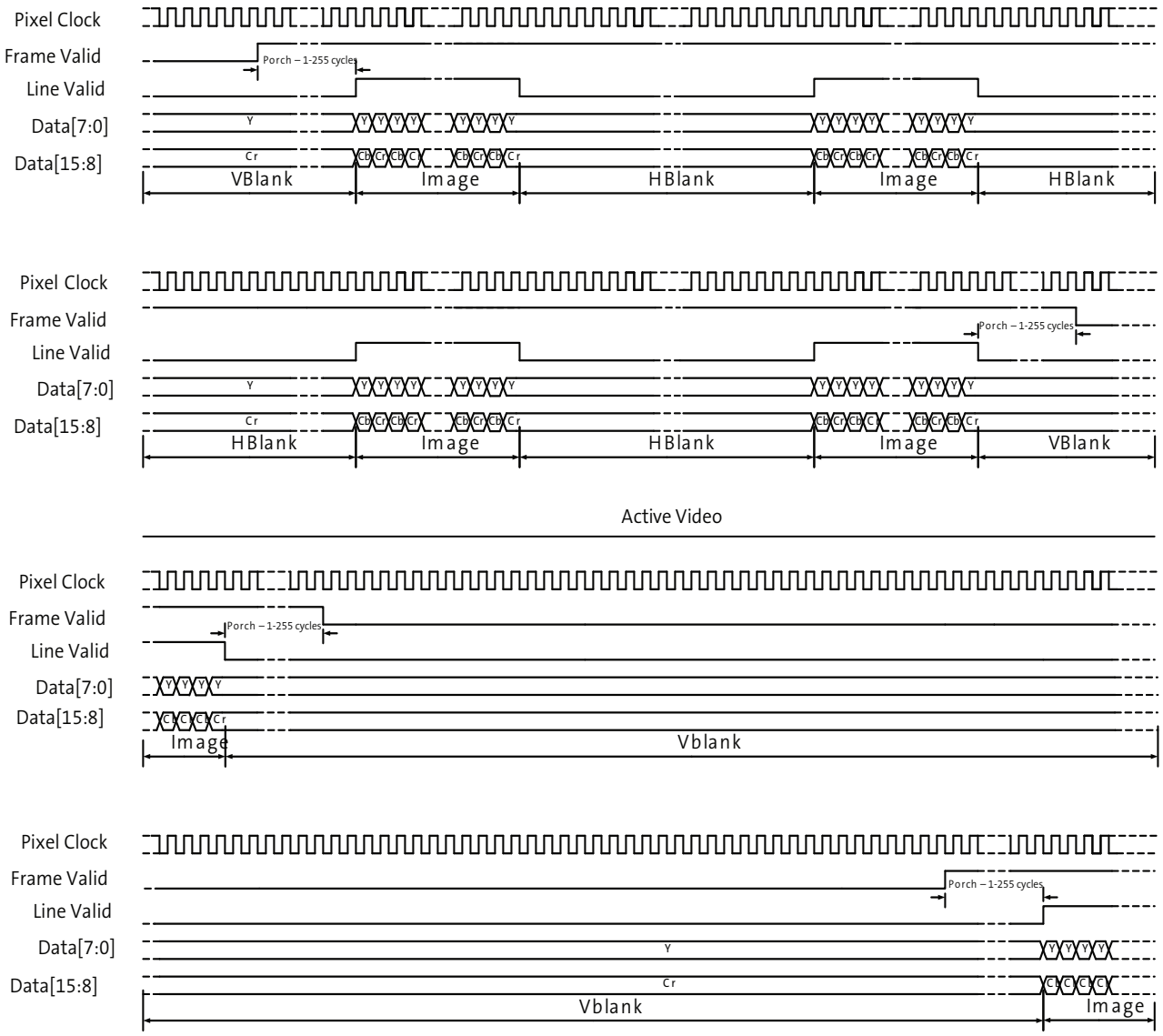
Notes: 1. YC Swapped mode: Y Cb Y Cr
2. cam_port_parallel_msb_align=0x0

Figure 14: 10-bit YCbCr Output (YCbCr_422_10_10)



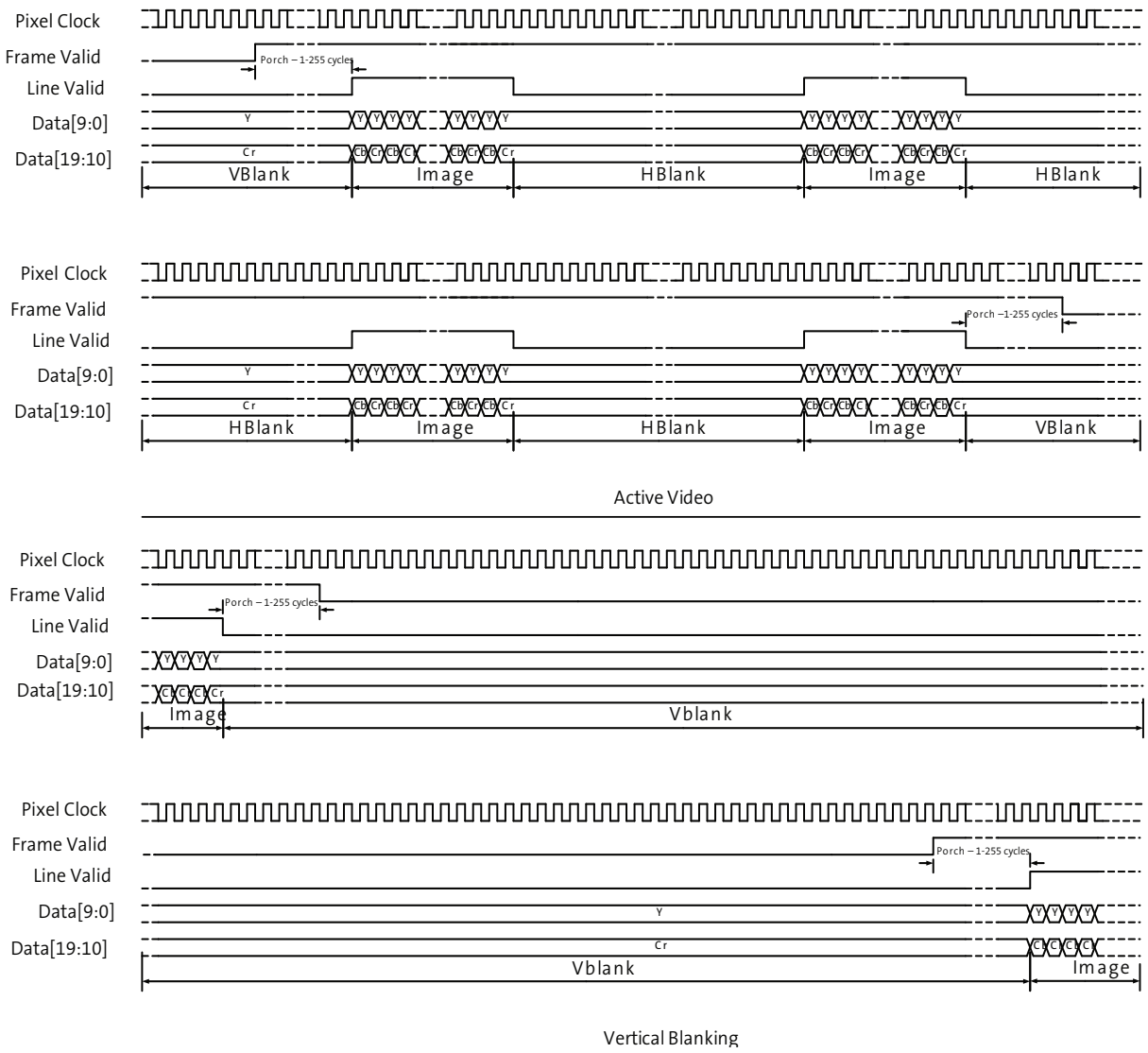
Notes:
1. YC Swapped mode: Y Cb Y Cr
2. cam_port_parallel_msb_align=0x0

Figure 15: 16-bit YCbCr Output (YCbCr_422_16)



Notes:
1. YC Swapped mode: Y Cb Y Cr
2. cam_port_parallel_msb_align=0x0

Figure 16: 20-bit YCbCr Output (YCbCr_422_20)

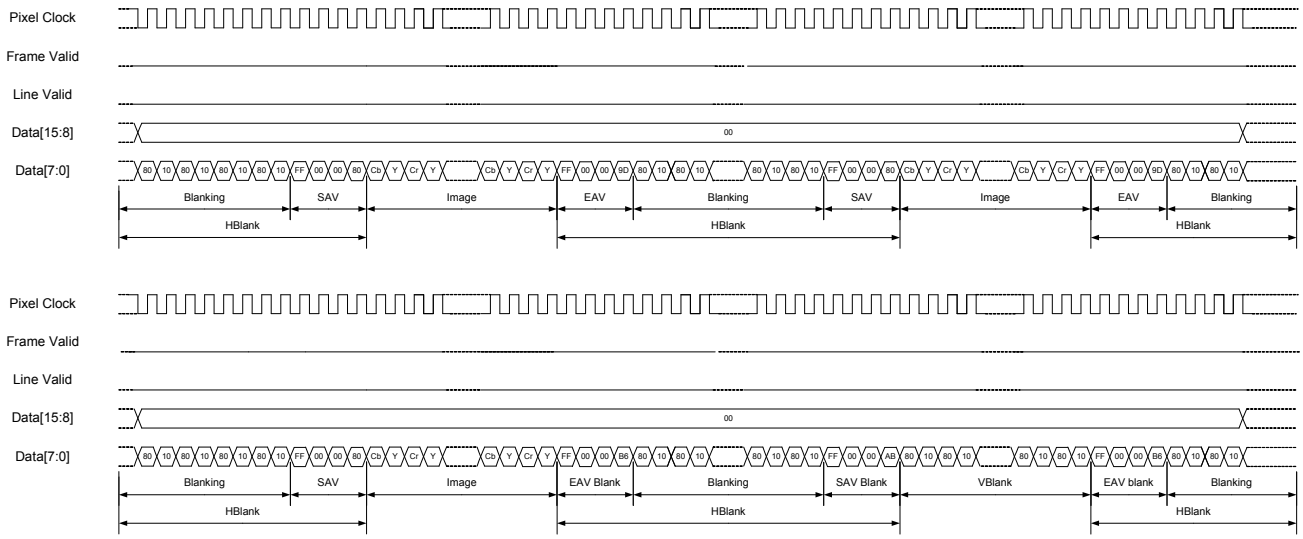


Notes:
1. YC Swapped mode: Y Cb Y Cr
2. cam_port_parallel_msb_align=0x0

Progressive CCIR656 Data Ordering (BTG.656)

The AP0202AT supports progressive CCIR656 mode.

Figure 17: CCIR656 (Progressive) Output



RGB888 Data Ordering

The AP0202AT supports RGB888 output mode. The data ordering for this mode is shown in Table 13 and Table 14:

Table 13: RGB888 Output Modes (cam_port_parallel_msb_align=0x01)

Mode	Byte	Pixel i	Pixel i+1	Notes
RGB888_12_12	Odd (DOUT [23:12])	Rm_Rl_Gm	Rm+1_Rl+1_Gm+1	
	Even (DOUT [23:12])	Gl_Bm_Bl	Gl+1_Bm+1_Bl+1	
RGB888_24	Single (DOUT [23:0])	R_G_B	R+1_G+1_B+1	

Note: Odd means first cycle; even means second cycle.

Table 14: RGB888 Output Modes (cam_port_parallel_msb_align=0x0)

Mode	Byte	Pixel i	Pixel i+1	Note
RGB888_12_12	Odd (DOUT[11:0])	Rm_Rl_Gm	Rm+1_Rl+1_Gm+1	
	Even (DOUT [11:0]	Gl_Bm_Bl	Gl+1_Bm+1_Bl+1	
RGB888_24	Single (DOUT [23:0])	R_G_B	R+1_G+1_B+1	

Figure 18: 24-bit RGB888 Output

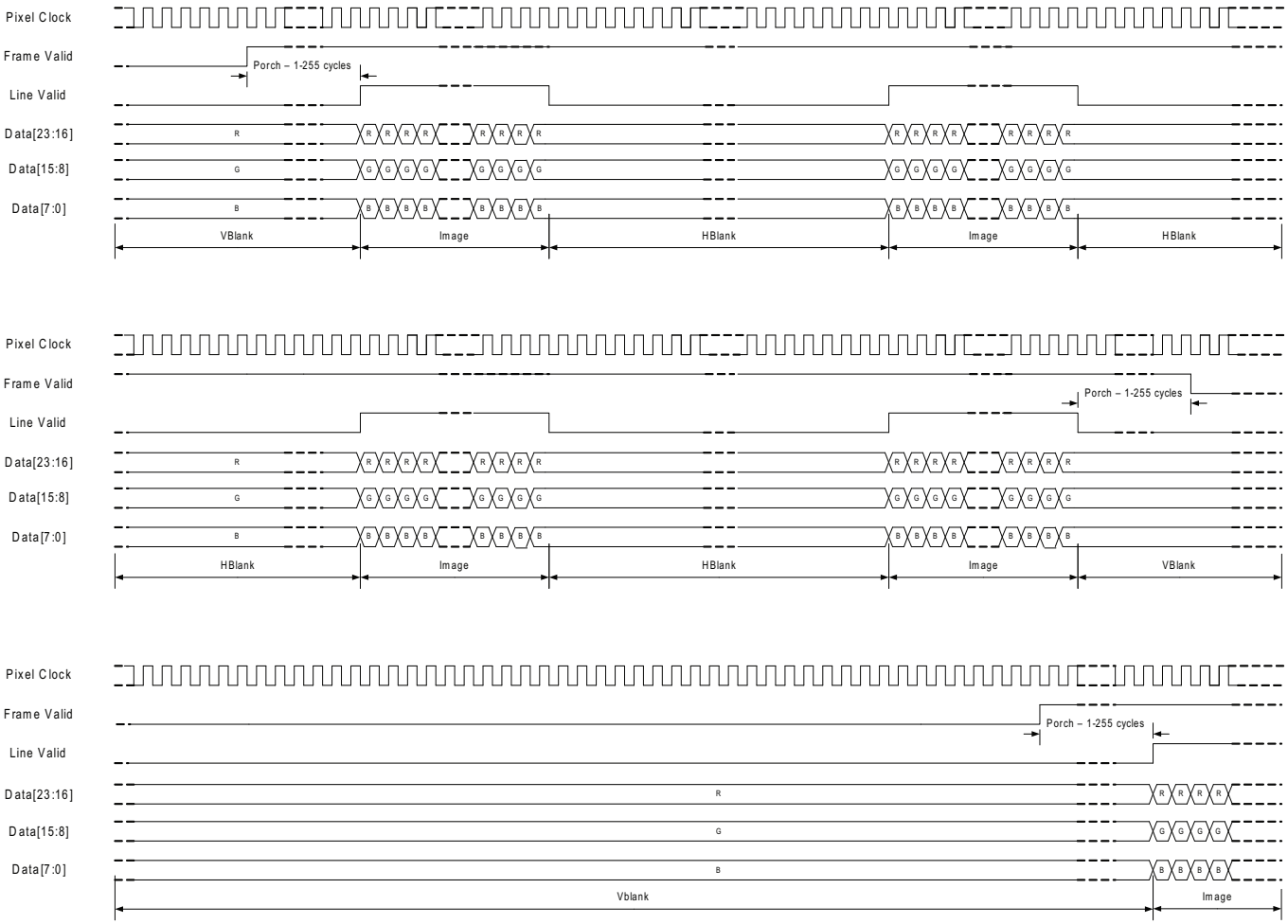
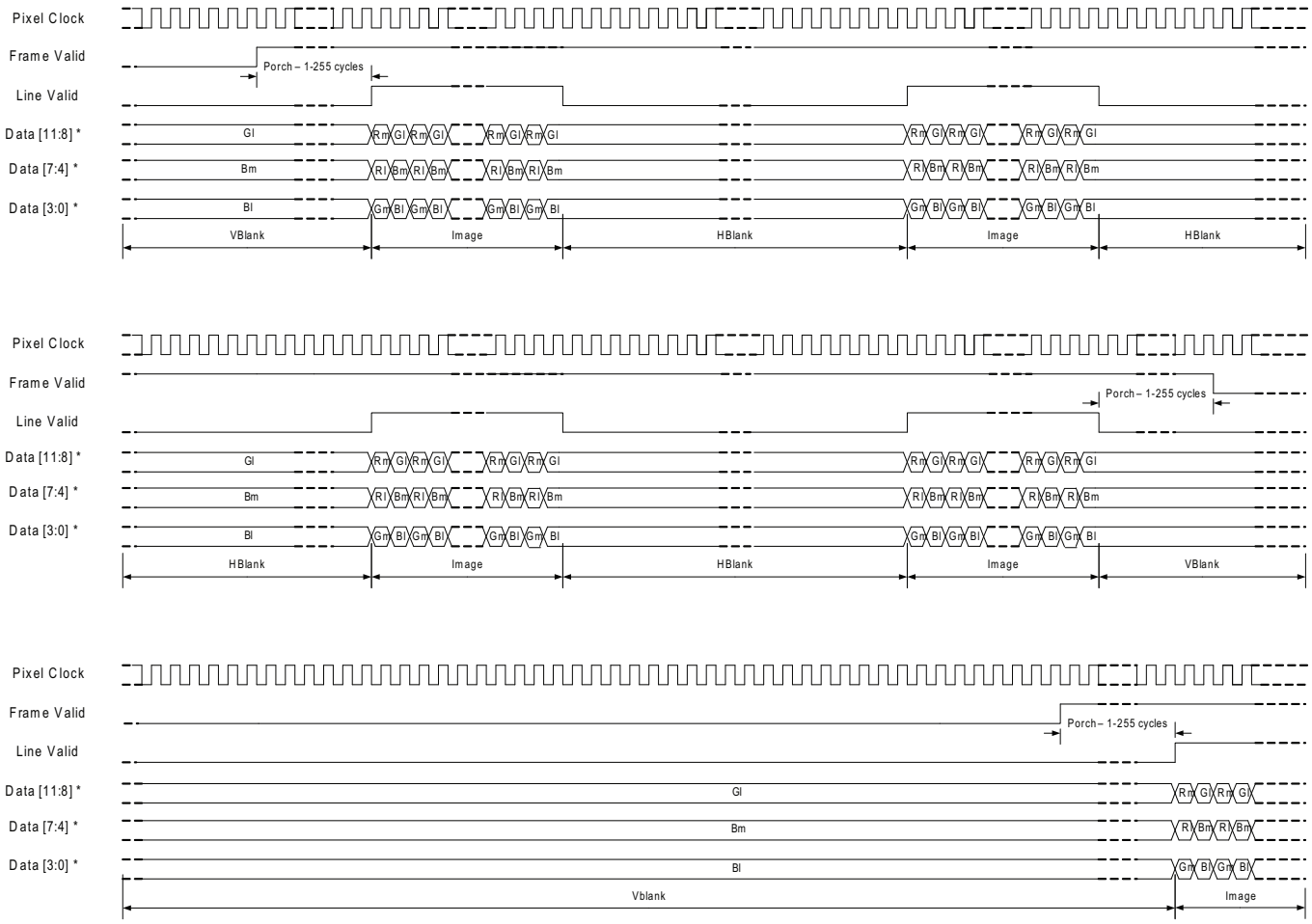


Figure 19: 12+12-bit RGB888 Output



Rm = R[7:4], Rl = R[3:0]
Gm = G[7:4], Gl = G[3:0]
Bm = B]7:4], Bl = B[3:0]

*The 12 active data bits can be aligned on DOUT[11:0] as shown here or on DOUT[23:12]

RGB565 Data Ordering

The AP0202AT supports RGB565 output mode. The data ordering for this mode is shown in Table 15 and Table 16:

Table 15: RGB565Output Modes (cam_port_parallel_msb_align=0x01)

Mode	Byte	Pixel i	Pixel i+1	Notes
RGB565_8_8	Odd (DOUT [23:16])	R_Gm	R+1_Gm+1	
	Even (DOUT [23:16])	Gl_B	Gl+1_B+1	
RGB565_16	Single (DOUT [23:8])	R_G_B	R+1_G+1_B+1	

Note: Odd means first cycle; even means second cycle.

Table 16: RGB565 Output Modes (cam_port_parallel_msb_align=0x0)

Mode	Byte	Pixel i	Pixel i+1	Note
RGB565_8_8	Odd (DOUT [7:0])	R_Gm	R+1_Gm+1	
	Even (DOUT [7:0])	Gl_B	Gl+1_B+1	
RGB565_16	Single (DOUT [15:0)	R_G_B	R+1_G+1_B+1	

Figure 20: RGB565_16

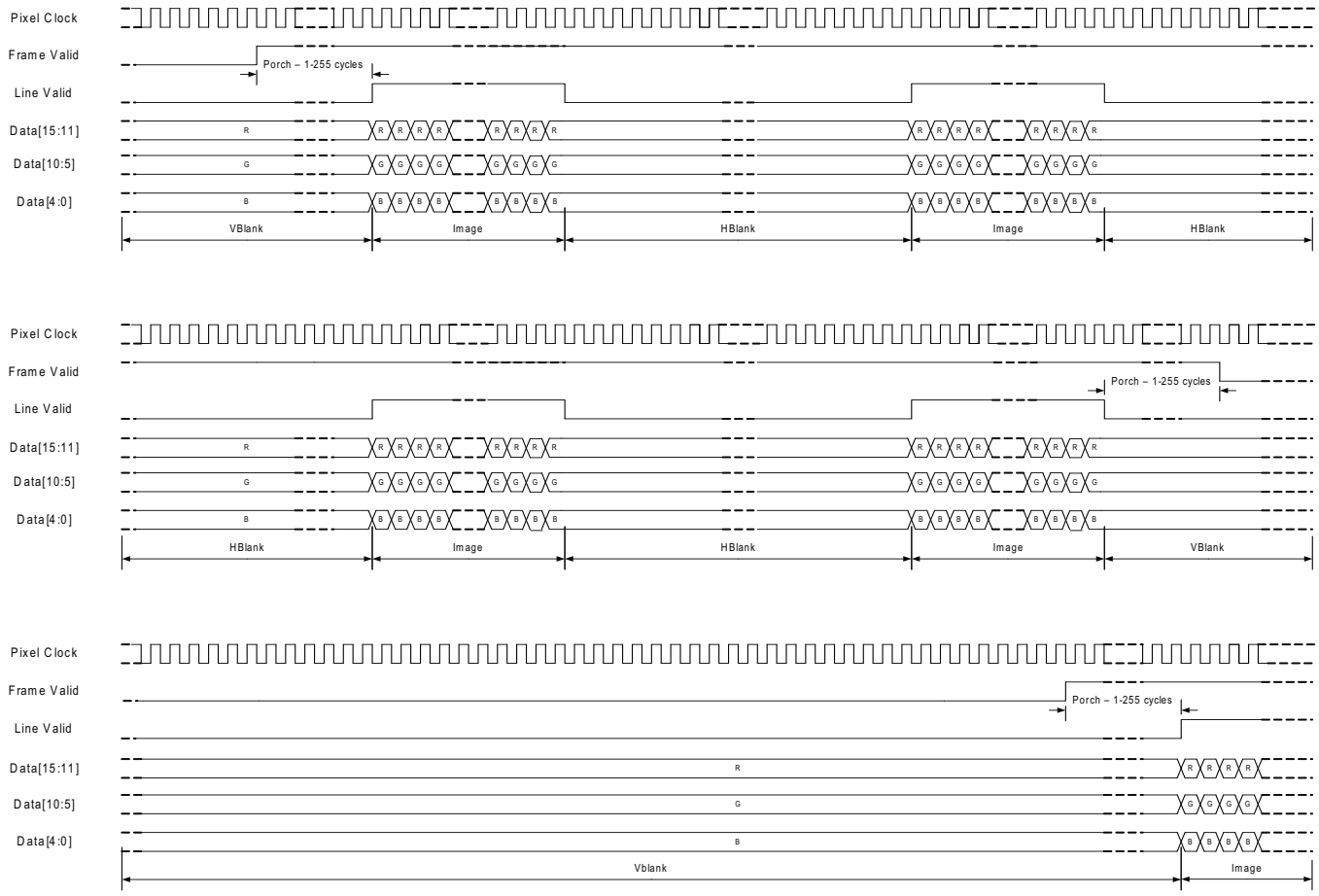
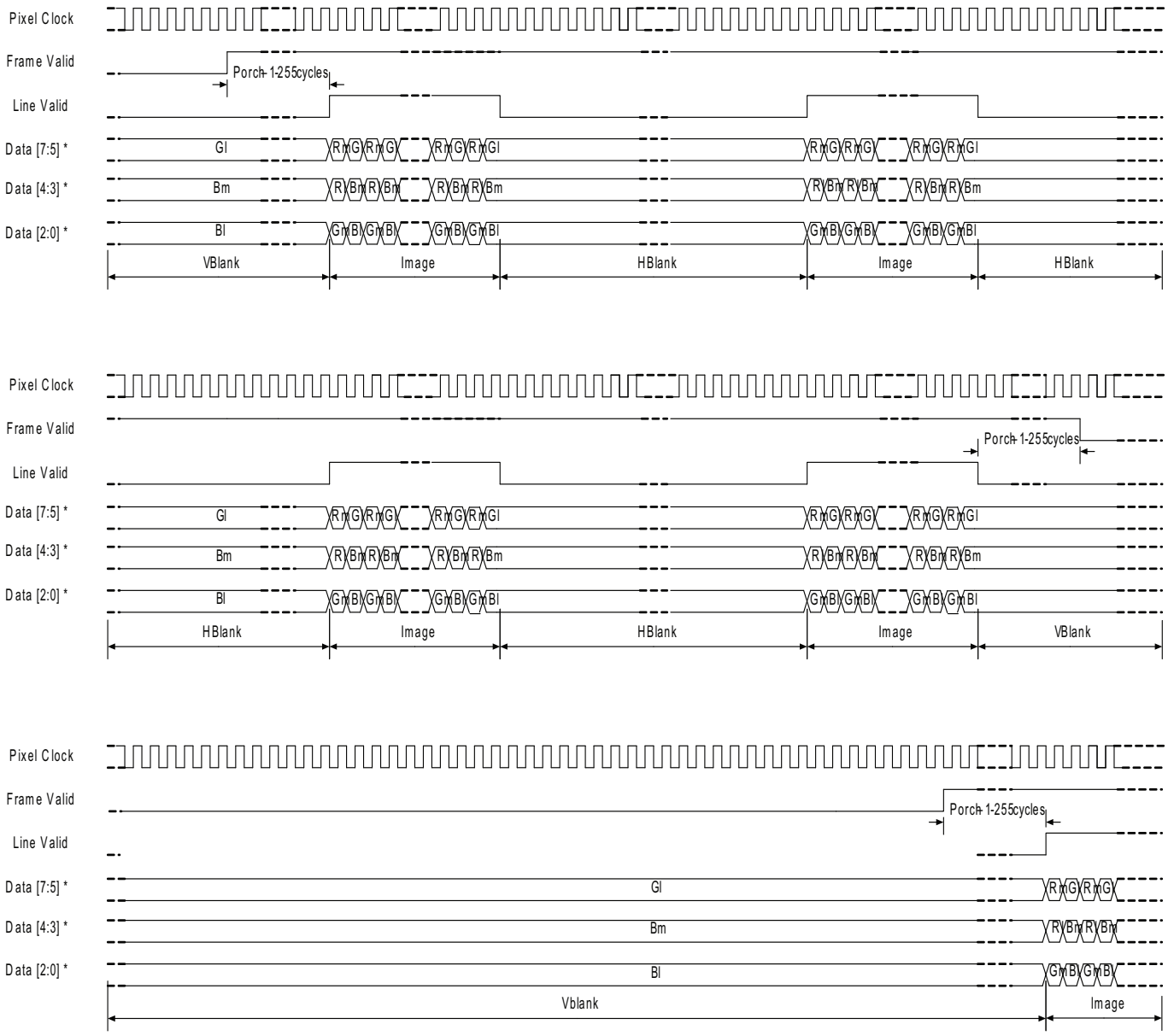


Figure 21: RGB565_8_8



Rm = R[7:5], Rl = R[4:3]
Gm = G[7:5], Gl = G[4:2]
Bm = B[7:6], Bl = B[5:3]

Bayer Modes

The data ordering for the ALTM Bayer output modes for AP0202AT are shown in Table 17. Shown is LSB aligned data; it is possible using register setting to obtain MSB aligned data.

Table 17: ALTM Bayer Output Modes

Mode	Byte	D23- D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALTM_Bayer_10	Single	0	0	0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALTM_Bayer_12	Single	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

The data ordering for the 12-bit Bayer output modes for AP0202AT are shown in shown in Table 18, Table 19, Table 20,and Table 21. Shown is LSB-aligned data; it is possible using register setting to obtain MSB-aligned data.

Table 18: 12-bit Bayer Output Mode

Mode	Byte	D23- D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bayer_12	Single	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 19: 14-bit Bayer Output Mode

Mode	Byte	D23- D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bayer_14	Single	0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 20: 16-bit Bayer Output Mode

Mode	Byte	D23- D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bayer_16	Single	0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 21: 20-bit Bayer Output Mode

Mode	Byte	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bayer_20	Single	0	0	0	0	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bayer_16+4	Odd	0	0	0	0	0	0	0	0	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4
	Even	0	0	0	0	0	0	0	0	D3	D2	D1	D0	0	0	0	0	0	0	0	0	0	0	0	0

Crossbar

The AP0202AT Rev 2 has a cross-bar functionality that allows the assignment of any Data, Vsync, Hsync, line valid, and frame valid signal to any of the 27 possible parallel output pins. Normally, as is the case for the legacy mode of the AP0202AT REV1, the 27 output pins are named DOUT[23:0], LINE_VALID, FRAM_VALID and META_LINE_VALID.

For AP0202 REV2 these output pins can be considered as DOUT[26:0] with no special assignments as any data bit or control signal may be assigned to any output. If desired, each data bit or control signal may even be assigned to multiple outputs at once.

The crossbar has 27 registers that define how each input should be assigned to each of the 27 possible outputs.

This feature affords a large amount of flexibility for the customer. For example, during PCB layout, the pins can be adjusted to minimize crossovers and optimize routing paths.

Embedded Data and Statistics

Some ON Semiconductor sensor's support a feature that, if enabled, inserts two extra lines at the beginning and end of each frame which contain information about that frame. The first two lines contain specific register values that were used to capture that frame. These values allow the host to know certain important things about how the sensor was configured for that frame, e.g. exposure, gain, image size, etc. The last two lines contain statistics about the image that was captured, e.g. mean values, intensity histograms, etc.

The AP0202AT includes these embedded data in its image data output as embedded data lines in all modes. This feature is supported on output image sizes from full resolution to VGA.

Slave Two-Wire Serial Interface (CCIS)

The two-wire slave serial interface bus enables read/write access to control and status registers within the AP0202AT.

The interface protocol uses a master/slave model in which a master controls one or more slave devices.

Protocol

Data transfers on the two-wire serial interface bus are performed by a sequence of low-level protocol elements, as follows:

- a start or restart condition
- a slave address/data direction byte
- a 16-bit register address
- an acknowledge or a no-acknowledge bit
- data bytes
- a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

The SADDR pin is used to select between two different addresses in case of conflict with another device. If SADDR is LOW, the slave address is 0x90; if SADDR is HIGH, the slave address is 0xBA. See Table 22 below. The user can change the slave address by changing a register value.

Table 22: Two-Wire Interface ID Address Switching

SADDR	Two-Wire Interface Address ID
0	0x90
1	0xBA

Start Condition

A start condition is defined as a HIGH-to-LOW transition on SDATA while SCLK is HIGH.

At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes. One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is low and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a write, and a “1” indicates a read. The default slave addresses used by the AP0202AT are 0x90 (write address) and 0x91 (read address). Alternate slave addresses of 0xBA (write address) and 0xBB (read address) can be selected by asserting the SADDR input signal.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data. The protocol used is outside the scope of the two-wire serial interface specification.

Acknowledge Bit

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No-Acknowledge Bit

The no-acknowledge bit is generated when the receiver does not drive SDATA low during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

Stop Condition

A stop condition is defined as a LOW-to-HIGH transition on SDATA while SCLK is HIGH.

Typical Operation

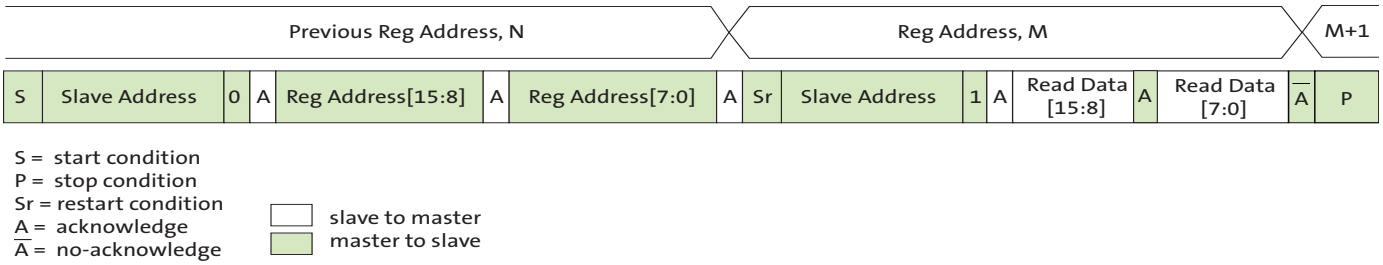
A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a READ or a WRITE, where a “0” indicates a WRITE and a “1” indicates a READ. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16-bit register address to which a WRITE will take place. This transfer takes place as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master will then transfer the 16-bit data, as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master stops writing by generating a (re)start or stop condition. If the request was a READ, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, just as in the write request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and clocks out the register data, 8 bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

Single READ from Random Location

Figure 22 shows the typical READ cycle of the host to the AP0202AT. The first two bytes sent by the host are an internal 16-bit register address. The following 2-byte READ cycle sends the contents of the registers to host.

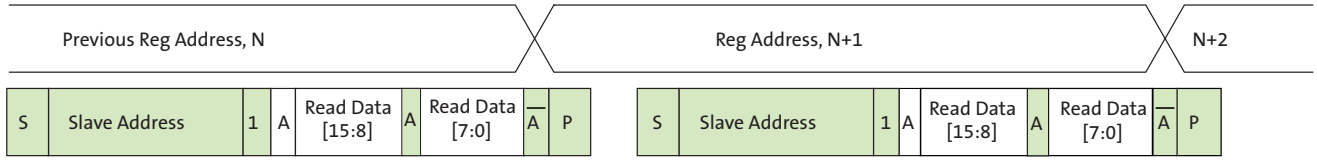
Figure 22: Single READ from Random Location



Single READ from Current Location

Figure 23 shows the single READ cycle without writing the address. The internal address will use the previous address value written to the register.

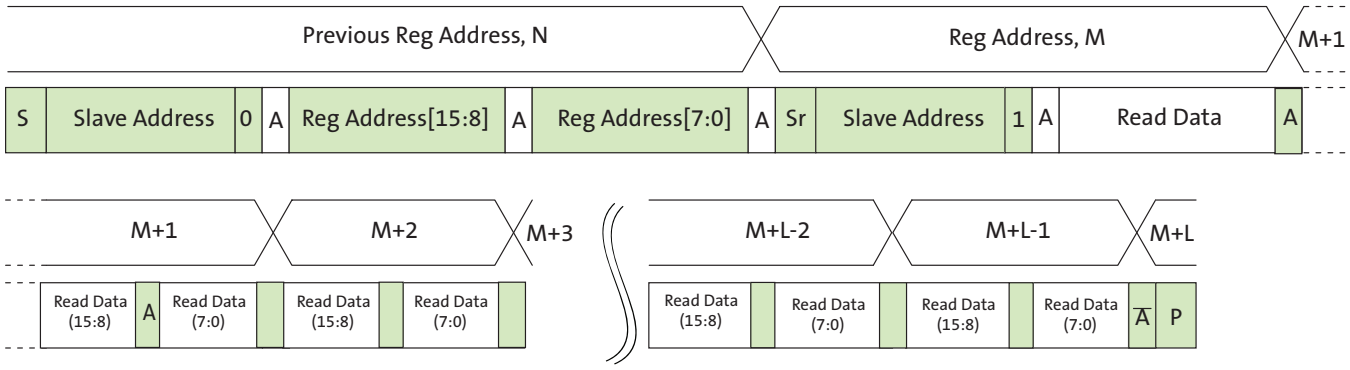
Figure 23: Single Read from Current Location



Sequential READ, Start from Random Location

This sequence (Figure 24) starts in the same way as the single READ from random location (Figure 22 on page 41). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

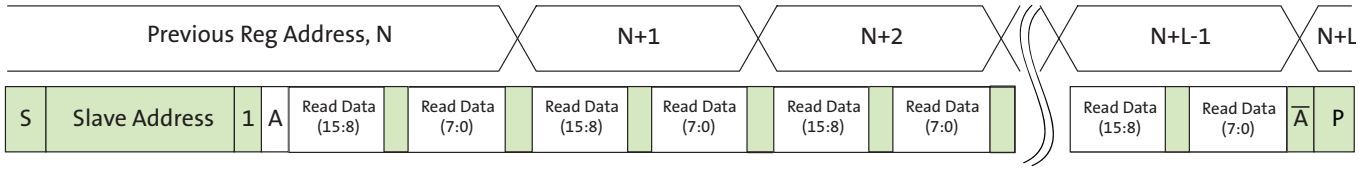
Figure 24: Sequential READ, Start from Random Location



Sequential READ, Start from Current Location

This sequence (Figure 25) starts in the same way as the single READ from current location (Figure 23). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte reads until "L" bytes have been read.

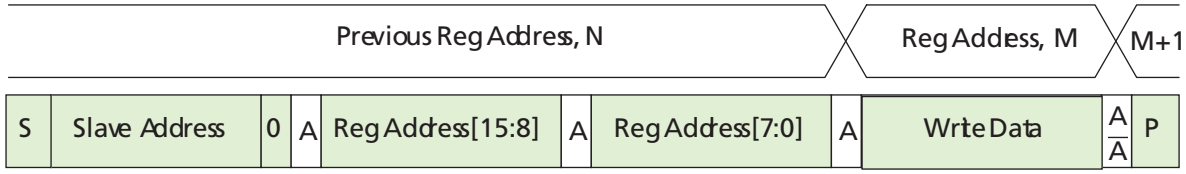
Figure 25: Sequential READ, Start from Current Location



Single Write to Random Location

Figure 26 shows the typical WRITE cycle from the host to the AP0202AT.The first 2 bytes indicate a 16-bit address of the internal registers with most-significant byte first. The following 2 bytes indicate the 16-bit data.

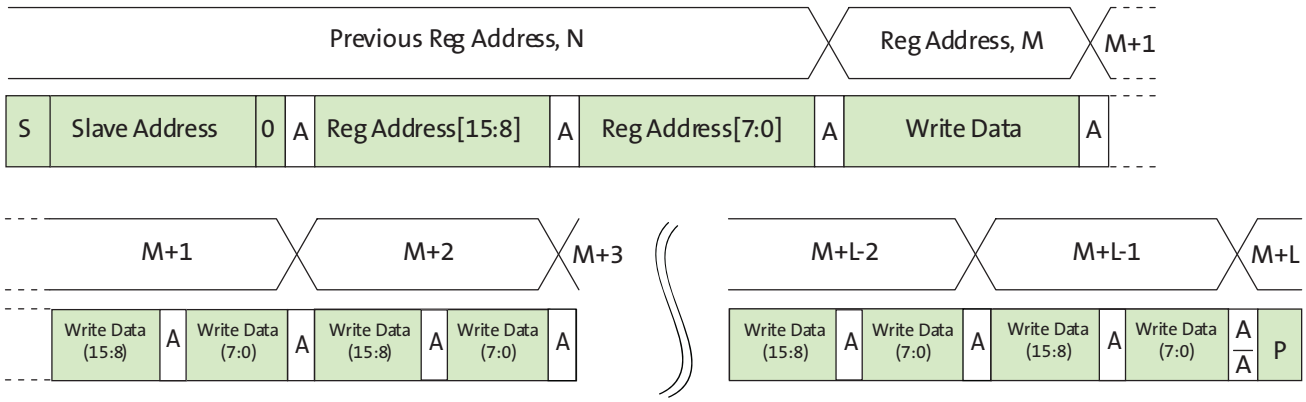
Figure 26: Single WRITE to Random Location



Sequential WRITE, Start at Random Location

This sequence (Figure 27) starts in the same way as the single WRITE to random location (Figure 26). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte writes until "L" bytes have been written. The WRITE is terminated by the master generating a stop condition.

Figure 27: Sequential WRITE, Start at Random Location



Supported SPI Devices

The supported devices are those that conform to the JEDEC-compliant programming interface. Please contact ON Semiconductor for specific design criteria and requirements. The maximum supported device size is 2 Gb.

Host Command Interface

The AP0202AT has a mechanism to write higher level commands, the Host Command Interface (HCI). Once a command has been written through the HCI, it will be executed by on chip firmware and the results are reported back. EEPROM or Flash memory is also available to store commands for later execution.

Full details of the Host Command Interface can be found in the AP0202AT Host Command Interface (HCI) Specification document.

Specifications

Caution **Stresses greater than those listed in Table 23 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

Table 23: Absolute Maximum Ratings

Parameter	Rating		Unit
	Min	Max	
Digital power (1.8V)	-0.3	4.95	V
Host I/O power (1.8V, 2.8V,3.3V)	1.7	4.95	V
Sensor I/O power (1.8V, 2.8V)	1.7	4.95	V
PLL power	1.1	1.8	V
Digital core power	1.1	1.8	V
OTPM power (2.8V, 3.3V)	2.25	4.95	V
DC Input Voltage	-0.3	VDDIO_*+0.3	V
DC Output Voltage	-0.3	VDDIO_*+0.3	V
Storage temperature	-50	150	°C

Table 24: Electrical Characteristics and Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
Supply input to on-chip regulator (VDD_REG)		1.71	1.8	1.89	V
Host IO voltage (VDDIO_H)		1.71	1.8/2.8/3.3	3.46	V
Sensor IO voltage (VDDIO_S)		1.71	1.8/2.8	2.94	V
Core voltage (VDD)		1.14	1.2	1.26	V
PLL voltage (VDD_PLL)		1.14	1.2	1.26	V
HiSPi PHY voltage (VDD_PHY)		2.3	2.8	3.1	V
OTPM power supply (VDDIO_OTPM)		2.38	2.8/3.3	3.47	V
Functional operating temperature (ambient - T_A)		-40		105	°C

Figure 28: I/O Timing Diagram

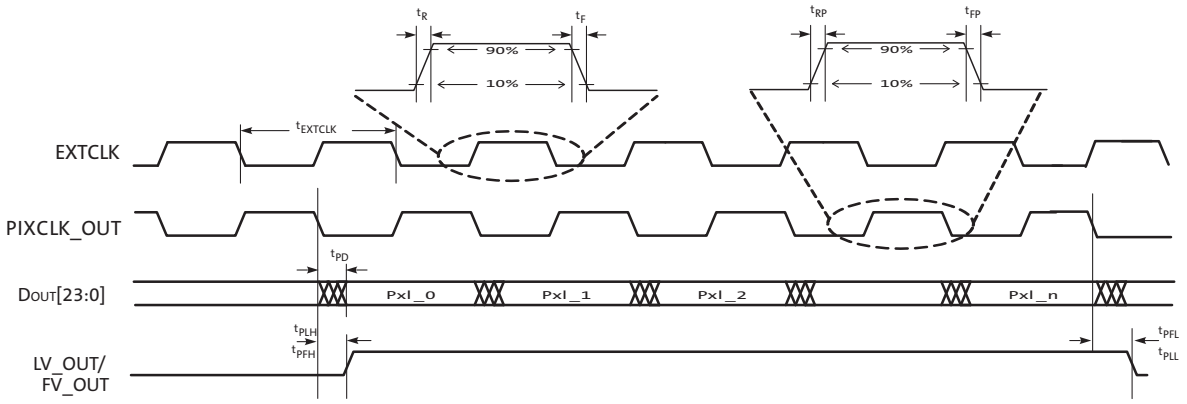


Table 25: I/O Timing Characteristics - Parallel Mode (2.8V V_{DD}_IO)[1,2]

Symbol	Definition	Condition	Min	Typ	Max	Unit
$f_{EXTCLK1}$	Input clock frequency	PLL Enabled	6	-	30	MHz
t_R	Input clock rise time	10%-90% VDDIO_H	-	2	5	ns
t_F	Input clock fall time	10%-90% VDDIO_H	-	2	5	ns
t_{JITTER}	Input clock jitter		-	500	-	ps
t_{RP}	PIXCLK_OUT rise time		-		-	ns
t_{FP}	PIXCLK_OUT fall time		-		-	ns
	Duty Cycle		40	50	60	%
f_{PIXCLK}	PIXCLK_OUT frequency		18	74.25	125	MHz
t_{PD}	PIXCLK_OUT to data valid		-3.5	-	2.0	ns
t_{PFH}	PIXCLK_OUT to FV HIGH		-3.5	-	2.0	ns
t_{PLH}	PIXCLK_OUT to LV HIGH		-3.5	-	2.0	ns
t_{PFL}	PIXCLK_OUT to FV LOW		-3.5	-	2.0	ns
t_{PLL}	PIXCLK_OUT to LV LOW		-3.5	-	2.0	ns

Notes:
1. 1. Minimum and maximum values are taken at 105°C, 2.5V and -40°C, 3.1V. All values are taken at the 50% transition point. The loading used is 10 pF.
2. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.
3. Max PIXCLK frequency varies with IO voltage.

Table 26: I/O Timing Characteristics - Parallel Mode (1.8V V_{DD}_IO)[1,2]

Symbol	Definition	Condition	Min	Typ	Max	Unit
$f_{EXTCLK1}$	Input clock frequency	PLL Enabled	6	-	30	MHz
t_R	Input clock rise time	10%-90% V_{DD}IO_H	-	2	5	ns
t_F	Input clock fall time	10%-90% V_{DD}IO_H	-	2	5	ns
t_{JITTER}	Input clock jitter		-	500	-	ps
t_{RP}	PIXCLK_OUT rise time		-		-	ns
t_{FP}	PIXCLK_OUT fall time		-		-	ns
	Duty Cycle		40	50	60	%
f_{PIXCLK}	PIXCLK_OUT frequency		18	74.25	80	ns
t_{PD}	PIXCLK_OUT to data valid		-3.5	-	2.0	ns
t_{PFH}	PIXCLK_OUT to FV HIGH		-3.5	-	2.0	ns
t_{PLH}	PIXCLK_OUT to LV HIGH		-3.5	-	2.0	ns
t_{PFL}	PIXCLK_OUT to FV LOW		-3.5	-	2.0	ns
t_{PLL}	PIXCLK_OUT to LV LOW		-3.5	-	2.0	ns

Notes: 1. Minimum and maximum values are taken at 105, 1.7V and -40C, 1.95V. All values are taken at the 50% transition point. The loading used is 10 pF.
2. Jitter from PIXCLK_OUT is already taken into account in the data for all of the output parameters.

Table 27: DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{IH}	Input HIGH voltage		V_{DD}IO_H or V_{DD}IO_S * 0.8	–	V	1
V_{IL}	Input LOW voltage		–	V_{DD}IO_H or V_{DD}IO_S * 0.2	V	1
I_{IN}	Input leakage current	V_{IN}= 0V or V_{IN} = V_{DD}IO_H or V_{DD}IO_S		10	µA	2
V_{OH}	Output HIGH voltage		V_{DD}IO_H or V_{DD}IO_S* 0.80	–	V	
V_{OL}	Output LOW voltage		–	V_{DD}IO_H or V_{DD}IO_S * 0.2	V	

Notes: 1. VIL and VIH have min/max limitations specified by absolute ratings.
2. Excludes pins that have internal PU resistors.

Table 28: Input Clocks

Clock	Min (MHz)	Typical (MHz)	Max (MHz)	Description
EXTCLK	10 - osc 20 - xtal	27	29	Primary system clock. Drives PLLs. Crystal frequency range is 20-29 MHz, otherwise 10-29 MHz.
PIXCLK_IN	10	74.25	80	Clock for parallel input bus (from sensor).
HiSPi_CLK	30		300	Clock for HISPI image data receiver.

Table 29: Output Clocks

Clock	Min (MHz)	Typical (MHz)	Max (MHz)	Description
EXTCLK_OUT	10	27	29	Primary clock to sensor. Equals EXTCLK.
PIXCLK_OUT	18	74.25	80	Clock of parallel output bus. If pad voltage is 1.8 V nominal, then max frequency is 80 MHz. If pad voltage is 2.5 V, the hold time will decrease to 1.9 ns from 2.0 ns at 125 MHz. If pad voltage is 3.3 V, then the max frequency is 125 MHz.
SPI_CLK	1		20	SPI clock to nonvolatile external memory.

Figure 29: Frame_Sync Diagram

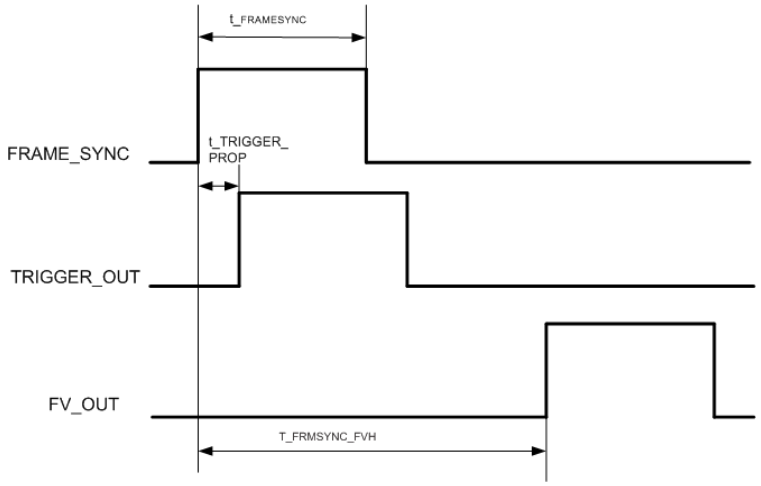


Table 30: Trigger Timing

Parameter	Name	Conditions	Min	Typ	Max	Unit
FRAME_SYNC to FV_OUT	$t_{FRMSYNC\_FVH}$		8 lines+ exposure time + sensor delay	–	–	Lines
FRAME_SYNC to TRIGGER_OUT	$t_{TRIGGER\_PROP}$		–	–	30	ns
t_{FRAME_SYNC}	$t_{FRAMESYNC}$		3	–	–	EXTCLK cycles

Table 31: Standby Current Consumption

Default Setup Conditions: f_{EXTCLK} = 27 MHz, V_{DD}_REG=1.8V; V_{DD}IO_H not included in measurement V_{DD}IO_S= 1.8V, V_{DD}IO_OTPM=2.8V, V_{DD}_PHY=2.8V, T_A = 105°C unless otherwise stated

Parameter	Condition	Typ	Max	Unit
IDD_REG		1.50	1.91	mA
IDDIO_S		0.19	0.24	mA
IDDIO_H		1.20	1.52	mA
IDDIO_OTPM		0.18	0.23	mA
IDDIO_PHY		0.00	0.00	mA
Total Standby Power		7.46	9.47	mW

Table 32: Inrush Current

Supply	Voltage	Typ	Max	Unit
V_{DD}_REG	1.8	130	180	mA
V_{DD}IO_H	2.8/3.3	140	190	mA
V_{DD}IO_S	2.8	90	105	mA
V_{DD}_PHY	2.8	180	180	mA
V_{DD}IO_OTPM	2.8/3.3	140	160	mA

Table 33: Operating Current Consumption

Default Setup Conditions: f_{EXTCLK} = 27 MHz, V_{DD}_REG=1.8V; V_{DD}IO_H not included in measurement V_{DD}IO_S= 1.8V, V_{DD}IO_OTPM=2.5V, V_{DD}_PHY=2.5V, T_A =105°C unless otherwise stated

Symbol	Input Data from Sensor	Min	Typ	Max	Unit
V_{DD}_REG	YCbCr		85	108	mA
V_{DD}IO_S	YCbCr		3.0	4.0	mA
V_{DD}IO_OTPM	YCbCr		0.2	0.3	mA
V_{DD}_PHY	YCbCr		0.2	0.3	mA
Total Power Consumption	YCbCr		159	202	mW

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (SCLK, SDATA) are shown in Figure 30 and Table 34.

Figure 30: Slave Two Wire Serial Bus Timing Parameters (CCIS)

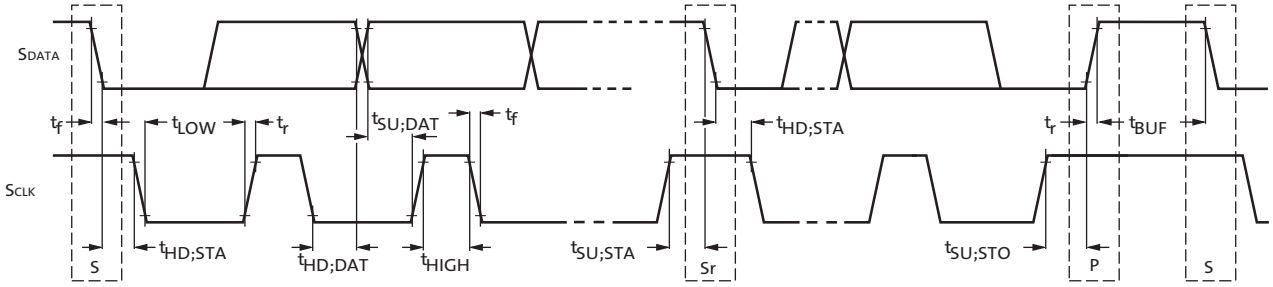


Table 34: Slave Two-Wire Serial Bus Characteristics (CCIS)

Default Setup Conditions: fEXTCLK = 27 MHz; VDDIO_H = VDD_OTPM = 2.8V; VDD_REG = VDDIO_S = 1.8V; T_A = 25°C unless otherwise stated

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	f_{SCL}	0	100	0	400	KHz
Hold time (repeated) START condition.						
After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	µs
LOW period of the SCLK clock	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of the SCLK clock	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µs
Data hold time	$t_{HD;DAT}$	0[2]	3.45[3]	0	0.9[3]	µSs
Data set-up time	$t_{SU;DAT}$	250	-	100	-	ns
Rise time of both SDATA and SCLK signals (10-90%)	t_r	-	1000	20 + 0.1Cb[4]	300	ns
Fall time of both SDATA and SCLK signals (10-90%)	t_f	-	300	20 + 0.1Cb[4]	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µs
Capacitive load for each bus line	Cb	-	400	-	400	pF
Serial interface input pin capacitance	C_{IN_SI}	-	3.3	-	3.3	pF
SDATA max load capacitance	C_{LOAD_SD}	-	30	-	30	pF
SDATA pull-up resistor	R_{SD}	1.5	4.7	1.5	4.7	KΩ

Notes:
1. All values referred to VIHmin = 0.9 VDDIO_H and VILmax = 0.1 VDDIO_H levels. EXCLK = 27 MHz.
2. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
3. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCLK signal.
4. Cb = total capacitance of one bus line in pF.

The electrical characteristics of the master two-wire serial register interface (M_SCLK, M_SDATA) are shown in Figure 31 and Table 35.

Figure 31: Master Two Wire Serial Bus Timing Parameters (CCIM)

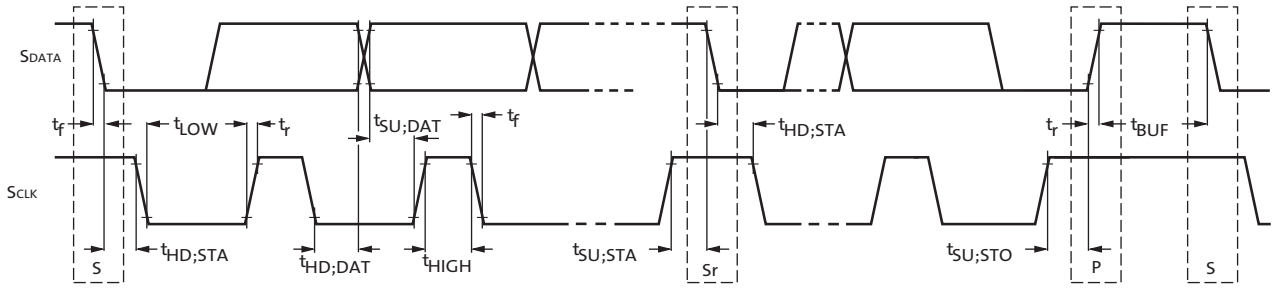


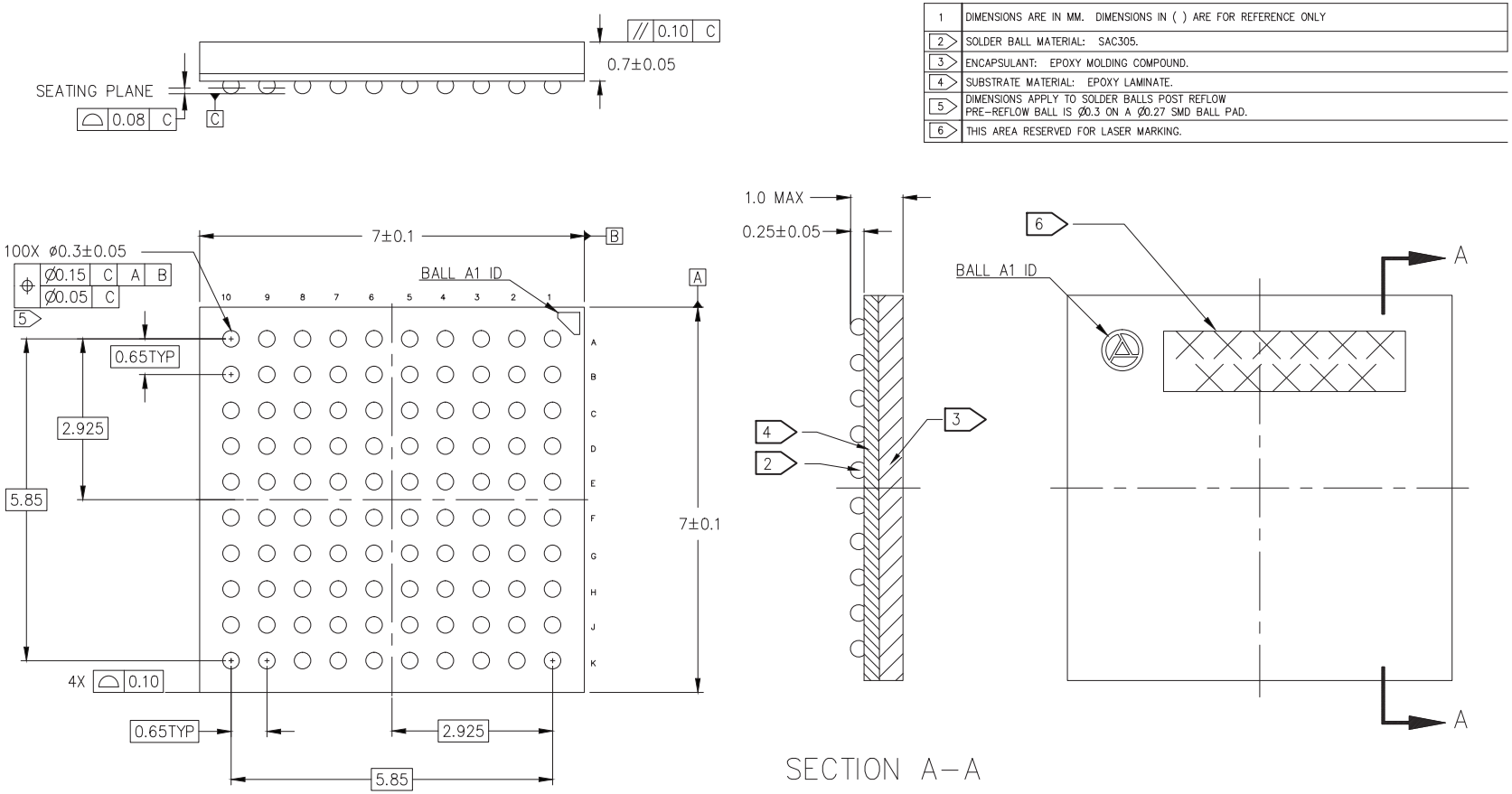
Table 35: Master Two-Wire Serial Bus Characteristics (CCIM)
Default Setup Conditions: f_{EXTCLK} = 27 MHz; V_{DDIO_H} = V_{DD_OTPM} = 2.8V; V_{DD_REG} = V_{DDIO_S} = 1.8V; T_A = 25°C unless otherwise stated

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
M_SCLK Clock Frequency	f_{SCL}	0	100	0	400	KHz
Hold time (repeated) START condition.						
After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	µs
LOW period of the M_SCLK clock	t_{LOW}	4.7	-	1.2	-	µs
HIGH period of the M_SCLK clock	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µs
Data hold time	$t_{HD;DAT}$	0[2]	3.45[3]	0	0.9[3]	µs
Data set-up time	$t_{SU;DAT}$	250	-	100	-	ns
Rise time of both M_SDATA and M_SCLK time (10-90%)	t_r	-	1000	20 + 0.1Cb[4]	300	ns
Fall time of both M_SDATA and M_SCLK time (10-90%)	t_f	-	300	20 + 0.1Cb[4]	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µs
Capacitive load for each bus line	Cb	-	400	-	400	pF
Serial interface input pin capacitance	C_{IN_SI}	-	3.3	-	3.3	pF
M_SDATA max load capacitance	C_{LOAD_SD}	-	30	-	30	pF
M_SDATA pull-up resistor	R_{SD}	1.5	4.7	1.5	4.7	KΩ

Notes:
1. All values referred to VIHmin = 0.9 V_{DDIO} and VILmax = 0.1 V_{DDIO} levels. EXCLK = 27 MHz.
2. A device must internally provide a hold time of at least 300 ns for the M_SDATA signal to bridge the undefined region of the falling edge of M_SCLK.
3. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the M_SCLK signal.
4. Cb = total capacitance of one bus line in pF.

Package Diagram

Figure 32: Package Diagram



1	DIMENSIONS ARE IN MM. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY
2	SOLDER BALL MATERIAL: SAC305.
3	ENCAPSULANT: EPOXY MOLDING COMPOUND.
4	SUBSTRATE MATERIAL: EPOXY LAMINATE.
5	DIMENSIONS APPLY TO SOLDER BALLS POST REFLOW PRE–REFLOW BALL IS Ø0.3 ON A Ø0.27 SMD BALL PAD.
6	THIS AREA RESERVED FOR LASER MARKING.

Revision History

Rev. 3, Advance 9/15

- Changes throughout

Rev. 3, Advance 5/15/15

- Updated "Ordering Information," on page 2
- Updated Table 1: "Key Performance Parameters," on page 1
- Updated "Functional Overview" on page 6
- Updated Figure 6: "Hard Reset Operation," on page 16
- Updated "Hard Standby Mode" on page 18
- Updated "Device Configuration" on page 19
- Updated "Usage Modes" on page 19
- Added "Crossbar" on page 38
- Updated "Supported SPI Devices" on page 43
- Updated Table 25, "I/O Timing Characteristics - Parallel Mode (2.8V V_{DD_IO})[1,2]," on page 45
- Updated Table 26, "I/O Timing Characteristics - Parallel Mode (1.8V V_{DD_IO})[1,2]," on page 46
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- Modified Figure 3: "Typical Parallel Configuration," on page 8
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- Deleted ASIL/ISO26262 Support Features
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- Added Table 27: "DC Electrical Characteristics," on page 46
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- Initial release

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