



SDLink datasheet

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This document describes SDLink specification.

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1.DC Electrical Characteristic

[Table1-1] Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Vcc1	Supply voltage for microSD	-0.5	+4.3	V
Vcc2	Supply voltage for Configuration	-0.5	+4.3	V
Tstg	Storage temperature	-40	+85	°C
Topr	Operating temperature	-20	+85	°C
Vin	DC input voltage	-2.0	+4.3	V
Iout	DC output voltage	-25	+25	mA

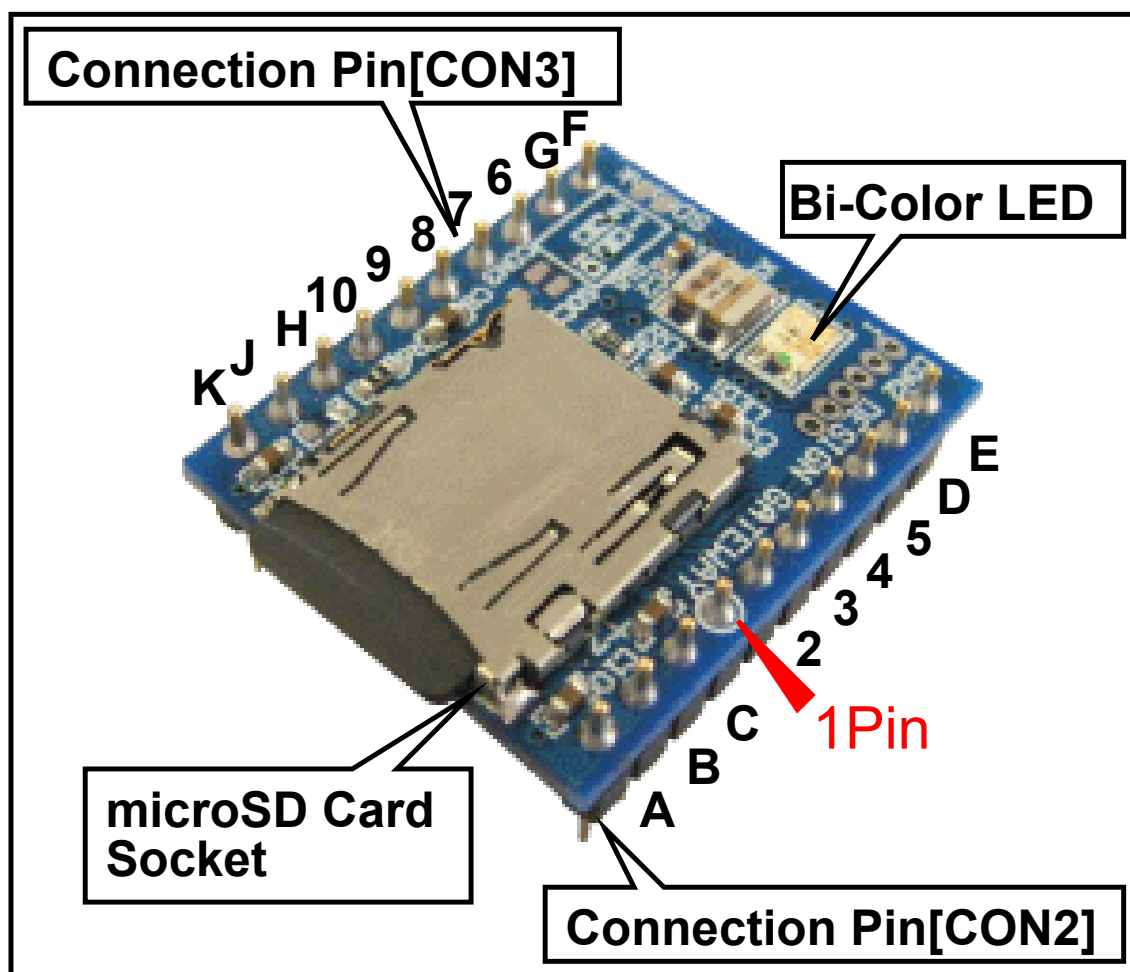
[Table1-2] Recommended Operating Condition

Symbol	Parameter	Min	Max	Unit
Vcc1	Supply voltage for microSD	+3.0	+3.6	V
Vcc2	Supply voltage for Configuration (3.3V)	+3.0	+3.6	V
	Supply voltage for Configuration (3.0V) ^(*)	+2.85	+3.15	
	Supply voltage for Configuration (2.5V)	+2.375	+2.625	V
	Supply voltage for Configuration (1.8V)	+1.7	+1.9	V
Topr	Operating temperature	0	+70	°C
Vih	High level input voltage (Vcc2=3.3V)	+1.7	+3.6	V
	High level input voltage (Vcc2=3.0V) ^(*)	+1.7	+3.15	V
	High level input voltage (Vcc2=2.5V)	+1.7	+2.625	V
	High level input voltage (Vcc2=1.8V)	+1.25	+1.9	V
Vil	Low level input voltage (Vcc2=3.3V)	-0.5	+0.8	V
	Low level input voltage (Vcc2=3.0V) ^(*)	-0.3	+0.8	V
	Low level input voltage (Vcc2=2.5V)	-0.5	+0.7	V
	Low level input voltage (Vcc2=1.8V)	-0.5	+0.7	V
Voh	High level output voltage (Vcc2=3.3V)	+2.4		V
	High level output voltage (Vcc2=3.0V) ^(*)	+2.4		V
	High level output voltage (Vcc2=2.5V)	+2.0		V
	High level output voltage (Vcc2=1.8V)	+1.35		V
Vol	Low level output voltage (Vcc2=3.3V)		+0.45	V
	Low level output voltage (Vcc2=3.0V) ^(*)		+0.45	V
	Low level output voltage (Vcc2=2.5V)		+0.45	V
	Low level output voltage (Vcc2=1.8V)		+0.45	V

Note:

(*) Vcc2=3.0V Configuration is valid only for Stratix4.

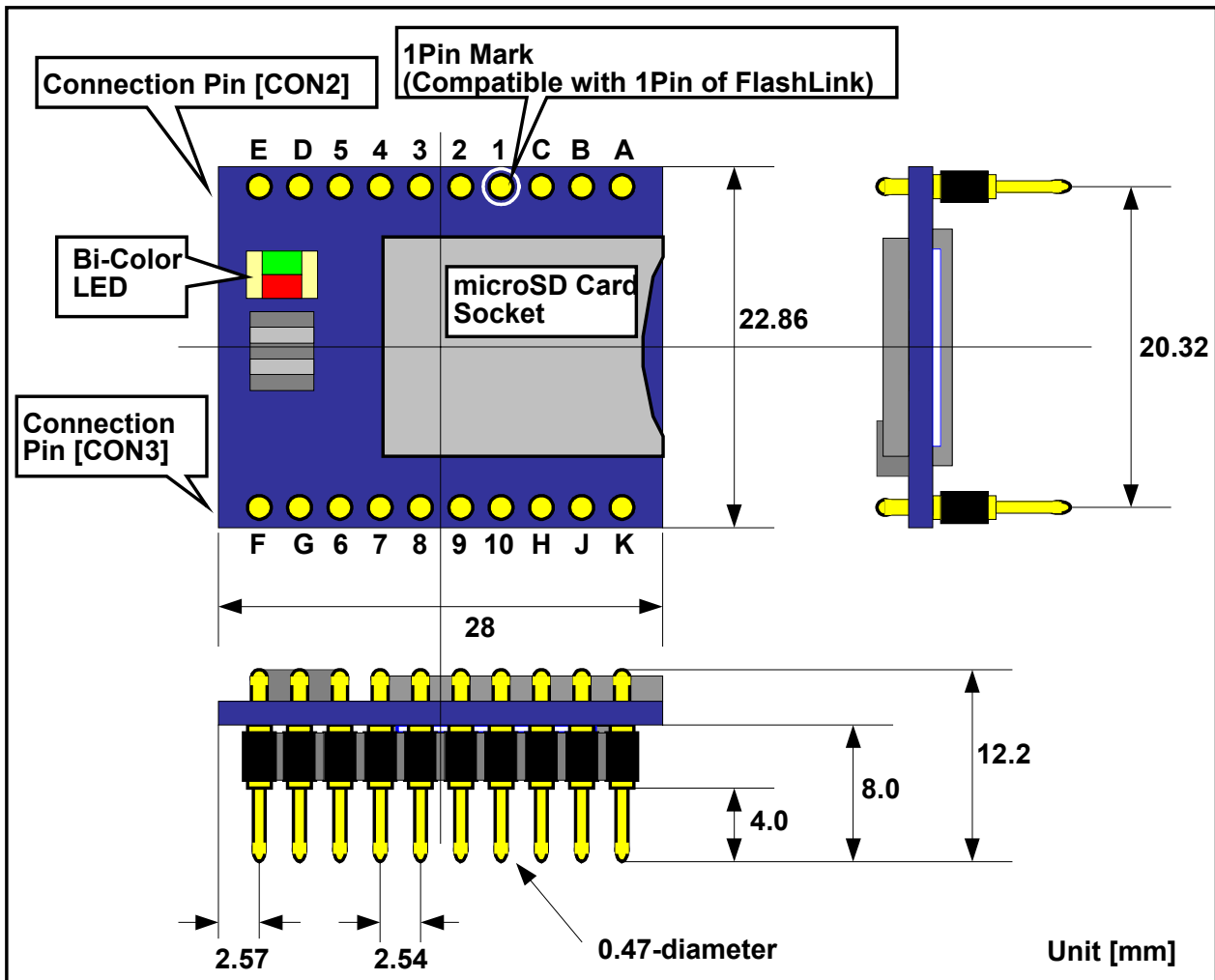
2.SDLink Module Outline



[Figure 2-1] SDLink Module Outline

- Connection Pins for user board connection are DIP type pins of two lines.
- 10 pins of pin number A, B, C, 1to5, D, and E are [CON2] side, and 10 pins of pin number F, G, 6to10, H, J, and K are [CON3] side.
- Pin number 1 at [CON2] side has white circle overlay indicator.
- For FlashLink-compatible version (SL001-FL), [CON2] only mounts pin number 1to5 and [CON3] only mounts pin number 6to10, so total pin count is 10.
- Because microSD card is push-lock type socket, prepare enough space at open side of the socket for microSD card insertion and extraction.
- Bi-color LED shows FPGA configuration status.

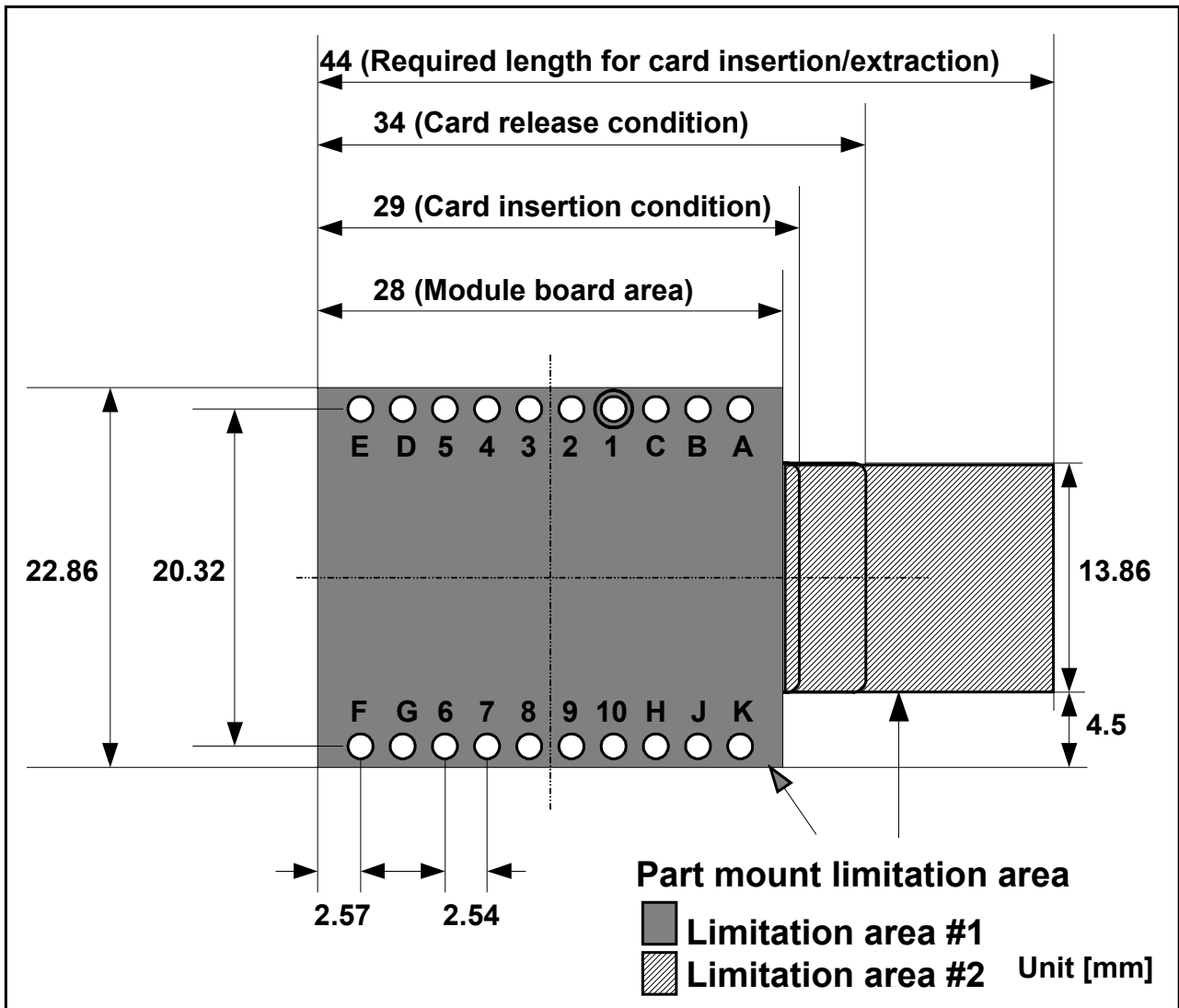
3. Mechanical Data



[Figure3-1] SDLink Mechanical Data

- SDLink module size is Length=28mm, Width=22.86mm, Height=12.2mm.
- When module is directly soldered on the user board, module height is about 8.5mm from the user board surface.
- Connection pin gap is 20.32mm (800mil), and pin pitch is 2.54mm (100mil).
- For FlashLink-compatible version (SL001-FL), pin number A, B, C, D, E, F, G, H, J, and K are not mounted.

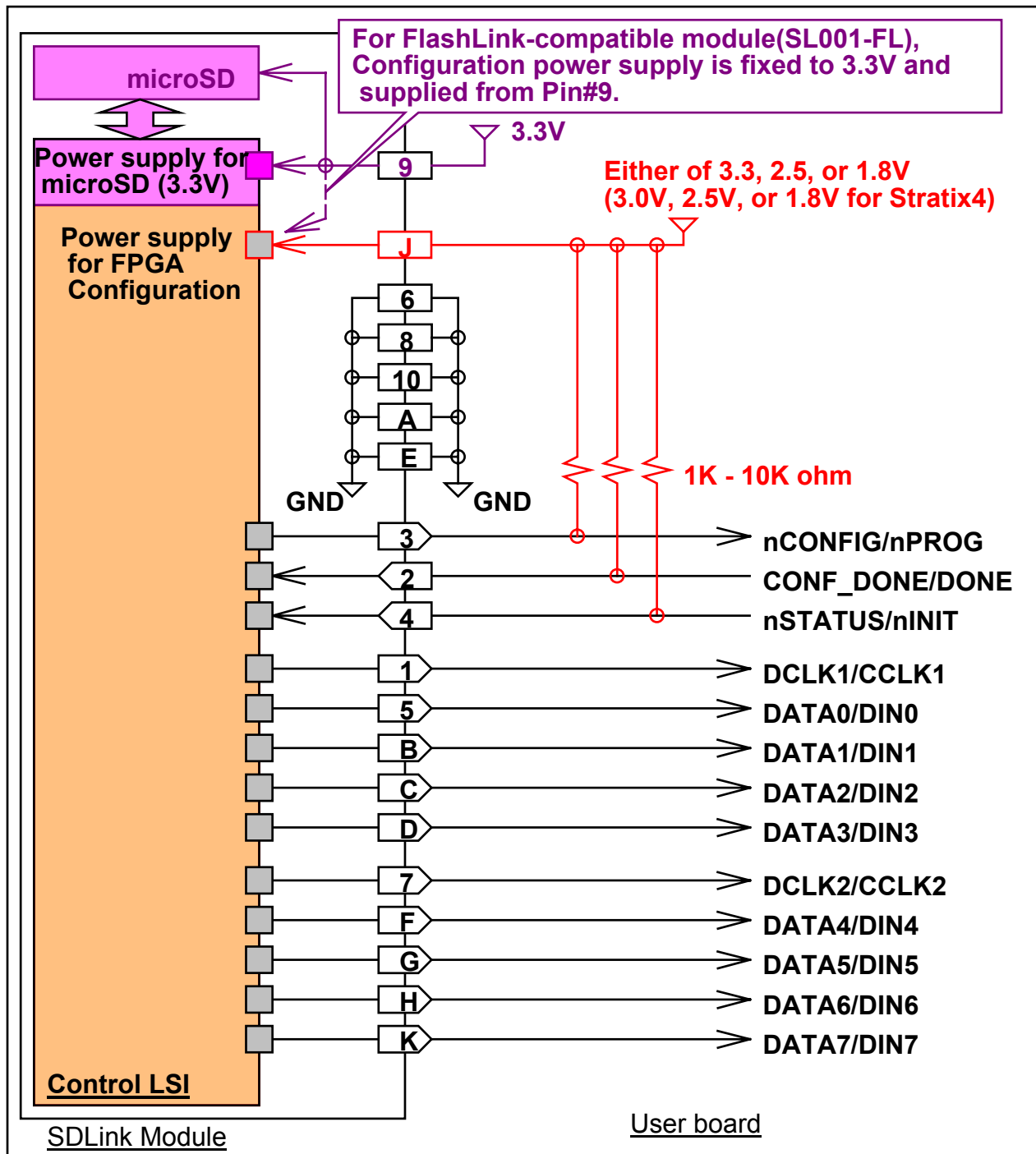
4. User Board Recommendation Pattern



[Figure 4-1] User board recommendation pattern

- Keep part mount limitation area shown in Figure4-1 on the user board.
- Gray area of Limitation area #1 specifies SDLink module mount area, and slanted area of Limitation area #2 specifies necessary space to insert/extract microSD card.
- Do not mount part on the Limitation area #1 (Pattern routing is possible).
- On the Limitation area#2, mount part height should be 3mm or less.

5.Connection Diagram and Pin Description



[Figure5-1] User board connection diagram

- Refer to [SDLink User Board Design Guide] (Document number: SL-AN01) for the practical circuit design.

[Table5-1] Connection Pin description (CON2)

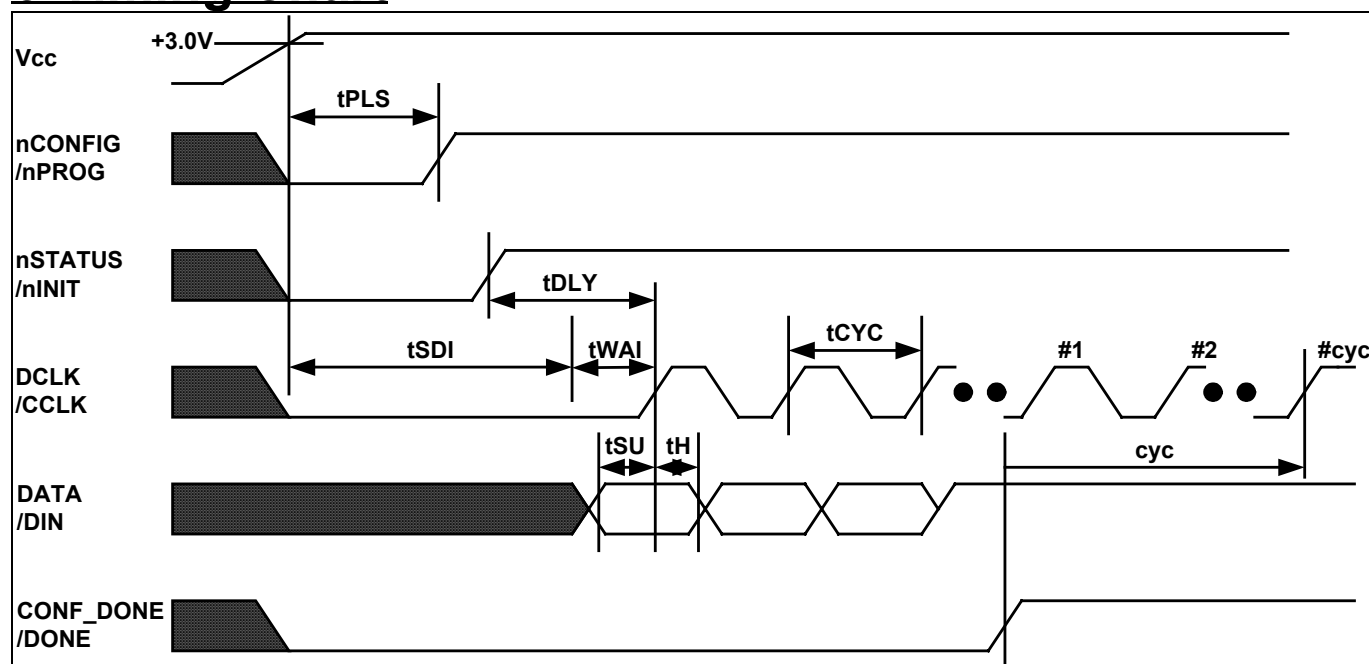
#	Signal Name	I/O	Polarity	Description
A	GND	Power	-	● Signal Ground
B	DATA1 /DIN1	Out	Positive	● Configuration data bit #1
C	DATA2 /DIN2	Out	Positive	● Configuration data bit #2
1	DCLK1 /CCLK1	Out	Positive	● Configuration clock #1 ● This pin and DCLK2/CCLK2 are the identical clock output. ● To keep clock signal quality, balance both clock fan out count. ● Mount Thevenin termination network that resistor value is about 330 to 1Kohm for both clock pattern traces. ● Build single stroke pattern starting from SDLink and end at termination resistor for clock signal.
2	CONF_DONE /DONE	In	Positive	● Configuration completion status ● Mount 1K to 10Kohm pull-up resistor toward the configuration power supply on the user board. ● This pin is 3.3V tolerant whichever VIO voltage is 1.8V, 2.5V, or 3.3V.
3	nCONFIG /nPROG	Out	Negative	● Configuration start signal ● Mount 1K to 10Kohm pull-up resistor toward the configuration power supply on the user board because it is open-drain output. ● SDLink will execute re-configuration when forced to low level on the user board. ● This pin is 3.3V tolerant whichever VIO voltage is 1.8V, 2.5V, or 3.3V.
4	nSTATUS /nINIT	In	Negative	● Configuration error status ● Mount 1K to 10Kohm pull-up resistor toward the configuration power supply on the user board. ● This pin is 3.3V tolerant whichever VIO voltage is 1.8V, 2.5V, or 3.3V.
5	DATA0 /DIN0	Out	Positive	● Configuration data bit #0
D	DATA3 /DIN3	Out	Positive	● Configuration data bit #3
E	GND	Power	-	● Signal Ground

[Table 5-2] Connection Pin description (CON3)

#	Signal Name	I/O	Polarity	Description
F	DATA4 /DIN4	Out	Positive	Configuration data bit #4
G	DATA5 /DIN5	Out	Positive	Configuration data bit #5
6	GND	Power	-	Signal Ground
7	DCLK2 /CCLK2	Out	Positive	- Configuration clock #2 - This pin and DCLK1/CCLK1 are the identical clock output. - To keep clock signal quality, balance both clock fan out count. - Mount Thevenin termination network that resistor value is about 330 to 1Kohm for both clock pattern traces. - Build single stroke pattern starting from SDLink and end at termination resistor for clock signal.
8	GND	Power	-	Signal Ground
9	+3.3V	Power	-	+3.3V power supply for microSD - User board must supply +3.3V - Mount bypass capacitor that capacity is 0.1uF or larger adjacent to this pin on the user board.
10	GND	Power	-	Signal Ground
H	DATA6 /DIN6	Out	Positive	Configuration data bit #6
J	VIO	Power	-	- Configuration power supply - Supply either of +3.3V (+3.0V for Stratix4), +2.5V, or +1.8V to adjust to the configuration power supply of FPGA. - Fundamentally, adjust this VIO voltage to the IO Bank voltage of configuration clock input in FPGA. - Mount bypass capacitor that capacity is 0.1uF or larger adjacent to this pin on the user board.
K	DATA7 /DIN7	Out	Positive	Configuration data bit #7

- For FlashLink-compatible version (SL001-FL), pin number A, B, C, D, E, F, G, H, J, and K are not mounted. And 3.3V configuration power is supplied via Pin#9.

6. Timing Chart



[Figure6-1] Timing Chart

[Table6-1] Timing characteristics

Symbol	Description	Min	Typ	Max	Unit
tPLS	nCONFIG/nPROG low pulse width		8		ms
tSDI	microSD initialization duration (It depends on microSD brand and type)		300		ms
tWAI	Variable delay set by SDLink software	0	0	2550	ms
tDLY	nSTATUS/nINIT high release to 1 st data output delay		250		ms
tSU	Configuration data setup time		12.5		ns
tH	Configuration data hold time		12.5		ns
tCYC	Configuration clock cycle time	400	50	25	ns
cyc	DCLK/CCLK additional clock cycle count after configuration completion.		256	512	(count)

Note:

- Timing Characteristics are tentative and might be changed without notice
- Typical condition: configuration in 1-bit Passive Serial mode, normal microSD Card, and highest configuration speed.
- tPLS : nCONFIG/nPROG is driven low by internal controller of SDLink. For power-up configuration, real tPLS duration will be extended to very long time (several hundred milli-sec) because of additional initialization period of SDLink internal controller and microSD.
- tDLY: Real tDLY duration will vary with FPGA size or microSD initialization time on the SDLink.

Revision History

Rev.	Date	Description
1.0	Mar/06/2008	Initial revision release
1.1	Mar/13/2008	Fixed timing chart specification
1.2	Apr/01/2008	Fixed Vin (Absolute Max rating of DC input voltage) value in Table1-1.
1.3	Dec/02/2008	Added Stratix4 Added Timing diagram description.

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