

1. General description

Planar passivated Silicon Controlled Rectifier in a SOT1259 (3-lead TO-3P) plastic package intended for use in applications requiring very high inrush current capability and high thermal cycling performance.

2. Features and benefits

- High thermal cycling performance
- · Planar passivated for voltage ruggedness and reliability
- High voltage capacity
- · Very high current surge capability

3. Applications

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control
- Uninterruptible Power Supply (UPS)
- Solid State Relay (SSR)
- Traction battery charging

4. Quick reference data

Table 1. Quid	ck reference data						
Symbol	Parameter	Conditions	IV	lin	Тур	Max	Unit
V _{DRM}	repetitive peak off- state voltage		-		-	1400	V
V _{RRM}	repetitive peak reverse voltage		-		-	1400	V
I _{TSM}	non-repetitive peak on- state current	half sine wave; T _{j(init)} = 25 °C; t _p = 10 ms; <u>Fig. 4</u> ; <u>Fig. 5</u>	-		-	750	A
		half sine wave; T _{j(init)} = 25 °C; t _p = 8.3 ms	-		-	825	A
Tj	junction temperature		-		-	150	°C
I _{T(AV)}	average on-state current	half sine wave; $T_{mb} \le 124 \text{ °C}$	-		-	60	A
I _{T(RMS)}	RMS on-state current	half sine wave; $T_{mb} \le 124 \text{ °C}$; <u>Fig. 1</u> ; <u>Fig. 2</u> ; <u>Fig. 3</u>	-		-	94	А

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; <u>Fig. 7;</u> <u>Fig. 8</u>	-	-	80	mA
Dynamic ch	naracteristics		·	·		
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 938 V; T _j = 150 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	150	0 -	-	V/µs

5. Pinning information

Table 2. Pinning information Pin Symbol Description **Simplified outline Graphic symbol** 1 Κ cathod А₽К $\bigcirc \bigcirc \land$ Ġ 2 А anode sym037 3 G gate 0 mounting base; connected to mb mb anode 2 3 TO3P (SOT1259)

6. Ordering information

Table 3. Ordering information						
Type number	Package					
	Name	Description	Version			
TYN60K-1400T	тозр	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO3P	SOT1259			

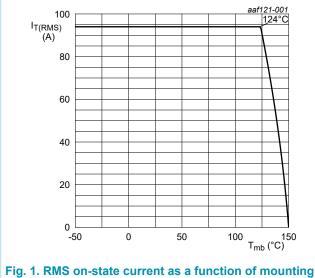
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7. Limiting values

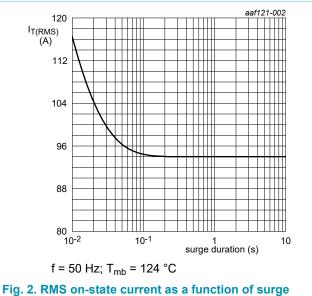
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DRM}	repetitive peak off-state voltage		-	1400	V
V _{RRM}	repetitive peak reverse voltage		-	1400	V
I _{T(AV)}	average on-state current	half sine wave; T _{mb} ≤ 124 °C	-	60	А
I _{T(RMS)}	RMS on-state current	half sine wave; T _{mb} ≤ 124 °C; <u>Fig. 1;</u> <u>Fig. 2; Fig. 3</u>	-	94	A
I _{TSM}	non-repetitive peak on- state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5	-	750	A
		half sine wave; T _{j(init)} = 25 °C; t _p = 8.3 ms	-	825	А
l ² t	I ² t for fusing	t _p = 10 ms; sine-wave pulse	-	2812	A²s
dl _T /dt	rate of rise of on-state current	I _G = 200 mA	-	150	A/µs
I _{GM}	peak gate current		-	8	А
V _{RGM}	peak reverse gate voltage		-	5	V
P _{GM}	peak gate power		-	20	W
P _{G(AV)}	average gate power	over any 20 ms period	-	1	W
T _{stg}	storage temperature		-40	150	°C
Tj	junction temperature		-	150	°C



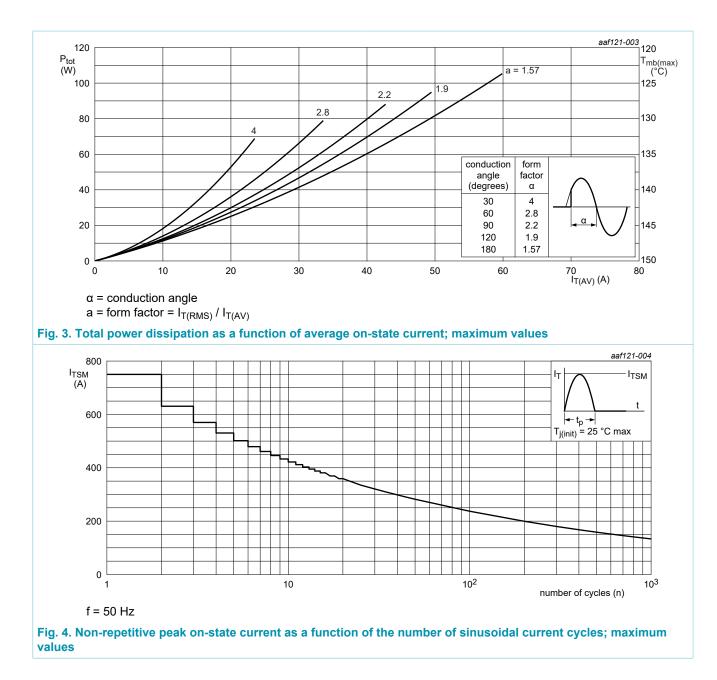
base temperature; maximum values



duration; maximum values

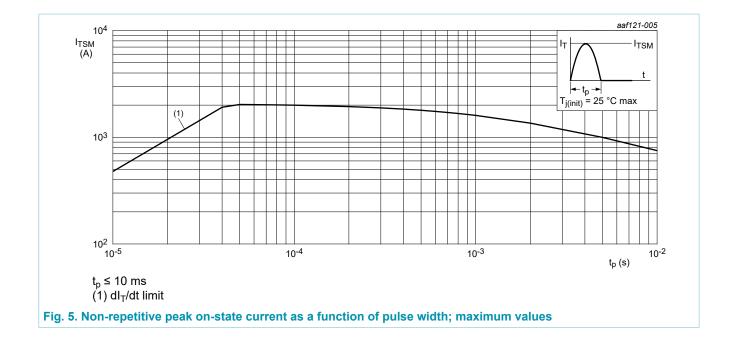
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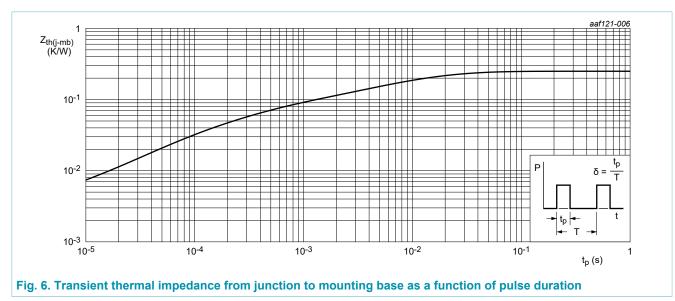
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8. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	full cycle; <u>Fig. 6</u>	-	-	0.25	K/W
R _{th(j-a)}	thermal resistance from junction to ambient free air	in free air	-	50	-	K/W



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9. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics	· · · · · ·				
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; <u>Fig. 7;</u> <u>Fig. 8</u>	-	-	80	mA
IL	latching current	V _D = 12 V; I _G = 0.1 A; T _j = 25 °C; <u>Fig. 9</u>	-	155	300	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 10</u>	-	115	200	mA
V _T	on-state voltage	I _T = 60 A; T _j = 25 °C; <u>Fig. 11</u>	-	-	1.35	V
		I _T = 120 A; T _j = 25 °C; <u>Fig. 11</u>	-	-	1.65	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; <u>Fig. 12</u>	-	0.7	1	V
		V _D = 800 V; I _T = 0.1 A; T _j = 150 °C; <u>Fig. 12</u>	0.2	0.45	-	V
ID	off-state current	V _D = 1400 V; T _j = 150 °C	-	5	10	mA
I _R	reverse current	V _R = 1400 V; T _j = 150 °C	-	3	10	mA
Dynamic ch	naracteristics	· · · · · · · · · · · · · · · · · · ·				
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 938 V; T _j = 150 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	150) -	-	V/µs
t _{gt}	gate-controlled turn-on time	I_{TM} = 40 A; V _D = 800 V; I _G = 0.1 A; dI _G / dt = 5 A/µs; T _j = 25 °C	-	2	-	μs
tq	commutated turn-off time	V_{DM} = 938 V; T _j = 125 °C; I _{TM} = 20 A; V _R = 25 V; (dI _T /dt) _M = 30 A/µs; dV _D / dt = 50 V/µs; R _{GK(ext)} = 100 kΩ; (V _{DM} = 67% of V _{DRM})	-	150	-	μs

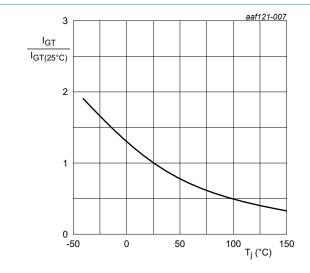
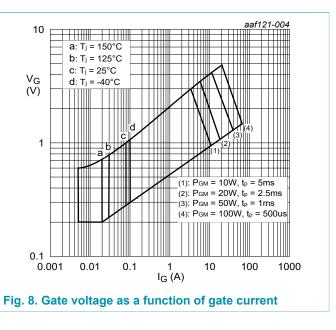


Fig. 7. Normalized gate trigger current as a function of junction temperature



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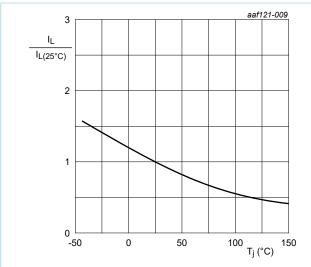
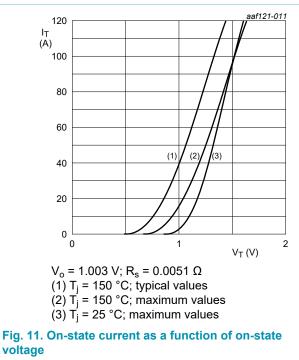
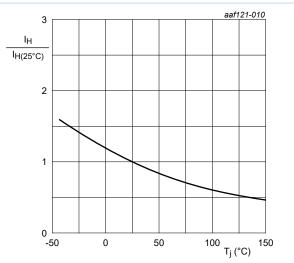


Fig. 9. Normalized latching current as a function of junction temperature







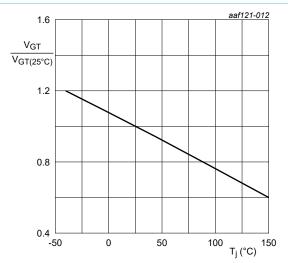
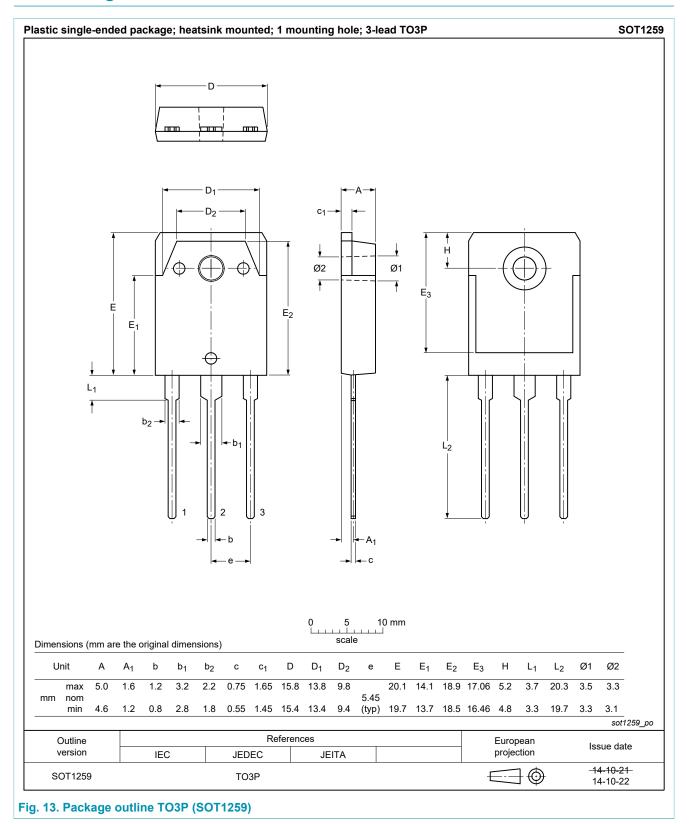


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

10. Package outline



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11. Legal information

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Document status [1][2]	Product status [<u>3]</u>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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