

Circuit Note CN-0290

Circuits from the **Lab**™ Reference Circuits

Circuits from the LabTM reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0290.

Devices Connected/Referenced		
ADF4106	PLL Frequency Synthesizer	
ADCLK905	ECL 1:1 Clock Buffer	
ADCLK925	ECL 1:2 Clock Buffer	
ADP150	3.3 V Low noise Linear Regulator	
ADP7102	5 V Low noise Linear Regulator	

Extending the Low Frequency Range of a High Performance Phase Locked Loop

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0290 Circuit Evaluation Board (EVAL-CN0290-SDPZ)
System Demonstration Platform (EVAL-SDP-CS1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a high performance phase locked loop (PLL) that uses high speed clock buffers and low noise LDOs to maintain low phase noise even at low reference and RF frequencies.

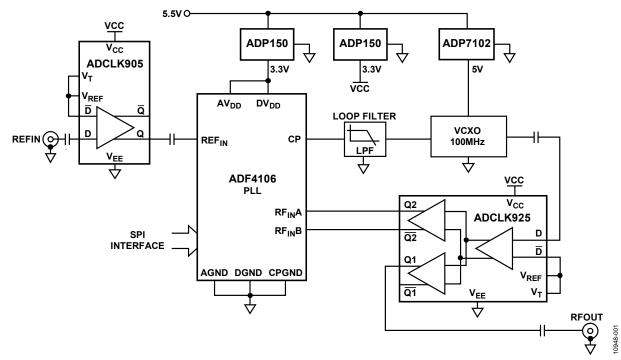


Figure 1. Block Diagram of the EVAL-CN0290-SDPZ. Simplified Schematic: All Connections and Decoupling not Shown

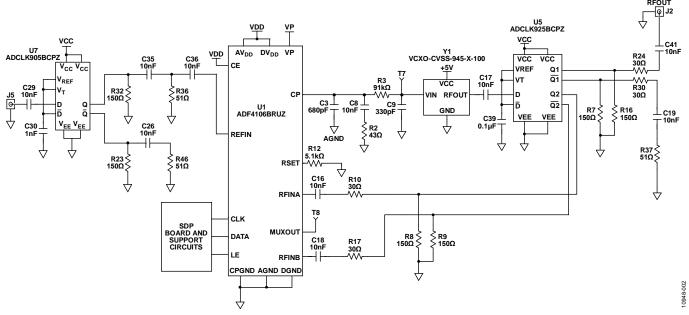
CN-0290 Circuit Note

For example, the minimum reference frequency and the RF input frequency of a number of Analog Devices PLLs, such as the ADF4106, are specified for 20 MHz and 500 MHz, respectively. The frequency range can be lowered to a 10 MHz reference frequency and a 100 MHz RF input using the additional clock buffers as in Figure 1.

CIRCUIT DESCRIPTION

The ADF4106 frequency synthesizer can be used to implement the local oscillator function in the up-conversion and downconversion sections of RF receivers, transmitters, signal analyzers, data generators, or any RF application that requires a local oscillator function. A complete phase-locked loop (PLL) is realized when the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO).

The ADF4106 is an integer-N PLL where the channel step size is an integer number N. This device has an RF frequency output range up to 6 GHz, is easy to use, and is specified for low phase noise, typically –223 dBc/Hz (normalized phase noise floor). Figure.1 shows the block diagram, and Figure 2 shows the simplified schematic of a complete phase locked loop using the ADF4106 in a low noise single frequency clock application.



 $Figure\ 2.\ Simplified\ Schematic\ of\ Low\ Phase\ Noise\ Phase\ Locked\ Loop\ with\ Clock\ Buffers\ for\ Reference\ Frequency\ and\ RF\ Frequency\ Inputs\ of\ ADF4106$

Circuit Note CN-0290

A low noise 10 MHz reference source is buffered by the ADCLK905 and ac coupled to the REF_{IN} of the ADF4106 PLL. The VCO is a low noise, 100 MHz sinewave VCXO, whose output is ac coupled to the 50 Ω input load of the ADCLK925. Interfacing between the VCXO and the ADCLK925 is very simple, as both devices are matched in terms of their load and signal level requirements. The ADCLK925 1:2 buffer output stage provides both and the RFOUT signal and the required RF feedback signal to the PLL.

The ADF4106 PLL is powered from a dedicated 3.3 V ADP150 low noise LDO, and the two clock buffers (ADCLK905, ADCLK925) are powered using a second ADP150. The ADP150 has an output voltage noise of only 9 μ V rms, which ensures low phase noise for both the PLL and the clock buffers.

The low noise VCXO is powered from the ADP7102 low noise 5 V linear regulator to reduce the impact of VCO pushing (equivalent to power supply rejection).

Reference Input Clock Buffer

The clock buffers for the REF $_{\rm IN}$ and the RF $_{\rm IN}$ input stages of the PLL need to have low additive jitter, sufficient slew rate at the frequency of operation, and adequate signal swing to match the ADF4106 requirements.

The ADCLK905/ADCLK925 are ultrafast ECL clock/data buffers, designed specifically to minimize added random jitter over a wide input slew rate. They feature full-swing ECL emitter coupled logic output drivers, 95 ps propagation delay and 60 fs random jitter. The rise/fall time (20% to 80%) of these parts is 60 ps typical which corresponds to a slew rate of approximately $8000\ V/\mu s$.

The ADCLK905 is used to buffer the 10 MHz REFIN frequency source. A reference frequency of 10 MHz is common in many applications. Depending on the signal swing available, the slew rate may not meet the minimum 50 V/ μ sec slew rate requirement of the ADF4106. For example, the slew rate of a 10 MHz 0 dBm sine wave is only 20 V/ μ s.

The ADCLK905 was chosen as the REF_{IN} clock buffer in order to increase the slew rate of the 10 MHz source. The ADCLK905 low additive jitter ensures that any additive jitter introduced by the REFIN clock buffer is minimal. Reference noise within the bandwidth of the PLL is not attenuated, therefore keeping the reference noise low, is a key factor in component choice. The low 60 fs additive jitter of the ADCLK905 ensures that this is the case. In a 50 Ω environment, input and output matching have a significant impact on performance. The input buffer of the ADCLK905 provides internal 50 Ω termination resistors for both D inputs. The center tap, V_T , between these 50 Ω resistors is connected externally to the complementary D input and to the V_{REF} pin. These pins are decoupled with a ceramic capacitor.

The PECL output stage of the ADCLK905 directly drives 800 mV each side into 50 Ω terminated to V_{CC} – 2 V. The termination is implemented with a single resistor termination to

each ADCLK905 output. For V_{CC} = 3.3 V, 150 Ω connected to ground is the recommended value.

The outputs are designed to drive transmission lines, and each output pin should see matched load impedances. The ADCLK905 Q output is ac coupled to a 50 Ω load, before ac coupling to the high impedance input of the ADF4106 REF_{IN}. The unused complementary Q output should be terminated with a similar load.

RF Input Clock Buffer

The ADCLK925 is used to buffer the 100 MHz RF $_{\rm IN}$ from the low noise VCXO. The RF $_{\rm IN}$ has a required minimum slew rate of 320 V/µsec. The ADCLK925 provides the required slew rate at the RF $_{\rm IN}$ input. The low additive jitter of the ADCLK925 has minimal impact on the PLL phase noise performance. The 1:2 output stage of the ADCLK925 simplifies feedback to the PLL without the need for a splitter and matching components.

The PECL output stages directly drives 800 mV each side into 50 Ω terminated to $V_{\rm CC}-2V$. This is achieved without the need for an additional supply by using a single 150 Ω resistor to ground, as shown in Figure 2. The RF $_{\rm IN}$ input stage of the ADF4106 is specified for a maximum signal level of \pm 600 mV. A series resistor of 30 Ω reduces the ADCLK925 output swing to below this value. The ADCLK925 output is ac coupled to the differential 50 Ω input of the ADF4106 The second ADCLK925 output is terminated in a similar manner and provides the RFOUT signal.

PLL Design and Performance

The ADIsimPLL™ software was used to design the loop filter of the PLL using the required low frequency values of 10 MHz REFIN and 100 MHz RFIN. The loop filter has 818 Hz bandwidth and 45° phase margin.

Figure 3 shows the ADIsimPLL simulated phase noise and indicates that the ADF4106 PLL loop locks at low frequency with a minimum increase in phase noise.

The actual measured phase noise of the PLL system is shown in Figure 4.

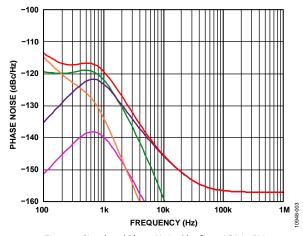


Figure 3. Simulated Phase Noise Plot from ADIsimPLL

CN-0290 Circuit Note

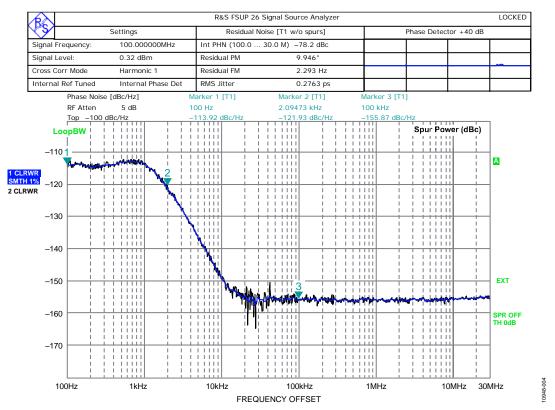


Figure 4. Measured Phase Noise Plot Using the Agilent FSSUP Spectrum Analyzer

The ADIsimPLL software used to generate the loop filter components can also be used to simulate the performance of the circuit. ADIsimPLL assumes an adequate signal slew rate and signal swing is provided by the REF $_{\rm IN}$ and RF $_{\rm IN}$ inputs. ADIsimPLL allows modeling the reference source used by the ADF4106 PLL, which for this setup is the R&S SMA100 signal generator.

The phase noise of the single-ended 10 MHz, 0 dBm reference input signal was modeled using the measured values at offsets of 10 Hz and 1 MHz. The Agilent FSUP spectrum analyzer was used to measure the reference phase noise at these offsets.

In order to simulate the VCO performance in ADIsimPLL, it is necessary to combine the phase noise from both the ADCLK925 datasheet and the CVSS-945 VCXO (Crystek Crystals, 12730 Commonwealth Drive, Fort Myers, Florida 33913) as shown in Table 1.

Table 1. Combined Phase Noise

Phase Noise Offset	ADCLK925 (dBc/Hz)	VCXO (dBc/Hz)	Total (dBc/Hz)
10 Hz	-140	-86	-86
1 MHz	-158	-172	–157

The combined 1/f phase noise is -86 dBc/Hz at 10 Hz offset. The -140 dBc value at 10 Hz offset from the ADCLK925 datasheet will have negligible effect on the combined 1/f phase noise.

The combined phase noise is $-157~\mathrm{dBc/Hz}$ at an offset of $1~\mathrm{MHz}$.

The ADCLK925 phase noise at 1 MHz offset in the data sheet is $-161 \, \mathrm{dBc/Hz}$. This is measured differentially, so it is necessary to adjust the datasheet measured noise floor by 3 dB when using a single-ended output. The VCXO phase noise of $-172 \, \mathrm{dBc/Hz}$ has an almost negligible contribution to the combined phase noise.

Comparison of Measured vs. Simulated Results

Table 2 shows simulated and measured results for phase noise and phase jitter. The phase noise is measured at offsets of 100 Hz, 2 kHz, and 100 kHz. Phase jitter is integrated from 100 Hz to 30 MHz. The ADIsimPLL program in this simulation uses a point floor model for the reference and VCO. As a result, the models in ADIsimPLL match very closely to the 1/f noise and the noise floor, but they can differ by several dB at intermediate offsets from the carrier.

Table 2. ADF4106 PLL System Simulated and Measured Phase Noise and Phase Jitter

Parameter	Simulated	Measured
PN Offset of 100 Hz dBc/Hz	-113 dBc/Hz	−114 dBc/Hz
PN Offset of 2 kHz dBc/Hz	–126 dBc/Hz	−122 dBc/Hz
PN Offset of 100 kHz dBc/Hz	–156 dBc/Hz	−156 dBc/Hz
Phase Jitter (100 Hz to 30 MHz)	208 fs	276 fs

Circuit Note CN-0290

COMMON VARIATIONS

A single supply PECL/LVPECL comparator, such as the ADCMP553, can be used for applications that require the REFIN to operate with signals having less than 10 V/µsec slew rates. The ADCMP553 uses an output stage similar to the ADCLK905/ADCLK925 to drive the REFIN/RFIN inputs, but the input of the comparator must be driven from a source impedance of 50 Ω with a common mode voltage that allows the required signal swing.

Other buffers such as the ADCMP600 high speed CMOS comparator can be used to increase the slew rate for the REFIN circuit, however the additive jitter should be evaluated for the application in question.

All additional components will introduce some amount of additive noise, which can degrade the in-band phase noise and phase noise jitter. This may be acceptable for some applications, where the degradation in phase noise performance is still within the acceptable limits.

The ADCLK9xx, family of clock buffers have very low additive jitter, however low slew rate signal inputs will degrade this specification. The ADCLK9xx data sheets should be consulted to evaluate this degradation.

A photo of the EVAL-CN0290-SDPZ circuit board is shown in Figure 5.



Figure 5. Photo of EVAL-CN0290-SDPZ Board Connected to the EVAL-SDP-CS1Z Board

CN-0290 Circuit Note

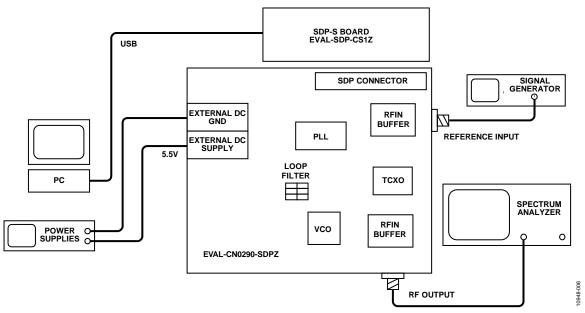


Figure 6. Measurement Setup for Phase Noise and Phase Jitter Testing

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0290-SDPZ circuit board and the EVAL-SDP-CS1Z System Demonstration Platform (SDP-S) evaluation board. The two boards have a 120-pin mating connectors, allowing for the quick setup and evaluation of the circuit performance. The EVAL-CN0290-SDPZ board contains the circuit described in this note. The SDP-S evaluation board is used with the Integer N evaluation software to program the ADF4106 on chip registers.

Equipment needed

- PC with a USB port and Windows* XP, Windows Vista* (32-bit), or Windows* 7 (32-bit)
- EVAL-CN0290-SDPZ circuit evaluation board
- EVAL-SDP-CS1Z SDP evaluation board
- Integer-N v7 or greater evaluation software
- Power supply: +5.5 V.
- RF signal source (R&S SMA100 or equivalent)
- Spectrum Analyzer (Agilent FSUP or equivalent)
- Coaxial RF cables with SMA connectors

Circuit Note CN-0290

Gettina Started

Refer to the UG-582 User Guide for software installation and test setup. The design support package includes the schematics, layout files, and the bill of materials (www.analog.com/CN0290-DesignSupport). For additional details, refer to the ADF4106, ADCLK905, and the ADCLK925 data sheets.

Functional Block Diagram

Refer to Figure 1 of this circuit note for the block diagram and Figure 2 for simplified schematic. A block diagram of the test setup is shown in Figure 6.

Setup and Test

After setting up the equipment, use standard RF test methods to measure the phase noise and phase jitter of the circuit.

LEARN MORE

CN0290 Design Support Package: http://www.analog.com/CN0290-DesignSupport

UG-582, User Guide, Evaluating the EVAL-CN0290-SDPZ

MT-031 Tutorial, Grounding Data Converters and Solving the Mystery of "AGND" and "DGND", Analog Devices.

MT-086 Tutorial, Fundamentals of Phase Locked Loops (PLLs), Analog Devices.

MT-101 Tutorial, Decoupling Techniques, Analog Devices.

ADIsimPLL Design Tool

AN-30 Application Note, Ask the Application Engineer—PLL Synthesizers, Analog Devices

AN-586 Application Note, LVDS Data Outputs for High-Speed Analog-to-Digital Converters.

Data Sheets and Evaluation Boards

EVAL-CN0290-SDPZ Evaluation Board

EVAL-SDP-CS1Z System Development Platform

ADF4106 Data Sheet

ADCLK905 Data Sheet

ADCLK925 Data Sheet

ADP150 Data Sheet

ADP7102 Data Sheet

CVSS-945 VCXO, Crystek Crystals, 12730 Commonwealth Drive, Fort Myers, Florida 33913.

REVISION HISTORY

8/13—Revision 0: Initial Version

(Continued from first page) Circuits from the Lab circuits are intended only for use with Analog Devices products and are the intellectual property of Analog Devices or its licensors. While you may use the Circuits from the Lab circuits in the design of your product, no other license is granted by implication or otherwise under any patents or other intellectual property by application or use of the Circuits from the Lab circuits. Information furnished by Analog Devices is believed to be accurate and reliable. However, Circuits from the Lab circuits are supplied "as is" and without warranties of any kind, express, implied, or statutory including, but not limited to, any implied warranty of merchantability, noninfringement or fitness for a particular purpose and no responsibility is assumed by Analog Devices for their use, nor for any infringements of patents or other rights of third parties that may result from their use. Analog Devices reserves the right to change any Circuits from the Lab circuits at any time without notice but is under no obligation to do so.





Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию.

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России, а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научноисследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,

Промышленная ул, дом № 19, литера Н,

помещение 100-Н Офис 331