



High-Speed, Low-Voltage, 0.7Ω CMOS Analog Switches/Multiplexers

MAX4781/MAX4782/MAX4783

General Description

The MAX4781/MAX4782/MAX4783 are high-speed, low-voltage, low on-resistance, CMOS analog multiplexers/switches configured as an 8-channel multiplexer (MAX4781), two 4-channel multiplexers (MAX4782), and three single-pole/double-throw (SPDT) switches (MAX4783).

These devices operate with a +1.6V to +3.6V single supply. When powered from a +3V supply, MAX4781/MAX4782/MAX4783 feature a 0.7Ω on-resistance (R_{ON}), with 0.3Ω R_{ON} matching between channels, and 0.1Ω R_{ON} flatness. These devices handle rail-to-rail analog signals while consuming less than 3μW of quiescent power. They are available in space-saving 16-pin thin QFN (3mm x 3mm) and TSSOP packages.

Applications

- Battery-Operated Equipment
- Audio Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communications Circuits

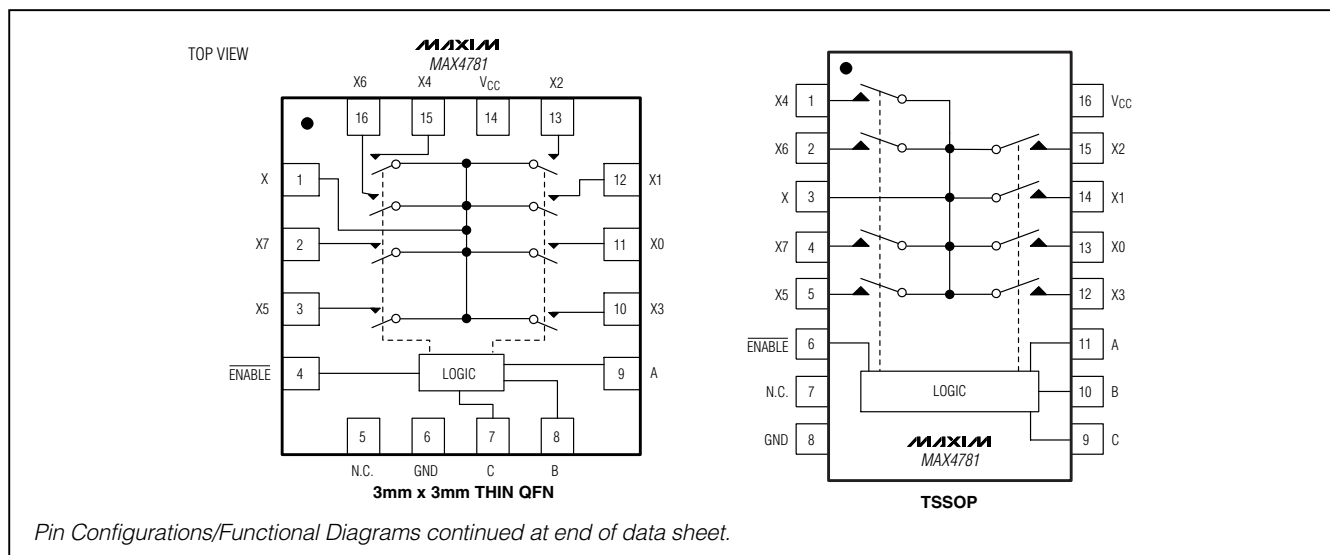
Features

- ◆ On-Resistance
0.7Ω (+3V Supply)
1.6Ω (+1.8V Supply)
- ◆ On-Resistance Match Between Channels
0.3Ω (+3V Supply)
- ◆ On-Resistance Flatness
0.1Ω (+3V Supply)
- ◆ Single-Supply Operation Down to 1.6V
- ◆ High-Current Handling Capacity (150mA Continuous)
- ◆ +1.8V CMOS-Logic Compatible
- ◆ Fast Switching Times: $t_{ON} = 11ns$, $t_{OFF} = 4ns$
- ◆ Pin Compatible with Industry-Standard 74HC4051/74HC4052/74HC4053 and MAX4617/MAX4618/MAX4619
- ◆ Available in 3mm x 3mm 16-Pin Thin QFN Packages

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|------------|----------------|-------------------------|
| MAX4781EUE | -40°C to +85°C | 16 TSSOP |
| MAX4781ETE | -40°C to +85°C | 16 Thin QFN (3mm x 3mm) |
| MAX4782EUE | -40°C to +85°C | 16 TSSOP |
| MAX4782ETE | -40°C to +85°C | 16 Thin QFN (3mm x 3mm) |
| MAX4783EUE | -40°C to +85°C | 16 TSSOP |
| MAX4783ETE | -40°C to +85°C | 16 Thin QFN (3mm x 3mm) |

Pin Configurations/Functional Diagrams



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ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND

V_{CC} , A, B, C, and \overline{ENABLE} -0.3V to +4.6V

Voltage at Any Other Terminal
(Note 1).....-0.3V to (V_{CC} + 0.3V)

Continuous Current into A, B, C, \overline{ENABLE} ± 10 mA

Continuous Current into X, Y, Z, X_{-} , Y_{-} , Z_{-} ± 150 mA

Peak Current into X, Y, Z, X_{-} , Y_{-} , Z_{-}
(pulsed at 1ms, 10% duty cycle)..... ± 300 mA

Continuous Power Dissipation

16-Pin Thin QFN (derate 16.9mW/°C above +70°C) ...1349mW

16-Pin TSSOP (derate 5.7mW/°C above +70°C) 457mW

Operating Temperature Range-40°C to +85°C

Junction Temperature.....+150°C

Storage Temperature Range-65°C to +150°C

Lead Temperature (soldering, 10s).....+300°C

Note 1: Signals on X, Y, Z, X_{-} , Y_{-} , and Z_{-} exceeding V_{CC} or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V_{CC} = +2.7V to +3.6V, GND = 0, V_{IH} = 1.4V, V_{IL} = 0.5V, T_A = T_{MIN} to T_{MAX} , unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | T_A | MIN | TYP | MAX | UNITS |
|--|--|---|------------------------|-----|-------|----------|----------|
| ANALOG SWITCH | | | | | | | |
| Analog Signal Range | $V_X, V_Y, V_Z,$ V_{X-}, V_{Y-}, V_{Z-} | | | 0 | | V_{CC} | V |
| On-Resistance (Note 4) | R_{ON} | V_{CC} = +2.7V; I_{X-}, I_{Y-}, I_{Z-} = 100mA; V_X, V_Y, V_Z = 1.7V | +25°C | | 0.7 | 1 | Ω |
| | | | T_{MIN} to T_{MAX} | | | 1.2 | |
| On-Resistance Match Between Channels (Notes 4, 5) | ΔR_{ON} | V_{CC} = +2.7V; I_{X-}, I_{Y-}, I_{Z-} = 100mA; V_X, V_Y, V_Z = 1.7V | +25°C | | 0.3 | 0.4 | Ω |
| | | | T_{MIN} to T_{MAX} | | | 0.6 | |
| On-Resistance Flatness (Note 6) | $R_{FLAT(ON)}$ | V_{CC} = +2.7V; I_{X-}, I_{Y-}, I_{Z-} = 100mA; V_X, V_Y, V_Z = 0, 0.7V, 1.7V | +25°C | | 0.1 | 0.2 | Ω |
| | | | T_{MIN} to T_{MAX} | | | 0.2 | |
| X_{-}, Y_{-}, Z_{-} Off-Leakage Current | $I_{X(OFF)}$ $I_{Y(OFF)}$ $I_{Z(OFF)}$ | V_{CC} = +3.6V; V_{X-}, V_{Y-}, V_{Z-} = 3.3V, 0.3V; V_X, V_Y, V_Z = 0.3V, 3.3V | +25°C | -2 | 0.002 | +2 | nA |
| | | | T_{MIN} to T_{MAX} | -7 | | +7 | |
| X Off-Leakage Current (MAX4781 Only) | $I_{X(OFF)}$ | V_{CC} = +3.6V; V_{X-} = 3.3V, 0.3V; V_{X-} = 0.3V, 3.3V | +25°C | -2 | 0.002 | +2 | nA |
| | | | T_{MIN} to T_{MAX} | -50 | | +50 | |
| X On-Leakage Current (MAX4781 Only) | $I_{X(ON)}$ | V_{CC} = +3.6V V_{X-} = 0.3V, 3.3V; V_{X-} = 0.3V, 3.3V or floating | +25°C | -2 | 0.002 | +2 | nA |
| | | | T_{MIN} to T_{MAX} | -50 | | +50 | |
| X, Y, Z Off-Leakage Current (MAX4782/MAX4783 Only) | $I_{X(OFF)}$ $I_{Y(OFF)}$ $I_{Z(OFF)}$ | V_{CC} = +3.6V; V_{X-}, V_{Y-}, V_{Z-} = 3.3V, 0.3V; V_X, V_Y, V_Z = 0.3V, 3.3V | +25°C | -2 | 0.002 | +2 | nA |
| | | | T_{MIN} to T_{MAX} | -25 | | +25 | |
| X, Y, Z On-Leakage Current (MAX4782/MAX4783 Only) | $I_{X(ON)}$ $I_{Y(ON)}$ $I_{Z(ON)}$ | V_{CC} = +3.6V; V_X, V_Y, V_Z = 0.3V, 3.3V; V_X, V_Y, V_Z = 0.3V, 3.3V or floating | +25°C | -2 | 0.002 | +2 | nA |
| | | | T_{MIN} to T_{MAX} | -25 | | +25 | |

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ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V_{CC} = +2.7V to +3.6V, GND = 0, V_{IH} = 1.4V, V_{IL} = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | T _A | MIN | TYP | MAX | UNITS |
|---------------------------------------|---|--|--------------------------------------|---------|--------|-----|-------|
| SWITCH DYNAMIC CHARACTERISTICS | | | | | | | |
| Turn-On Time | t _{ON} | V _X , V _Y , V _Z = 1.5V; R _L = 50Ω; C _L = 35pF; Figure 1 | +25°C | 11 | 25 | ns | |
| | | | T _{MIN} to T _{MAX} | 27 | | | |
| Turn-Off Time | t _{OFF} | V _X , V _Y , V _Z = 1.5V; R _L = 50Ω; C _L = 35pF; Figure 1 | +25°C | 4 | 15 | ns | |
| | | | T _{MIN} to T _{MAX} | 20 | | | |
| Address Transition Time | t _{TRANS} | V _X , V _Y , V _Z = 1.5V; R _L = 50Ω; C _L = 35pF; Figure 2 | +25°C | 11 | 25 | ns | |
| | | | T _{MIN} to T _{MAX} | 27 | | | |
| Break-Before-Make Time (Note 7) | t _{BBM} | V _X , V _Y , V _Z = 1.5V; R _L = 50Ω; C _L = 35pF; Figure 3 | +25°C | 18 | | ns | |
| | | | T _{MIN} to T _{MAX} | 2 | | | |
| Charge Injection | Q | V _{GEN} = 0, R _{GEN} = 0, C _L = 1nF, Figure 4 | +25°C | -110 | | pC | |
| Input Off-Capacitance | C _{X(OFF)} , C _{Y(OFF)} , C _{Z(OFF)} | f = 1MHz, Figure 6 | +25°C | 38 | | pF | |
| Output Off-Capacitance | C _{X(OFF)} , C _{Y(OFF)} , C _{Z(OFF)} | f = 1MHz, Figure 6 | +25°C | MAX4781 | 310 | | pF |
| | | | | MAX4782 | 158 | | |
| | | | | MAX4783 | 75 | | |
| Output On-Capacitance | C _{X(ON)} , C _{Y(ON)} , C _{Z(ON)} | f = 1MHz, Figure 6 | +25°C | MAX4781 | 380 | | pF |
| | | | | MAX4782 | 224 | | |
| | | | | MAX4783 | 140 | | |
| Off-Isolation (Note 8) | V _{ISO} | R _L = 50Ω, C _L = 35pF, Figure 5 | f = 10MHz | -75 | | dB | |
| | | | f = 1MHz | -90 | | | |
| Channel-to-Channel Crosstalk (Note 9) | V _{CT} | R _L = 50Ω, C _L = 35pF, Figure 5 | f = 10MHz | -65 | | dB | |
| | | | f = 1MHz | -80 | | | |
| Total Harmonic Distortion | THD | f = 20Hz to 20kHz, 0.5V _{p-p} , R _L = 32Ω | | 0.045 | | % | |
| DIGITAL I/O | | | | | | | |
| Input Logic High | V _{IH} | | T _{MIN} to T _{MAX} | 1.4 | | V | |
| Input Logic Low | V _{IL} | | T _{MIN} to T _{MAX} | 0.5 | | V | |
| Input Leakage Current | I _{INL} | V _A , V _B , V _C = V _{ENABLE} = 0 or 3.6V | T _{MIN} to T _{MAX} | -1 | 0.0005 | +1 | μA |
| POWER SUPPLY | | | | | | | |
| Power-Supply Range | V _{CC} | | | +1.6 | +3.6 | | V |
| Positive Supply Current | I _{CC} | V _{CC} = 3.6V; V _A , V _B , V _C ; V _{ENABLE} = 3.6V or 0 | | 1 | | μA | |

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ELECTRICAL CHARACTERISTICS—Single +1.8V Supply

($V_{CC} = +1.8V$, $GND = 0$, $V_{IH} = 1V$, $V_{IL} = 0.4V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Notes 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | T_A | MIN | TYP | MAX | UNITS |
|---|---|--|------------------------|-----|-------|----------|----------|
| ANALOG SWITCH | | | | | | | |
| Analog Signal Range | $V_{X-}, V_{Y-}, V_{Z-}, V_X, V_Y, V_Z$ | | | 0 | | V_{CC} | V |
| On-Resistance (Note 4) | R_{ON} | $V_{CC} = 1.8V; I_{X-}, I_{Y-}, I_{Z-} = 10mA; V_X, V_Y, V_Z = 1.0V$ | $+25^\circ C$ | | 1.6 | 2.5 | Ω |
| | | | T_{MIN} to T_{MAX} | | | 3.5 | |
| On-Resistance Match Between Channels (Notes 4, 5) | ΔR_{ON} | $V_{CC} = 1.8V; I_{X-}, I_{Y-}, I_{Z-} = 10mA; V_X, V_Y, V_Z = 1.0V$ | $+25^\circ C$ | | 0.3 | 0.4 | Ω |
| | | | T_{MIN} to T_{MAX} | | | 0.6 | |
| SWITCH DYNAMIC CHARACTERISTICS | | | | | | | |
| Turn-On Time | t_{ON} | $V_{X-}, V_{Y-}, V_{Z-} = 1.0V; R_L = 50\Omega; C_L = 35pF$; Figure 1 | $+25^\circ C$ | | 17 | 30 | ns |
| | | | T_{MIN} to T_{MAX} | | | 32 | |
| Turn-Off Time | t_{OFF} | $V_{X-}, V_{Y-}, V_{Z-} = 1.0V; R_L = 50\Omega; C_L = 35pF$; Figure 1 | $+25^\circ C$ | | 8 | 20 | ns |
| | | | T_{MIN} to T_{MAX} | | | 22 | |
| Address Transition Time | t_{TRANS} | $V_{X-}, V_{Y-}, V_{Z-} = 1.0V; R_L = 50\Omega; C_L = 35pF$; Figure 2 | $+25^\circ C$ | | 17 | 30 | ns |
| | | | T_{MIN} to T_{MAX} | | | 32 | |
| Break-Before-Make Time (Note 7) | t_{BBM} | $V_{X-}, V_{Y-}, V_{Z-} = 1V; R_L = 50\Omega; C_L = 35pF$; Figure 3 | $+25^\circ C$ | | 26 | | ns |
| | | | T_{MIN} to T_{MAX} | | 1 | | |
| Charge Injection | Q | $V_{GEN} = 0, R_{GEN} = 0, C_L = 1nF$; Figure 4 | $+25^\circ C$ | | -40 | | pC |
| DIGITAL I/O | | | | | | | |
| Input Logic High | V_{IH} | | T_{MIN} to T_{MAX} | 1 | | | V |
| Input Logic Low | V_{IL} | | T_{MIN} to T_{MAX} | | | 0.4 | V |
| Input Leakage Current | I_{IN-} | $V_A, V_B, V_C = V_{ENABLE} = 0$ or $3.6V$ | T_{MIN} to T_{MAX} | -1 | 0.000 | +1 | μA |
| POWER SUPPLY | | | | | | | |
| Power-Supply Range | V_{CC} | | | 1.6 | | 3.6 | V |
| Positive Supply Current | I_{CC} | $V_{CC} = 3.6V; V_A, V_B, V_C, V_{ENABLE} = 0$ or $3.6V$ | | | | 1 | μA |

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: Devices are tested at maximum hot temperature and are guaranteed by design and correlation at $T_A = +25^\circ C$ and $-40^\circ C$ specifications.

Note 4: R_{ON} and ΔR_{ON} matching specifications for thin QFN-packaged parts are guaranteed by design.

Note 5: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 7: Guaranteed by design; not production tested.

Note 8: Off-isolation = $20\log_{10}(V_{COM-} / V_{NO})$, V_{COM-} = output, V_{NO} = input to off switch.

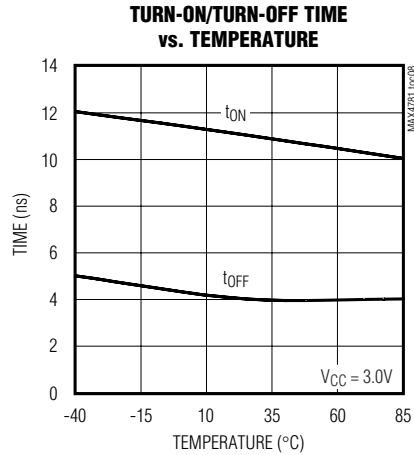
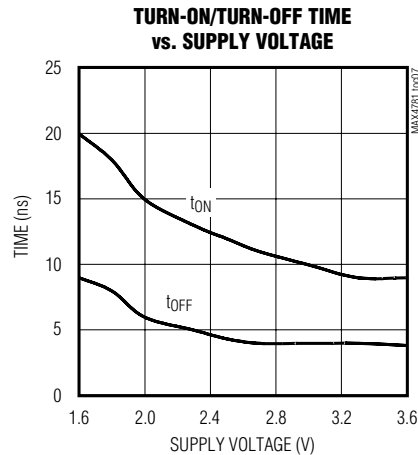
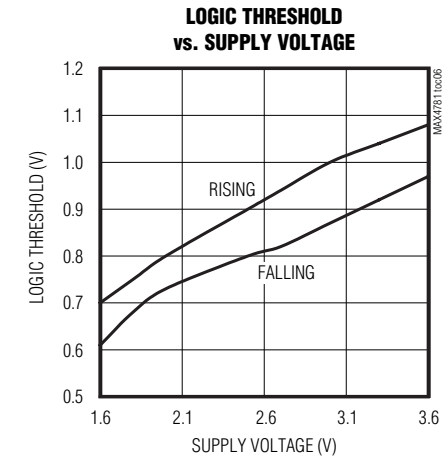
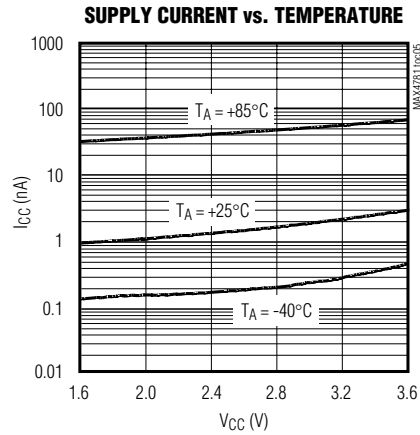
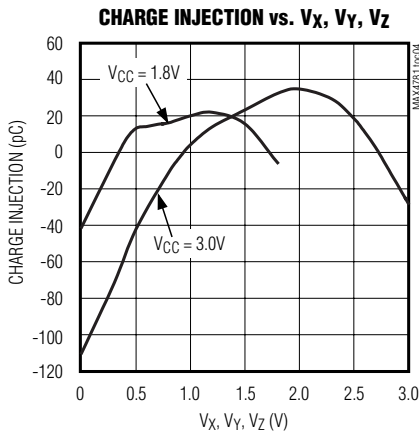
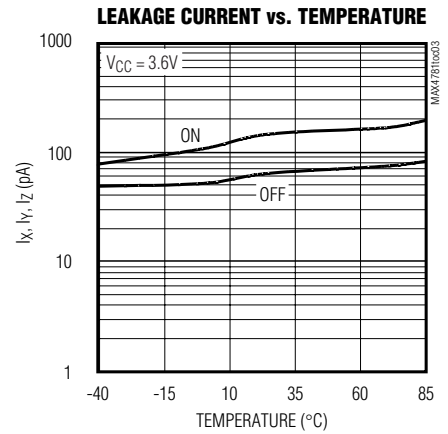
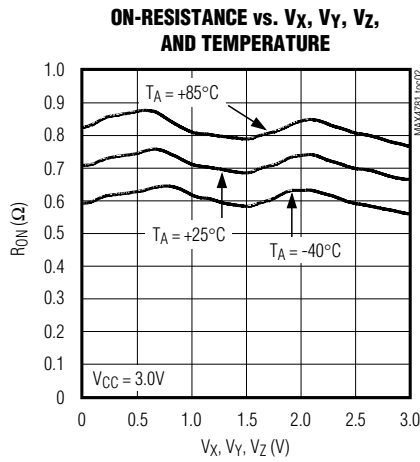
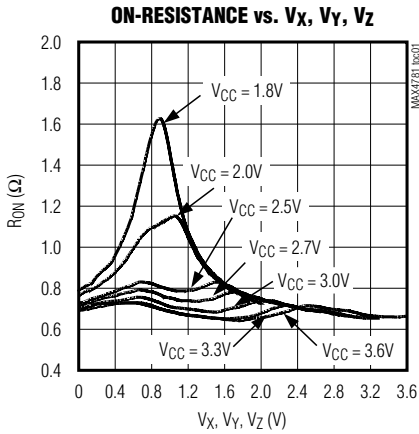
Note 9: Between any two channels.

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Typical Operating Characteristics

(GND = 0, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

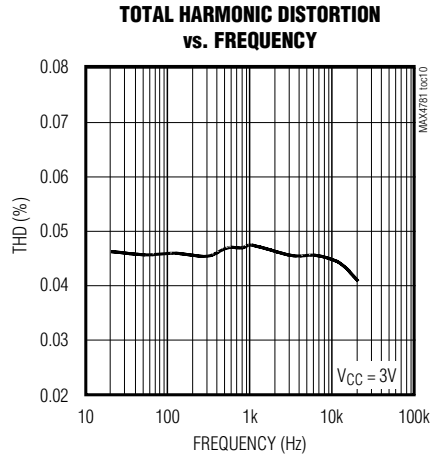
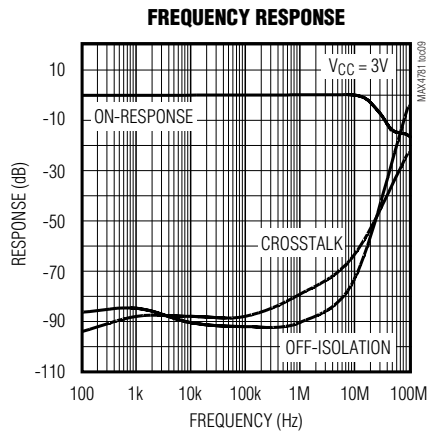
MAX4781/MAX4782/MAX4783



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Typical Operating Characteristics (continued)

(GND = 0, T_A = +25°C, unless otherwise noted.)



MAX4781 Pin Description

| PIN | | NAME | FUNCTION |
|----------------------------------|------------------------------------|----------------------------|---|
| TSSOP | THIN QFN | | |
| 3 | 1 | X | Analog Switch Output |
| 6 | 4 | $\overline{\text{ENABLE}}$ | Digital Enable Input. Normally connect to GND. Drive to logic high to set all switches off. |
| 7 | 5 | N.C. | No Connection. Not internally connected. |
| 8 | 6 | GND | Ground |
| 9 | 7 | C | Digital Address C Input |
| 10 | 8 | B | Digital Address B Input |
| 11 | 9 | A | Digital Address A Input |
| 13, 14, 15, 12, 1, 5, 2, 4 | 11, 12, 13, 10, 15, 3, 16, 2 | X0–X7 | Analog Switch Inputs X0–X7 |
| 16 | 14 | V _{CC} | Positive Analog and Digital Supply Voltage Input |
| — | EP | PAD | Exposed Pad. Connect to GND. |

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MAX4782 Pin Description

| PIN | | NAME | FUNCTION |
|----------------|---------------|----------------------------|---|
| TSSOP | THIN QFN | | |
| 1, 5, 2, 4 | 15, 3, 16, 2 | Y0–Y3 | Analog Switch Y Inputs Y0–Y3 |
| 3 | 1 | Y | Analog Switch Y Output |
| 6 | 4 | $\overline{\text{ENABLE}}$ | Digital Enable Input. Normally connect to GND. Drive to logic high to set all switches off. |
| 7 | 5 | N.C. | No Connection. Not internally connected. |
| 8 | 6 | GND | Ground |
| 9 | 7 | B | Digital Address B Input |
| 10 | 8 | A | Digital Address A Input |
| 12, 14, 15, 11 | 10, 12, 13, 9 | X0–X3 | Analog Switch X Inputs X0–X3 |
| 13 | 11 | X | Analog Switch X Output |
| 16 | 14 | VCC | Positive Analog and Digital Supply Voltage Input |

MAX4783 Pin Description

| PIN | | NAME | FUNCTION |
|-------|----------|----------------------------|---|
| TSSOP | THIN QFN | | |
| 1 | 15 | Y1 | Analog Switch Y Normally Open Input |
| 2 | 16 | Y0 | Analog Switch Y Normally Closed Input |
| 3 | 1 | Z1 | Analog Switch Z Normally Open Input |
| 4 | 2 | Z | Analog Switch Z Output |
| 5 | 3 | Z0 | Analog Switch Z Normally Closed Input |
| 6 | 4 | $\overline{\text{ENABLE}}$ | Digital Enable Input. Normally connect to GND. Drive to logic high to set all switches off. |
| 7 | 5 | N.C. | No Connection. Not internally connected. |
| 8 | 6 | GND | Ground |
| 9 | 7 | C | Digital Address C Input |
| 10 | 8 | B | Digital Address B Input |
| 11 | 9 | A | Digital Address A Input |
| 12 | 10 | X0 | Analog Switch X Normally Closed Input |
| 13 | 11 | X1 | Analog Switch X Normally Open Input |
| 14 | 12 | X | Analog Switch X Output |
| 15 | 13 | Y | Analog Switch Y Output |
| 16 | 14 | VCC | Positive Analog and Digital Supply Voltage Input |

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Applications Information

Power-Supply Considerations

Overview

The MAX4781/MAX4782/MAX4783 construction is typical of most CMOS analog switches. There are two supply inputs: V_{CC} and GND. V_{CC} and GND drive the internal CMOS switches and set the limits of the analog voltage on any switch. Internal reverse ESD-protection diodes are connected between each analog signal input and both V_{CC} and GND. If any analog signal exceeds V_{CC} or GND, one of these diodes conducts. During normal operation, these and other reverse-biased ESD diodes leak, forming the only current drawn from V_{CC} or GND.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal input are identical and therefore fairly well balanced, they are reverse-biased differently. Each diode is biased by either V_{CC} or GND and the analog signal. Their leakages vary as the signal varies. The difference in the two diodes' leakages to V_{CC} and GND constitutes the analog-signal-path leakage current. All analog leakage current flows between each input and one of the supply terminals, not to the other switch terminal. Both sides of a given switch can show leakage currents of either the same or opposite polarity.

V_{CC} and GND power the internal logic and set the input logic limits. Logic inputs have ESD-protection diodes to ground.

Power Supply

The MAX4781/MAX4782/MAX4783 operate from a single supply between +1.6V and +3.6V. Switch on-resistance increases as the supply voltage is lowered.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see the *Typical Operating Characteristics*). Above 20MHz, the on-response has several minor peaks that are highly layout dependent. In the off state, the switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off-isolation is approximately -50dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedance also degrades off-isolation. Adjacent channel attenuation is approximately 3dB above that of a bare IC socket and is entirely because of capacitive coupling.

Pin Nomenclature

The MAX4781/MAX4782/MAX4783 are pin compatible with the industry-standard 74HC4051/74HC4052/74HC4053 and the MAX4617/MAX4618/MAX4619. In single-supply applications, they function identically and have identical logic diagrams, although these parts differ electrically. The pin designations and logic diagrams in this data sheet conform to the original 1972 specifications published by RCA for the CD4051/CD4052/CD4053. These designations differ from the standard Maxim switch and mux designations found on other Maxim data sheets such as the MAX4051/MAX4052/MAX4053. Designers who are more comfortable with Maxim's standard designations are advised that the pin designations and logic diagrams on the MAX4051/MAX4052/MAX4053 data sheet can be applied to the MAX4781/MAX4782/MAX4783.

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Table 1. Truth Table/Switch Programming

| ENABLE INPUT | SELECT INPUT | | | ON SWITCHES | | |
|--------------|--------------|---|---|-------------------|----------------------|----------------------|
| | C* | B | A | MAX4781 | MAX4782 | MAX4783 |
| H | ✓ | ✓ | ✓ | All switches open | All switches open | All switches open |
| L | L | L | L | X-X0 | X-X0 Y-Y0 Z-Z0 | X-X0 Y-Y0 Z-Z0 |
| L | L | L | H | X-X1 | X-X1 Y-Y1 | X-X1 Y-Y0 Z-Z0 |
| L | L | H | L | X-X2 | X-X2 Y-Y2 | X-X0 Y-Y1 Z-Z0 |
| L | L | H | H | X-X3 | X-X3 Y-Y3 | X-X1 Y-Y1 Z-Z0 |
| L | H | L | L | X-X4 | X-X0 Y-Y0 | X-X0 Y-Y0 Z-Z1 |
| L | H | L | H | X-X5 | X-X1 Y-Y1 | X-X1 Y-Y0 Z-Z1 |
| L | H | H | L | X-X6 | X-X2 Y-Y2 | X-X0 Y-Y1 Z-Z1 |
| L | H | H | H | X-X7 | X-X3 Y-Y3 | X-X1 Y-Y1 Z-Z1 |

✓ = Don't care.

*Not present on MAX4782.

Note: Input and output pins are identical and interchangeable. Either can be considered an input or output. Signals pass equally well in either direction.

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Test Circuits/Timing Diagrams

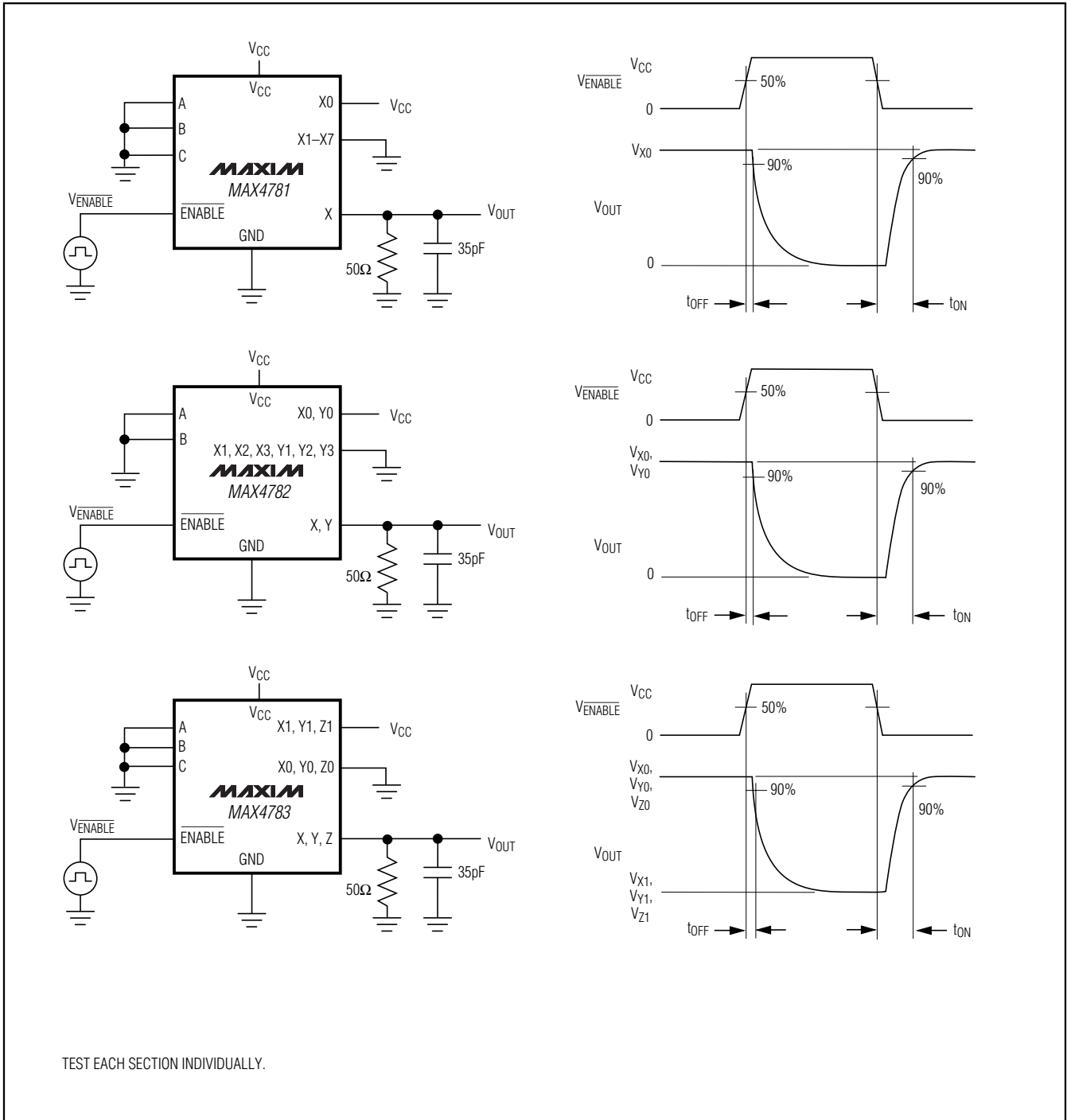


Figure 1. Enable Switching Times

High-Speed, Low-Voltage, 0.7Ω CMOS Analog Switches/Multiplexers

Test Circuits/Timing Diagrams (continued)

MAX4781/MAX4782/MAX4783

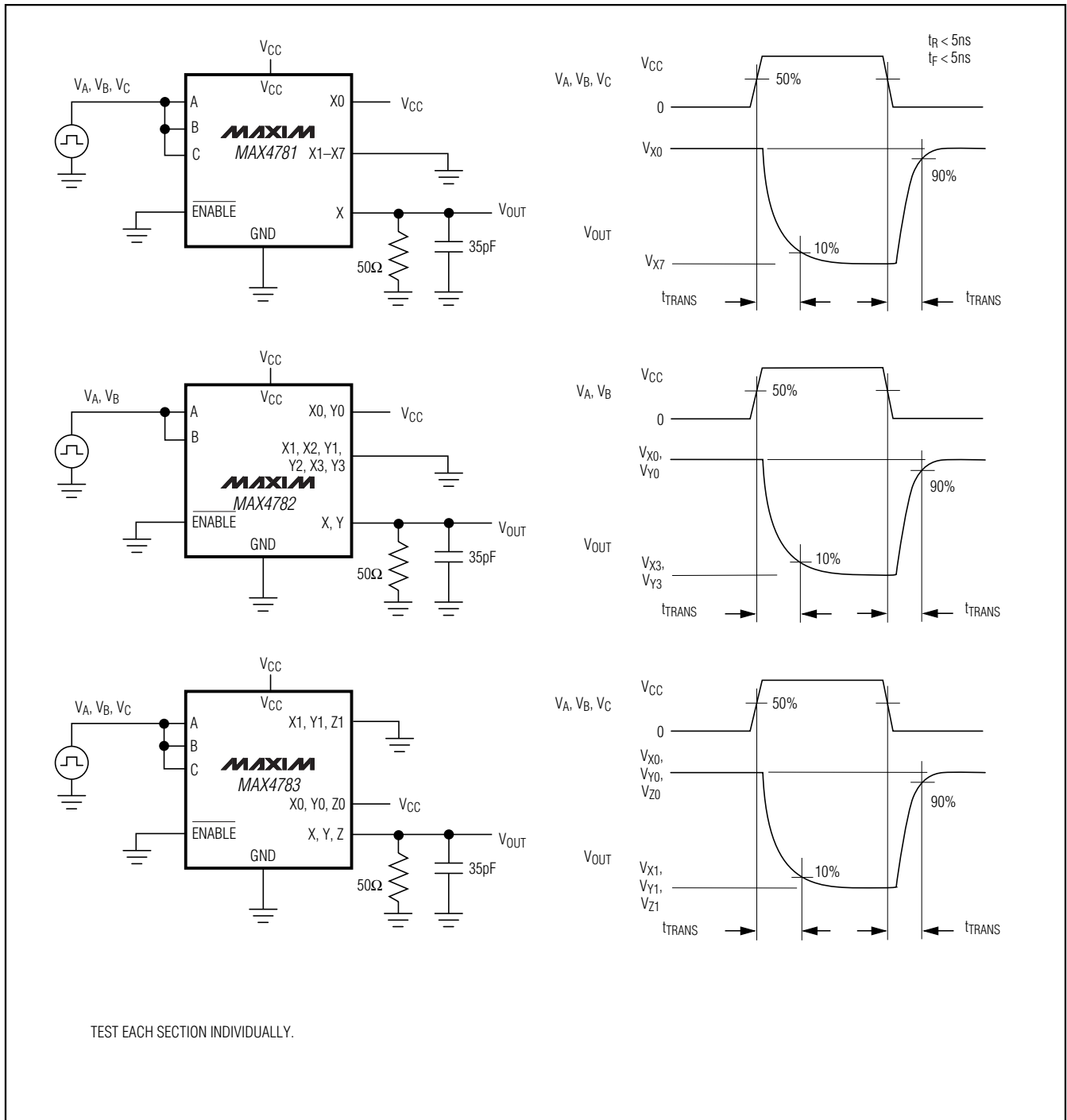


Figure 2. Address Transition Times

High-Speed, Low-Voltage, 0.7Ω CMOS Analog Switches/Multiplexers

Test Circuits/Timing Diagrams (continued)

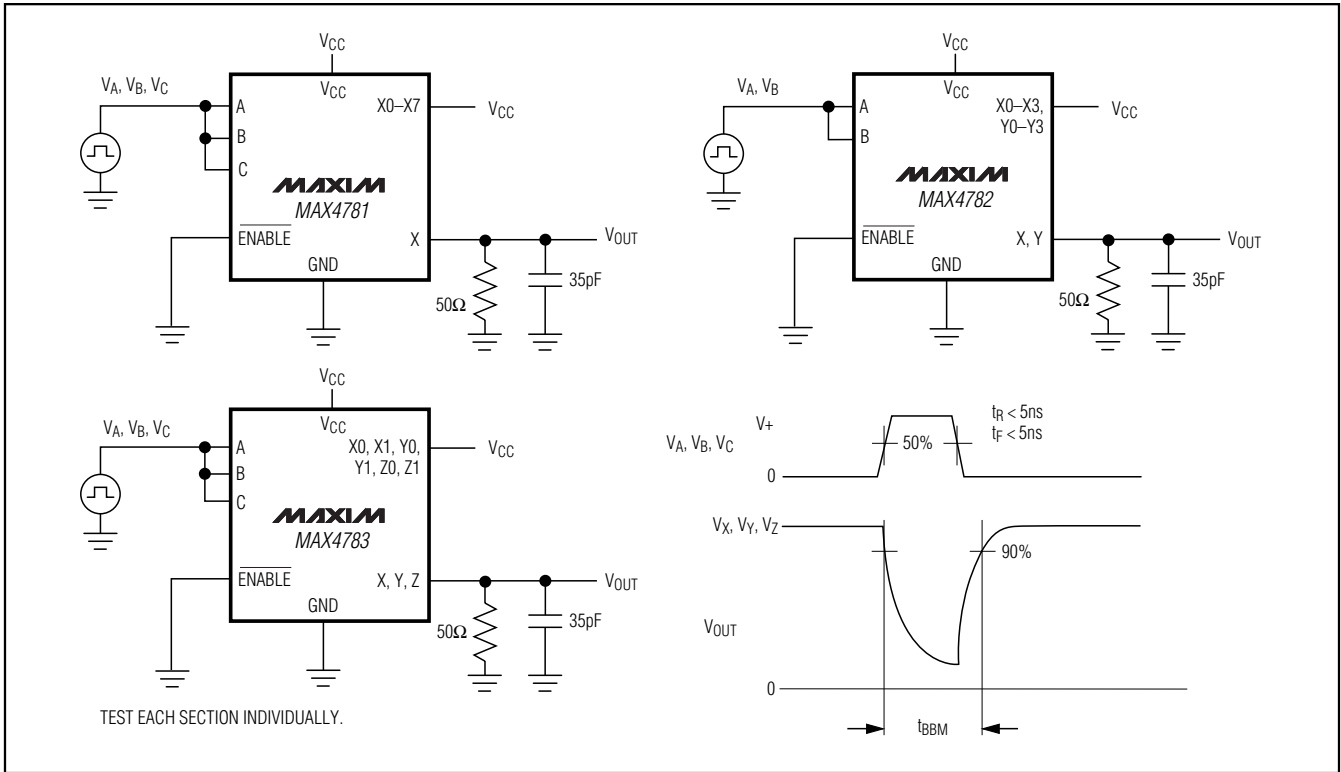


Figure 3. Break-Before-Make Interval

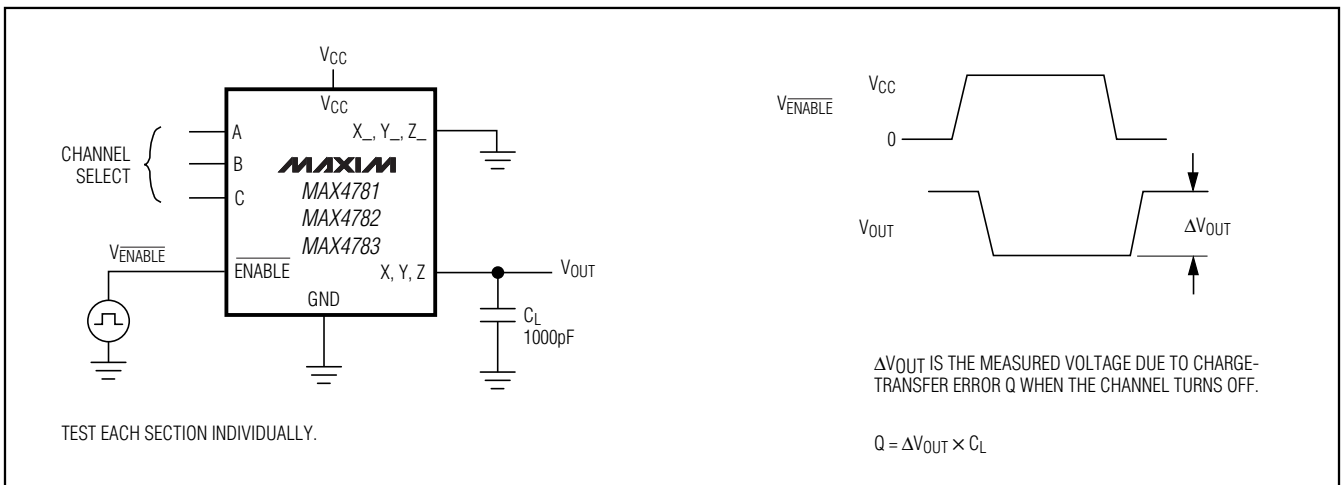


Figure 4. Charge Injection

High-Speed, Low-Voltage, 0.7Ω CMOS Analog Switches/Multiplexers

Test Circuits/Timing Diagrams (continued)

MAX4781/MAX4782/MAX4783

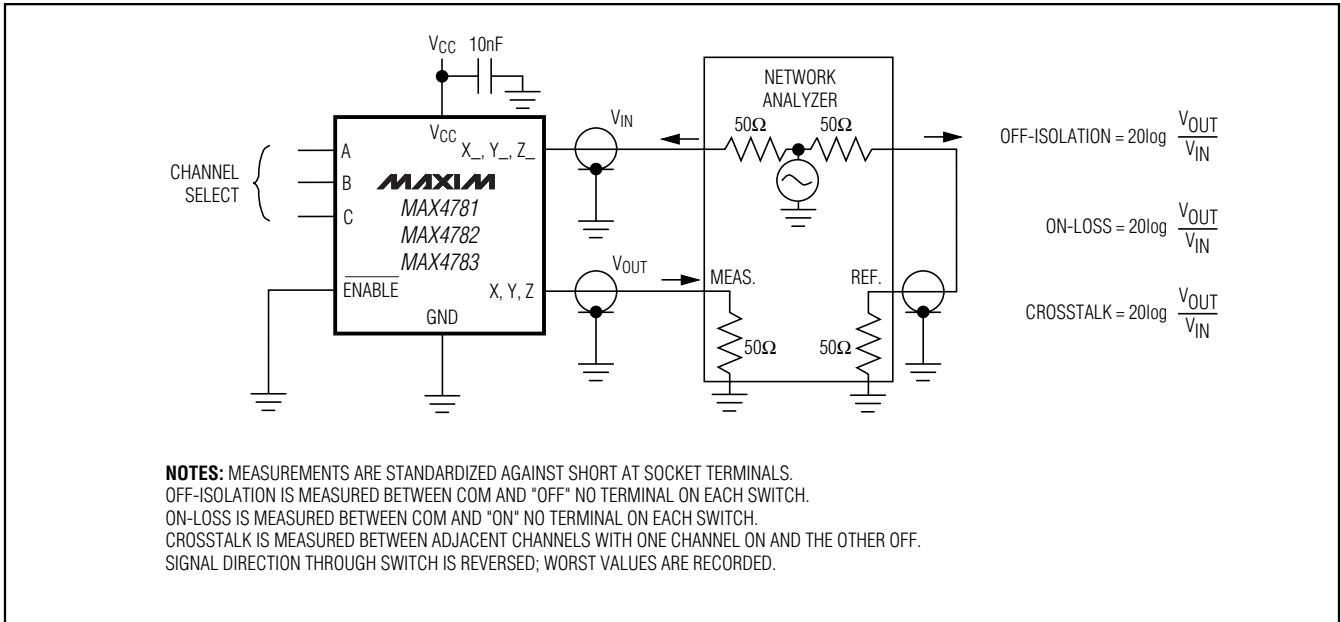


Figure 5. Off-Isolation, On-Loss, and Crosstalk

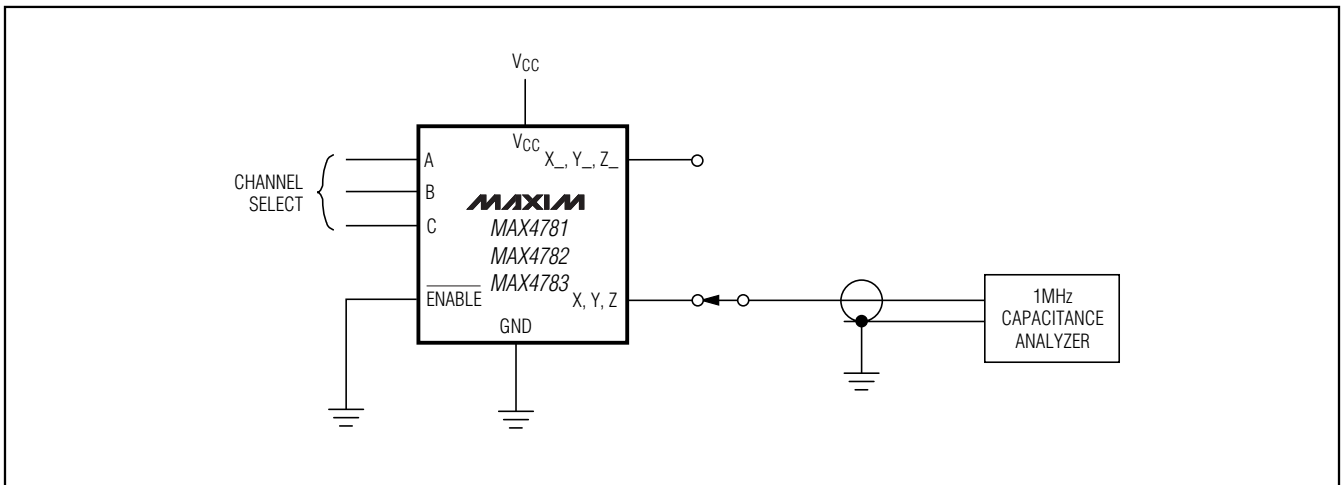


Figure 6. Capacitance

Chip Information

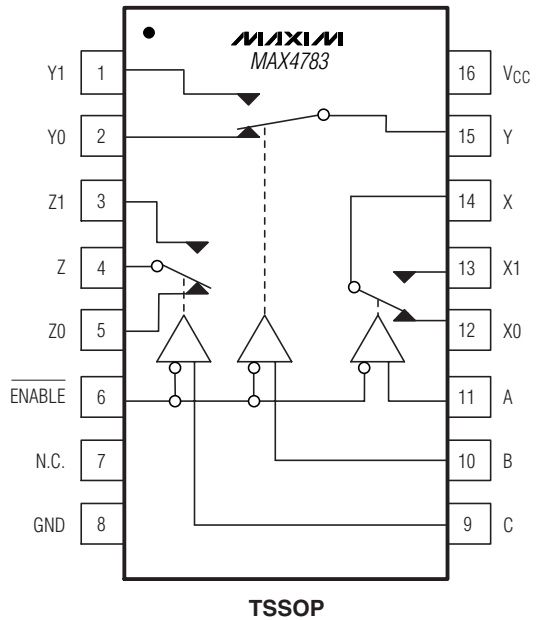
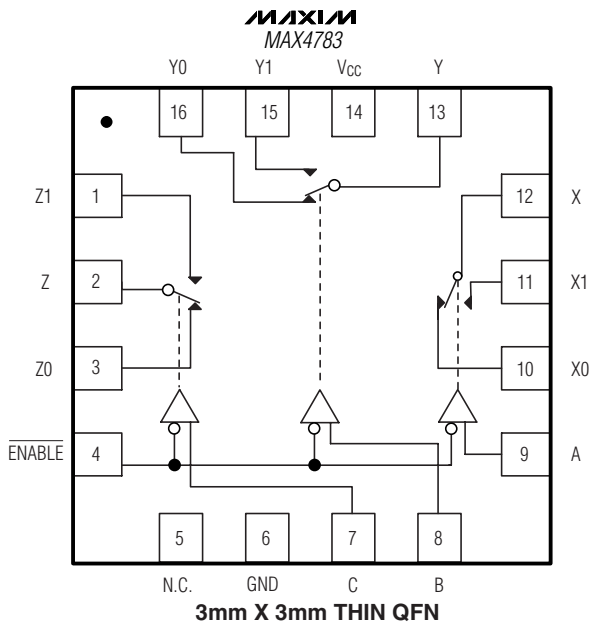
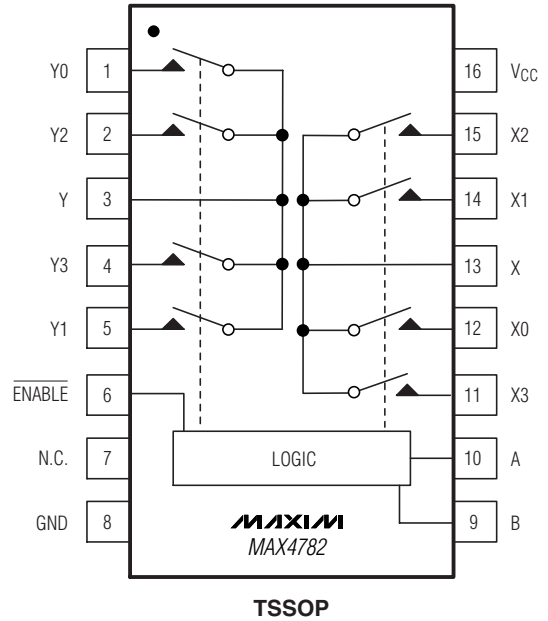
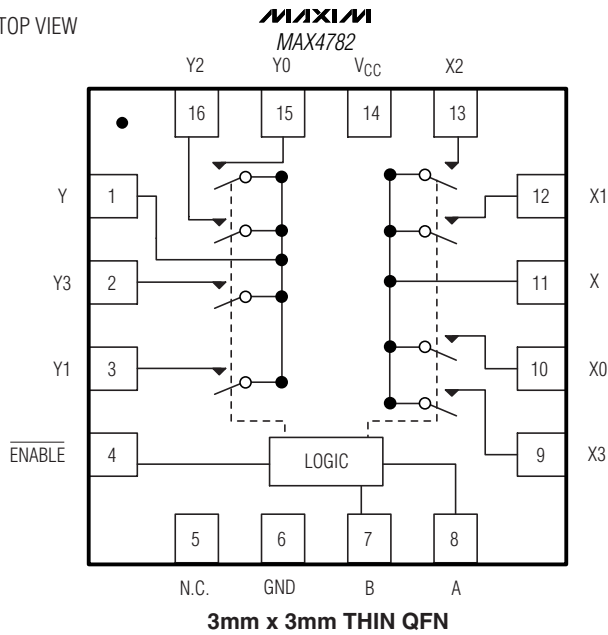
TRANSISTOR COUNT: 659

PROCESS: CMOS

High-Speed, Low-Voltage, 0.7Ω CMOS Analog Switches/Multiplexers

Pin Configurations/Functional Diagrams (continued)

TOP VIEW



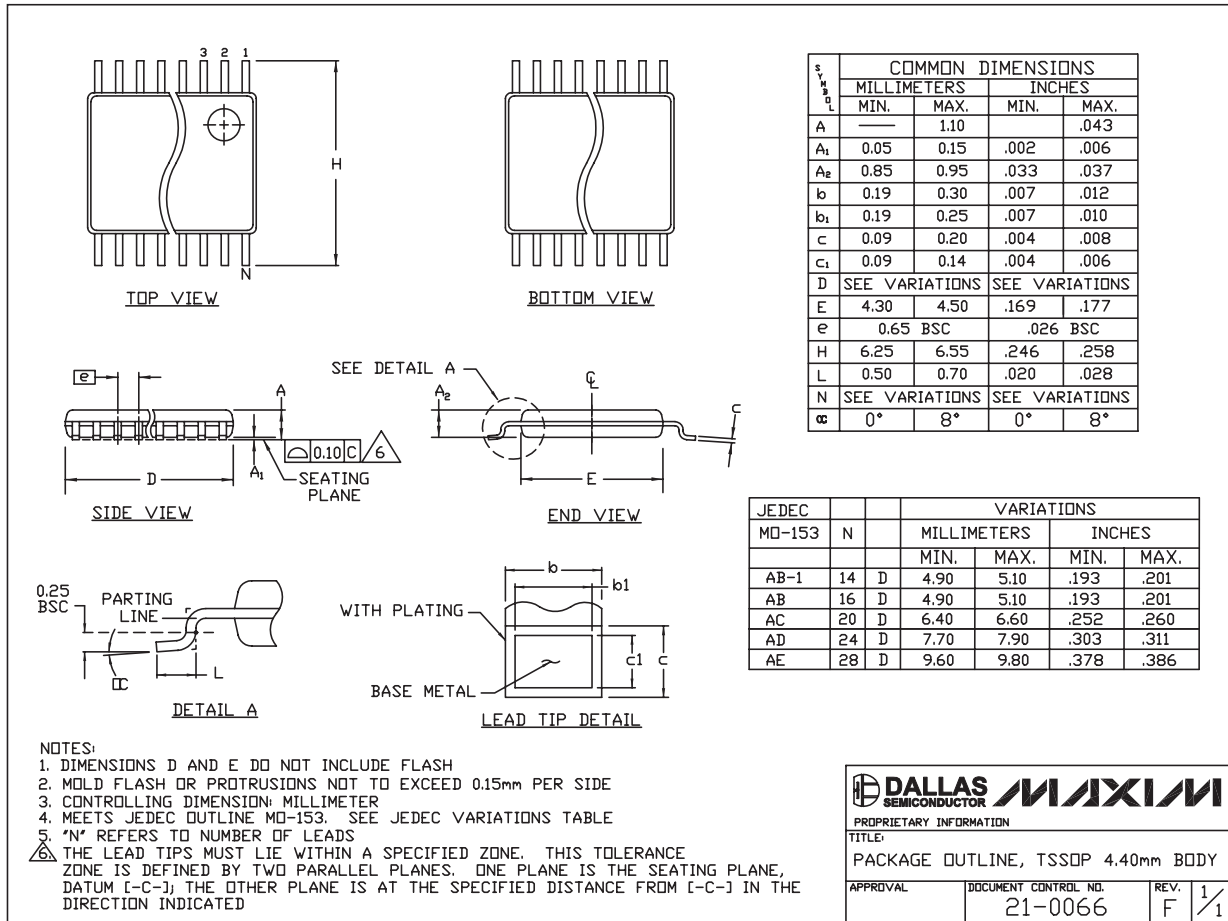
High-Speed, Low-Voltage, 0.7Ω CMOS Analog Switches/Multiplexers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX4781/MAX4782/MAX4783

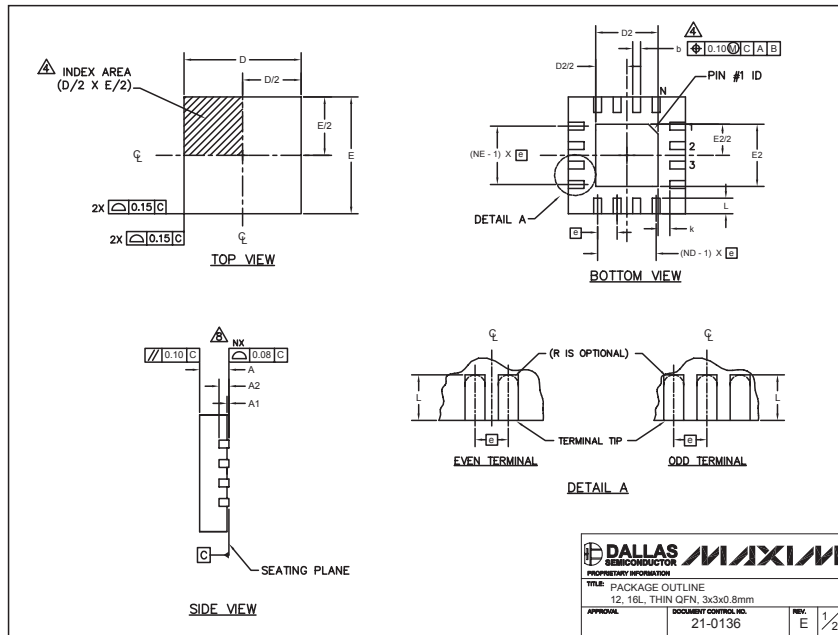
TSSOP4.40mm.EPS



High-Speed, Low-Voltage, 0.7Ω CMOS Analog Switches/Multiplexers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



12x16L OFN THINLEPS

| PKG REF. | 12L 3x3 | | | 16L 3x3 | | |
|----------|-----------|------|------|-----------|------|------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| b | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 |
| D | 2.90 | 3.00 | 3.10 | 2.90 | 3.00 | 3.10 |
| E | 2.90 | 3.00 | 3.10 | 2.90 | 3.00 | 3.10 |
| e | 0.50 BSC. | | | 0.50 BSC. | | |
| L | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 |
| N | 12 | | | 16 | | |
| ND | 3 | | | 4 | | |
| NE | 3 | | | 4 | | |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 |
| A2 | 0.20 REF. | | | 0.20 REF. | | |
| k | 0.25 | - | - | 0.25 | - | - |

| PKG. CODES | D2 | | | E2 | | | PIN ID | JEDEC | DOWN BONDS ALLOWED |
|------------|------|------|------|------|------|------|-------------|--------|--------------------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | | | |
| T1233-1 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45° | WEED-1 | NO |
| T1233-3 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45° | WEED-1 | YES |
| T1633-1 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45° | WEED-2 | NO |
| T1633-2 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45° | WEED-2 | YES |
| T1633F-3 | 0.65 | 0.80 | 0.95 | 0.65 | 0.80 | 0.95 | 0.225 x 45° | WEED-2 | N/A |
| T1633-4 | 0.95 | 1.10 | 1.25 | 0.95 | 1.10 | 1.25 | 0.35 x 45° | WEED-2 | NO |

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-D12. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220 REVISION C.

DALLAS SEMICONDUCTOR **MAXIM**

PROPRIETARY INFORMATION

TITLE PACKAGE OUTLINE
12, 16L, THIN OFN, 3x3x0.8mm

APPROVAL _____ DOCUMENT CONTROL NO. 21-0136 REV. E 2/2

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