Synchronous Buck or Boost Controller for 2-Cell Li+ Battery Operated Portable Communication Devices

FEATURES

- Voltage Mode Control
- 5-V to 10-V Input Voltage Range for V_{DD}
- 5-V to 12.6-V Input Voltage Range for V_S – Boost
- Programmable PWM/PSM Control
  - Up to 2-MHz Switching Frequency in PWM
  - Synchronous Rectification in PWM
  - Less than 350-μA I_{DD} in PSM
- Very High Efficiencies In Buck or Boost Modes
- Low Dropout Operation at 100% Duty Cycle In Buck Mode
- Integrated UVLO and POR
- Integrated Soft-Start
- Synchronization
- Logic Controlled Micropower Shutdown Current <2 μA
- Fast Line and Load Transient Response
- Available in 16-Lead TSSOP Package

APPLICATIONS

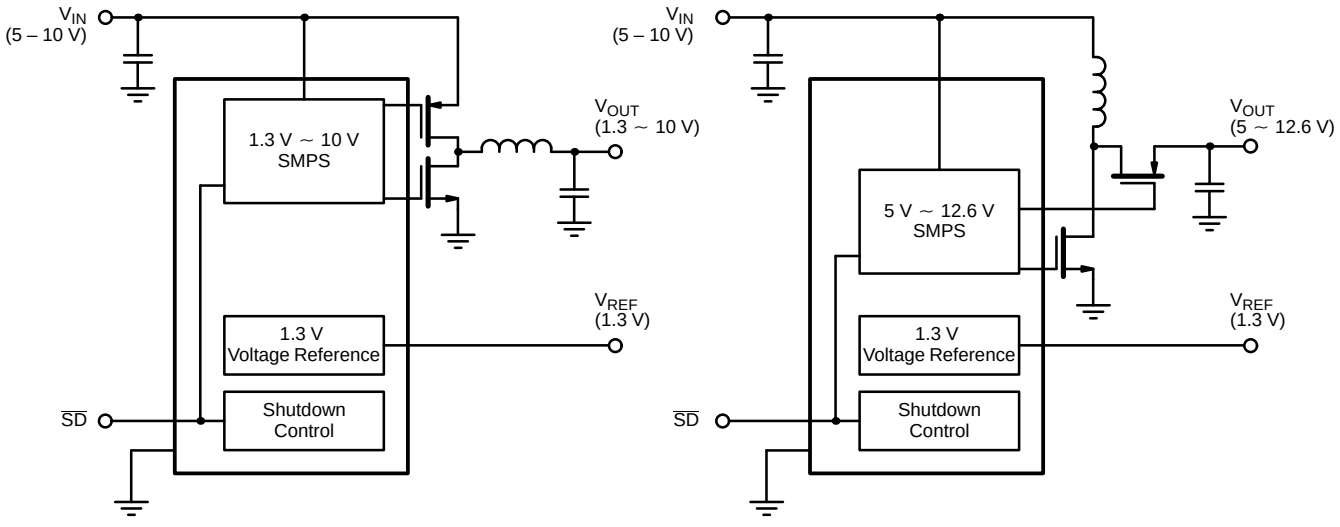
- Cellular Telephones
- Wireless Modems
- Portable Instruments
- Notebook and Palmtop Computers
- PDA's
- Battery Operated Devices

DESCRIPTION

The Si9168 is a synchronous buck or boost controller for 2-cell Li+ battery operated portable communication devices. Designed for use with external high-frequency MOSFETs, the Si9168 is ideal for providing power to various power amplifiers such as TDMA, CDMA, GSM, or PCS. For ultra-high efficiency, converters are designed to operate in synchronous rectified PWM mode under full load, while transforming into externally controlled pulse skipping mode (PSM) under light load conditions. All these features are provided by Si9168 without sacrificing system integration requirements of fitting these circuits into ever demanding smaller space. The Si9168 is capable of switching up to 2 MHz to minimize the size of the output inductor and capacitor, in order to decrease the overall converter footprint. The programmability to design a buck or boost converter with this IC makes it convenient to power either the high voltage (7.2-V) or low voltage (4-V) PAs.

The Si9168 is available in TSSOP-16 pin package and specified to operate over the industrial temperature range of –25°C to 85°C.

FUNCTIONAL BLOCK DIAGRAM



Buck Mode **Boost Mode**

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to AGND
V_{DD} . . . . . 13.2 V
V_{SS}–V_{DD} . . . . . 2 V
PWM/$\overline{PSM}$, SYNC, $\overline{SD}$, V_{REF}, R_{OSC}, COMP, FB, Mode . . . . . –0.3 V to V_{DD} + 0.3 V
V_O . . . . . –0.3 V to V_S + 0.3 V
PGND . . . . . ±0.3V
Voltages Referenced to PGND
V_S. . . . . 13.2 V
D_H, D_L . . . . . –0.3 V to V_S + 0.3 V

Peak Output Current (D_H, D_L) . . . . . 1 A
Storage Temperature . . . . . –65 to 150°C
Operating Junction Temperature . . . . . 150°C
Power Dissipation (Package)[a]
16-Pin TSSOP (Q Suffix)[b] . . . . . 925 mW
Thermal Impedance (Θ_{JA})
16-Pin TSSOP . . . . . 135°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.4 mW/°C above 25°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Voltages Referenced to AGND
V_{DD} . . . . . 5 V to 10 V
F_{OSC} . . . . . 200 kHz to 2 MHz
R_{OSC} . . . . . 25 kΩ to 300 kΩ
PWM/$\overline{PSM}$, SYNC, $\overline{SD}$, Mode . . . . . 0 V to V_{DD}

V_{REF} . . . . . 0.1 µF
Voltages Referenced to PGND
V_S . . . . . 5.0 V to 10 V (Buck)
V_S . . . . . 5.0 V to 12.6 V (Boost)

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified 5 V ≤ V_{DD}, V_S ≤ 10 V	Limits –25°C to 85°C Min[a]	Typ[b]	Max[a]	Unit
Reference						
Output Voltage	V_{REF}	I_{REF} = 0 A	1.268	1.3	1.332	V
		V_{DD} = 7.2 V, 25°C	1.280	1.3	1.320	
V_{REF} Current	I_{REF}		–500			µA
Power Supply Rejection	P_{SRR}			60		dB
UVLO						
Under Voltage Lockout (Turn-On)	$V_{UVLO/LH}$		4.3	4.5	4.7	V
Hysteresis	V_{HYS}			0.2		
Soft-Start Time						
SS Time	t_{SS}			3		ms
SD, SYNC, PWM/$\overline{PSM}$						
Logic High	V_{IH}		2.4			V
Logic Low	V_{IL}				0.8	
Input Current	I_L		–1.0		1.0	µA
Mode						
Logic High	V_{IH}		70% V_{DD}			V
Logic Low	V_{IL}				30% V_{DD}	
Input Current	I_L		–1.0		1.0	µA

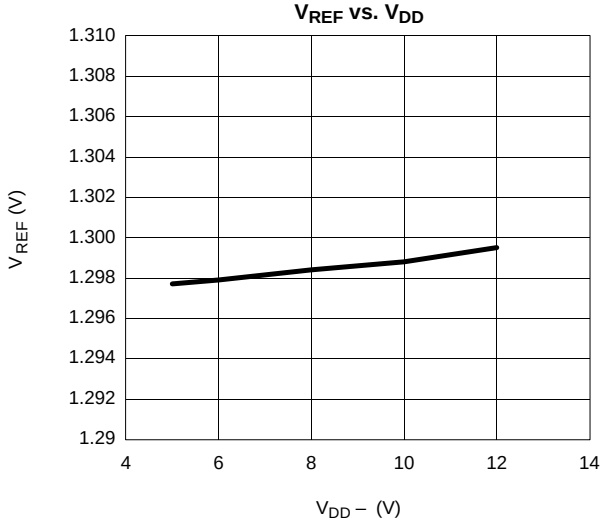
SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified 5 V ≤ V_{DD}, V_S ≤ 10 V	Limits –25°C to 85°C Min[a]	Typ[b]	Max[a]	Unit
Oscillator						
Maximum Frequency	F_{MAX}		2			MHz
Accuracy		1% External Resistor	–20		20	%
Maximum Duty Cycle (Buck, Non LDO Mode)	D_{MAX}	F_{SW} = 2 MHZ	75	80		%
Maximum Duty Cycle (Boost)	D_{MAX}	R_{OSC} = 130 kΩ, V_{DD} = 5 V, V_S = 12.6 V	65	71		%
SYNC Range	F_{SYNC}/F_{OSC}		1.2		1.5	
SYNC Low Pulse Width			50			ns
SYNC High Pulse Width			50			ns
SYNC t_r, t_f	t_r, t_f				50	ns
Error Amplifier						
Input Bias Current	I_{BIAS}	V_{FB} = 1.4 V	–1		1	µA
Open Loop Voltage Gain	A_{VOL}		50	60		dB
Offset Voltage	V_{OS}		–10		10	mV
Unity Gain BW	BW			2		MHz
Output Current (Source)	I_{EA}	V_{FB} = 1.05 V		–2	–1	mA
Output Current (Sink)	I_{EA}	V_{FB} = 1.55 V	1	3		mA
Power Supply Rejection	P_{SRR}			60		dB
PSM Modulator						
Switch On Time	t_{ON}	V_{DD} = 7.2 V, V_{OUT} = 3.3 V, Buck Mode		180		ns
Switch Off Blanking Time	t_{OFF}	V_{DD} = 7.2 V, V_{OUT} = 3.3 V, Buck Mode		330		ns
Output Drive (D_H and D_L)						
Output High Voltage	V_{OH}	V_S = 7.2 V, I_{OUT} = –20 mA	7.08	7.14		V
Output Low Voltage	V_{OL}	V_S = 7.2 V, I_{OUT} = 20 mA		0.06	0.12	V
Peak Output Source	I_{SOURCE}	V_S = 7.2 V, D_H = D_L = V_S/2		–1000	–500	mA
Peak Output Sink	I_{SINK}	V_S = 7.2 V, D_H = D_L = V_S/2	500	1000		mA
Break-Before-Make	t_{BBM}	V_S = V_{DD} = 10 V		40		ns
Supply						
Normal Mode	I_{DD}	V_{DD} = 7.2 V, f_{OSC} = 2 MHz			1100	µA
PSM Mode	I_{DD}	V_{DD} = 7.2 V			350	µA
Shutdown Mode	I_{DD}	V_{DD} = 7.2 V, $\overline{SD}$ = 0 V			2.0	µA

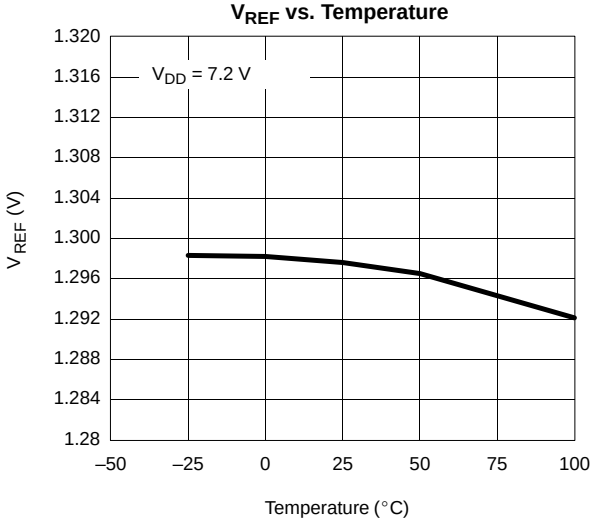
Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
b. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
c. Guaranteed by design and characterization, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

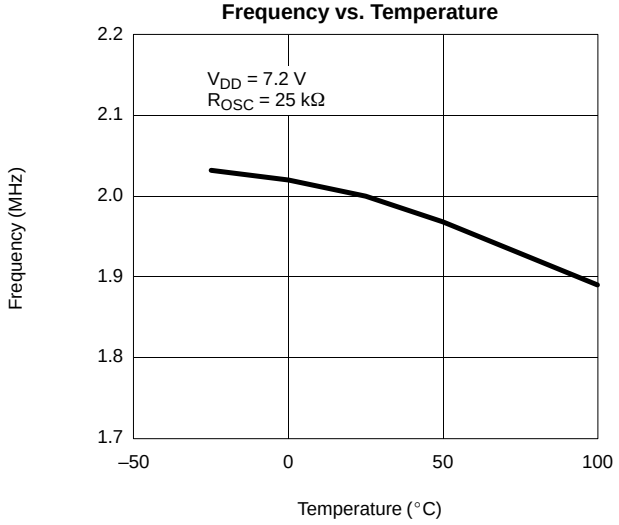
V_{REF} vs. V_{DD}



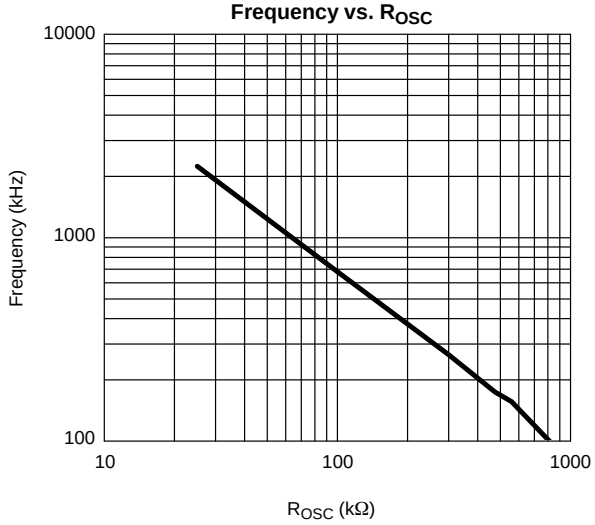
V_{REF} vs. Temperature



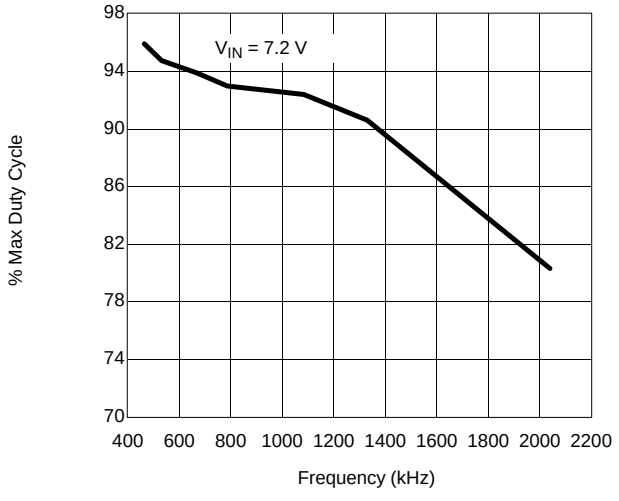
Frequency vs. Temperature



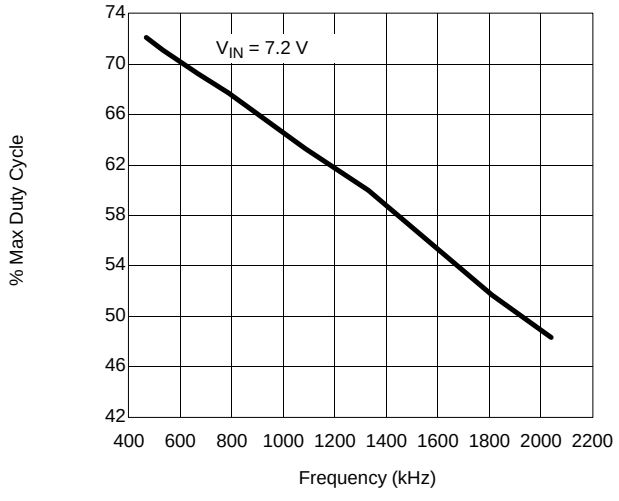
Frequency vs. R_{OSC}



Max Duty Cycle vs. Frequency (Buck Mode)

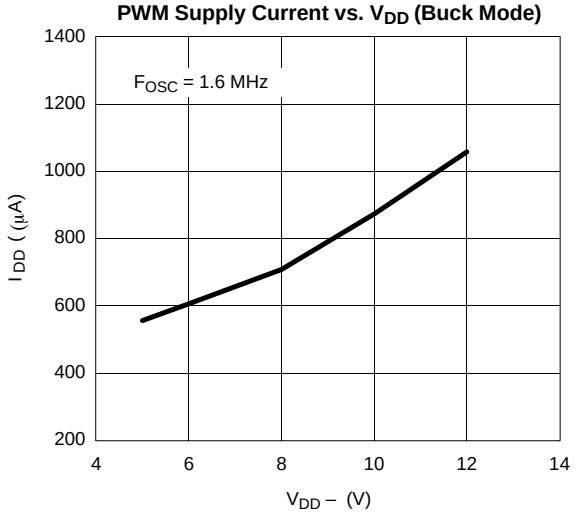


Max Duty Cycle vs. Frequency (Boost Mode)

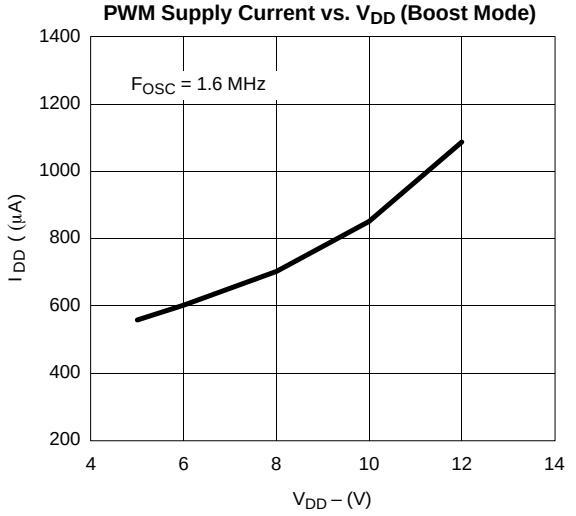


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

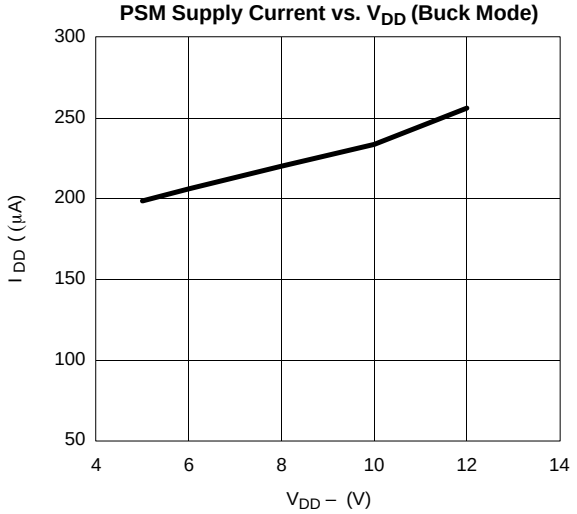
PWM Supply Current vs. V_{DD} (Buck Mode)



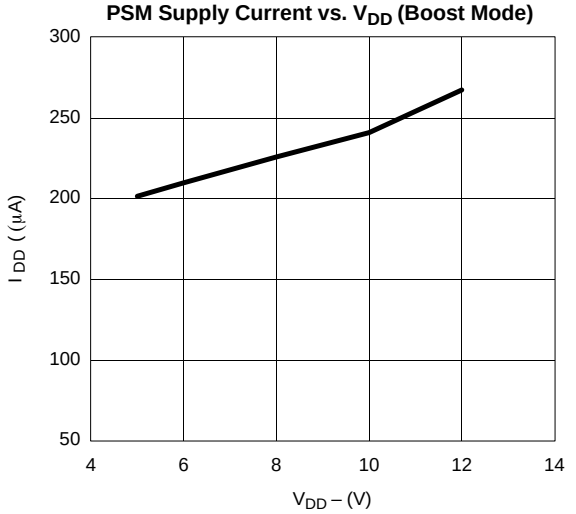
PWM Supply Current vs. V_{DD} (Boost Mode)



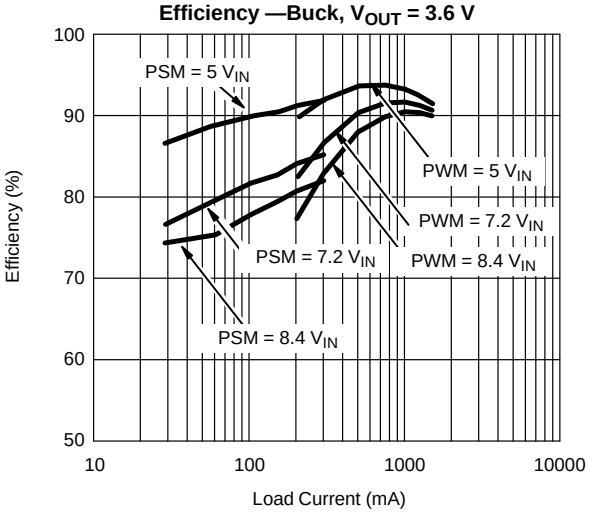
PSM Supply Current vs. V_{DD} (Buck Mode)



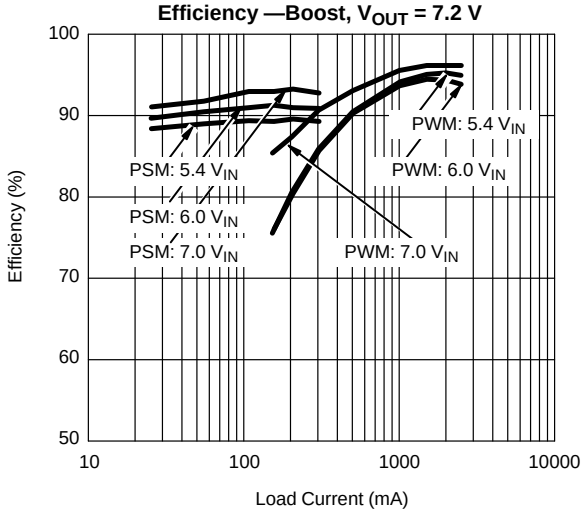
PSM Supply Current vs. V_{DD} (Boost Mode)



Efficiency —Buck, V_{OUT} = 3.6 V

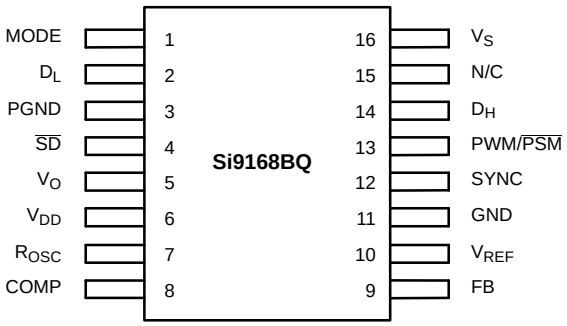


Efficiency —Boost, V_{OUT} = 7.2 V



PIN CONFIGURATION

TSSOP-16



Top View

ORDERING INFORMATION		
Part Number	**Temperature Range**	**Package**
Si9168BQ-T1	–25 to 85°C	Tape and Reel

Eval Kit	**Temperature Range**	**Board Type**
Si9168DB	–25 to 85°C	Surface Mount

PIN DESCRIPTION

Pin Number	Name	Function
1	MODE	Determines the converter topology. Connect to AGND for buck or V_{DD} for boost.
2	D_L	The gate drive output for the low-side n-channel MOSFET for buck and boost converter
3	PGND	Power ground for output drive stage
4	$\overline{SD}$	Logic low shuts down the IC completely and decreases the current consumption of IC to <2 μA.
5	V_O	Direct output voltage sense
6	V_{DD}	Input supply voltage for the analog circuit. V_{DD} voltage should be the ac filtered voltage of V_{SS}. Input voltage range is 5 V to 10 V.
7	R_{OSC}	External resistor to determine the switching frequency.
8	COMP	Error amplifier output for external compensation network.
9	FB	Output voltage feedback connected to the inverting input of an error amplifier.
10	V_{REF}	1.3-V reference voltage. Connected internally to non-inverting error amplifier input. Decouple with 0.1-μF ceramic capacitor.
11	GND	Low power controller ground
12	SYNC	Externally controlled synchronization signal. Logic high to low transition forces the clock synchronization. If not used, the pin must be connected to V_{DD}, or logic high.
13	PWM/$\overline{PSM}$	Logic high = PWM mode, logic low = PSM mode. In PSM mode, synchronous rectification drive is disabled.
14	D_H	The gate drive output for the high-side p-channel MOSFET for buck and boost converter
15	N/C	Not used.
16	V_S	Supply voltage for the output driver section. Voltage range is 5 V to 10 V (Buck), 5 to 12.6 V (Boost).

BLOCK DIAGRAM

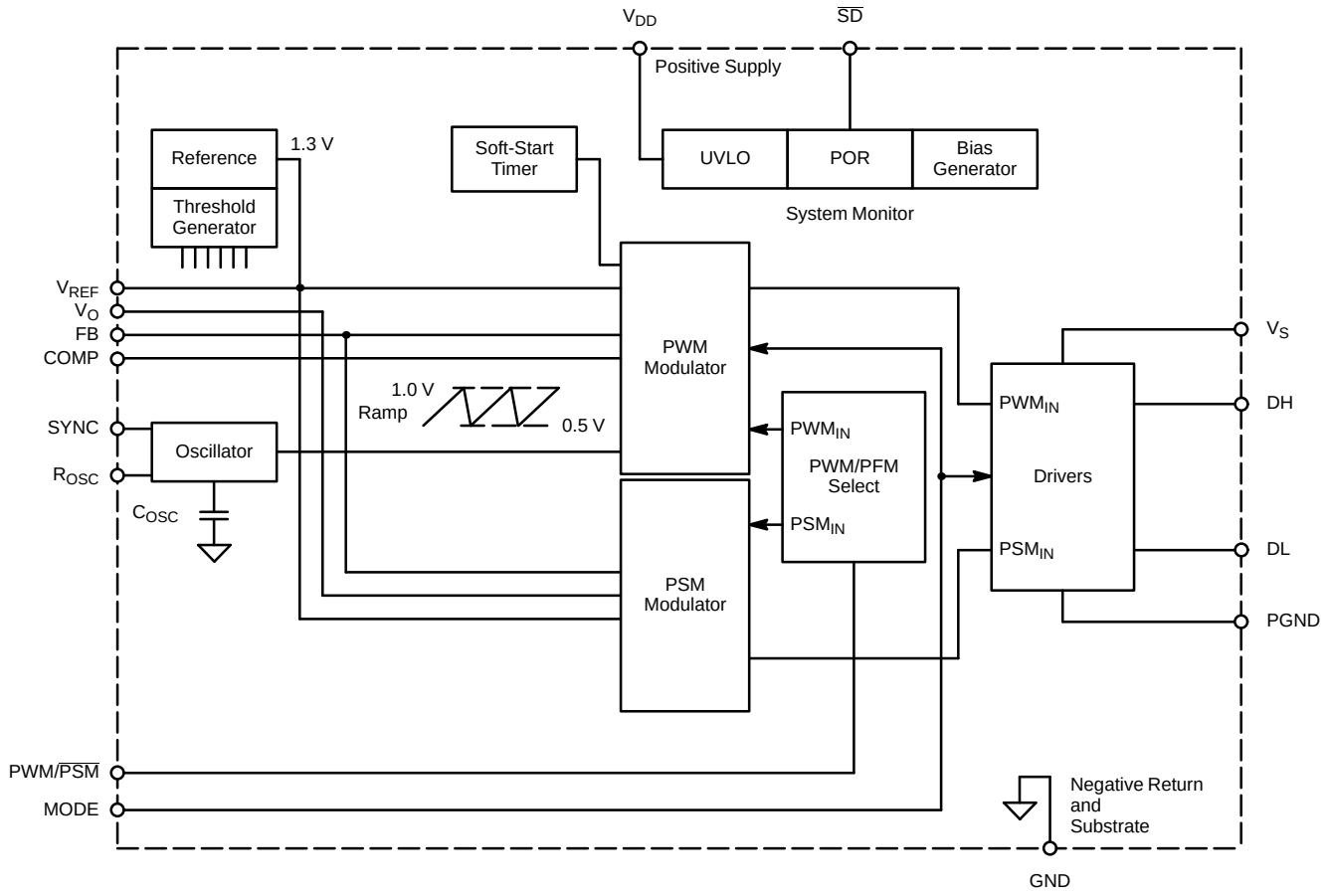


FIGURE 1.

DETAIL OPERATIONAL DESCRIPTION

Start-Up

The UVLO circuit prevents the controller output driver and oscillator circuit from turning on, if the voltage on V_{DD} pin is less than 4.5 V. With typical UVLO hysteresis of 0.2 V, the controller is continuously powered on until the V_{DD} voltage drops below 4.3 V. This hysteresis prevents the converter from oscillating during the start-up phase and unintentionally locking up the system. Once the V_{DD} voltage exceeds the UVLO threshold, and with no other shutdown condition detected, an internal power-on-reset timer is activated while most circuitry, except the output driver, are turned on. After the POR time-out of about 1 ms, the internal soft-start capacitor is allowed to charge. When the soft-start capacitor voltage reaches 0.5 V, the PWM circuit is enabled. Thereafter, the constant current charging of the soft-start capacitor will force the converter output voltage to rise gradually without overshooting. To prevent negative undershoot, the synchronous switch is tri-stated until the duty cycle reaches about 10%. See start-up timing diagram. In tri-state, the high-side p-channel MOSFET is turned off by pulling up the gate voltage (D_H) to V_S potential. The low-side n-channel MOSFET is turned off by pulling down the gate voltage (D_L) to PGND potential. Note that Si9168 will always soft starts in the PWM mode regardless of the voltage level on the PWM/PSM pin.

Shutdown

Si9168 is designed to conserve as much battery life as possible by decreasing current consumption of IC during normal operation as well as the shutdown mode. With logic low level on the $\overline{SD}$ pin, current consumption of the Si9168 decreases to less than 2 μA by shutting off most of the circuits. The logic high enables the controller and starts up as described in “Start-Up” section above.

DETAIL OPERATIONAL DESCRIPTION

PWM Mode

With PWM/$\overline{\text{PSM}}$ mode pin in logic high condition, Si9168 operates in constant frequency (PWM) mode. As the load and input voltage vary, switching frequency remain constant. The switching frequency is programmed by the R_{OSC} value as shown by the oscillator curve. In the PWM mode, the synchronous drive is always enabled, even when the output current reaches 0 A. In continuous current mode, the transfer function of the converter remain constant providing fast transient response. If the converter operates in discontinuous current mode, overall loop gain decreases and transient response time can be 10 times longer than if the converter remain in continuous current mode. This transient response time advantage can significantly decrease the hold-up capacitors needed on the output of dc-dc converter to meet the transient voltage regulation. Therefore, the PWM/PSM pin is available to dynamically program the controller. If the synchronous rectifier switch is not used, the converter may not operate in PWM mode if the load current is low enough to force the converter into pulse skipping mode.

The maximum duty cycle of the Si9168 can reach 100% in buck mode. The duty cycle will continue to increase as the input voltage decreases until it reaches 100%. This allows the system designers to extract out the maximum stored energy from the battery. Once the controller delivers 100% duty cycle, the converter operates like a saturated linear regulator. At 100% duty cycle, synchronous rectification is completely turned off. At up to 80% duty cycle at 2-MHz switching frequency, the controller maintains perfect output voltage regulation. If the input voltage drops below the level where the converter requires greater than 80% duty cycle, the controller will deliver 100% duty cycle. This instantaneous jump in duty cycle is due to fixed BBM time and the internal propagation delays. In order to maintain regulation, the controller might fluctuate its duty cycle back and forth from 100% to something lower than 80% during this input voltage range. If the input voltage drops further, the controller will remain on for 100% duty cycle. If the input voltage increases to a point where it's requiring less than 80% duty cycle, synchronous rectification is once again activated.

The maximum duty cycle under boost mode is internally limited to 75% to prevent inductor saturation. If the converter is turned on for 100% duty cycle, the inductor never gets a chance to discharge its energy and eventually saturate. In boost mode, the synchronous rectifier is always turned on for minimum or greater duration as long as the switch has been turned on. The controller will deliver 0% duty cycle, if the input voltage is greater than the programmed output voltage. Because of fixed BBM time, the controller will not transition smoothly from minimum controllable duty cycle to 0% duty cycle. For example, controller may decrease its duty cycle from 5% to 0% abruptly, instead of the gradual decrease seen from 75% to 5%.

Pulse Skipping Mode

The gate charge losses produced from the Miller capacitance of MOSFETs are the dominant power dissipation parameter during light load (i.e. < 200 mA). Therefore, less gate switching will improve overall converter efficiency. This is exactly why the Si9168 is designed with pulse skipping mode. If the PWM/$\overline{\text{PSM}}$ pin is connected to logic low level, converter operates in pulse skipping modulation (PSM) mode. During the pulse skipping mode, quiescent current of the controller is decreased to approximately 350 μA, instead of 900 μA during the PWM mode. This is accomplished by turning off most of the internal control circuitry and utilizing a simple constant on-time control with the feedback comparator. The controller is designed to have a constant on-time and a minimum off-time acting as the feedback comparator blanking time. If the output voltage drops below the desired level, the main switch is first turned on and then off. If the applied on-time is insufficient to provide the desired voltage, the controller will force another on and off sequence, until the desired voltage is accomplished. If the applied on-time forces the output to exceed the desired level, as typically found in the light load condition, the converter stays off. The excess energy is delivered to the output slowly, forcing the converter to skip pulses as needed to maintain regulation. The on-time and off-time are set internally based on the inductor used (2-μH typical) and the maximum load current. Therefore, with this control method, duty cycles ranging from 0 to 100% are possible depending on whether the boost or buck mode is chosen.

Reference

The reference voltage for the Si9168 is set at 1.3 V. The reference voltage is internally connected to the non-inverting inputs of the error amplifier. The REF pin requires a 0.1-μF decoupling capacitor.

Error Amplifier

The error amplifier gain-bandwidth product and slew rate are critical parameters which determines the transient response of converter. The transient response is function of both small and large signal responses. The small signal response is determined by the feedback compensation network while the large signal is determined by the error amplifier dv/dt and the inductor di/dt slew rate. Besides the inductance value, the error amplifier determines the converter response time. In order to minimize the response time, Si9168 is designed with a 2-MHz error amplifier gain-bandwidth product to generate the widest converter bandwidth and a 3.5-V/μsec slew rate for ultra-fast large signal response.

Oscillator

The oscillator is designed to operate up to 2-MHz minimum. The 2-MHz operating frequency allows the converter to minimize the inductor and capacitor size, improving the power density of the converter. Even with a 2-MHz switching frequency, quiescent current is only 1100 μA (max) with the unique power saving circuit design. The switching frequency is easily programmed by attaching a resistor to the R_{OSC} pin. See oscillator frequency versus Rosc curve to select the proper timing values for the desired operating frequency. The tolerance on the operating frequency is ±20% with a 1% tolerance resistor.

DETAIL OPERATIONAL DESCRIPTION

Synchronization

The synchronization to external clock is easily accomplished by connecting the external clock into the SYNC pin. The logic high to low transition synchronizes the clock. The external clock frequency must be within 1.2 to 1.5 times the internal clock frequency.

Break-Before-Make Timing

A proper BBM time is essential in order to prevent shoot-through current and to maintain high efficiency. The break-before-make time is set internally at 20 to 60 ns @ V_S = 7.2 V. The high- and low-side gate drive voltages are monitored and when the gate-to-source voltage reaches 3.5 V above or below the initial starting voltage, 20- to 60-ns BBM time is set before the other gate drive transitions to its proper state. The maximum and minimum duty cycle is limited by the BBM time. Since the BBM time is fixed, controllable maximum duty cycle will vary depending on the switching frequency.

Output Driver Stage

The D_H pin is designed to drive the main switch MOSFET and D_L pin is designed to drive the synchronous rectifier MOSFET. The driver stage is sized to sink and source peak currents up to 1000 mA with V_S = 7.2 V. The ringing from the gate drive output trace inductance can produce negative voltage on the D_H and D_L respect to PGND. The gate drive circuit is capable of withstanding these negative voltages without any functional defects.

APPLICATIONS

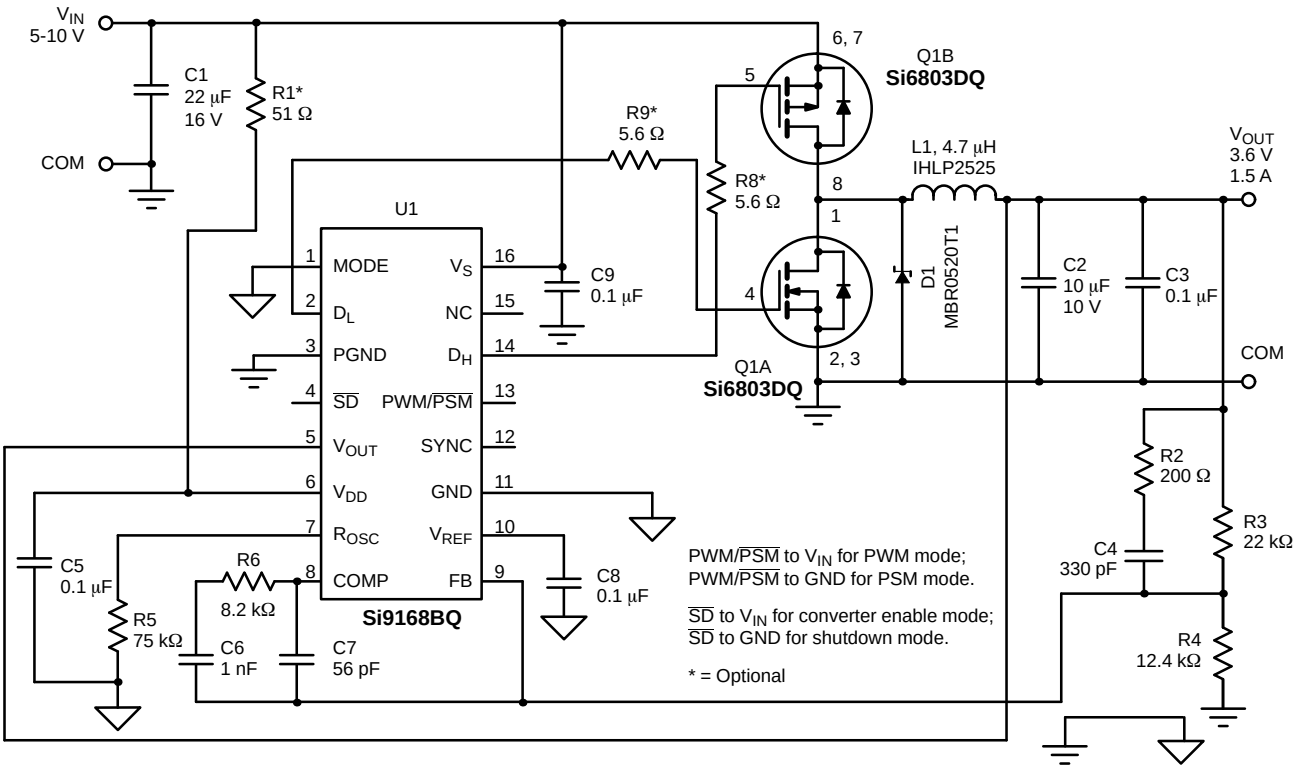


FIGURE 2. 1.5-A Buck Regulator Using the Si9168BQ

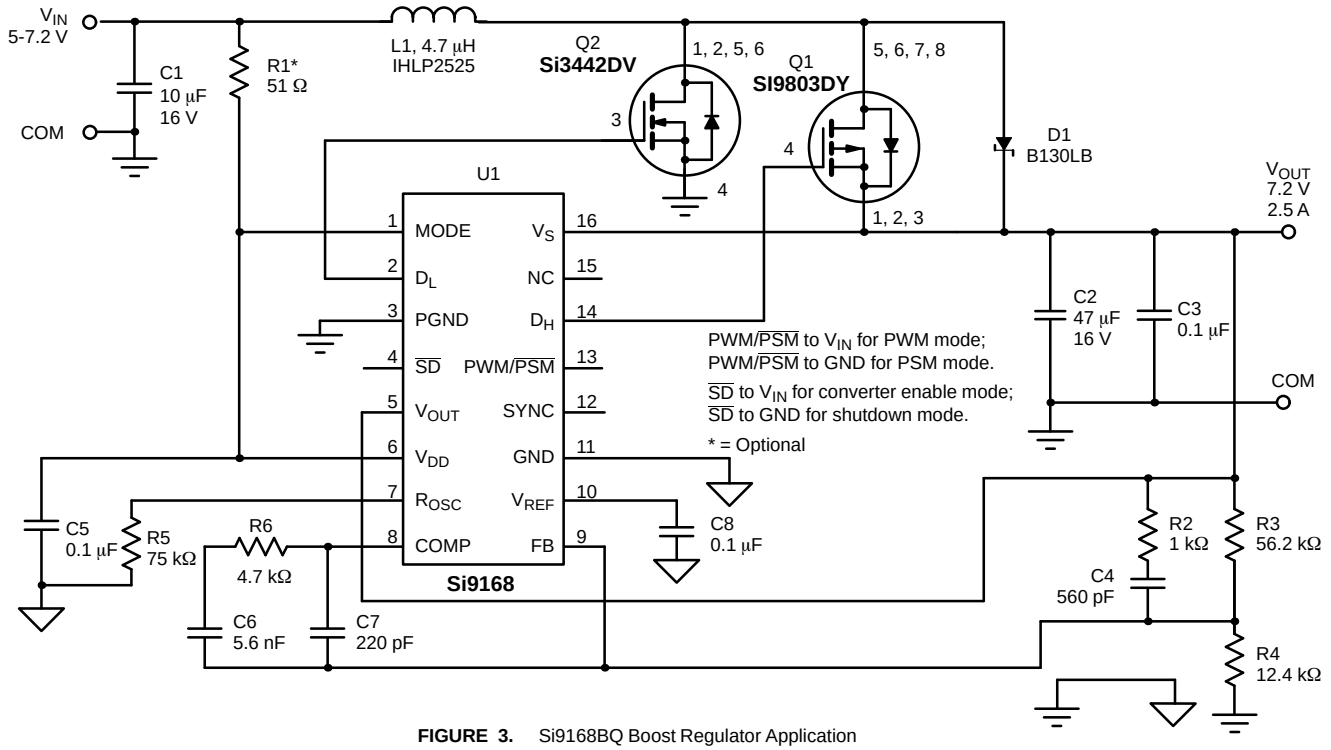


FIGURE 3. Si9168BQ Boost Regulator Application

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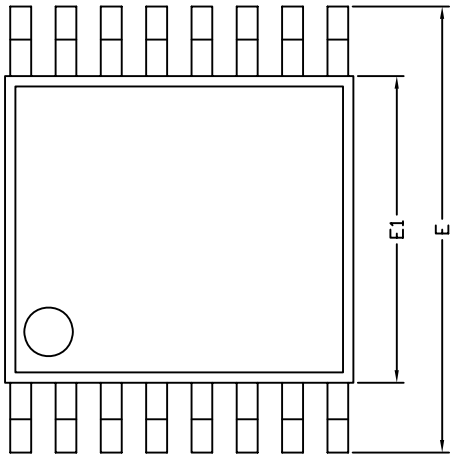
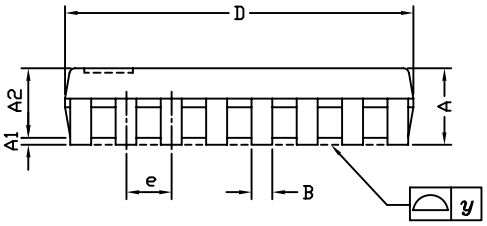
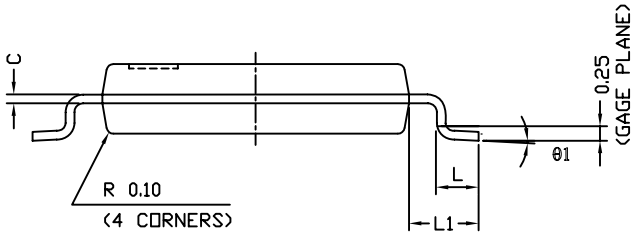
TSSOP: 16-LEAD

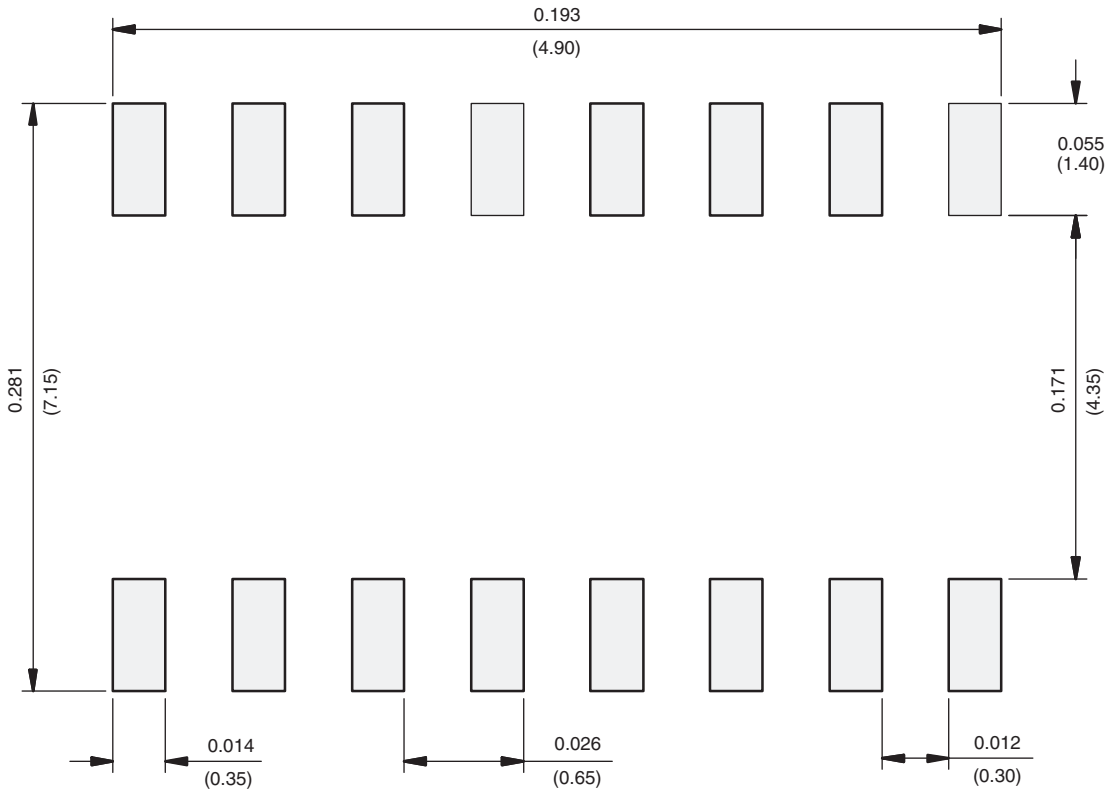






Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624			

RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

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