

8-Ch/Dual 4-Ch High-Performance CMOS Analog Multiplexers

DESCRIPTION

The DG408 is an 8 channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A_0 , A_1 , A_2). The DG409 is a dual 4 channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2-bit binary address (A_0 , A_1). Break-before-make switching action protects against momentary crosstalk between adjacent channels.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address (A_x) and enable (EN) are TTL compatible over the full specified operating temperature range.

Applications for the DG408, DG409 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

Designed in the 44 V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 V. Additionally, single supply operation is also allowed. An epitaxial layer prevents latchup.

For additional information please see Technical Article TA201.

FEATURES

- Low on-resistance - $R_{DS(on)}$: 100 Ω
- Low charge injection - Q: 20 pC
- Fast transition time - t_{TRANS} : 160 ns
- Low power - I_{SUPPLY} : 10 μ A
- Single supply capability
- 44 V supply max. rating
- TTL compatible logic
- **Compliant to RoHS Directive 2002/95/EC**



BENEFITS

- Reduced switching errors
- Reduced glitching
- Improved data throughput
- Reduced power consumption
- Increased ruggedness
- Wide supply ranges (± 5 V to ± 20 V)

APPLICATIONS

- Data acquisition systems
- Audio signal routing
- ATE systems
- Battery powered systems
- Single supply systems
- Medical instrumentation

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



* Pb containing terminations are not RoHS compliant, exemptions may apply

TRUTH TABLE (DG408)				
A ₂	A ₁	A ₀	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE (DG409)			
A ₁	A ₀	EN	ON SWITCH
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Notes

- Logic "0" = $V_{AL} \leq 0.8\text{ V}$
- Logic "1" = $V_{AH} \geq 2.4\text{ V}$
- X = Do not care

ORDERING INFORMATION (Commercial)				
PART	CONFIGURATION	TEMP. RANGE	PACKAGE	ORDERING PART NUMBER
DG408	8:1 x 1	- 40 °C to 85 °C	16-pin plastic DIP	DG408DJ
				DG408DJ-E3
				DG408DY
			16-pin SOIC	DG408DY-E3
				DG408DY-T1
				DG408DY-T1-E3
			16-pin TSSOP	DG408DQ
				DG408DQ-E3
				DG408DQ-T1
DG409	4:1 x 2	- 40 °C to 85 °C	16-pin plastic DIP	DG409DJ
				DG409DJ-E3
				DG409DY
			16-pin SOIC	DG409DY-E3
				DG409DY-T1
				DG409DY-T1-E3
			16-pin TSSOP	DG409DQ
				DG409DQ-E3
				DG409DQ-T1
			DG409DQ-T1-E3	

ABSOLUTE MAXIMUM RATINGS			
PARAMETER		LIMIT	UNIT
Voltages Referenced to V-	V+	44	V
	GND	25	
Digital Inputs ^a , V _S , V _D		(V-) - 2 to (V+) + 2 or 20 mA, whichever occurs first	
Current (any terminal)		30	mA
Peak Current, S or D (pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage Temperature	(DJ, DY suffix)	- 65 to 125	°C
Power Dissipation (Package) ^b	16-pin plastic DIP ^c	450	mW
	16-pin narrow SOIC and TSSOP ^d	600	

Notes

- Signals on S_X, D_X or I_{NX} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads soldered or welded to PC board.
- Derate 6 mW/°C above 75 °C.
- Derate 7.6 mW/°C above 75 °C.



SPECIFICATIONS ^a									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED			D SUFFIX - 40 °C to 85 °C		UNIT		
		V ₊ = 15 V, V ₋ = - 15 V			TEMP. ^b	TYP. ^c		MIN. ^d	MAX. ^d
		V _{AL} = 0.8 V, V _{AH} = 2.4 V ^f							
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}			Full	-	- 15	15	V	
Drain-Source On-Resistance	R _{DS(on)}	V _D = ± 10 V, I _S = - 10 mA		Room	40	-	100	Ω	
				Full	-	-	125		
R _{DS(on)} Matching Between Channels ⁹	ΔR _{DS(on)}	V _D = ± 10 V		Room	-	-	15		
Source Off Leakage Current	I _{S(off)}	V _S = ± 10 V, V _D = ± 10 V, V _{EN} = 0 V		Room	-	- 0.5	0.5		
				Full	-	- 5	5		
DG408	Drain Off Leakage Current	V _D = ± 10 V, V _S = ± 10 V, V _{EN} = 0 V		Room	-	- 1	1	nA	
DG408				Full	-	- 20	20		
DG409				Room	-	- 1	1		
DG409				Full	-	- 10	10		
DG408	Drain On Leakage Current	V _S = V _D = ± 10 V sequence each switch on		Room	-	- 1	1		
DG408				Full	-	- 20	20		
DG409				Room	-	- 1	1		
DG409				Full	-	- 10	10		
Digital Control									
Logic High Input Voltage	V _{INH}			Full	-	2.4	-	V	
Logic Low Input Voltage	V _{INL}			Full	-	-	0.8		
Logic High Input Current	I _{AH}	V _A = 2.4 V, 15 V		Full	-	- 10	10	μA	
Logic Low Input Current	I _{AL}	V _{EN} = 0 V, 2.4 V, V _A = 0 V		Full	-	- 10	10		
Logic Input Capacitance	C _{in}	f = 1 MHz		Room	8	-	-	pF	
Dynamic Characteristics									
Transition Time	t _{TRANS}	see figure 2		Full	160	-	250	ns	
Break-Before-Make Interval	t _{OPEN}	see figure 4		Room	-	10	-		
Enable Turn-On Time	t _{ON(EN)}	see figure 3		Room	115	-	150		
Enable Turn-Off Time	t _{OFF(EN)}			Full	-	-	-		
Charge Injection	Q	C _L = 10 nF, V _S = 0 V		Room	20	-	-	pC	
Off Isolation ^h	OIRR	V _{EN} = 0 V, R _L = 1 kΩ, f = 1 MHz		Room	- 75	-	-	pF	
Source Off Capacitance	C _{S(off)}	V _{EN} = 0 V, V _S = 0 V, f = 1 MHz		Room	3	-	-		
DG408	Drain Off Capacitance	V _{EN} = 0 V, V _D = 0 V, f = 1 MHz		Room	26	-	-		
DG409				Room	14	-	-		
DG408	Drain On Capacitance			Room	37	-	-		
DG409				Room	25	-	-		
Power Supplies									
Positive Supply Current	I ₊	V _{EN} = V _A = 0 V or 5 V		Full	10	-	75	μA	
Negative Supply Current	I ₋			Full	1	- 75	-		
Positive Supply Current	I ₊	V _{EN} = V _A = 0 V or 5 V		Room	0.2	-	0.5	mA	
Negative Supply Current	I ₋			Full	-	-	2		
				Full	-	- 500	-	μA	



SPECIFICATIONS ^a (Single Supply)							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED	TEMP. ^b	TYP. ^c	D SUFFIX - 40 °C to 85 °C		UNIT
		V ₊ = 12 V, V ₋ = 0 V			MIN. ^d	MAX. ^d	
		V _{AL} = 0.8 V, V _{AH} = 2.4 V ^f					
Analog Switch							
Drain-Source On-Resistance ^{e, f}	R _{DS(on)}	V _D = 3 V, 10 V, I _S = -1 mA	Room	90	-	-	Ω
Dynamic Characteristics							
Switching Time of Multiplexer ^e	t _{TRANS}	V _{S1} = 8 V, V _{S8} = 0 V, V _{IN} = 2.4 V	Room	180	-	-	ns
Enable Turn-On Time ^e	t _{ON(EN)}	V _{INH} = 2.4 V, V _{INL} = 0 V, V _{S1} = 5 V	Room	180	-	-	
Enable Turn-Off Time ^e	t _{OFF(EN)}		Room	120	-	-	
Charge Injection ^e	Q	C _L = 1 nF, V _S = 0 V, R _S = 0	Room	5	-	-	pC

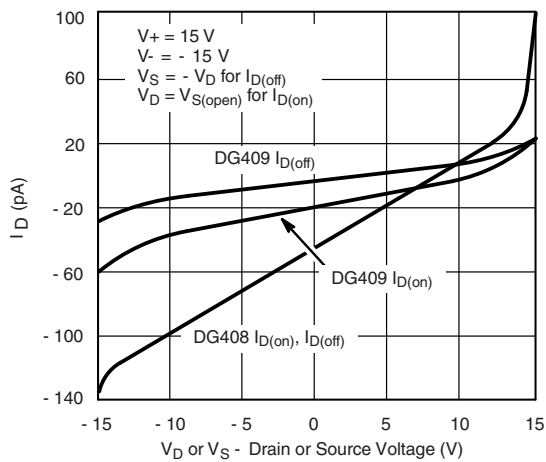
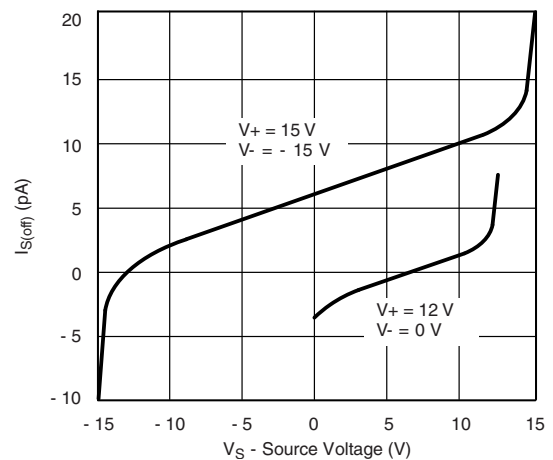
Notes

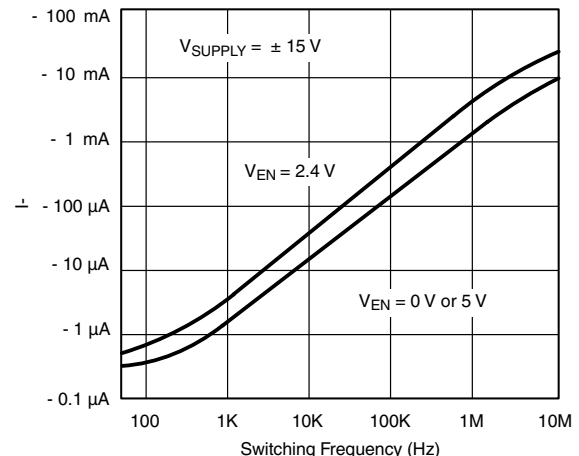
- Refer to PROCESS OPTION FLOWCHART.
- Room = 25 °C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.
- ΔR_{DS(on)} = R_{DS(on)} max. - R_{DS(on)} min.
- Worst case isolation occurs on channel 4 due to proximity to the drain pin.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source/Drain Capacitance vs. Analog Voltage

Drain Leakage Current vs. Source/Drain Voltage (Single 12 V Supply)

Drain Leakage Current vs. Source/Drain Voltage

Source Leakage Current vs. Source Voltage

Input Switching Threshold vs. Supply Voltage

Negative Supply Current vs. Switching Frequency

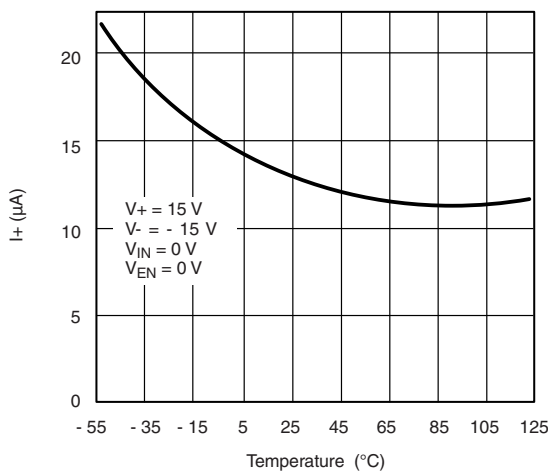
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Positive Supply Current vs. Switching Frequency



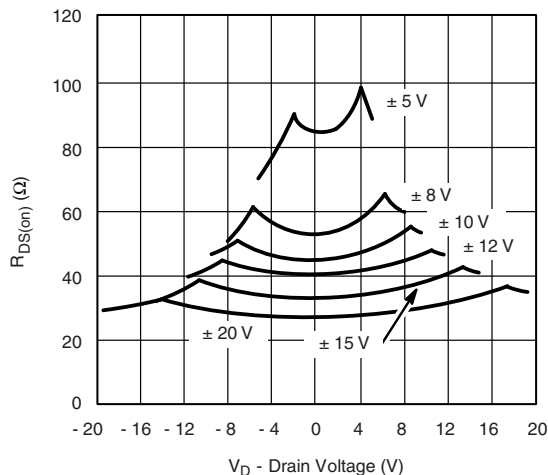
I_{SUPPLY} vs. Temperature



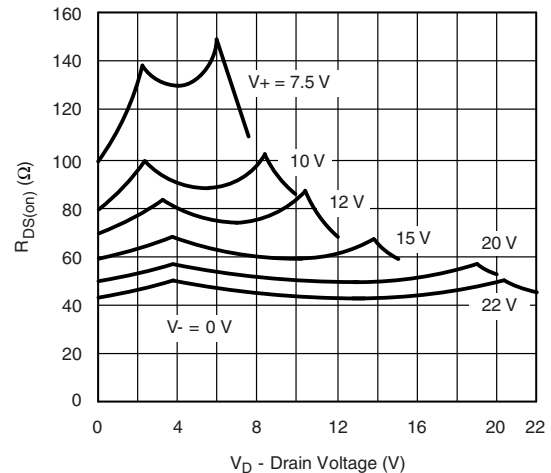
Positive Supply Current vs. Temperature (DG408)



Charge Injection vs. Analog Voltage



$R_{DS(on)}$ vs. V_D and Supply

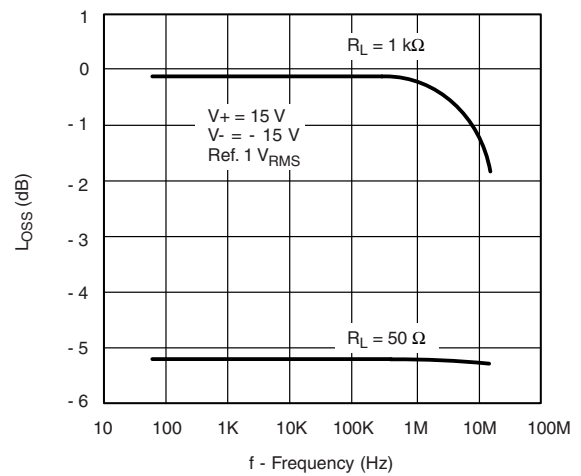


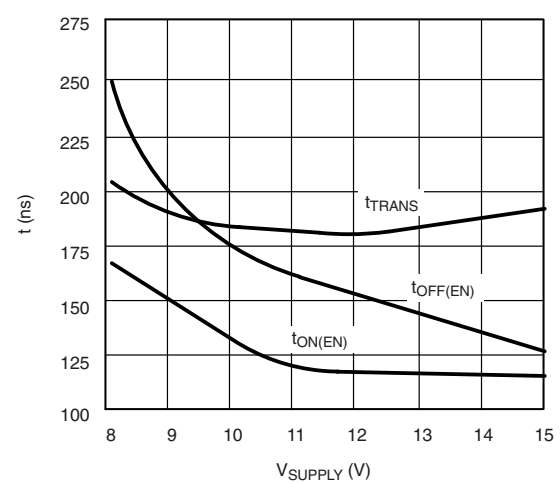
$R_{DS(on)}$ vs. V_D and Supply (Single Supply)

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

 $R_{DS(on)}$ vs. V_D and Temperature

 $R_{DS(on)}$ vs. V_D and Temperature (Single Supply)

Off Isolation and Crosstalk vs. Frequency

Insertion Loss vs. Frequency

Switching Time vs. Bipolar Supply

Switching Time vs. Single Supply

SCHEMATIC DIAGRAM (Typical Channel)



Fig. 1

TEST CIRCUITS

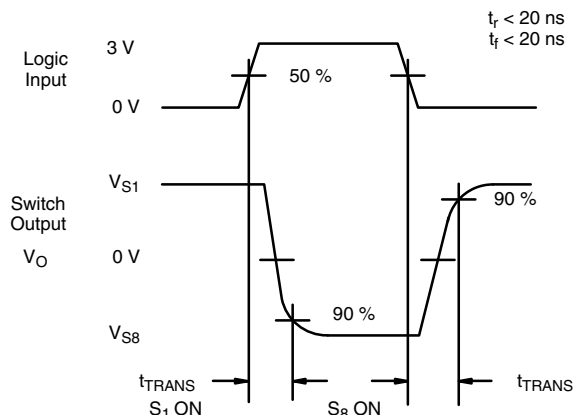
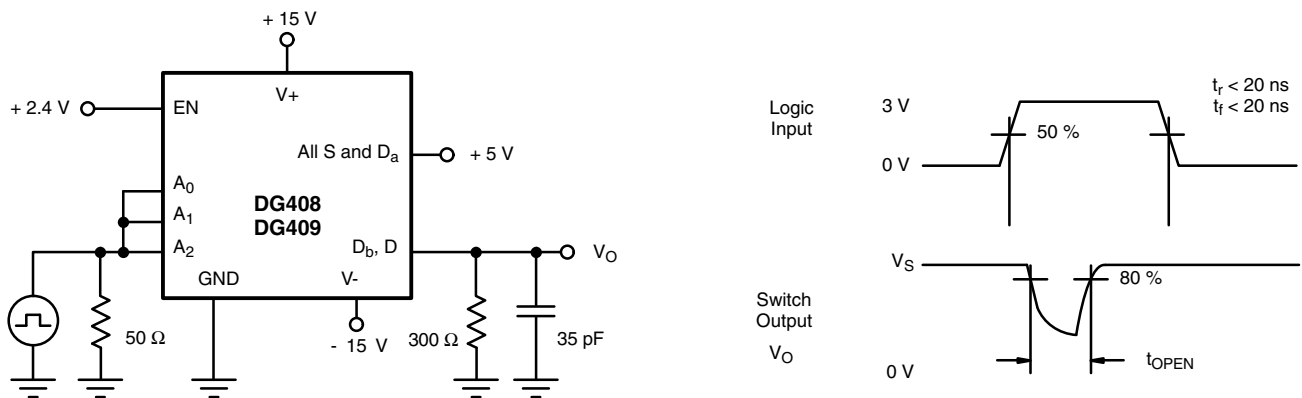


Fig. 2 - Transition Time

TEST CIRCUITS

Fig. 3 - Enable Switching Time

Fig. 4 - Break-Before-Make Interval

TEST CIRCUITS

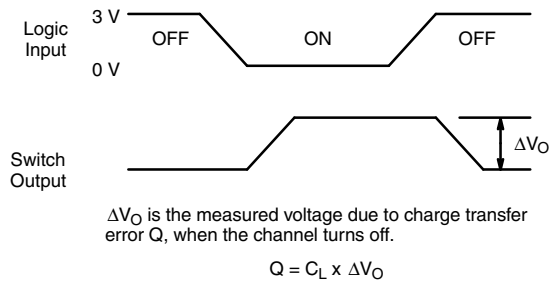
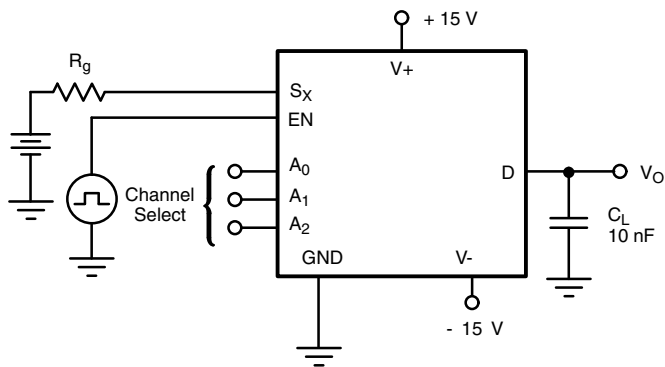


Fig. 5 - Charge Injection



Fig. 6 - Off Isolation

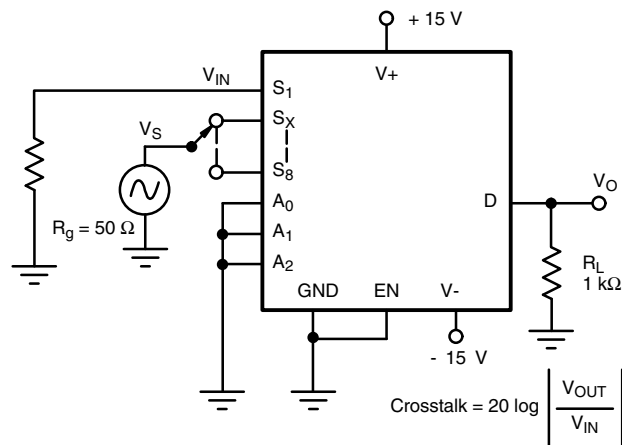


Fig. 7 - Crosstalk

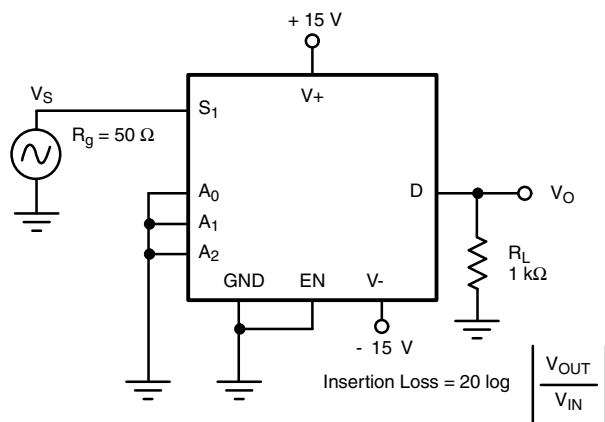


Fig. 8 - Insertion Loss

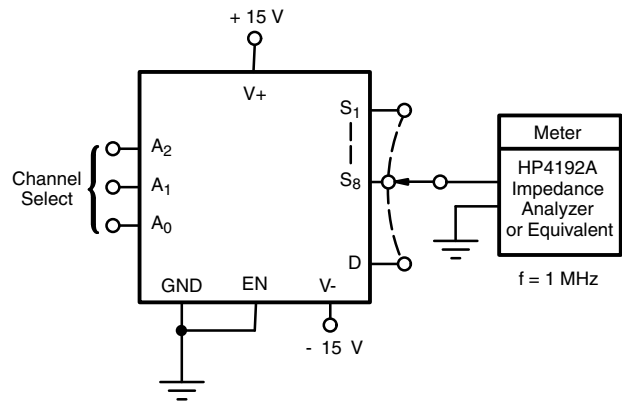


Fig. 9 - Source Drain Capacitance

APPLICATION HINTS

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see figure 10). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal $V+$ or $V-$ value. In this case the overvoltage signal actually becomes the power

supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference $V_S - (V-)$ does not exceed + 44 V. The addition of these diodes will reduce the analog signal range to 1 V below $V+$ and 1 V above $V-$, but it preserves the low channel resistance and low leakage characteristics.



Fig. 10 - Overvoltage Protection Using Blocking Diodes

8-Channel Sequential Multiplexer/Demultiplexer

Differential 4-Channel Sequential Multiplexer/Demultiplexer

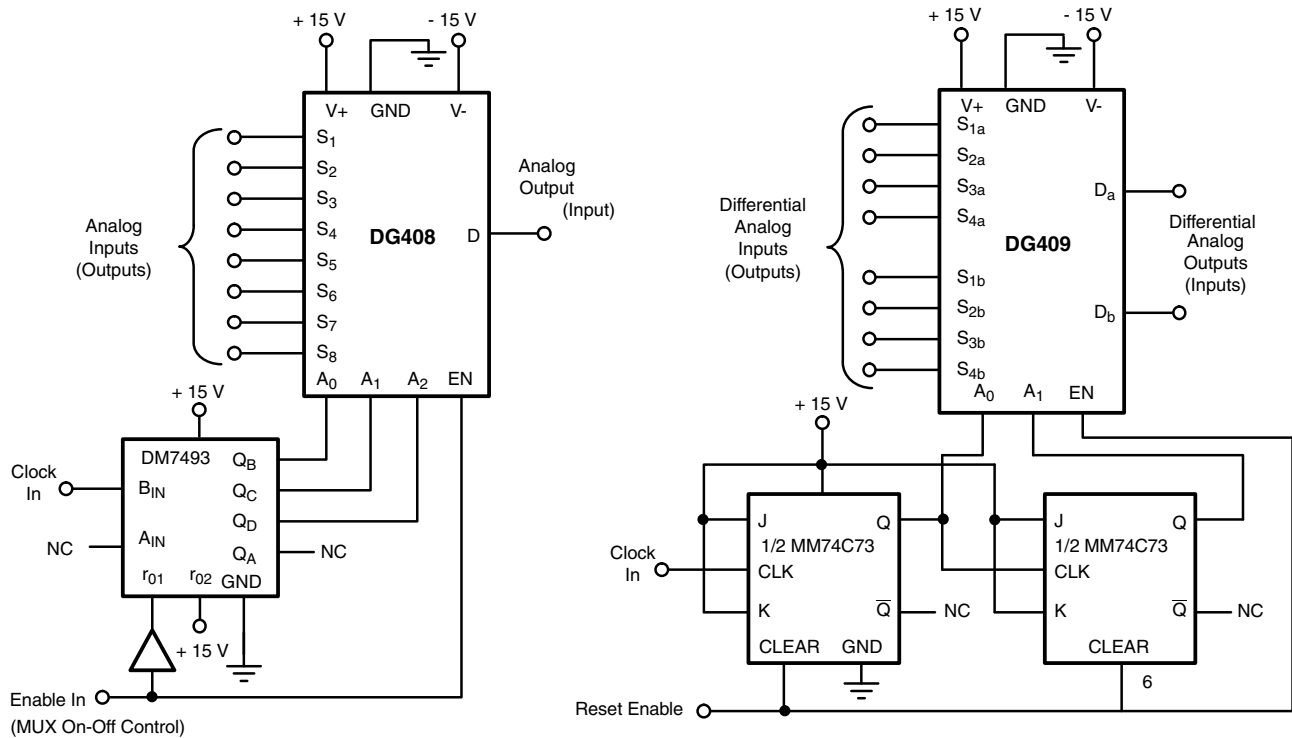


Fig. 11

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70062.



SOIC (NARROW): 16-LEAD
JEDEC Part Number: MS-012



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
∅	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



PDIP: 16-LEAD

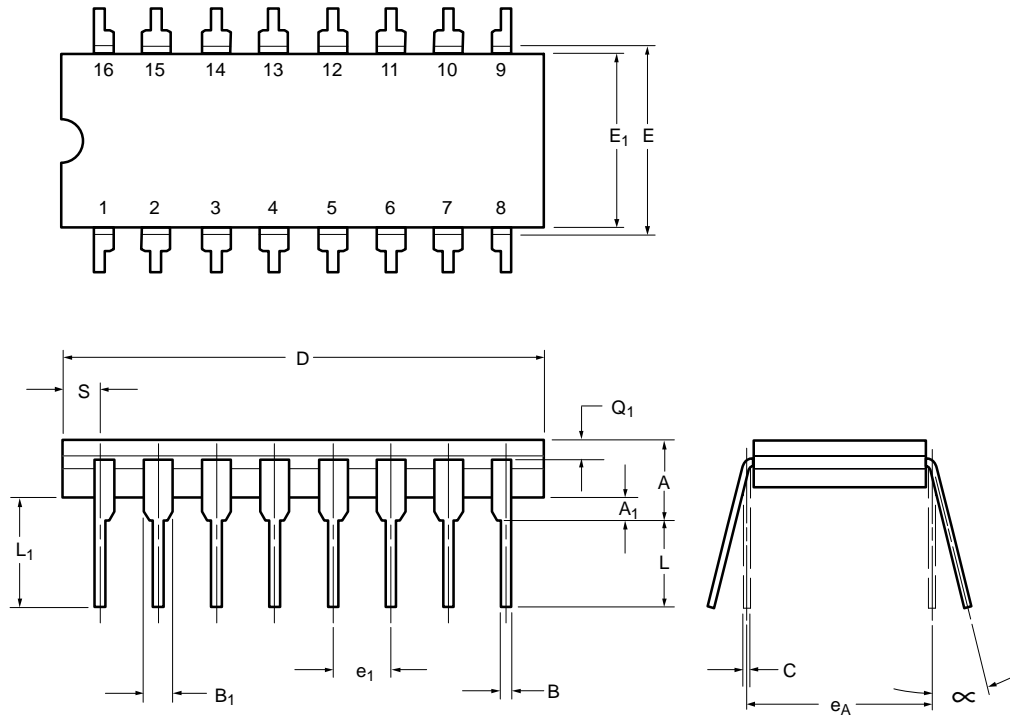


Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A₁	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B₁	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E₁	5.59	7.11	0.220	0.280
e₁	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q₁	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060

ECN: S-03946—Rev. D, 09-Jul-01
DWG: 5482



CERDIP: 16-LEAD

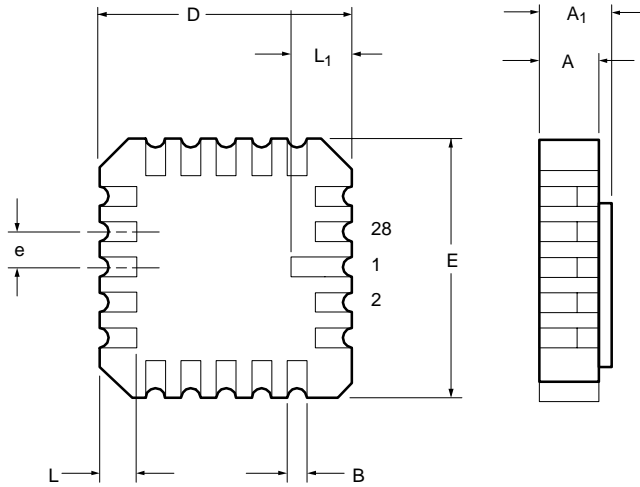


Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A ₁	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B ₁	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D	19.05	19.56	0.750	0.770
E	7.62	8.26	0.300	0.325
E ₁	6.60	7.62	0.260	0.300
e ₁	2.54 BSC		0.100 BSC	
e _A	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L ₁	3.81	5.08	0.150	0.200
Q ₁	1.27	2.16	0.050	0.085
S	0.38	1.14	0.015	0.045
∞	0°	15°	0°	15°

ECN: S-03946—Rev. G, 09-Jul-01
DWG: 5403



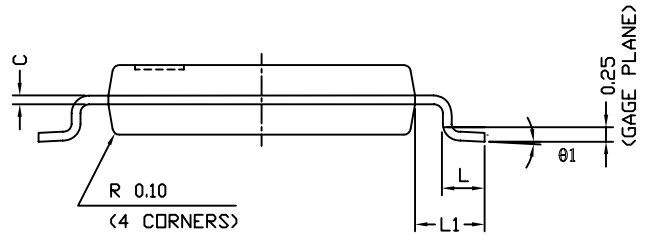
20-LEAD LCC



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.37	2.24	0.054	0.088
A₁	1.63	2.54	0.064	0.100
B	0.56	0.71	0.022	0.028
D	8.69	9.09	0.342	0.358
E	8.69	9.09	0.442	0.358
e	1.27 BSC		0.050 BSC	
L	1.14	1.40	0.045	0.055
L₁	1.96	2.36	0.077	0.093

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5321

TSSOP: 16-LEAD



Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
theta1	0°	3°	6°

ECN: S-61920-Rev. D, 23-Oct-06
DWG: 5624

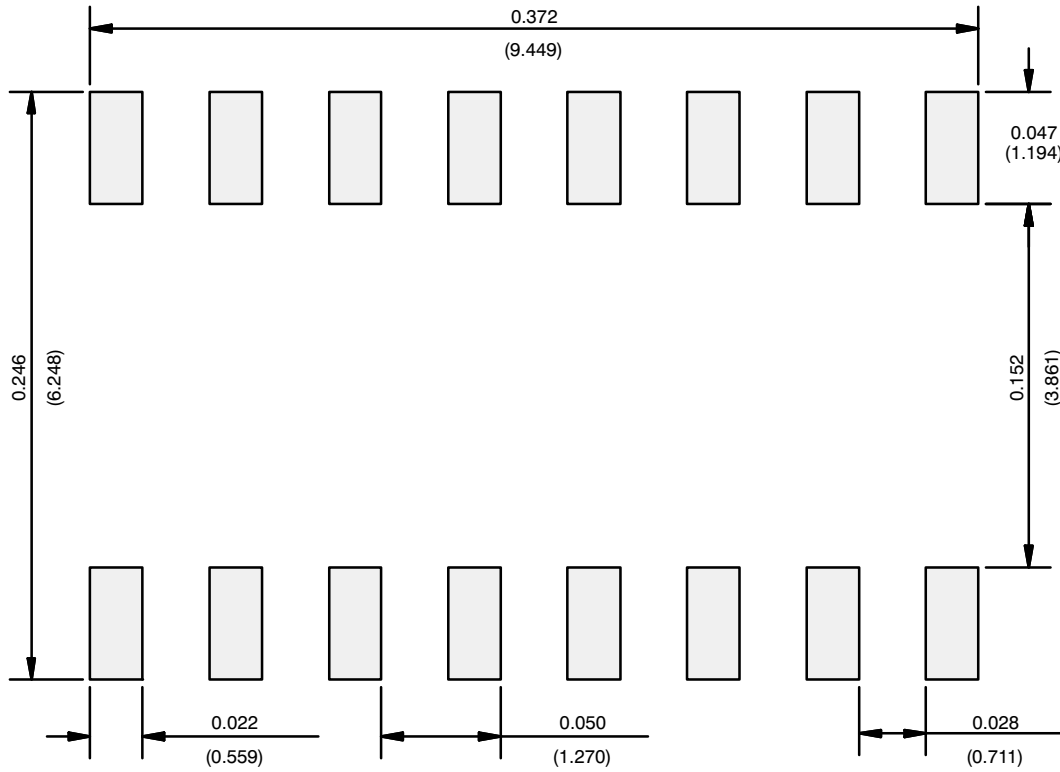


RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

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