

## MAX14941/MAX14942

## 5kV Isolated 20Mbps Half-Duplex PROFIBUS/ RS-485 Transceivers with $\pm 35\text{kV}$ ESD Protection

### General Description

The MAX14941/MAX14942 isolated RS-485/PROFIBUS-DP transceivers provide  $5000V_{RMS}$  (60s) of galvanic isolation between the cable-side (RS-485 driver/receiver-side) and the UART-side of the device. Isolation improves communication by breaking ground loops and reduces noise when there are large differences in ground potential between ports. These devices allow for robust communication up to 20Mbps.

An integrated LDO provides a simple and space-efficient architecture for providing power to the cable side of the IC.

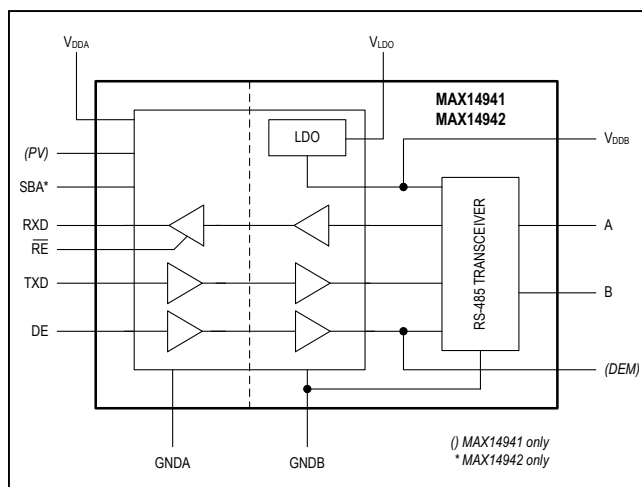
Each device includes one half-duplex driver/receiver channel. The receiver is 1/4-unit load, allowing up to 128 transceivers on a common bus.

Integrated true fail-safe circuitry ensures a logic-high on the receiver output when inputs are shorted or open. Undervoltage lockout disables the driver when cable-side or UART-side power supplies are below functional levels.

The driver outputs/receiver inputs are protected from  $\pm 35\text{kV}$  electrostatic discharge (ESD) to GNDB on the cable side, as specified by the Human Body Model (HBM).

The MAX14941/MAX14942 are available in a wide-body 16-pin SOIC package and operate over the  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$  temperature range.

### Functional Diagram



### Benefits and Features

- High-Performance Transceiver Enables Flexible Designs
  - Integrated LDO for Cable-Side Power
  - Compliant with RS-485 EIA/TIA-485 Standard
  - 20Mbps Maximum Data Rate
  - Allows Up to 128 Devices on the Bus
- Integrated Protections Ensures Robust Communication
  - $\pm 35\text{kV}$  ESD (HBM) on Driver Outputs/Receiver Inputs
  - $5\text{kV}_{RMS}$  Withstand Isolation Voltage for 60s ( $V_{ISO}$ )
  - $1200V_{PEAK}$  Maximum Repetitive Peak-Isolation Voltage ( $V_{IORM}$ )
  - $848V_{RMS}$  Maximum Working-Isolation Voltage ( $V_{IOWM}$ )
  - > 30 Years Lifetime at Rated Working Voltage
  - Withstands  $\pm 10\text{kV}$  Surge per IEC 61000-4-5
  - Thermal Shutdown

### Safety Regulatory Approvals Pending

- UL According to UL1577
- cUL According to CSA Bulletin 5A

### Applications

- Industrial Automation Equipment
- Programmable Logic Controllers
- HVAC
- Power Meters

Ordering Information appears at end of data sheet.

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**Absolute Maximum Ratings**

V <sub>DDA</sub> to GNDA .....	-0.3V to +6V	Continuous Power Dissipation (T <sub>A</sub> = +70°C) 16-pin W SOIC (derate 14.1mW/°C above +70°C) ..... 1126.8mW Operating Temperature Range..... -40°C to +105°C Junction Temperature..... +150°C Storage Temperature Range..... -65°C to +150°C Lead Temperature (soldering, 10s)..... +300°C Soldering Temperature (reflow)..... +260°C
V <sub>DDB</sub> to GNDB .....	-0.3V to +6V	
V <sub>LDO</sub> to GNDB .....	-0.3V to +16V	
TXD, DE, $\overline{RE}$ , PV to GNDA .....	-0.3V to +6V	
S $\overline{BA}$ , RXD to GNDA .....	-0.3V to (V <sub>DDA</sub> + 0.3V)	
DEM to GNDB .....	-0.3V to (V <sub>DDB</sub> + 0.3V)	
A, B to GNDB .....	-8V to +13V	
Short Circuit Duration (RXD, S $\overline{BA}$ to GNDA, A, B, DEM, V <sub>DDB</sub> to GNDB).....	Continuous	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Package Thermal Characteristics (Note 1)**

Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ) .....	71°C/W	Junction-to-Case Thermal Resistance (θ <sub>JC</sub> ).....	23°C/W
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**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

**DC Electrical Characteristics**

(V<sub>DDA</sub> – V<sub>GNDA</sub> = 1.71V to 5.5V, V<sub>DDB</sub> – V<sub>GNDB</sub> = 4.5V to 5.5V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V<sub>DDA</sub> – V<sub>GNDA</sub> = 3.3V, V<sub>DDB</sub> – V<sub>GNDB</sub> = 5V, V<sub>GNDA</sub> = V<sub>GNDB</sub>, and T<sub>A</sub> = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER</b>						
Supply Voltage	V <sub>DDA</sub>		1.71		5.5	V
	V <sub>DDB</sub>		4.5		5.5	
Supply Current	I <sub>DDA</sub>	V <sub>DDA</sub> = 5V, DE = high, $\overline{RE}$ = TXD = low, RXD unconnected, no bus load		4	6.6	mA
	I <sub>DDB</sub>	DE = high, $\overline{RE}$ = TXD = low, RXD unconnected, no bus load, V <sub>DDB</sub> = 5V		7.6	12.5	
Undervoltage Lockout Threshold	V <sub>UVLOA</sub>	V <sub>DDA</sub> rising	1.50	1.58	1.65	V
	V <sub>UVLOB</sub>	V <sub>DDB</sub> rising	2.55	2.7	2.85	
Undervoltage Lockout Threshold Hysteresis	V <sub>UVHYSTA</sub>			50		mV
	V <sub>UVHYSTB</sub>			200		
<b>LDO</b>						
LDO Supply Voltage	V <sub>LDO</sub>	Relative to GNDB, LDO is on (Note 4)	4.68		14	V
LDO Supply Current	I <sub>LDO</sub>	DE = high, TXD = low, no bus load, V <sub>LDO</sub> = 5V		7.7	12.9	mA
LDO Output Voltage	V <sub>DDB</sub>		4.5	5	5.5	V
LDO Current Limit				300		mA
Load Regulation		V <sub>LDO</sub> = 5.68V, I <sub>LOAD</sub> = 20mA to 40mA		0.19	1.7	mV/mA
Line Regulation		V <sub>LDO</sub> = 5.68V to 14V, I <sub>LOAD</sub> = 20mA		0.12	1.8	mV/V

**DC Electrical Characteristics (continued)**

( $V_{DDA} - V_{GNDA} = 1.71\text{V}$  to  $5.5\text{V}$ ,  $V_{DDB} - V_{GNDB} = 4.5\text{V}$  to  $5.5\text{V}$ ,  $T_A = T_{\text{MIN}}$  to  $T_{\text{MAX}}$ , unless otherwise noted. Typical values are at  $V_{DDA} - V_{GNDA} = 3.3\text{V}$ ,  $V_{DDB} - V_{GNDB} = 5\text{V}$ ,  $V_{GNDA} = V_{GNDB}$ , and  $T_A = +25^\circ\text{C}$ .) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dropout Voltage		$V_{LDO} = 4.68\text{V}$ , $I_{DDB} = 120\text{mA}$		100	180	mV
Load Capacitance		Nominal value (Note 8)	1		10	$\mu\text{F}$
<b>LOGIC INTERFACE (TXD, RXD, DE, <math>\overline{\text{RE}}</math>, <math>\overline{\text{SBA}}</math>, PV, DEM)</b>						
Input High Voltage	$V_{IH}$	$\overline{\text{RE}}$ , TXD, DE, PV to GNDA	$2.25\text{V} < V_{DDA} < 5.5\text{V}$	0.7 x $V_{DDA}$		V
			$1.71\text{V} < V_{DDA} < 1.89\text{V}$	0.78 x $V_{DDA}$		
Input Low Voltage	$V_{IL}$	$\overline{\text{RE}}$ , TXD, DE, PV to GNDA	$2.25\text{V} < V_{DDA} < 5.5\text{V}$	0.8		V
			$1.71\text{V} < V_{DDA} < 1.89\text{V}$	0.6		
Input Hysteresis	$V_{HYS}$	$\overline{\text{RE}}$ , TXD, DE, PV to GNDA		220		mV
Input Capacitance	$C_{IN}$	$\overline{\text{RE}}$ , TXD, DE, PV, $f = 1\text{MHz}$		2		pF
Input Pull-Up Current	$I_{PU}$	TXD, PV	-10	-4.5	-1.5	$\mu\text{A}$
Input Pull-Down Current	$I_{PD}$	DE, $\overline{\text{RE}}$	1.5	4.5	10	$\mu\text{A}$
$\overline{\text{SBA}}$ Pull-Up Resistance	$R_{SBA}$	MAX14942 only	3	5	8	k $\Omega$
Output Voltage High	$V_{OH}$	RXD to GNDA, $I_{OUT} = -4\text{mA}$	$V_{DDA} - 0.4$		V	
		MAX14941 only, DEM to GNDB, $I_{OUT} = -4\text{mA}$	$V_{DDB} - 0.4$			
Output Voltage Low	$V_{OL}$	RXD to GNDA, $I_{OUT} = 4\text{mA}$	0.40		V	
		MAX14941 only, DEM to GNDB, $I_{OUT} = 4\text{mA}$	0.40			
		MAX14942 only, $\overline{\text{SBA}}$ to GNDA, $I_{OUT} = 4\text{mA}$	0.45			
Short Circuit Output Pull-Up Current	$I_{SH\_PU}$	$0\text{V} \leq V_{RXD} \leq V_{DDA}$ , $\overline{\text{RE}} = \text{low}$	-42		mA	
		MAX14941 only, $0\text{V} \leq V_{DEM} \leq V_{DDB}$ , DE = high, PV = high	-42			
Short Circuit Output Pull-Down Current	$I_{SH\_PD}$	$0\text{V} \leq V_{RXD} \leq V_{DDA}$ , $\overline{\text{RE}} = \text{low}$	+40		mA	
		MAX14941 only, $0\text{V} \leq V_{DEM} \leq V_{DDB}$ , DE = low, PV = high	+40			
		MAX14942 only, $0\text{V} \leq V_{\overline{\text{SBA}}} \leq V_{DDA}$ , side B is powered and working	+60			
Tri-State Output Current	$I_{OZ}$	$0\text{V} \leq V_{RXD} \leq V_{DDA}$ , $\overline{\text{RE}} = \text{high}$	-1		+1	$\mu\text{A}$
<b>DRIVER</b>						
Differential Driver Output	$ V_{OD} $	$R_L = 54\Omega$ , TXD = high or low, Figure 1a	2.1		V	
		$R_L = 100\Omega$ , TXD = high or low, Figure 1a	2.9			
		$-7\text{V} \leq V_{CM} \leq +12\text{V}$ , Figure 1b	1.5			5

**DC Electrical Characteristics (continued)**

( $V_{DDA} - V_{GNDA} = 1.71\text{V}$  to  $5.5\text{V}$ ,  $V_{DDB} - V_{GNDB} = 4.5\text{V}$  to  $5.5\text{V}$ ,  $T_A = T_{\text{MIN}}$  to  $T_{\text{MAX}}$ , unless otherwise noted. Typical values are at  $V_{DDA} - V_{GNDA} = 3.3\text{V}$ ,  $V_{DDB} - V_{GNDB} = 5\text{V}$ ,  $V_{GNDA} = V_{GNDB}$ , and  $T_A = +25^\circ\text{C}$ .) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Driver Peak-to-Peak Output	$V_{\text{ODPP}}$	Figure 2 (Note 5)	4.0		6.8	V
Change in Magnitude of Differential Driver Output Voltage	$\Delta V_{\text{OD}}$	$R_L = 54\Omega$ (Note 6)	-0.2		+0.2	V
Driver Common Mode Output Voltage	$V_{\text{OC}}$	$R_L = 54\Omega$ , Figure 1a		1.8	3	V
Change in Magnitude of Common-Mode Voltage	$\Delta V_{\text{OC}}$	$R_L = 54\Omega$ , Figure 1a (Note 6)	-0.2		+0.2	V
Driver Short-Circuit Output Current	$I_{\text{OSD}}$	$\text{GNDB} \leq V_{\text{OUT}} \leq +12\text{V}$ , output low (Note 7)			+250	mA
		$-7\text{V} \leq V_{\text{OUT}} \leq V_{\text{DDB}}$ , output high (Note 7)	-250			
Driver Short-Circuit Foldback Output Current	$I_{\text{OSDF}}$	$(V_{\text{DDB}} - 1\text{V}) \leq V_{\text{OUT}} \leq +12\text{V}$ , output low (Note 7, 8)	+15			mA
		$-7\text{V} \leq V_{\text{OUT}} \leq +1\text{V}$ , output high (Note 7, 8)			-15	
<b>RECEIVER</b>						
Input Current (A and B)	$I_A, I_B$	DE = low, $V_{\text{DDB}} = \text{GNDB}$ or $5.5\text{V}$	$V_{\text{IN}} = +12\text{V}$		+250	$\mu\text{A}$
			$V_{\text{IN}} = -7\text{V}$	-200		
Receiver Differential Threshold Voltage	$V_{\text{TH}}$	$-7\text{V} \leq V_{\text{CM}} \leq +12\text{V}$	-200	-125	-50	mV
Receiver Input Hysteresis	$\Delta V_{\text{TH}}$	$V_{\text{CM}} = 0\text{V}$		15		mV
Receiver Input Resistance	$R_{\text{IN}}$	$-7\text{V} \leq V_{\text{CM}} \leq +12\text{V}$ , DE = low	48			$\text{k}\Omega$
Differential Input Capacitance	$C_{A,B}$	Measured between A and B, DE = $\overline{\text{RE}}$ = low at 6MHz		8		pF
<b>PROTECTION</b>						
Thermal-Shutdown Threshold	$T_{\text{SHDN}}$	Temperature Rising		+160		$^\circ\text{C}$
Thermal-Shutdown Hysteresis	$T_{\text{HYST}}$			15		$^\circ\text{C}$
ESD Protection (A and B Pins to GNDB)		Human Body Model		$\pm 35$		kV
		IEC 61000-4-2 Air Gap Discharge		$\pm 12$		
		IEC 61000-4-2 Contact Discharge		$\pm 10$		
ESD Protection (All Other Pins)		Human Body Model		$\pm 4$		kV

## Switching Electrical Characteristics

( $V_{DDA} - V_{GNDA} = 1.71\text{V}$  to  $5.5\text{V}$ ,  $V_{DDB} - V_{GNDB} = 4.5\text{V}$  to  $5.5\text{V}$ ,  $T_A = T_{\text{MIN}}$  to  $T_{\text{MAX}}$ , unless otherwise noted. Typical values are at  $V_{DDA} - V_{GNDA} = 3.3\text{V}$ ,  $V_{DDB} - V_{GNDB} = 5\text{V}$ ,  $V_{GNDA} = V_{GNDB}$ , and  $T_A = +25^\circ\text{C}$ .) (Note 8)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DYNAMIC</b>						
Common Mode Transient Immunity	CMTI	(Note 9)		35		kV/ $\mu\text{s}$
Glitch Rejection		TXD, DE, RXD	10	17	29	ns
<b>DRIVER</b>						
Driver Propagation Delay	$t_{\text{DPLH}}$ , $t_{\text{DPHL}}$	$R_L = 54\Omega$ , $C_L = 50\text{pF}$ , Figure 3 and Figure 4			68	ns
Differential Driver Output Skew $ t_{\text{DPLH}} - t_{\text{DPHL}} $	$t_{\text{DSKEW}}$	$R_L = 54\Omega$ , $C_L = 50\text{pF}$ , Figure 3 and Figure 4			6	ns
Driver Differential Output Rise or Fall Time	$t_{\text{LH}}$ , $t_{\text{HL}}$	$R_L = 54\Omega$ , $C_L = 50\text{pF}$ , Figure 3 and 4			15	ns
Maximum Data Rate	DRMAX		20			Mbps
Driver Enable to Output High	$t_{\text{DZH}}$	$R_L = 500\Omega$ , $C_L = 50\text{pF}$ , Figure 5			88	ns
Driver Enable to Output Low	$t_{\text{DZL}}$	$R_L = 500\Omega$ , $C_L = 50\text{pF}$ , Figure 6			88	ns
Driver Disable Time from Low	$t_{\text{DLZ}}$	$R_L = 500\Omega$ , $C_L = 50\text{pF}$ , Figure 6			80	ns
Driver Disable Time from High	$t_{\text{DHZ}}$	$R_L = 500\Omega$ , $C_L = 50\text{pF}$ , Figure 5			80	ns
<b>RECEIVER</b>						
Receiver Propagation Delay	$t_{\text{RPLH}}$ , $t_{\text{RPHL}}$	$C_L = 15\text{pF}$ , Figure 7 and 8 (Note 10)			68	ns
Receiver Output Skew $ t_{\text{RPLH}} - t_{\text{RPHL}} $	$t_{\text{RSKEW}}$	$C_L = 15\text{pF}$ , Figure 7 and 8 (Note 10)			6	ns
Maximum Data Rate	DRMAX		20			Mbps
Receiver Enable to Output High	$t_{\text{RZH}}$	$R_L = 1\text{k}\Omega$ , $C_L = 15\text{pF}$ , S2 closed, Figure 9			20	ns
Receiver Enable to Output Low	$t_{\text{RZL}}$	$R_L = 1\text{k}\Omega$ , $C_L = 15\text{pF}$ , S1 closed, Figure 9			30	ns
Receiver Disable Time From Low	$t_{\text{RLZ}}$	$R_L = 1\text{k}\Omega$ , $C_L = 15\text{pF}$ , S1 closed, Figure 9			20	ns
Receiver Disable Time From High	$t_{\text{RHZ}}$	$R_L = 1\text{k}\Omega$ , $C_L = 15\text{pF}$ , S2 closed, Figure 9			20	ns

**Note 2:** All devices are 100% production tested at  $T_A = +25^\circ\text{C}$ . Specifications over temperature are guaranteed by design.

**Note 3:** All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or GNDB), unless otherwise noted.

**Note 4:**  $V_{\text{LDO max}}$  indicates voltage capability of the circuit. Power dissipation requirements may limit  $V_{\text{LDO max}}$  to a lower value.

**Note 5:**  $V_{\text{ODPP}}$  is the difference in  $V_{\text{OD}}$  when TXD is high and when TXD is low.

**Note 6:**  $\Delta V_{\text{OD}}$  and  $\Delta V_{\text{OC}}$  are the changes in  $V_{\text{OD}}$  and  $V_{\text{OC}}$ , respectively, when the TXD input changes state.

**Note 7:** The short circuit output current applies to the peak current just prior to current limiting.

**Note 8:** Not production tested. Guaranteed by design.

**Note 9:** CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output states. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB.  $\Delta V_{\text{CM}} = 1\text{kV}$ .

**Note 10:** Capacitive load includes test probe and fixture capacitance.

**Insulation Characteristics**

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	$V_{PR}$	Method B1 = $V_{IORM} \times 1.875$ ( $t = 1s$ , partial discharge < 5pC)	2250	$V_P$
Maximum Repetitive Peak Isolation Voltage	$V_{IORM}$	(Note 11)	1200	V
Maximum Working Isolation Voltage	$V_{IOWM}$	(Note 11)	848	$V_{RMS}$
Maximum Transient Isolation Voltage	$V_{IOTM}$	$t = 1s$	8400	$V_P$
Maximum Withstand Isolation Voltage	$V_{ISO}$	$t = 60s, f = 60Hz$ (Note 11, 12)	5000	$V_{RMS}$
Maximum Surge Isolation Voltage	$V_{ISOM}$	IEC 61000-4-5, 1.2/50 $\mu s$	10	kV
Insulation Resistance	$R_S$	$T_A = +150^\circ C, V_{IO} = 500V$	> $10^9$	$\Omega$
Barrier Capacitance Input-to-Output	CIO	$f = 1MHz$	2	pF
Minimum Creepage Distance	CPG	Wide SOIC	8	mm
Minimum Clearance Distance	CLR	Wide SOIC	8	mm
Internal Clearance		Distance through insulation	0.015	mm
Comparative Tracking Resistance Index	CTI	Material Group II (IEC 60112)	575	
Climatic Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

**Note 11:**  $V_{IORM}$ ,  $V_{IOWM}$ , and  $V_{ISO}$  are defined by the IEC 60747-5-5 standard.

**Note 12:** Product is qualified at  $V_{ISO}$  for 60 seconds. 100% production tested at 120% of  $V_{ISO}$  for 1 second.

**Safety Regulatory Approvals**

<b>UL</b>
The MAX14941/MAX14942 is certified under UL1577. For more details, see File E351759.
Rate up to $5000V_{RMS}$ isolation voltage for basic insulation.
<b>cUL</b>
The MAX14941/MAX14942 is certified under UL1577. For more details, see File E351759. Rate up to $5000V_{RMS}$ isolation voltage for basic insulation.

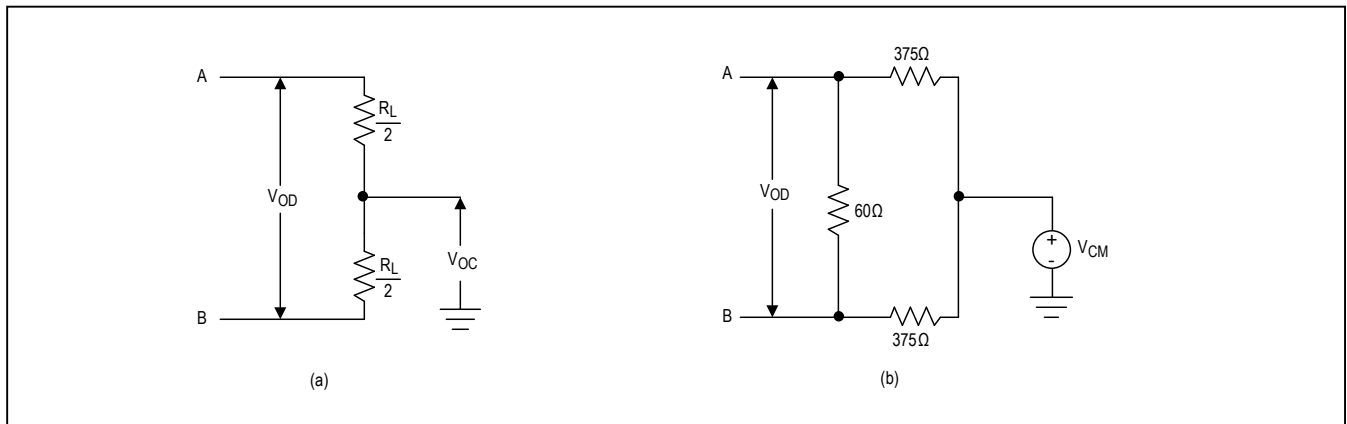


Figure 1. Driver DC Test Load

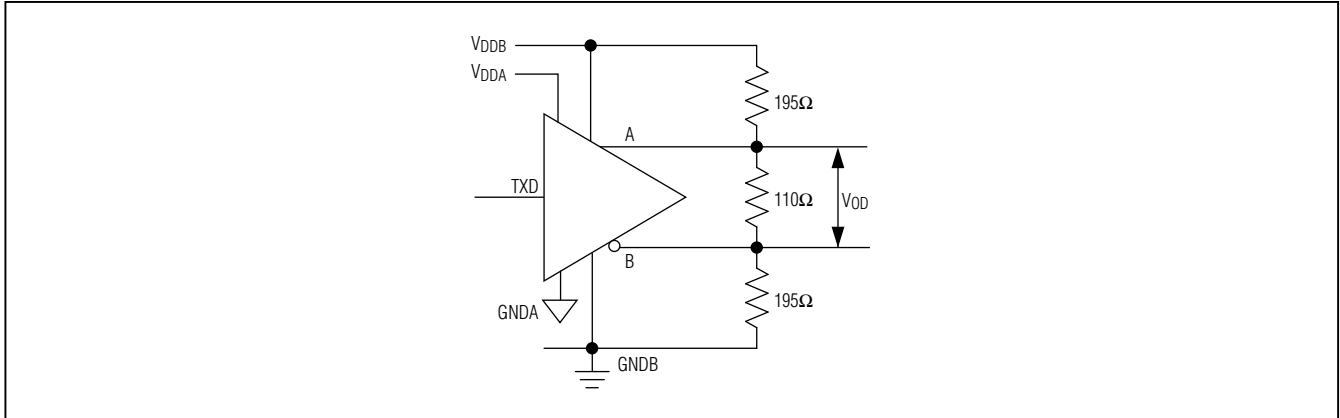


Figure 2.  $V_{ODPP}$  Swing Under Profibus Equivalent Load Test

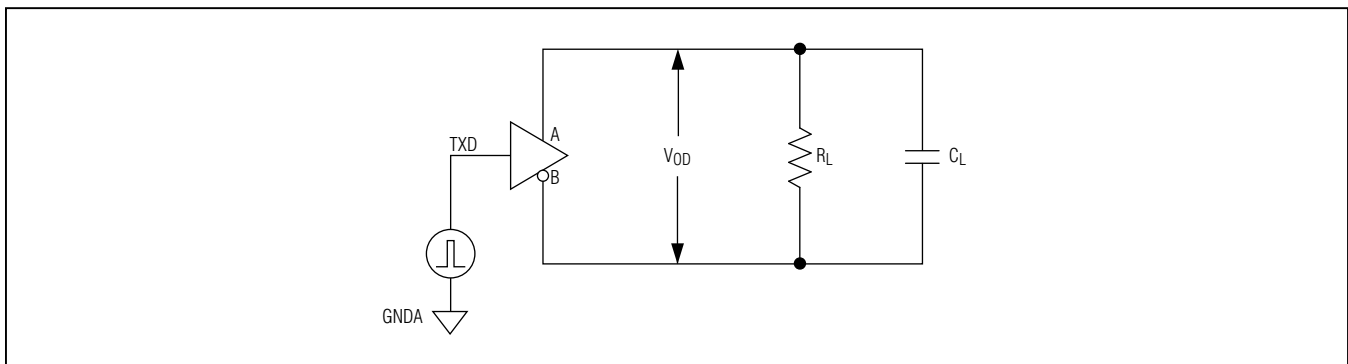


Figure 3. Driver Timing Test Circuit

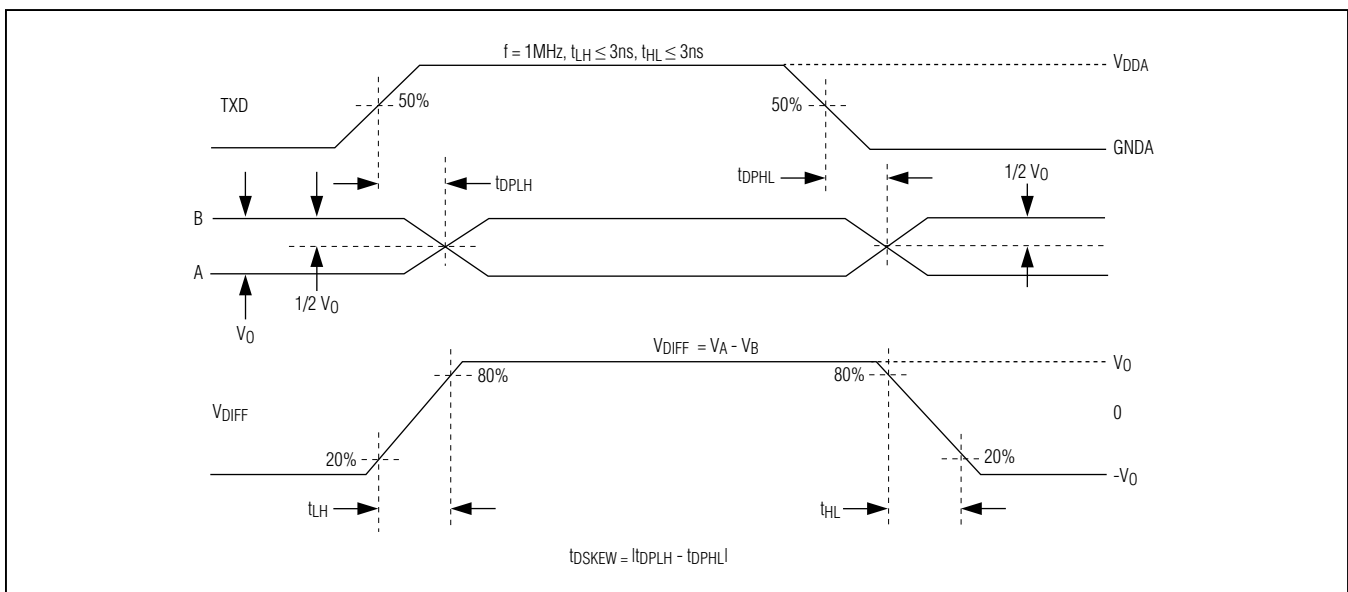


Figure 4. Driver Propagation Delays

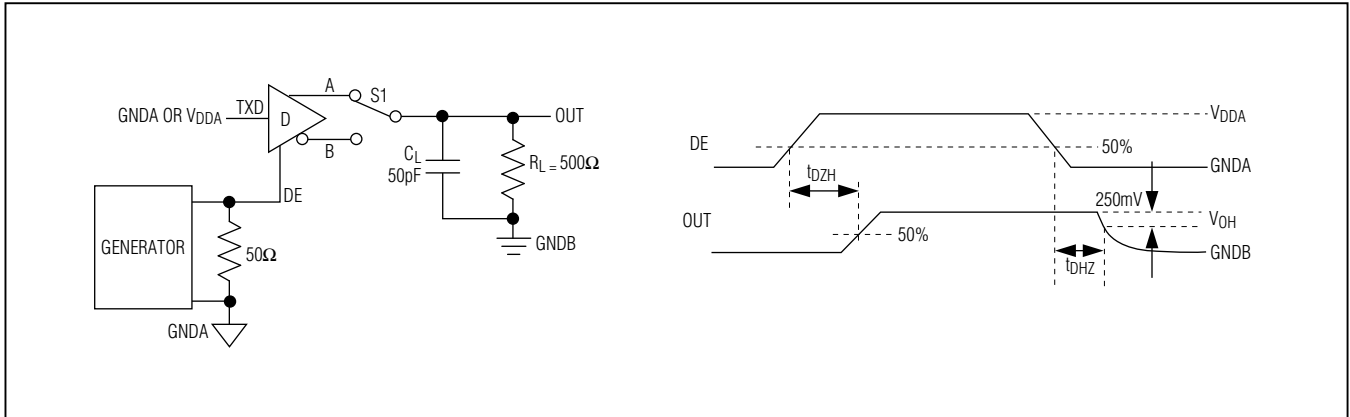


Figure 5. Driver Enable and Disable Times ( $t_{DZH}$ ,  $t_{DZL}$ )

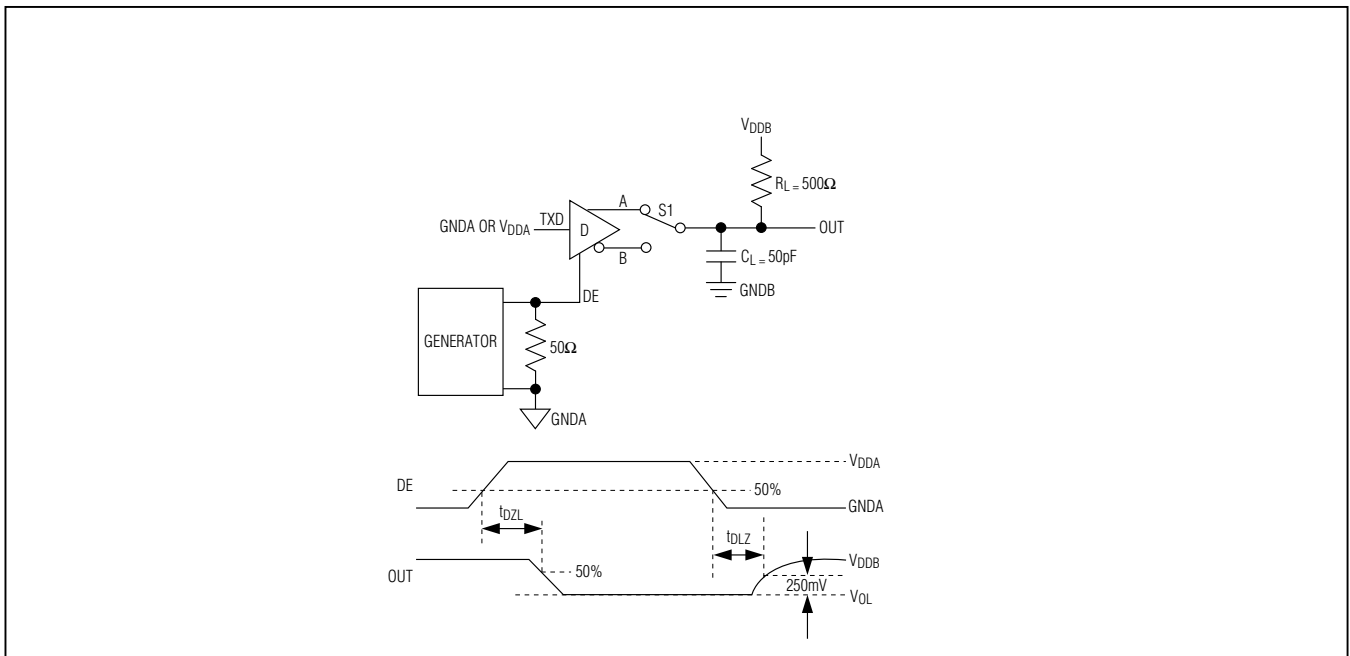


Figure 6. Driver Enable and Disable Times ( $t_{DZL}$ ,  $t_{DZL}$ )

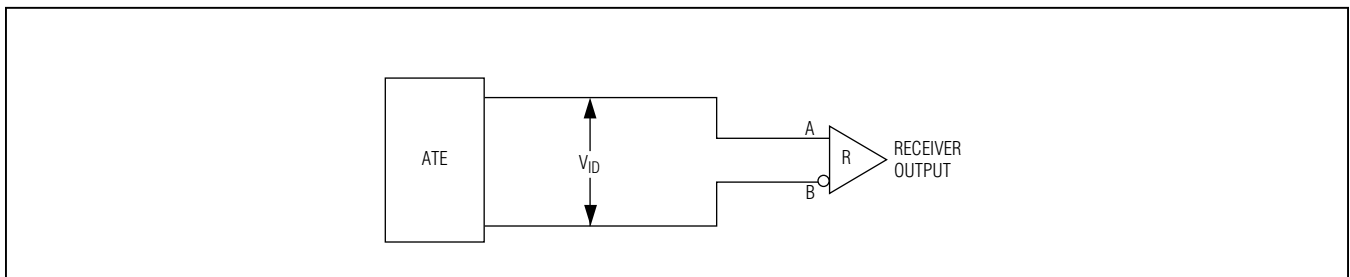


Figure 7. Receiver Propagation Delay Test Circuit



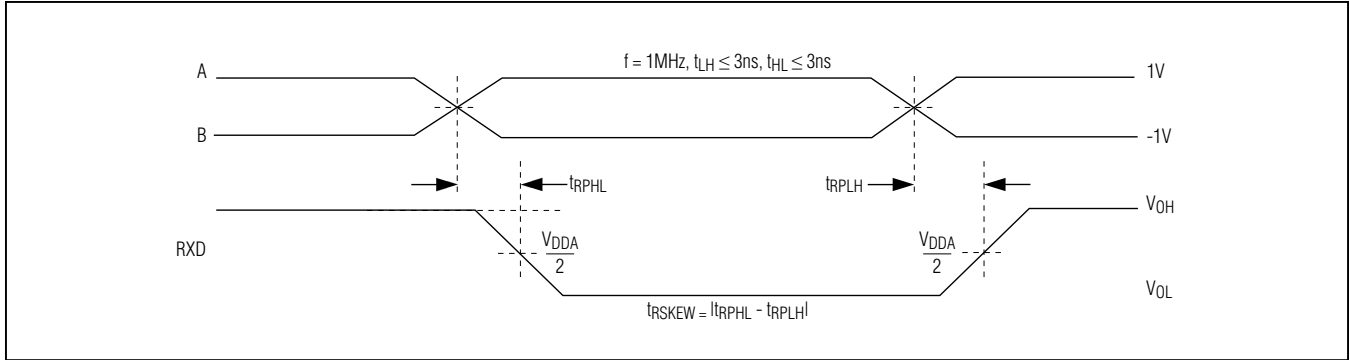


Figure 8. Receiver Propagation Delays

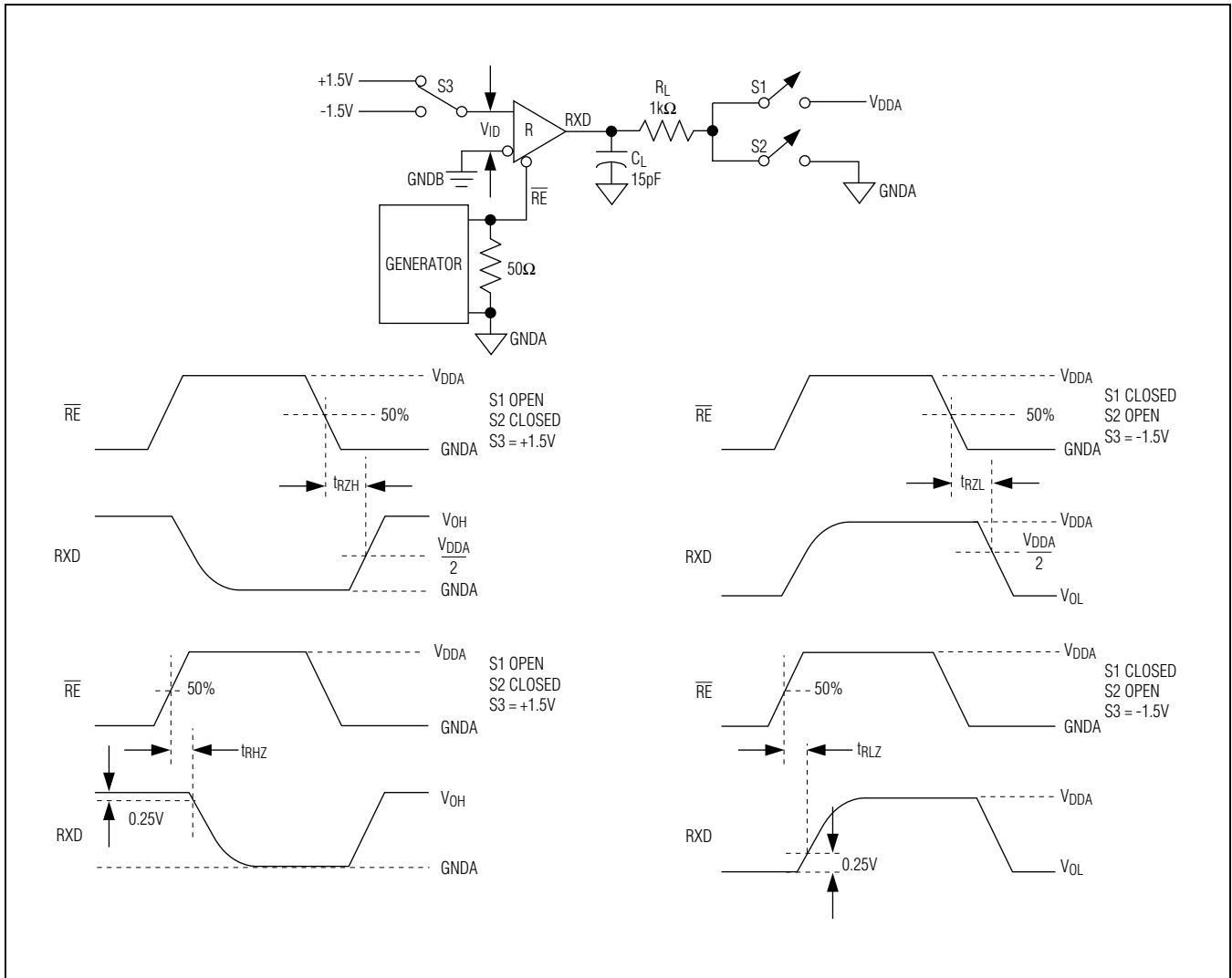
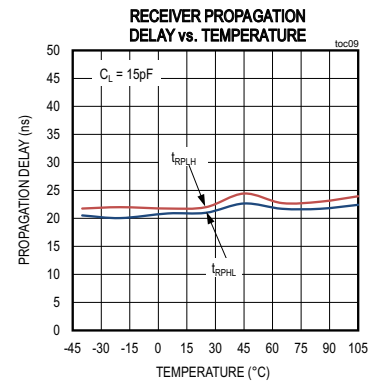
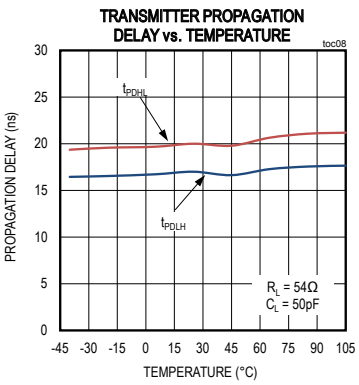
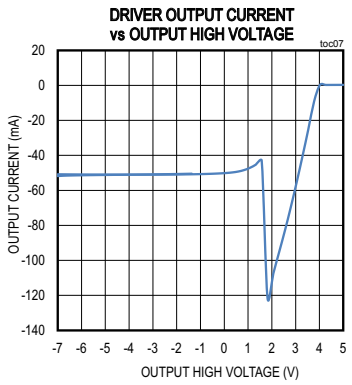
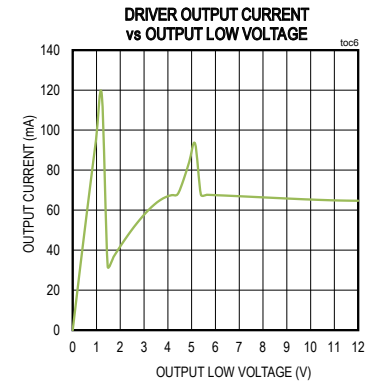
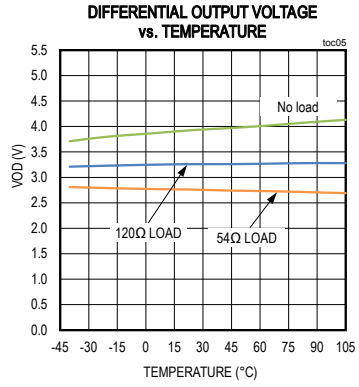
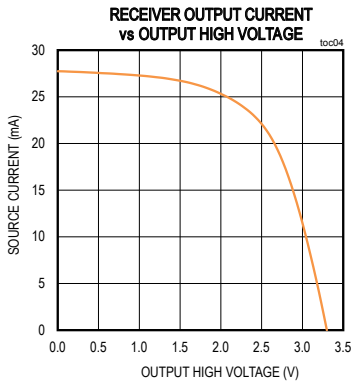
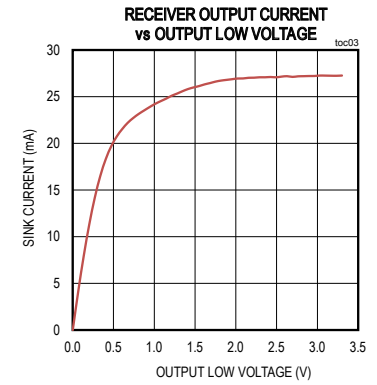
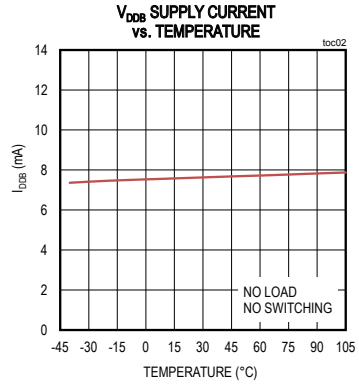
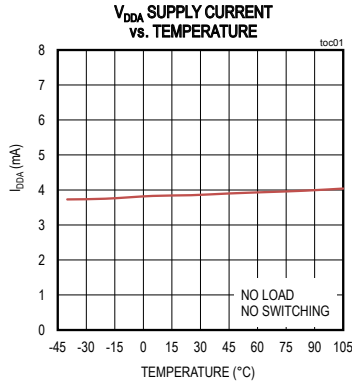


Figure 9. Receiver Enable and Disable Times

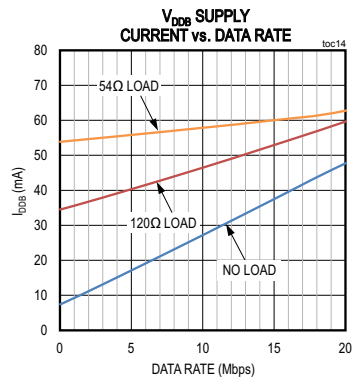
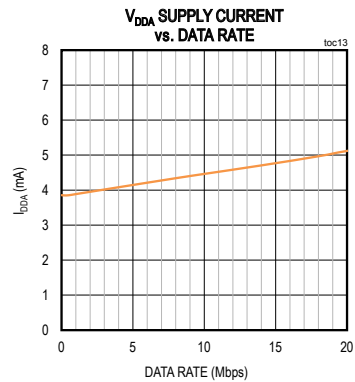
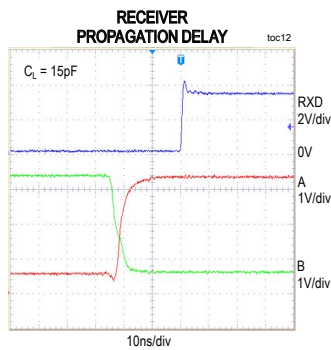
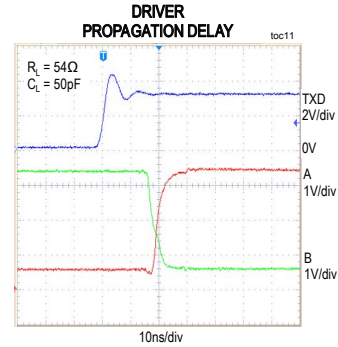
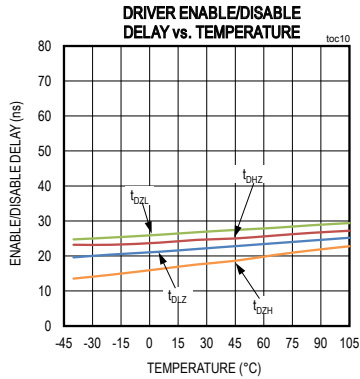
Typical Operating Characteristics

( $V_{DDA} - V_{GNDA} = 3.3V$ ,  $V_{DDB} - V_{GNDB} = 5V$ ,  $V_{GNDA} = V_{GNDB}$ , and  $T_A = +25^\circ C$ , unless otherwise noted.)

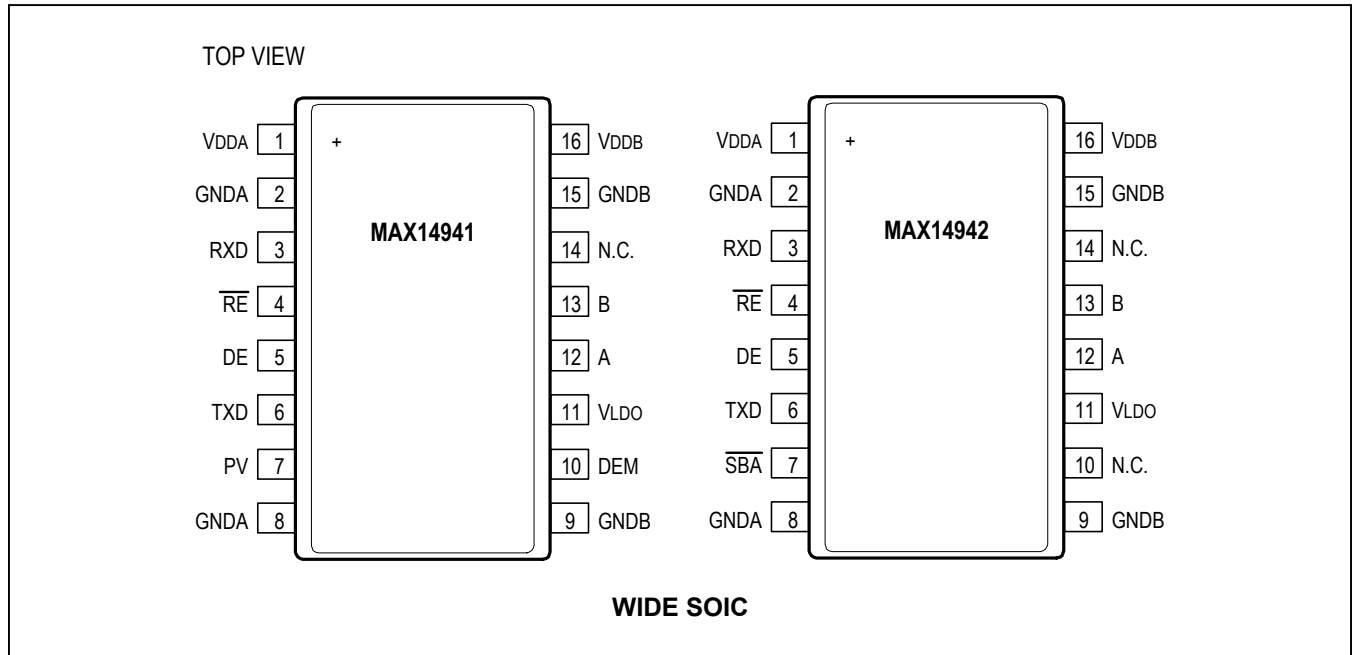


Typical Operating Characteristics (continued)

( $V_{DDA} - V_{GNDA} = 3.3V$ ,  $V_{DDB} - V_{GNDB} = 5V$ ,  $V_{GNDA} = V_{GNDB}$ , and  $T_A = +25^\circ C$ , unless otherwise noted.)



Pin Configuration



Pin Description

PIN		NAME	REFERENCE	FUNCTION
MAX14941	MAX14942			
1	1	VDDA	GNDA	UART/Logic-Side Power Input. Bypass VDDA to GNDA with both 0.1µF and 1µF capacitors as close to the device as possible.
2, 8	2, 8	GNDA	-	UART/Logic-Side Ground. GNDA is the ground reference for digital signals.
3	3	RXD	GNDA	Receiver Data Output. Drive $\overline{RE}$ low to enable RXD. With $\overline{RE}$ low, RXD is high when $(V_A - V_B) > -50mV$ and is low when $(V_A - V_B) < -200mV$ . RXD is high when VDDB is less than VUVLOB. RXD is high impedance when $\overline{RE}$ is high.
4	4	$\overline{RE}$	GNDA	Receiver Output Enable. Drive $\overline{RE}$ low or connect to GNDA to enable RXD. Drive $\overline{RE}$ high to disable RXD. RXD is high-impedance when $\overline{RE}$ is high. $\overline{RE}$ has an internal 4.5µA pull-down to GNDA.
5	5	DE	GNDA	Driver Output Enable. Drive DE high to enable bus driver outputs A and B. Drive DE low or connect to GNDA to disable A and B. A and B are high impedance when DE is low. DE has an internal 4.5µA pull-down to GNDA.
6	6	TXD	GNDA	Driver Input. With DE high, a low on TXD forces the noninverting output (A) low and the inverting output (B) high. Similarly, a high on TXD forces the noninverting output high and the inverting output low. TXD has an internal 4.5µA pull-up to VDDA.

## Pin Description (continued)

PIN		NAME	REFERENCE	FUNCTION
MAX14941	MAX14942			
7	-	PV	GNDA	Power Valid Input. Hold PV low to disable the driver while the supplies stabilize. Pull PV high when power is stable to enable the driver. PV has an internal $4.5\mu\text{A}$ pull-up to $V_{DDA}$ .
-	7	$\overline{\text{SBA}}$	GNDA	Side B Active Indicator Output. $\overline{\text{SBA}}$ asserts low when side B is powered and working. $\overline{\text{SBA}}$ has an internal $5\text{k}\Omega$ pull-up resistor to $V_{DDA}$ .
9, 15	9, 15	GNDB	-	Cable-Side Ground. GNDB is the ground reference for the internal LDO, the DEM output, and the Profibus/RS-485 bus signals.
10	-	DEM	GNDB	Driver Enable Monitor Output. DEM is high when the transmitter is enabled. See the <a href="#">Function Tables</a> for more information.
14	10, 14	N.C.	-	No Connection. Not internally-connected.
11	11	$V_{LDO}$	GNDB	LDO Power Input. Connect a minimum voltage of $4.68\text{V}$ to $V_{LDO}$ to power the cable-side of the transceiver. Bypass $V_{LDO}$ to GNDB with both $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors as close to the device as possible. To disable the internal LDO, leave $V_{LDO}$ unconnected or connect to GNDB.
12	12	A	GNDB	Noninverting Receiver Input and Noninverting Driver Output
13	13	B	GNDB	Inverting Receiver Input and Inverting Driver Output
16	16	$V_{DDB}$	GNDB	Cable-Side Power Input/Isolated LDO Power Output. Bypass $V_{DDB}$ to GNDB with both $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitor as close to the device as possible. $V_{DDB}$ is the output of the internal LDO when power is applied to $V_{LDO}$ . When the internal LDO is not used ( $V_{LDO}$ is unconnected or connected to GNDB), $V_{DDB}$ is the positive supply input for the cable-side of the IC.

Function Tables

TRANSMITTING							
INPUTS					OUTPUTS		
V <sub>DDA</sub>	V <sub>DDB</sub>	DE	TXD	PV**	A	B	DEM**
≥ V <sub>UVLOA</sub>	≥ V <sub>UVLOB</sub>	1	X	0	High-Z	High-Z	1
≥ V <sub>UVLOA</sub>	≥ V <sub>UVLOB</sub>	1	1	1	1	0	1
≥ V <sub>UVLOA</sub>	≥ V <sub>UVLOB</sub>	1	0	1	0	1	1
≥ V <sub>UVLOA</sub>	≥ V <sub>UVLOB</sub>	0	X	X	High-Z	High-Z	0
< V <sub>UVLOA</sub>	≥ V <sub>UVLOB</sub>	X	X	X	High-Z	High-Z	0
≥ V <sub>UVLOA</sub>	< V <sub>UVLOB</sub>	X	X	X	High-Z	High-Z	0
< V <sub>UVLOA</sub>	< V <sub>UVLOB</sub>	X	X	X	High-Z	High-Z	0

\*Note: Drive DE low to disable the transmitter outputs. Drive DE high to enable the transmitter outputs. DE has an internal pull-down to GNDA.

\*\* MAX14941 only, X = Don't care

RECEIVING				
INPUTS				OUTPUTS
V <sub>DDA</sub>	V <sub>DDB</sub>	RE	(V <sub>A</sub> - V <sub>B</sub> )	RXD
≥ V <sub>UVLOA</sub>	≥ V <sub>UVLOB</sub>	0	> -50mV	1
≥ V <sub>UVLOA</sub>	≥ V <sub>UVLOB</sub>	0	< -200mV	0
≥ V <sub>UVLOA</sub>	≥ V <sub>UVLOB</sub>	0	Open/Short	1
≥ V <sub>UVLOA</sub>	≥ V <sub>UVLOB</sub>	1	X	High-Z
< V <sub>UVLOA</sub>	≥ V <sub>UVLOB</sub>	X	X	High-Z
≥ V <sub>UVLOA</sub>	< V <sub>UVLOB</sub>	0	X	1
< V <sub>UVLOA</sub>	< V <sub>UVLOB</sub>	X	X	High-Z

\*Note: Drive RE high to disable the receiver output. Drive RE low to enable to receiver output. RE has an internal pull-down to GNDA.

X = Don't care

SBA		
V <sub>DDA</sub>	V <sub>DDB</sub>	SBA
< V <sub>UVLOA</sub>	< V <sub>UVLOB</sub>	High
< V <sub>UVLOA</sub>	≥ V <sub>UVLOB</sub>	High
≥ V <sub>UVLOA</sub>	< V <sub>UVLOB</sub>	High
≥ V <sub>UVLOA</sub>	≥ V <sub>UVLOB</sub>	Low

## Detailed Description

The MAX14941/MAX14942 isolated PROFIBUS-DP/RS-485 transceivers provide  $2500\text{V}_{\text{RMS}}$  (60s) of galvanic isolation between the PROFIBUS-DP/RS-485 cableside of the transceiver and the UART-side. These devices allow fast (20Mbps) communication across an isolation barrier when a large potential exists between grounds on each side of the barrier.

### Isolation

Data isolation is achieved using high-voltage capacitors that allow data transmission between the UART-side and the Profibus/RS-485 cable-side of the transceiver.

### Integrated LDO

The devices include an internal low-dropout regulator with a set 5V (typ) output that is used to power the cable-side of the IC. The output of the LDO is  $V_{\text{DDB}}$ . In addition to powering the transceiver,  $V_{\text{DDB}}$  can source up to 10mA, allowing external termination resistors to be powered without the need for an external regulator. The LDO has a 300mA (typ) current limit. If the LDO is unused, connect  $V_{\text{LDO}}$  to  $\text{GNDB}$  and apply +5V directly to  $V_{\text{DDB}}$ .

### True Fail-Safe

The MAX14941/MAX14942 guarantee a logic-high on the receiver output when the receiver inputs are shorted or open, or when connected to a terminated transmission line with all drivers disabled. The receiver threshold is fixed between  $-50\text{mV}$  and  $-200\text{mV}$ . If the differential receiver input voltage ( $V_{\text{A}} - V_{\text{B}}$ ) is greater than or equal to  $-50\text{mV}$ ,  $\text{RXD}$  is logic-high. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to zero by the termination resistors. Due to the receiver thresholds of the MAX14941/MAX14942, this results in a logic-high at  $\text{RXD}$ .

### Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or bus contention. The first, a foldback mode current limit on the output stage, provides immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds  $+160^{\circ}\text{C}$  (typ).

### Thermal Shutdown

The devices are protected from overtemperature damage by integrated thermal shutdown circuitry. When the junction temperature ( $T_{\text{J}}$ ) exceeds  $+160^{\circ}\text{C}$  (typ), the driver outputs go high-impedance. The device resumes normal operation when  $T_{\text{J}}$  falls below  $+145^{\circ}\text{C}$  (typ).

## Applications Information

### 128 Transceivers on the Bus

The standard RS-485 receiver input impedance is one unit load. A standard driver can drive up to 32 unit-loads. The MAX14941/MAX14942 transceivers have a  $\frac{1}{4}$ -unit load receiver, which allows up to 128 transceivers, connected in parallel, on one communication line. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit-loads to the line.

### Typical Application

The MAX14941/MAX14942 transceivers are designed for bidirectional data communications on multipoint bus transmission lines. [Figure 10](#) and [Figure 11](#) show typical network application circuits. To minimize reflections, the bus should be terminated at both ends in its characteristics impedance, and stub lengths off the main line should be kept as short as possible.

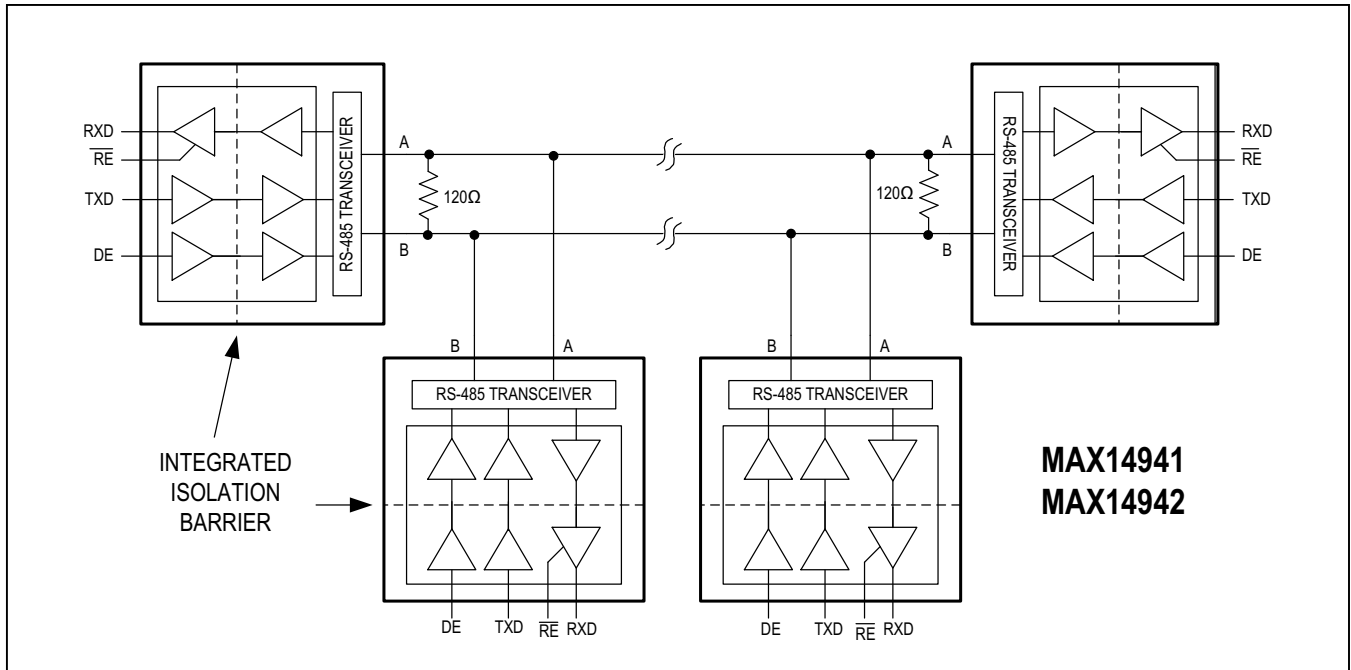


Figure 10. Typical Isolated Half-Duplex RS-485 Application

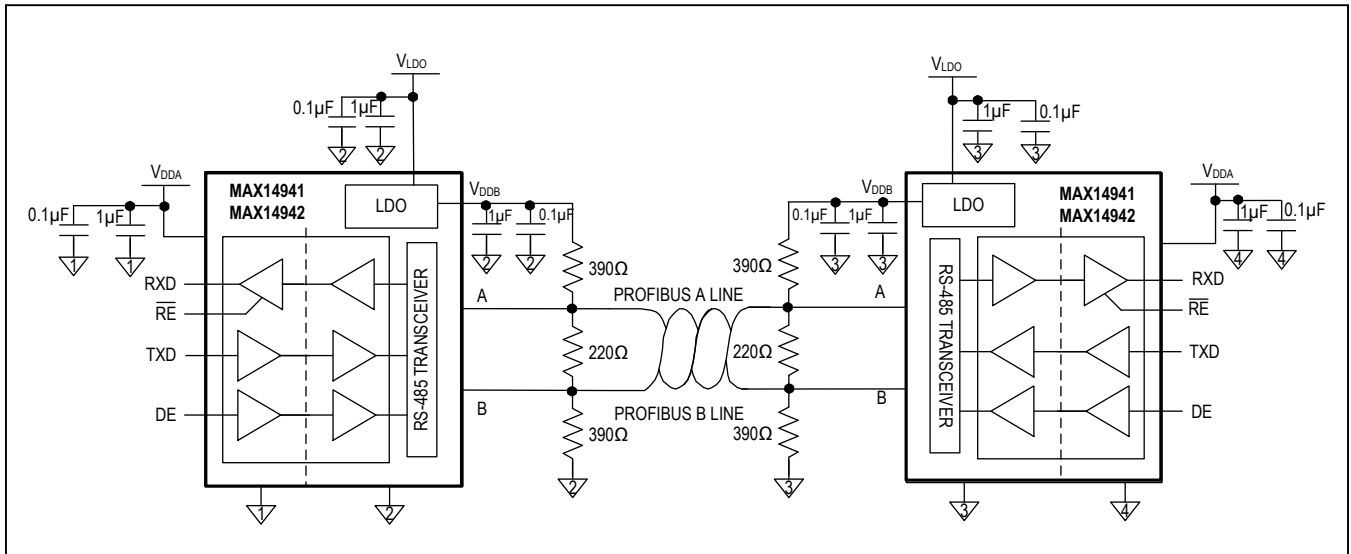


Figure 11. Typical Isolated Profibus Application



### Profibus Termination

These devices are designed for driving PROFIBUS DP terminated networks. The driver maintains 2.1V (min) when driving a worst-case loading condition of two standard 220 $\Omega$  termination resistors with 390 $\Omega$  pullups/pulldowns.

### Layout Considerations

It is recommended to design an isolation, or “keep-out,” channel underneath the isolator that is free from ground and signal planes. Any galvanic or metallic connection between the cable-side and UART-side will defeat the isolation.

Ensure that the decoupling capacitors between  $V_{DDA}$  and  $GNDA$  and between  $V_{LDO}$ ,  $V_{DDB}$ , and  $GNDB$  are located as close as possible to the IC to minimize inductance.

Route important signal lines close to the ground plane to minimize possible external influences. On the cable-side of the MAX14941/MAX14942, it is good practice to have the bus connectors and termination resistor as close as possible to the A and B pins.

### Extended ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharge encountered during handling and assembly. The driver outputs and receiver inputs of the MAX14941/MAX14942 have extra protection against static electricity to both the UART-side and cable-side ground references. The ESD structures withstand high-ESD events during normal operation and when powered down. After an ESD event, the devices keep working without latch-up or damage.

Bypass  $V_{DDA}$  to  $GNDA$  and bypass  $V_{DDB}$  and  $V_{LDO}$  to  $GNDB$  with 0.1 $\mu\text{F}$  and 1 $\mu\text{F}$  capacitors to ensure maximum ESD protection.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the MAX14941/MAX14942 are characterized for protection to the cable-side ground ( $GNDB$ ) to the following limits:

- $\pm 35\text{kV}$  HBM
- $\pm 12\text{kV}$  using the Air-Gap Discharge method specified in IEC 61000-4-2
- $\pm 10\text{kV}$  using the Contact Discharge method specified in IEC 61000-4-2

### ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

### Human Body Model (HBM)

[Figure 12](#) shows the HBM test model, while [Figure 13](#) shows the current waveform it generates when discharged in a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5k $\Omega$  resistor.

### IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX14941/MAX14942 help in designing equipment to meet IEC 61000-4-2 without the need for additional ESD protection components.

The major difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the HBM.

[Figure 14](#) shows the IEC 61000-4-2 model and [Figure 15](#) shows the current waveform for IEC 61000-4-2 ESD Contact Discharge Test.

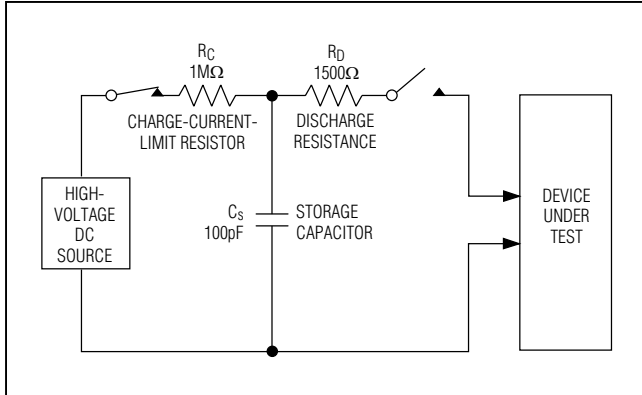


Figure 12. Human Body ESD Test Model

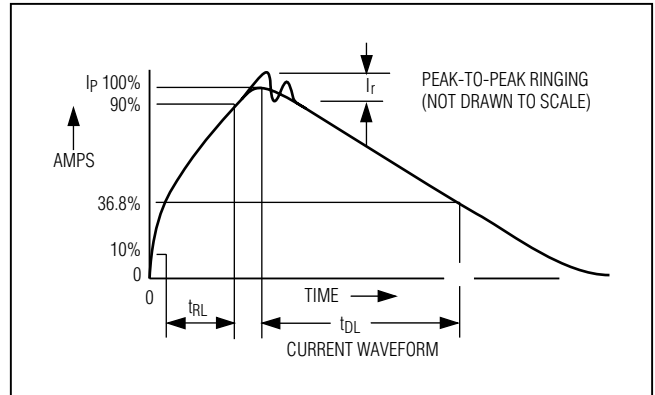


Figure 13. Human Body Current Waveform

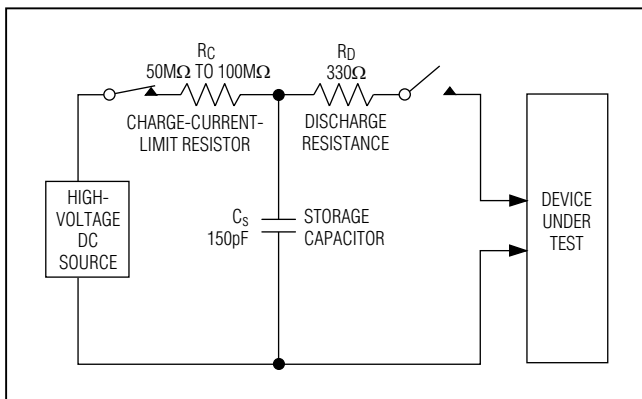


Figure 14. IEC 61000-4-2 ESD Test Model

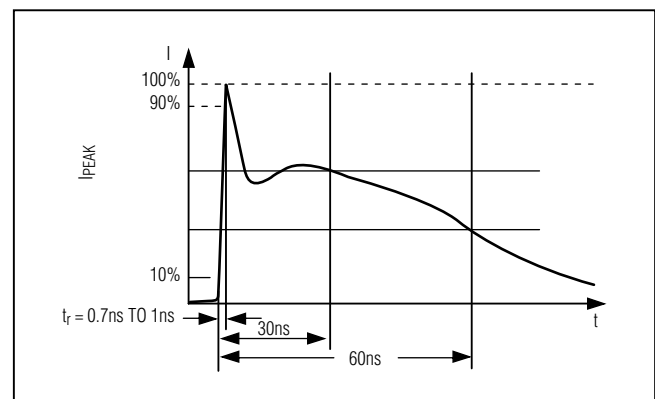
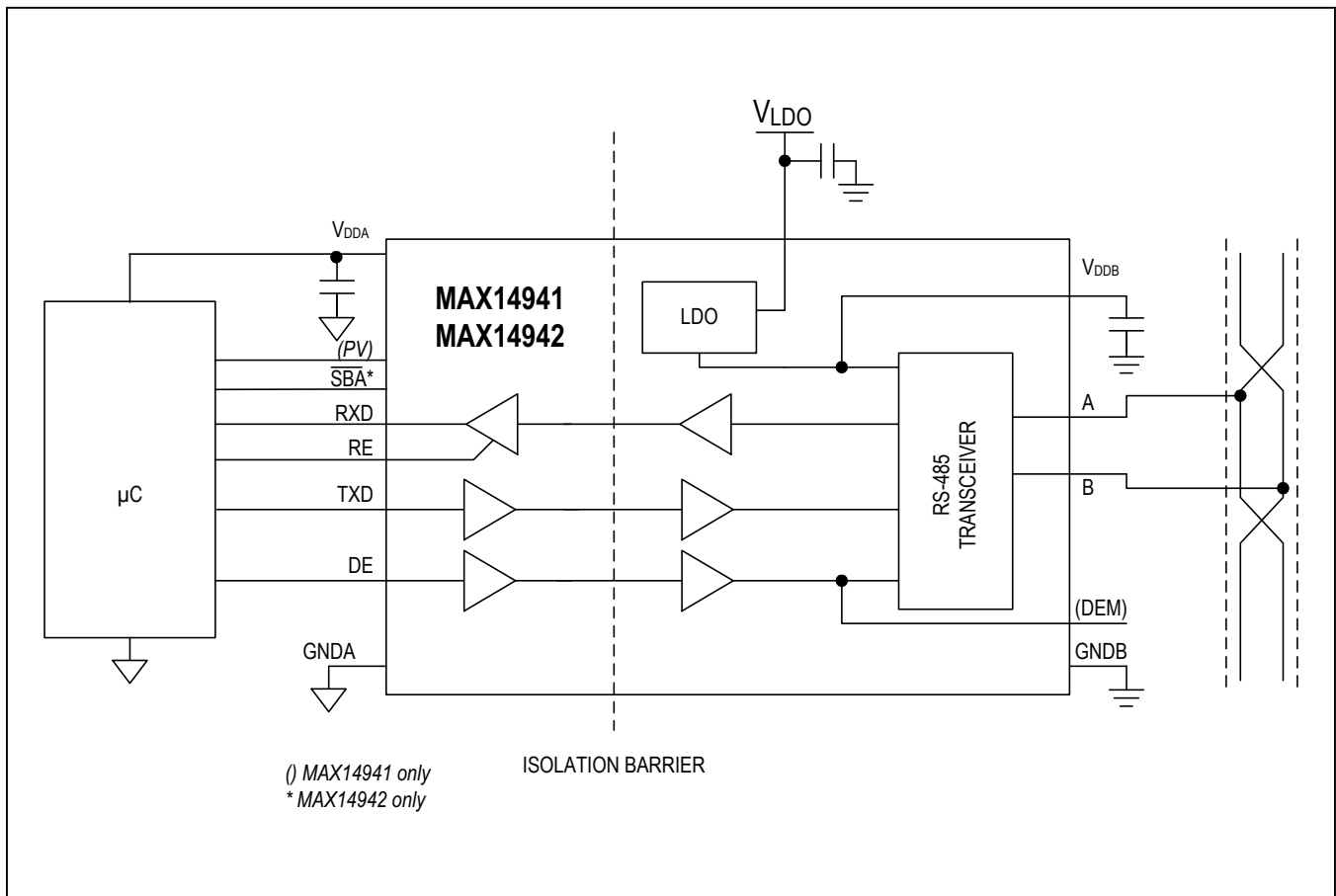


Figure 15. IEC 61000-4-2 ESD Generator Current Waveform

Typical Application Circuit



MAX14941/MAX14942

5kV Isolated 20Mbps Half-Duplex PROFIBUS/  
RS-485 Transceivers with ±35kV ESD Protection

### Ordering Information/Selector Guide

PART	DEM	PV	SBA	TEMP RANGE	PIN-PACKAGE
MAX14941GWE+	√	√	-	-40°C to +105°C	16 SOIC (W)
MAX14941GWE+T	√	√	-	-40°C to +105°C	16 SOIC (W)
MAX14942GWE+	-	-	√	-40°C to +105°C	16 SOIC (W)
MAX14942GWE+T	-	-	√	-40°C to +105°C	16 SOIC (W)

+Denotes a lead(Pb)-free/RoHS-compliant package.  
T = Tape and Reel

### Chip Information

PROCESS: BiCMOS

### Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 SOIC	W16M+9	<a href="#">21-0042</a>	<a href="#">90-0107</a>

MAX14941/MAX14942

5kV Isolated 20Mbps Half-Duplex PROFIBUS/  
RS-485 Transceivers with  $\pm 35\text{kV}$  ESD Protection

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/15	Initial release	—
1	1/17	Updated pending safety approvals	1, 6

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

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**Телефон:** +7 812 627 14 35

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**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331