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# **FDPC8011S** PowerTrench<sup>®</sup> Power Clip 25V Asymmetric Dual N-Channel MOSFET

### Features

Q1: N-Channel

• Max  $r_{DS(on)}$  = 7.3 m $\Omega$  at V<sub>GS</sub> = 4.5 V, I<sub>D</sub> = 12 A

Q2: N-Channel

- Max  $r_{DS(on)}$  = 2.1 m $\Omega$  at V<sub>GS</sub> = 4.5 V, I<sub>D</sub> = 24 A
- Low inductance packaging shortens rise/fall times, resulting in lower switching losses
- MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
- RoHS Compliant



### **General Description**

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET<sup>TM</sup> (Q2) have been designed to provide optimal power efficiency.

### Applications

- Computing
- Communications
- General Purpose Point of Load



### MOSFET Maximum Ratings T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V <sub>DS</sub>	Drain to Source Voltage	25	25	V
V <sub>GS</sub>	Gate to Source Voltage		12	V
	Drain Current -Continuous (Package limited) $T_C = 25 \text{ °C}$	20	60	
I <sub>D</sub>	-Continuous $T_A = 25 \ ^\circ C$		27 <sup>1b</sup>	А
	-Pulsed	40	120	
E <sub>AS</sub>	Single Pulse Avalanche Energy (Note 3)		97	mJ
D	Power Dissipation for Single Operation $T_A = 25 \ ^{\circ}C$	1.6 <sup>1a</sup>	2.0 <sup>1b</sup>	۱۸/
FD	Power Dissipation for Single Operation $T_A = 25 \text{ °C}$		0.9 <sup>1d</sup>	vv
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to	+150	°C

### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	77 <sup>1a</sup>	63 <sup>1b</sup>	
$R_{ ext{ heta}JA}$	Thermal Resistance, Junction to Ambient	151 <sup>1c</sup>	135 <sup>1d</sup>	°C/W
$R_{ ext{ heta}JC}$	Thermal Resistance, Junction to Case	5.0	3.5	

### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
130D/150D	FDPC8011S	Power Clip 33	13 "	12 mm	3000 units

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Electrical Characteristics T <sub>J</sub> = 25 °C unless otherwise noted									
Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units		
Off Chara	cteristics								
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \ \mu A, \ V_{GS} = 0 \ V$ $I_D = 1 \ m A, \ V_{GS} = 0 \ V$	Q1 Q2	25 25			V		
$\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta \text{T}_{\text{J}}}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \ \mu$ A, referenced to 25 °C $I_D = 10 \ m$ A, referenced to 25 °C	Q1 Q2		14 24		mV/°C		
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 20 V, V_{GS} = 0 V$ $V_{DS} = 20 V, V_{GS} = 0 V$	Q1 Q2			1 500	μΑ μΑ		
I <sub>GSS</sub>	Gate to Source Leakage Current, Forward	$V_{GS} = 12 \text{ V}/-8 \text{ V}, V_{DS} = 0 \text{ V}$ $V_{GS} = 12 \text{ V}/-8 \text{ V}, V_{DS} = 0 \text{ V}$	Q1 Q2			±100 ±100	nA nA		
On Chara	cteristics								
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \ \mu A$ $V_{GS} = V_{DS}, I_D = 1 \ m A$	Q1 Q2	0.8 1.1	1.2 1.4	2.2 2.2	V		
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \ \mu$ A, referenced to 25 °C $I_D = 10 \ m$ A, referenced to 25 °C	Q1 Q2		-4 -3		mV/°C		
r	Drain to Source On Pesictance		Q1		4.6 5.4 5.6	6.0 7.3 7.3			
r <sub>DS(on)</sub>	Drain to Source On Resistance		Q2		1.2 1.4 1.7	1.8 2.1 2.4	- 1115.2		
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 5 V, I_D = 13 A$ $V_{DS} = 5 V, I_D = 27 A$	Q1 Q2		97 231		S		

### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	Q1: V <sub>DS</sub> = 13 V, V <sub>GS</sub> = 0 V, f = 1 MHZ	Q1 Q2	1240 4335	pF
C <sub>oss</sub>	Output Capacitance	Q2:	Q1 Q2	332 1126	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	V <sub>DS</sub> = 13 V, V <sub>GS</sub> = 0 V, f = 1 MHZ	Q1 Q2	49 143	pF
R <sub>g</sub>	Gate Resistance		Q1 Q2	0.4 0.5	Ω

### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time			Q1 Q2	7 13	ns
t <sub>r</sub>	Rise Time	Q1: V <sub>DD</sub> = 13 V, I <sub>D</sub> = 13	8 A, R <sub>GEN</sub> = 6 Ω	Q1 Q2	2 5	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	Q2: Vpp = 13 V lp = 27	$A B_{OEN} = 6 \Omega$	Q1 Q2	20 38	ns
t <sub>f</sub>	Fall Time	_ (00 - 10 (, 10 - 21	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	Q1 Q2	2 4	ns
Qg	Total Gate Charge	$V_{GS} = 0$ V to 10 V	Q1	Q1 Q2	19 64	nC
Qg	Total Gate Charge	$V_{GS} = 0$ V to 4.5 V	V <sub>DD</sub> = 13 V, I <sub>D</sub> = 13 A	Q1 Q2	9 30	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		Q2 Vpp = 13 V	Q1 Q2	2.6 9.3	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		$I_{\rm D} = 27  {\rm A}$	Q1 Q2	2.3 7.7	nC

FDPC8011S PowerTrench<sup>®</sup> Power Clip

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Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
Drain-Sou	urce Diode Characteristics						
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	$V_{GS} = 0 V, I_S = 13 A$ (Note 2) $V_{GS} = 0 V, I_S = 27 A$ (Note 2)	Q1 Q2		0.8 0.8	1.2 1.2	V
t <sub>rr</sub>	Reverse Recovery Time	Q1 I <sub>F</sub> = 13 A, di/dt = 100 A/μs	Q1 Q2		22 30		ns
Q <sub>rr</sub>	Reverse Recovery Charge	Q2 I <sub>F</sub> = 27 A, di/dt = 300 A/μs	Q1 Q2		8 32		nC





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### Typical Characteristics (continued)

### SyncFET<sup>™</sup> Schottky body diode Characteristics

35

30 25

02 (A) 01 (A) 01 (D)

5

0 -5

100

150

200

Fairchild's SyncFET<sup>TM</sup> process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC8011S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.



Figure 27. FDPC8011S SyncFET<sup>TM</sup> body diode reverse recovery characteristic

250

TIME (ns)

350

300

400

di/dt = 300 A/µs

# Figure 28. SyncFET<sup>TM</sup> body diode reverse leakage versus drain-source voltage

## **Application Information**

### Typical Application Diagram (Synchronous Rectifier Buck Converter)



### Figure 1. Power Clip in Buck Converter Topology

As shown in Figure 1, in the Power Clip package Q1 is the High Side MOSFET (Control MOSFET) and Q2 is the Low Side MOSFET (Synchronous MOSFET). Figure 2 below shows the package pin out. The blue overlay on the drawing indicates a typical PCB land pattern for the part.



### Figure 2.Top View of Power Clip

Table 1 Pin Information shows the name and description of each pin.

PIN	Description	
Name	Description	
HSG	Gate signal input of Q1 Gate	
SW	Switch or Phase node, Source of Q1 and Drain of Q2	
GND,GND(LSS) PAD	Ground, Source of Q2	
LSG	Gate signal input of Q2 Gate	
V+, V+(HSD) PAD	Input voltage of SR Buck converter, Drain of Q1	
	PIN Name HSG SW GND,GND(LSS) PAD LSG V+, V+(HSD) PAD	

Table 1. Pin Information

### **Recommended PCB Layout Guidelines**

As a PCB designer, it is necessary to address critical issues in layout to minimize losses and optimize the performance of the power train. Power Clip is a high power density solution and all high current flow paths, such as V+(HSD), SW and GND(LSS) should be short and wide for minimal resistance and inductance. V+(HSD) and GND(LSS) are the primary heat flow paths for the Power Clip. A recommended layout procedure is discussed below to maximize the electrical and thermal performance of the part.



Figure 3.Top/Component (green) View and Bottom (red) PCB View

#### Following is a guideline, not a requirement which the PCB designer should consider.

Figure 3 shows an example of a well designed layout. The discussion that follows summarizes the key features of this layout.

- "The input ceramic bypass capacitor between VIN and GND should be placed as close as possible to the pins V+ / V+(HSD) PAD and GND / GND(LSS) PAD to help reduce parasitic inductance and high frequency ringing. Several capacitors may be placed in parallel, and capacitors may be placed on both the top and bottom side of the board. The capacitor located immediately adjacent to the Power Clip will be the most effective at reducing HF parasitic. Caps located farther away, or on the opposite side of the board will also assist, but will be less effective due to increased trace inductance.
- "The Power Clip package design, with very short distance between pins V+ and GND, allows for a short connect distance to the input cap. This is a factor that enables the Power Clip switch loop to have very low parasitic inductance.
- "Use large copper areas on the component side to connect the V+ pin and V+ (HSD) pad, and the GND and GND(LSS) PAD.
- "The SW to inductor copper trace is a high current path. It will also be a high noise region due to switching voltage transients. The trace should be short and wide to enable a low resistance path and to minimize the size of the noise region. Care should be taken to minimize coupling of this trace to adjacent traces. The layout in Figure 3 shows a good example of this short, wide path.
- "The Power Trench<sup>®</sup> Technology MOSFETs used in the Power Clip are effective at minimizing SW node ringing. They incorporate a proprietary design<sup>1</sup> that minimizes the peak overshoot ring voltage on the switch node (SW). They allow the part to operate well within the breakdown voltage limits. For most layouts, this eliminates the need to add an external snubber circuit. If the designer chooses to use an RC snubber, it should be placed close to the part between the SW pins and GND / GND (LSS) PAD to dampen the high frequency ringing.
- "The Driver IC should be placed relatively closed to HSG pin and LSG pin to minimize G drive trace inductance. Excessive G trace length may slow the switching speed of the HS drive. And it may lead to excessive ringing on the LS G. If the designer must place the driver a significant distance away from the Power Clip, it would be a good practice to include a 0 Ohm resistor in the LS G path as a place holder. In the final design, if the LS G exhibits excessive LF ringing, efficiency can often be improved by changing this resistor to a few Ohms to dampen the LS G LF ringing.
- "The Power Clip has very good Junction-PCB heat transfer from all power pins. It has much better heat transfer Junction-GND (LSS) than traditional dual FET packages. In most cases, board ground will be the most effective heat transfer path on the PCB. Use a large copper area between GND / GND(LSS)PAD pins and board ground. To ensure the best thermal and electrical connection to ground, we recommend using multiple vias to interconnect ground plane layers as shown in Figure 3.

<sup>1.</sup>Patent Pending

- "Use multiple vias in parallel on each copper region to interconnect top, inner and bottom layers. This will reduce resistance and inductance of the vias and will improve thermal conductivity. Vias should be relatively large, around 8 mils to 10 mils.
- "Avoid using narrow thermal relief traces on the V+ / V+(HSD) PAD and GND / GND(LSS)PAD pins. These will increase HF switch loop inductance. And these will increase ringing of the HF power loop and the SW node.

FDPC8011S PowerTrench<sup>®</sup> Power Clip







BOTTOM VIEW

OR VIAS WITHIN THE KEEP OUT AREA. F) DRAWING FILE NAME: MKT-PQFN08GREV4



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