

74LVC2G08

Dual 2-input AND gate

Rev. 16 — 29 July 2019

Product data sheet

1. General description

The 74LVC2G08 provides a 2-input AND gate function.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of the 74LVC2G08 as a translator in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant outputs for interfacing with 5 V logic
- High noise immunity
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC2G08DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G08DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G08GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm	SOT833-1
74LVC2G08GF	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1 x 0.5 mm	SOT1089
74LVC2G08GM	-40 °C to +125 °C	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm	SOT902-2
74LVC2G08GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 x 1.0 x 0.35 mm	SOT1116
74LVC2G08GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1.0 x 0.35 mm	SOT1203
74LVC2G08GX	-40 °C to +125 °C	X2SON8	plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 x 0.8 x 0.35 mm	SOT1233

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74LVC2G08DP	V08
74LVC2G08DC	V08
74LVC2G08GT	V08
74LVC2G08GF	VE
74LVC2G08GM	V08
74LVC2G08GN	VE
74LVC2G08GS	VE
74LVC2G08GX	VE

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

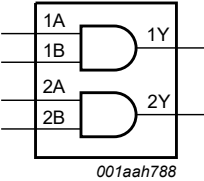


Fig. 1. Logic symbol

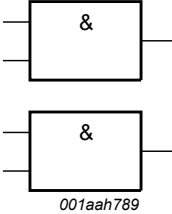


Fig. 2. IEC logic symbol

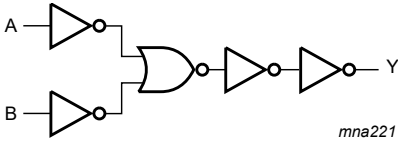


Fig. 3. Logic diagram (one gate)

6. Pinning information

6.1. Pinning

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Diagram showing pin configuration for SOT505-2 and SOT765-1 packages. The package is a square with pins 1 through 8. Pin 1 is at the top left, 2 at the top right, 3 at the bottom left, and 4 at the bottom right. Pins 5 through 8 are on the right side. Pin 1A is connected to pin 1, 1B to pin 2, 2Y to pin 3, and GND to pin 4. Pins 8, 7, 6, and 5 are connected to VCC, 1Y, 2B, and 2A respectively.

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Transparent top view

Diagram showing pin configuration for SOT833-1, SOT1089, SOT1116, and SOT1203 packages. The package is a square with pins 1 through 8. Pin 1 is at the top left, 2 at the top right, 3 at the bottom left, and 4 at the bottom right. Pins 5 through 8 are on the right side. Pin 1A is connected to pin 1, 1B to pin 2, 2Y to pin 3, and GND to pin 4. Pins 8, 7, 6, and 5 are connected to VCC, 1Y, 2B, and 2A respectively.

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Transparent top view

Diagram showing pin configuration for SOT902-2 package. The package is a square with pins 1 through 8. Pin 1 is at the top left, 2 at the top right, 3 at the bottom left, and 4 at the bottom right. Pins 5 through 8 are on the right side. Pin 1A is connected to pin 1, 1B to pin 2, 2Y to pin 3, and GND to pin 4. Pins 8, 7, 6, and 5 are connected to VCC, 1Y, 2B, and 2A respectively.

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Transparent top view

Diagram showing pin configuration for SOT1233 package. The package is a square with pins 1 through 8. Pin 1 is at the top left, 2 at the top right, 3 at the bottom left, and 4 at the bottom right. Pins 5 through 8 are on the right side. Pin 1A is connected to pin 1, 1B to pin 2, 2Y to pin 3, and GND to pin 4. Pins 8, 7, 6, and 5 are connected to VCC, 1Y, 2B, and 2A respectively.

Fig. 4. Pin configuration SOT505-2 and SOT765-1

Fig. 5. Pin configuration SOT833-1, SOT1089, SOT1116 and SOT1203

Fig. 6. Pin configuration SOT902-2

Fig. 7. Pin configuration SOT1233

6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT505-2, SOT765-1, SOT833-1, SOT1089, SOT1116, SOT1203 and SOT1233	SOT902-2	
1A	1	7	data input
1B	2	6	data input
2Y	3	5	data output
GND	4	4	ground (0 V)
2A	5	3	data input
2B	6	2	data input
1Y	7	1	data output
V _{CC}	8	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input		Output
nA	nB	nY
L	X	L
X	L	L
H	H	H

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage	[1]	-0.5	+6.5	V
V_O	output voltage	Active mode [1]	-0.5	$V_{CC} + 0.5$	V
		Power-down mode [1]	-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V or $V_O > V_{CC}$	-	± 50	mA
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	250	mW
		$T_{amb} = -40$ °C to +125 °C [3]	-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT505-2 (TSSOP8) packages: P_{tot} derates linearly with 4.6 mW/K above 96 °C.

For SOT765-1 (VSSOP8) packages: P_{tot} derates linearly with 4.9 mW/K above 99 °C.

For SOT833-1 (XSON8) packages: P_{tot} derates linearly with 3.1 mW/K above 68 °C.

For SOT1089 (XSON8) packages: P_{tot} derates linearly with 4.0 mW/K above 88 °C.

For SOT902-2 (XQFN8) packages: P_{tot} derates linearly with 4.1 mW/K above 89 °C.

For SOT1116 (XSON8) packages: P_{tot} derates linearly with 4.2 mW/K above 90 °C.

For SOT1203 (XSON8) packages: P_{tot} derates linearly with 3.6 mW/K above 81 °C.

[3] For SOT1233 (X2SON8) packages: P_{tot} derates linearly with 7.7 mW/K above 118 °C.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }5.5\text{ V}$	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$T_{amb} = -40\text{ °C to }+85\text{ °C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3 \times V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\text{ mA}; V_{CC} = 1.65\text{ V}$	1.2	1.53	-	V
		$I_O = -8\text{ mA}; V_{CC} = 2.3\text{ V}$	1.9	2.13	-	V
		$I_O = -12\text{ mA}; V_{CC} = 2.7\text{ V}$	2.2	2.50	-	V
		$I_O = -24\text{ mA}; V_{CC} = 3.0\text{ V}$	2.3	2.60	-	V
		$I_O = -32\text{ mA}; V_{CC} = 4.5\text{ V}$	3.8	4.10	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	-	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 1.65\text{ V}$	-	0.08	0.45	V
		$I_O = 8\text{ mA}; V_{CC} = 2.3\text{ V}$	-	0.14	0.3	V
		$I_O = 12\text{ mA}; V_{CC} = 2.7\text{ V}$	-	0.19	0.4	V
		$I_O = 24\text{ mA}; V_{CC} = 3.0\text{ V}$	-	0.37	0.55	V
		$I_O = 32\text{ mA}; V_{CC} = 4.5\text{ V}$	-	0.43	0.55	V

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_I	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	± 0.1	± 1	μA
I_{OFF}	power-off leakage current	V_I or $V_O = 5.5 \text{ V}$; $V_{CC} = 0 \text{ V}$	-	± 0.1	± 2	μA
I_{CC}	supply current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 1.65 \text{ V}$ to 5.5 V ; $I_O = 0 \text{ A}$	-	0.1	4	μA
ΔI_{CC}	additional supply current	per pin; $V_I = V_{CC} - 0.6 \text{ V}$; $I_O = 0 \text{ A}$; $V_{CC} = 2.3 \text{ V}$ to 5.5 V	-	5	500	μA
C_i	input capacitance		-	2.5	-	pF
$T_{amb} = -40 \text{ }^\circ\text{C}$ to $+125 \text{ }^\circ\text{C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65 \text{ V}$ to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7 \text{ V}$ to 3.6 V	2.0	-	-	V
		$V_{CC} = 4.5 \text{ V}$ to 5.5 V	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65 \text{ V}$ to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7 \text{ V}$ to 3.6 V	-	-	0.8	V
		$V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	$0.3 \times V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100 \mu\text{A}$; $V_{CC} = 1.65 \text{ V}$ to 5.5 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -4 \text{ mA}$; $V_{CC} = 1.65 \text{ V}$	0.95	-	-	V
		$I_O = -8 \text{ mA}$; $V_{CC} = 2.3 \text{ V}$	1.7	-	-	V
		$I_O = -12 \text{ mA}$; $V_{CC} = 2.7 \text{ V}$	1.9	-	-	V
		$I_O = -24 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$	2.0	-	-	V
		$I_O = -32 \text{ mA}$; $V_{CC} = 4.5 \text{ V}$	3.4	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100 \mu\text{A}$; $V_{CC} = 1.65 \text{ V}$ to 5.5 V	-	-	0.1	V
		$I_O = 4 \text{ mA}$; $V_{CC} = 1.65 \text{ V}$	-	-	0.70	V
		$I_O = 8 \text{ mA}$; $V_{CC} = 2.3 \text{ V}$	-	-	0.45	V
		$I_O = 12 \text{ mA}$; $V_{CC} = 2.7 \text{ V}$	-	-	0.60	V
		$I_O = 24 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$	-	-	0.80	V
		$I_O = 32 \text{ mA}$; $V_{CC} = 4.5 \text{ V}$	-	-	0.80	V
I_I	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	± 1	μA
I_{OFF}	power-off leakage current	V_I or $V_O = 5.5 \text{ V}$; $V_{CC} = 0 \text{ V}$	-	-	± 2	μA
I_{CC}	supply current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 1.65 \text{ V}$ to 5.5 V ; $I_O = 0 \text{ A}$	-	-	4	μA
ΔI_{CC}	additional supply current	per pin; $V_I = V_{CC} - 0.6 \text{ V}$; $I_O = 0 \text{ A}$; $V_{CC} = 2.3 \text{ V}$ to 5.5 V	-	-	500	μA

[1] All typical values are measured at $T_{amb} = 25 \text{ }^\circ\text{C}$.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nA, nB to nY; see Fig. 8 [2]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.0	3.2	9.0	1.0	11.3	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.5	2.2	5.1	0.5	6.4	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	2.5	5.3	1.0	6.7	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	0.5	2.1	4.7	0.5	5.9	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.5	1.7	3.8	0.5	4.8	ns
C_{PD}	power dissipation capacitance	per gate; $V_I = \text{GND to } V_{CC}$ [3]	-	14.4	-	-	-	pF

[1] Typical values are measured at nominal V_{CC} and at $T_{amb} = 25 \text{ °C}$.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

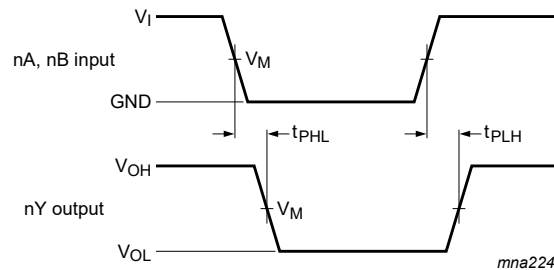
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit



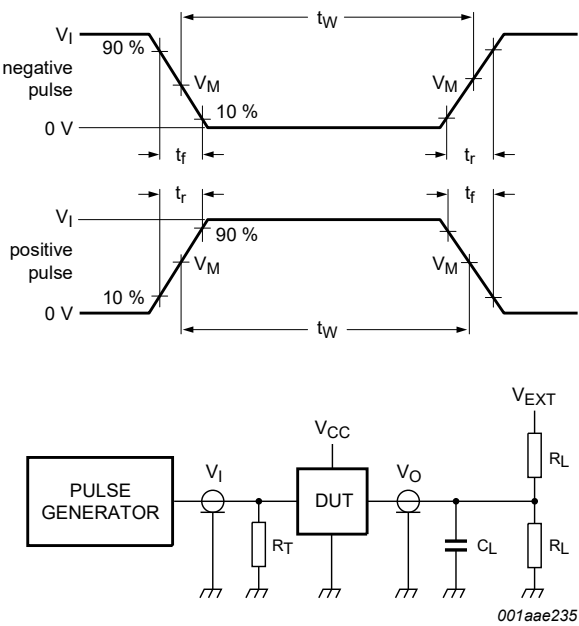
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. Input (nA, nB) to output (nY) propagation delays

Table 9. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Test data is given in [Table 10](#).
Definitions for test circuit:
 R_L = Load resistance
 C_L = Load capacitance including jig and probe capacitance
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator
 V_{EXT} = Test voltage for switching times

Fig. 9. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

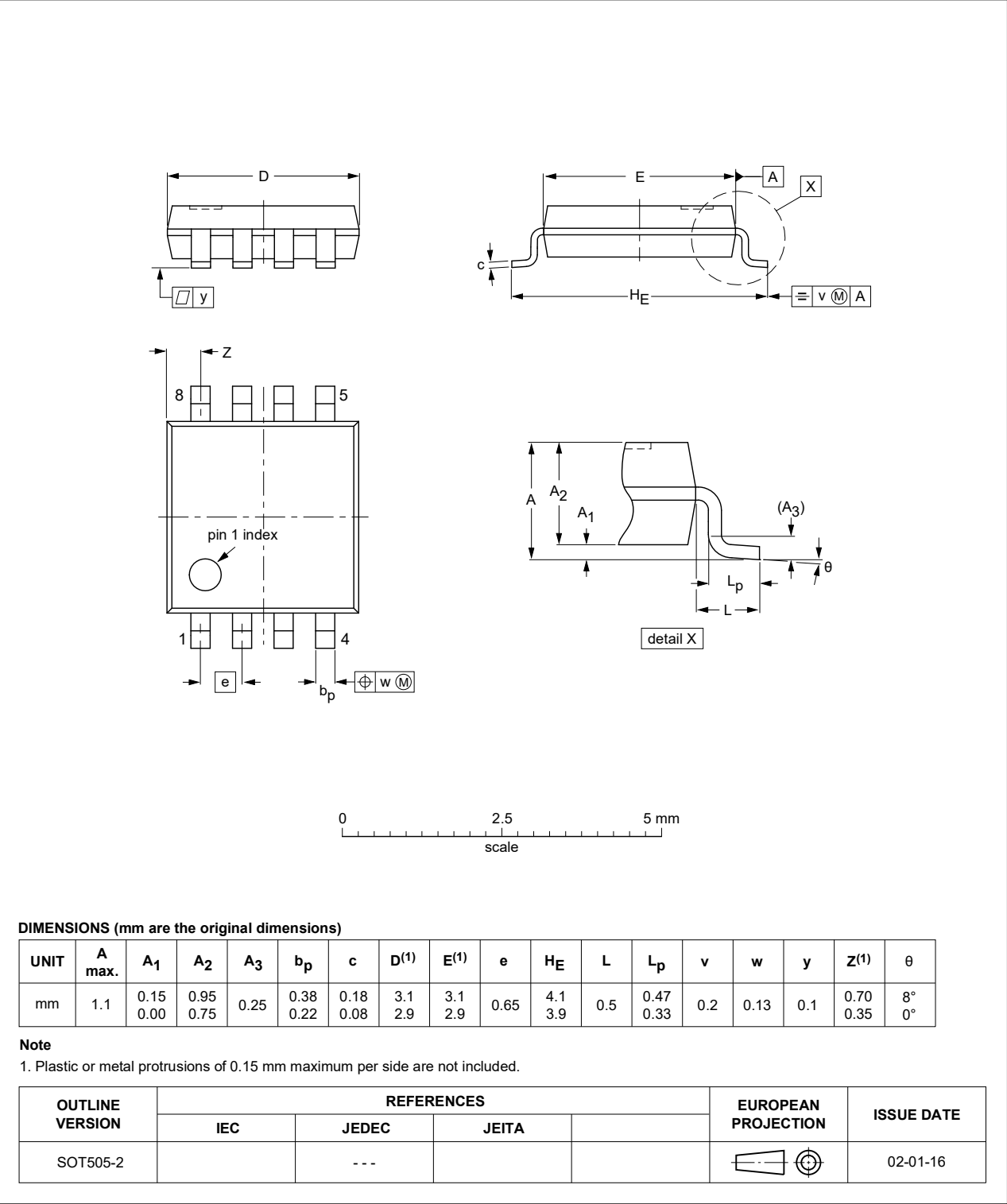
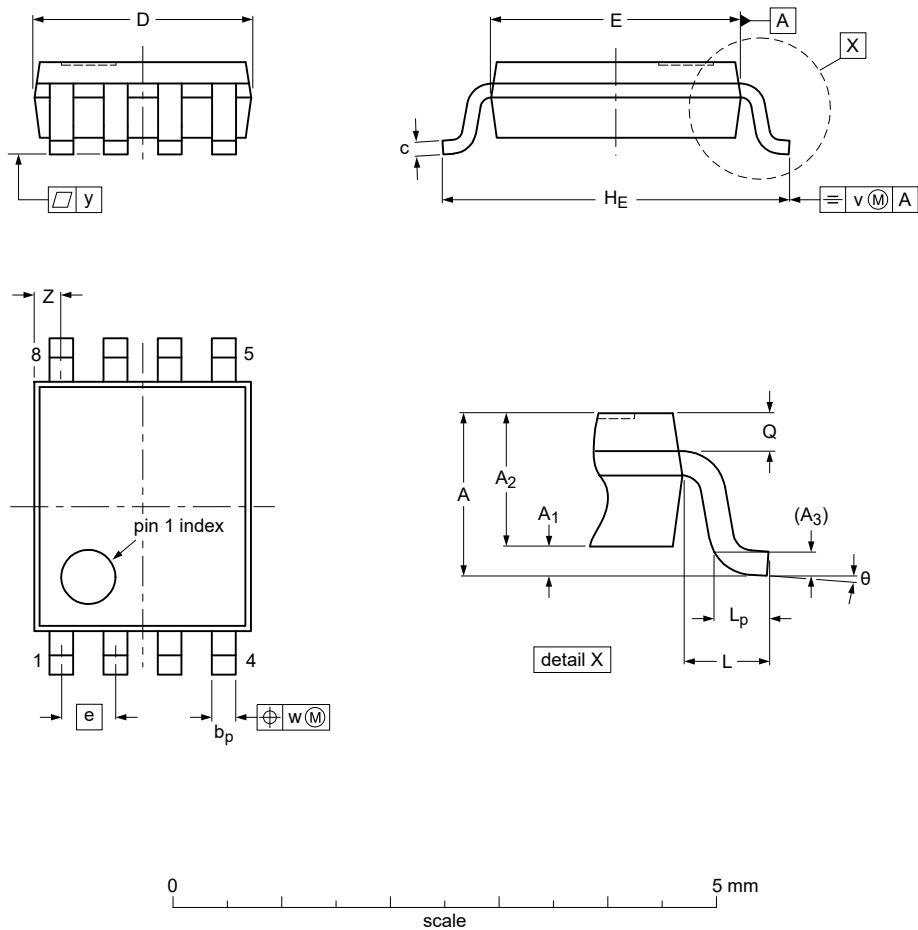


Fig. 10. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm SOT765-1



Dimensions (mm are the original dimensions)

Unit	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
max		0.15	0.85		0.27	0.23	2.1	2.4		3.2		0.40	0.21				0.4	8°
mm	nom	1		0.12					0.5		0.4			0.2	0.08	0.1		
min			0.60		0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

- Note
- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
 - 2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

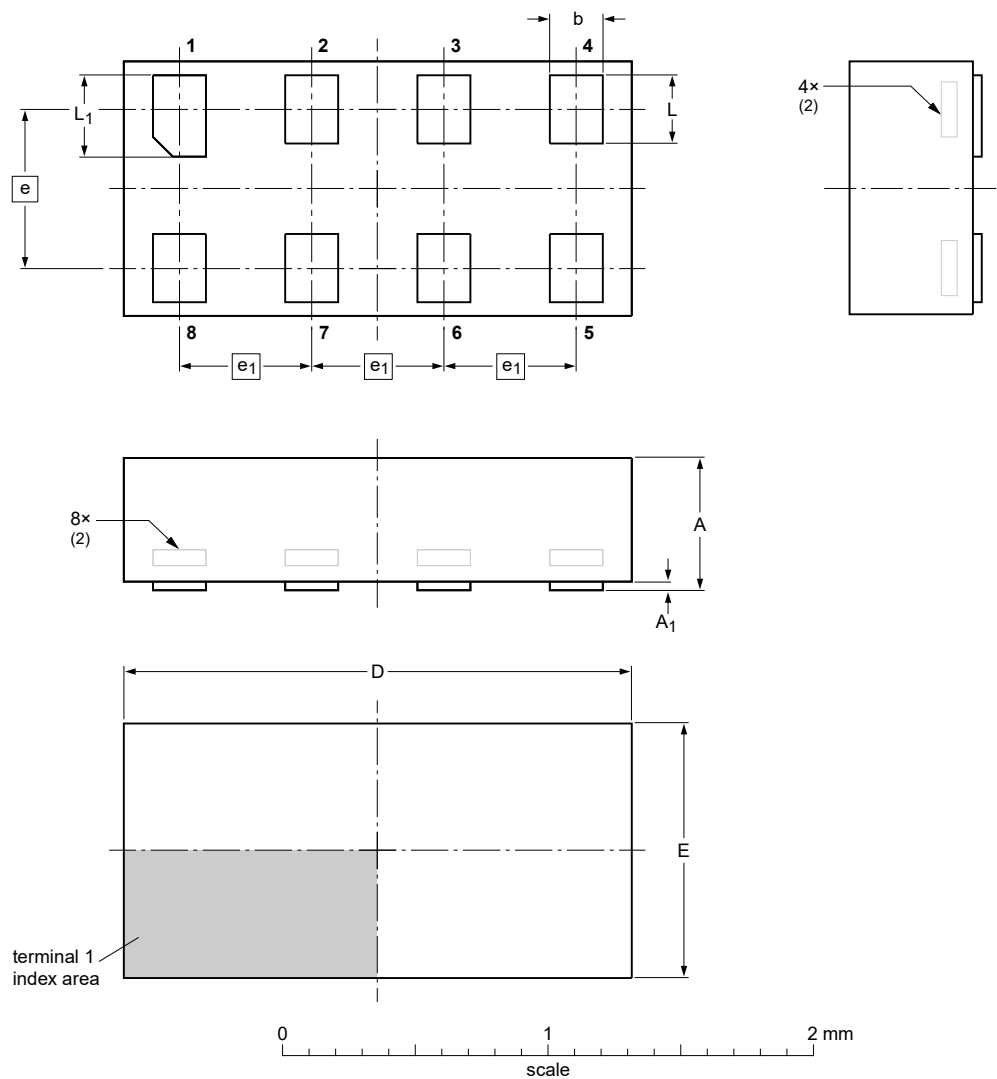
sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				-07-06-02- 16-05-31

Fig. 11. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max	A ₁ max	b	D	E	e	e ₁	L	L ₁
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

- Notes
- 1. Including plating thickness.
 - 2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	---	MO-252	---			-07-11-14- 07-12-07

Fig. 12. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1 x 0.5 mm

SOT1089

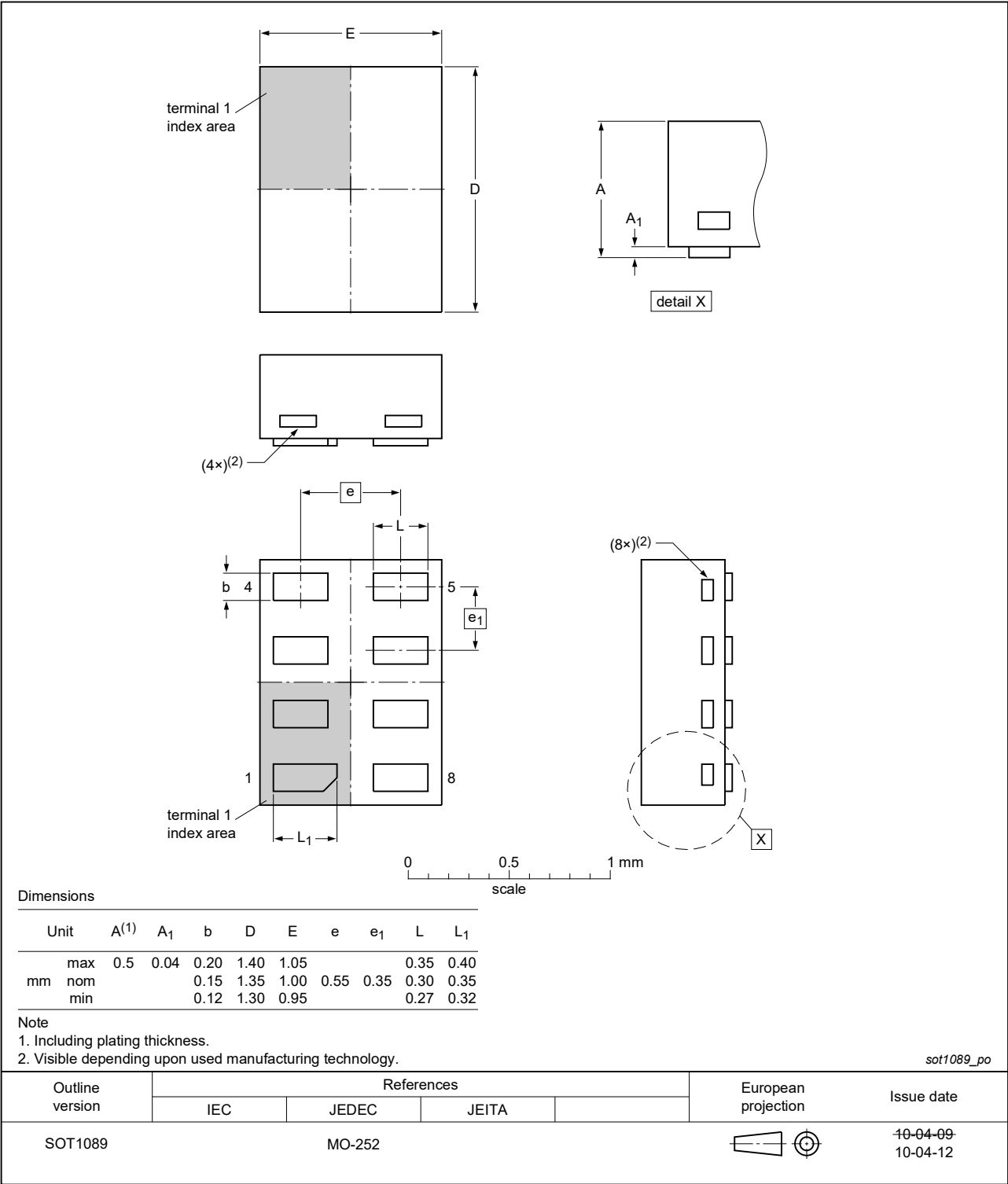


Fig. 13. Package outline SOT1089 (XSON8)

XQFN8: plastic, extremely thin quad flat package; no leads;
8 terminals; body 1.6 x 1.6 x 0.5 mm

SOT902-2

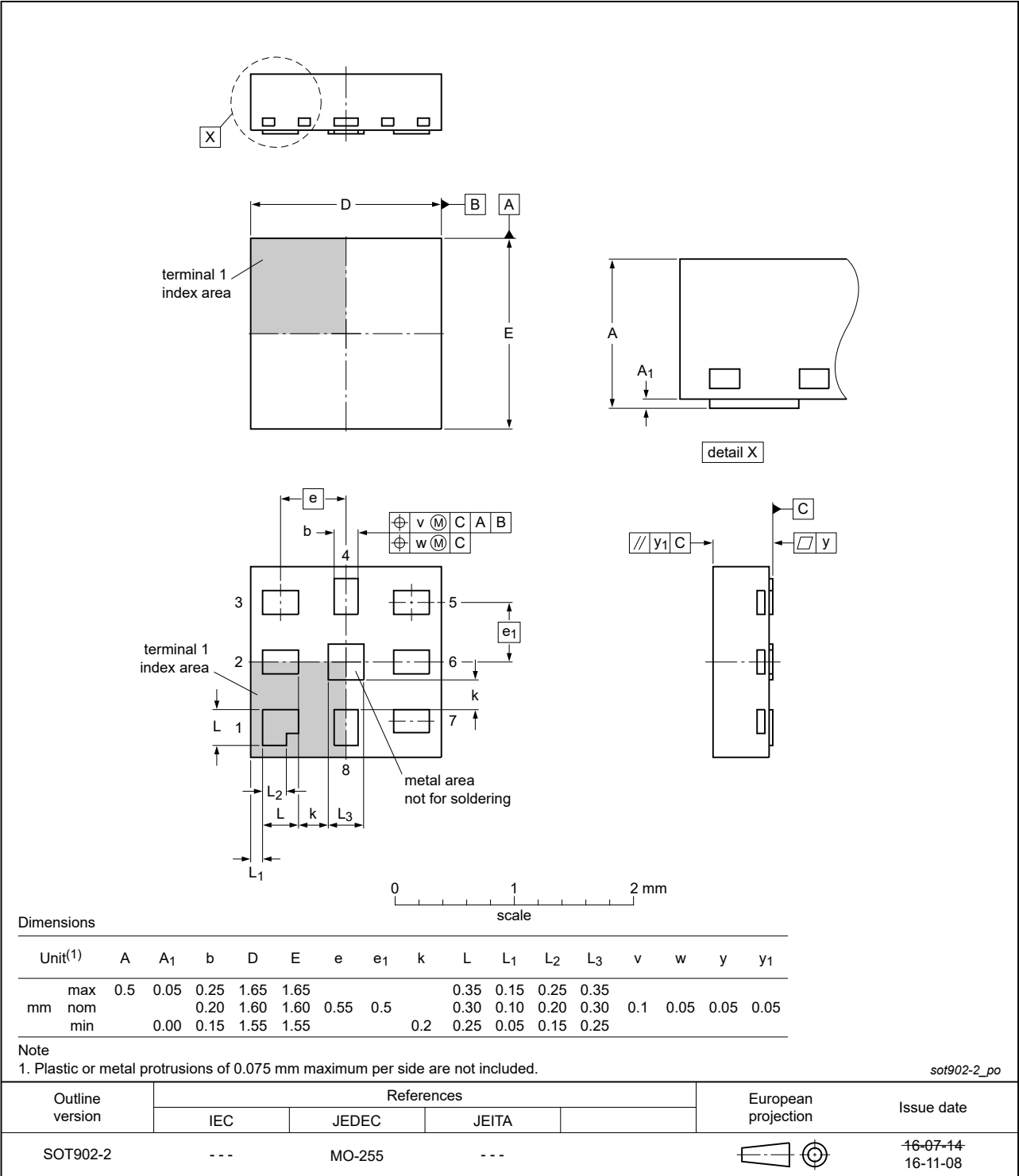
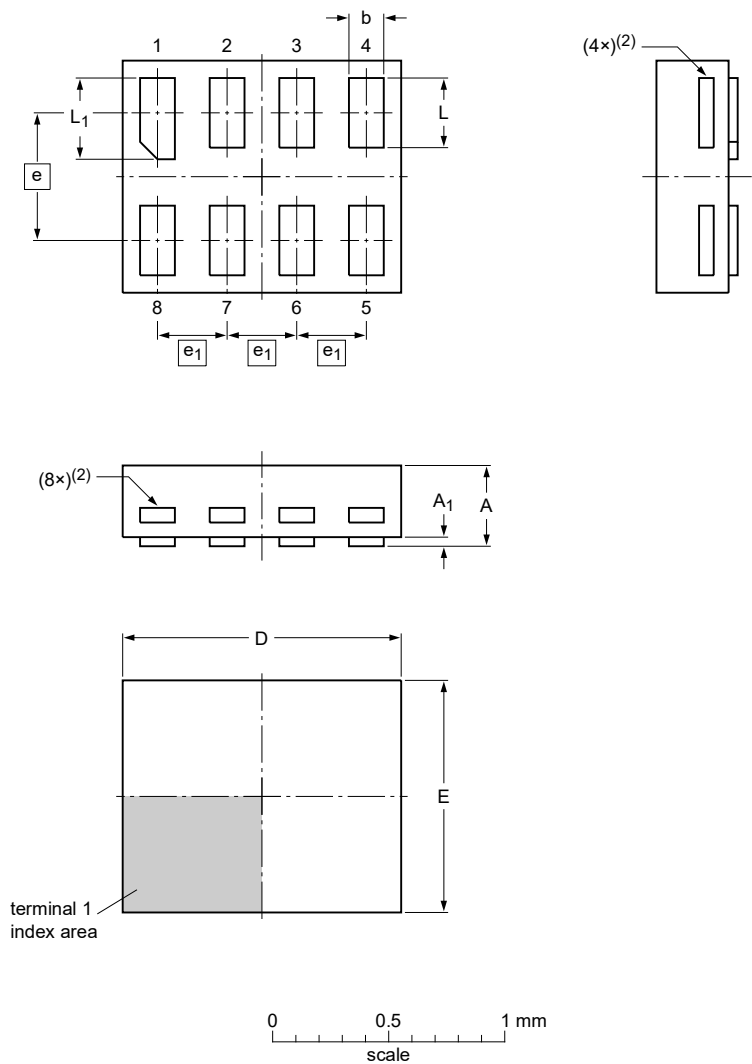


Fig. 14. Package outline SOT902-2 (XQFN8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.2 x 1.0 x 0.35 mm

SOT1116



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
mm	max	0.35	0.04	0.20	1.25	1.05		0.35	0.40
	nom			0.15	1.20	1.00	0.55	0.30	0.35
	min			0.12	1.15	0.95		0.27	0.32

Note

- 1. Including plating thickness.
- 2. Visible depending upon used manufacturing technology.

sot1116_po

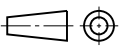
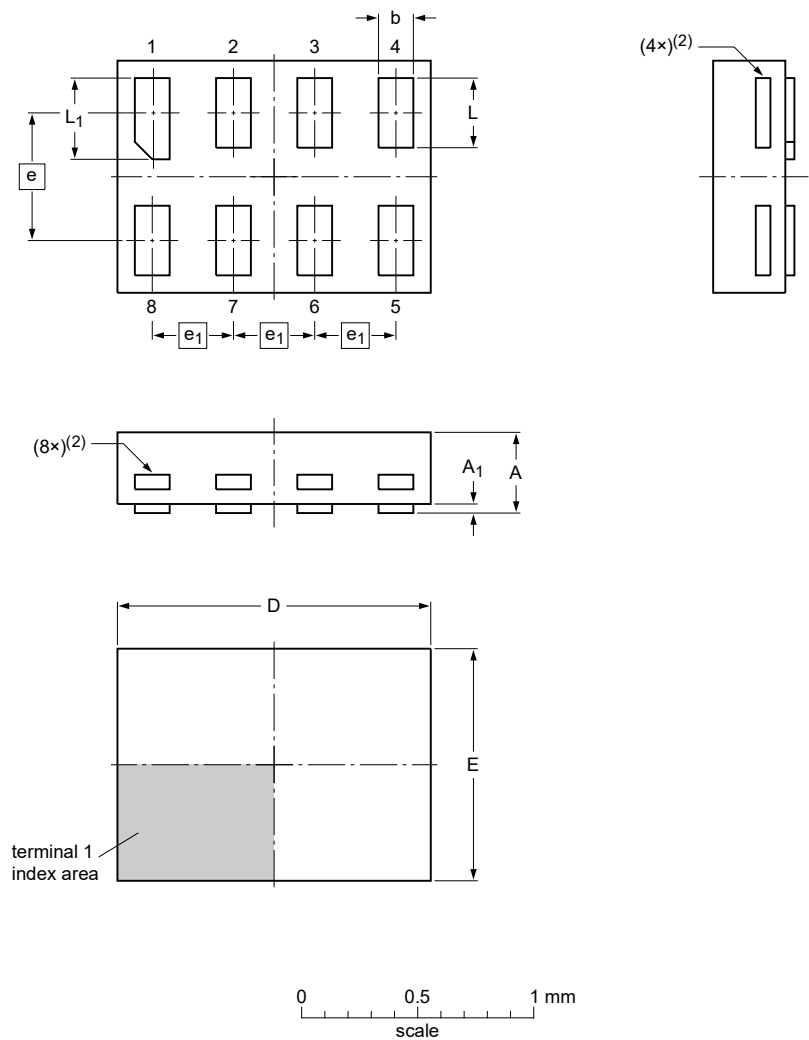
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1116						10-04-02 10-04-07

Fig. 15. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1.0 x 0.35 mm

SOT1203



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
mm	max	0.35	0.04	0.20	1.40	1.05		0.35	0.40
	nom			0.15	1.35	1.00	0.55	0.30	0.35
	min			0.12	1.30	0.95		0.27	0.32

Note

- 1. Including plating thickness.
- 2. Visible depending upon used manufacturing technology.

sot1203_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1203						~~10-04-02~~ 10-04-06

Fig. 16. Package outline SOT1203 (XSON8)

X2SON8: plastic thermal enhanced extremely thin small outline package; no leads;
8 terminals; body 1.35 x 0.8 x 0.35 mm

SOT1233

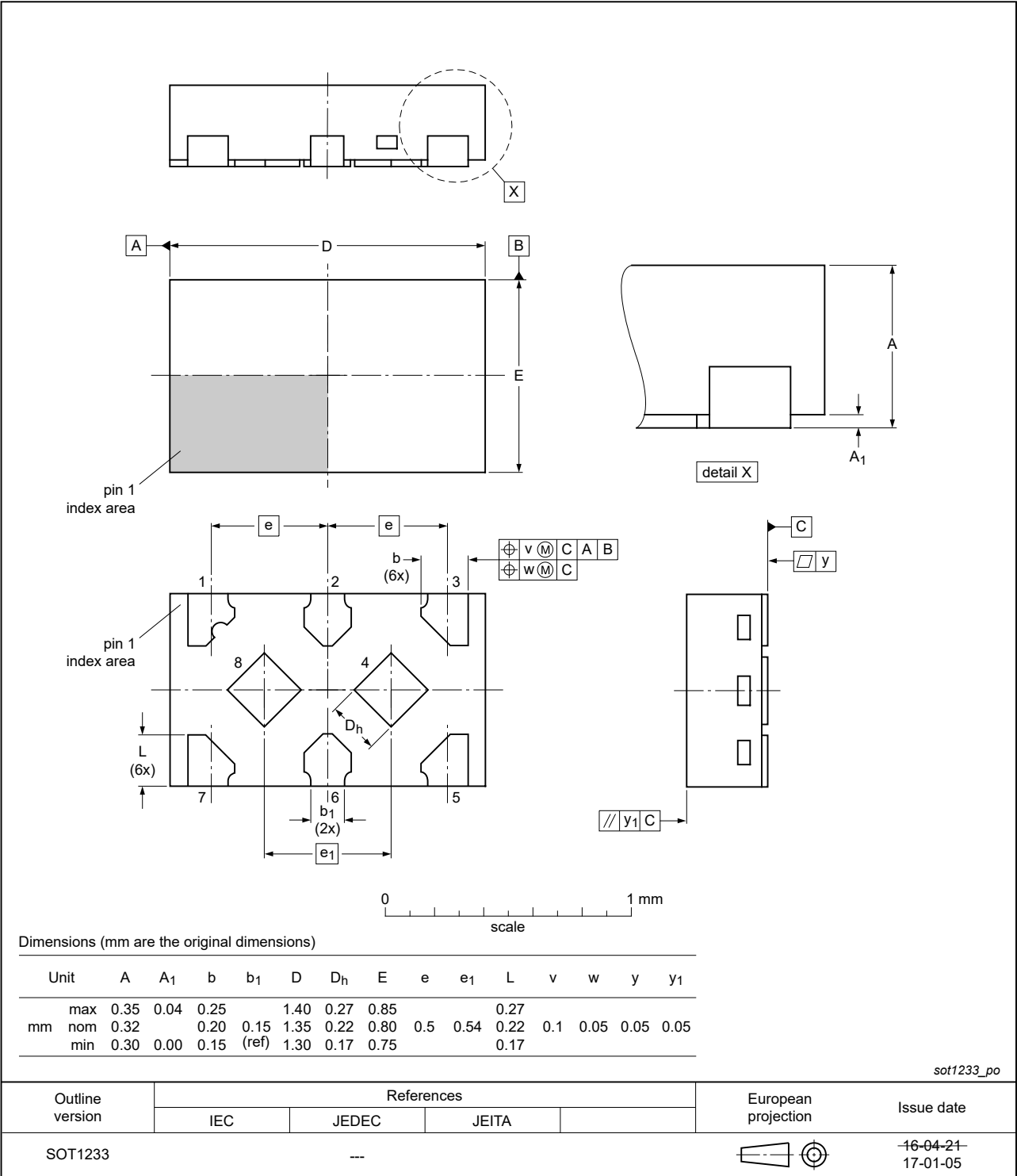


Fig. 17. Package outline SOT1233 (X2SON8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G08 v.16	20190729	Product data sheet	-	74LVC2G08 v.15
Modifications:	- Type number 74LVC2G08GD (SOT996-2/XSON8) removed. Table 5: P_{tot} total power dissipation and derating values updated.			
74LVC2G08 v.15	20170703	Product data sheet	-	74LVC2G08 v.14
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. Fig. 17: Package outline drawing for SOT1233 has changed.			
74LVC2G08 v.14	20161214	Product data sheet	-	74LVC2G08 v.13
Modifications:	Table 7: The maximum limits for leakage current and supply current have changed.			
74LVC2G08 v.13	20161028	Product data sheet	-	74LVC2G08 v.12
Modifications:	Added type number 74LVC2G08GX (SOT1233/X2SON8)			
74LVC2G08 v.12	20130402	Product data sheet	-	74LVC2G08 v.11
Modifications:	For type number 74LVC2G08GD XSON8U has changed to XSON8.			
74LVC2G08 v.11	20120622	Product data sheet	-	74LVC2G08 v.10
Modifications:	For type number 74LVC2G08GM the SOT code has changed to SOT902-2.			
74LVC2G08 v.10	20111201	Product data sheet	-	74LVC2G08 v.9
Modifications:	Legal pages updated.			
74LVC2G08 v.9	20101020	Product data sheet	-	74LVC2G08 v.8
74LVC2G08 v.8	20080609	Product data sheet	-	74LVC2G08 v.7
74LVC2G08 v.7	20080303	Product data sheet	-	74LVC2G08 v.6
74LVC2G08 v.6	20070904	Product data sheet	-	74LVC2G08 v.5
74LVC2G08 v.5	20060515	Product data sheet	-	74LVC2G08 v.4
74LVC2G08 v.4	20050201	Product specification	-	74LVC2G08 v.3
74LVC2G08 v.3	20040915	Product specification	-	74LVC2G08 v.2
74LVC2G08 v.2	20031020	Product specification	-	74LVC2G08 v.1
74LVC2G08 v.1	20030825	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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