

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON) \max}$	Package	$I_{D \max}$ $T_A = +25^\circ\text{C}$
12V	10m Ω @ $V_{GS} = 4.5\text{V}$	U-DFN2020-6 Type E	11A
	12m Ω @ $V_{GS} = 2.5\text{V}$		10
	14m Ω @ $V_{GS} = 1.8\text{V}$		9A
	18m Ω @ $V_{GS} = 1.5\text{V}$		8A
	41m Ω @ $V_{GS} = 1.2\text{V}$		5A

Description

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

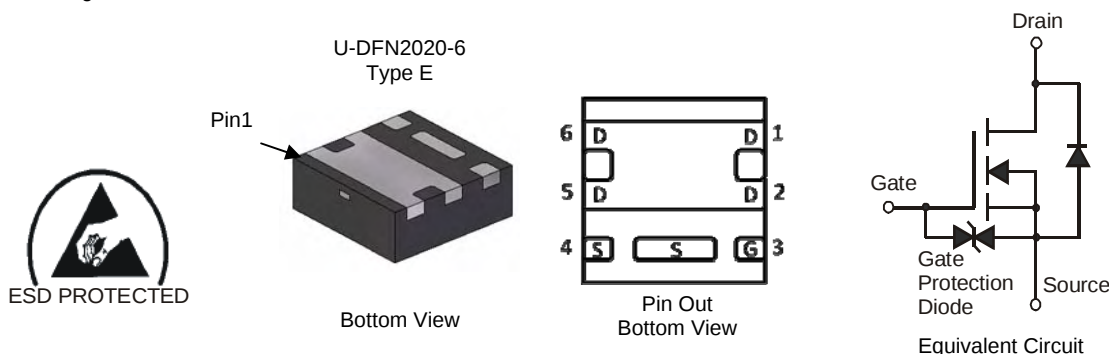
- Load Switching
- Battery Management Application
- Power Management Functions

Features

- 0.6mm profile – ideal for low profile applications
- PCB footprint of 4mm²
- Low Gate Threshold Voltage
- Fast Switching Speed
- ESD Protected Gate
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: U-DFN2020-6 Type E
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208 (e4)
- Weight: 0.007 grams (approximate)

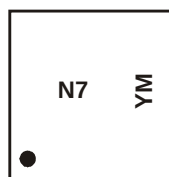


Ordering Information (Note 4)

Part Number	Marking	Reel size (inches)	Quantity per reel
DMN1019UFDE-7	N7	7	3,000

- Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
 2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com>.

Marking Information



N7 = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: Y = 2011)
 M = Month (ex: 9 = September)

Date Code Key

Year	2011	2012	2013	2014	2015	2016	2017
Code	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DS}	12	V
Gate-Source Voltage			V_{GS}	± 8	V
Continuous Drain Current (Note 5) $V_{GS} = 4.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$	I_D	11	A
		$T_A = +70^\circ\text{C}$		9	A
	$t < 5\text{s}$	$T_A = +25^\circ\text{C}$	I_D	14	A
		$T_A = +70^\circ\text{C}$		11	A
Maximum Continuous Body Diode Current			I_S	3.0	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)			I_{DM}	100	A

Thermal Characteristics

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	P_D	0.69	W
	$T_A = +70^\circ\text{C}$		0.44	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	182	$^\circ\text{C/W}$
	$t < 5\text{s}$		118	
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$	P_D	2.17	W
	$T_A = +70^\circ\text{C}$		1.38	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	$R_{\theta JA}$	58	$^\circ\text{C/W}$
	$t < 5\text{s}$		38	
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	10	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

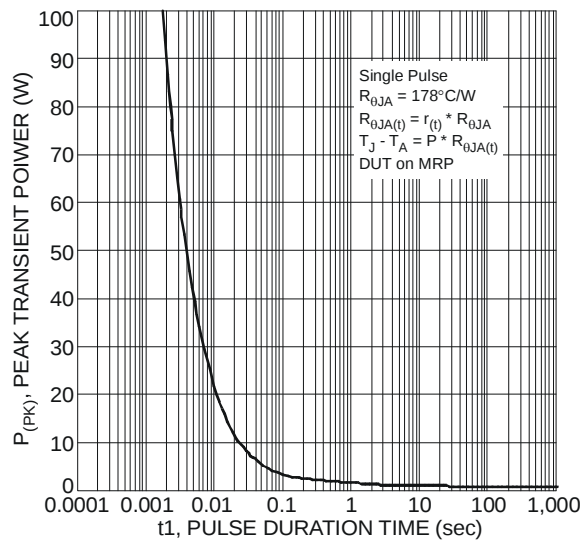


Fig. 1 Single Pulse Maximum Power Dissipation

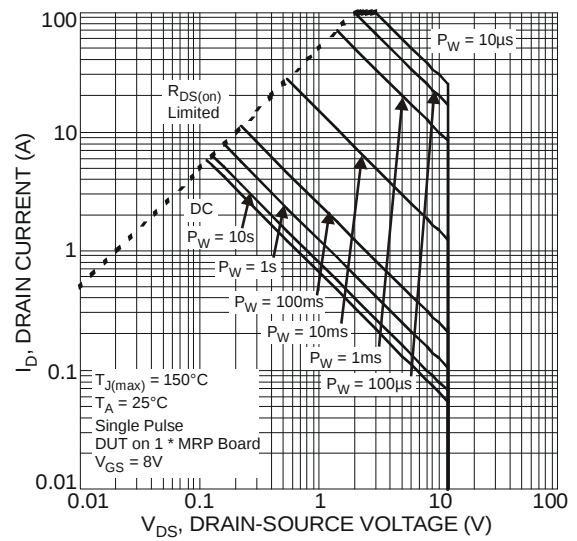
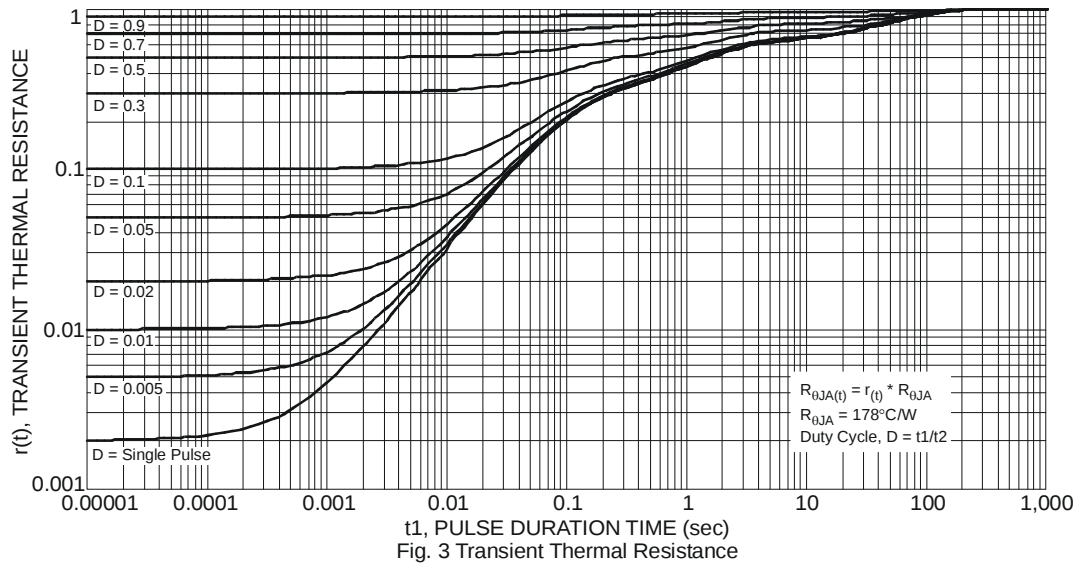


Fig. 2 SOA, Safe Operation Area



Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV _{DSS}	12	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	—	—	1	μA	V _{DS} = 12V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±2	μA	V _{GS} = ±8V, V _{DS} = 0V
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	V _{GS(th)}	0.35	—	0.8	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(on)}	—	7	10	mΩ	V _{GS} = 4.5V, I _D = 9.7A
			8	12		V _{GS} = 2.5V, I _D = 9A
			10	14		V _{GS} = 1.8V, I _D = 8.1A
			14	18		V _{GS} = 1.5V, I _D = 4.5A
			28	41		V _{GS} = 1.2V, I _D = 2.4A
Forward Transfer Admittance	Y _{fs}	—	28	—	S	V _{DS} = 4V, I _D = 9.7A
Diode Forward Voltage	V _{SD}	—	0.8	1.2	V	V _{GS} = 0V, I _S = 10A
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C _{iss}	—	2425	—	pF	V _{DS} = 10V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	396	—		
Reverse Transfer Capacitance	C _{rss}	—	375	—		
Gate Resistance	R _g	—	1.1	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge V _{GS} = 8V	Q _g	—	50.6	—	nC	V _{DS} = 4V, I _D = 10A
Total Gate Charge V _{GS} = 4.5V	Q _g	—	27.3	—		
Gate-Source Charge	Q _{gs}	—	3.4	—		
Gate-Drain Charge	Q _{gd}	—	5.2	—		
Turn-On Delay Time	t _{D(on)}	—	7.6	—	ns	V _{DD} = 4V, V _{GS} = 10V, I _D = 10A R _G = 1Ω, R _L = 0.4Ω
Turn-On Rise Time	t _r	—	22.2	—		
Turn-Off Delay Time	t _{D(off)}	—	57.6	—		
Turn-Off Fall Time	t _f	—	16.8	—		

- Notes:
- Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to production testing.

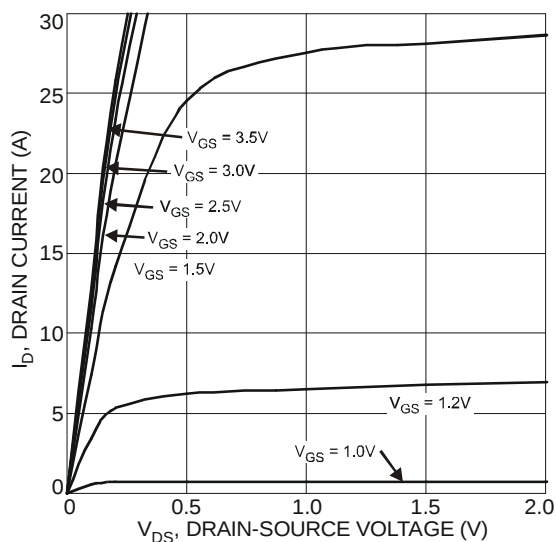


Fig. 4 Typical Output Characteristic

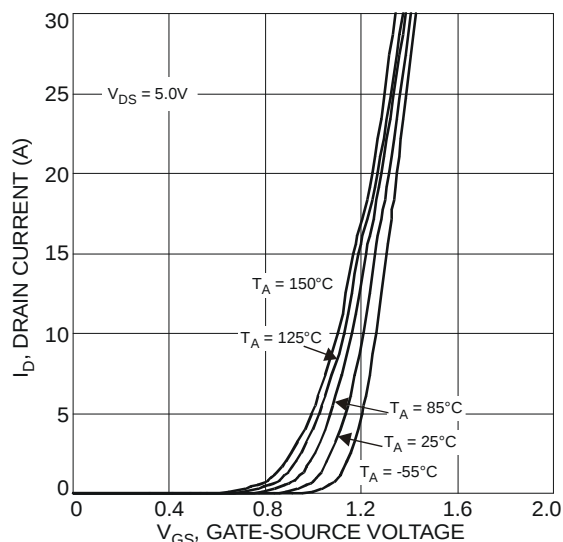


Fig. 5 Typical Transfer Characteristics

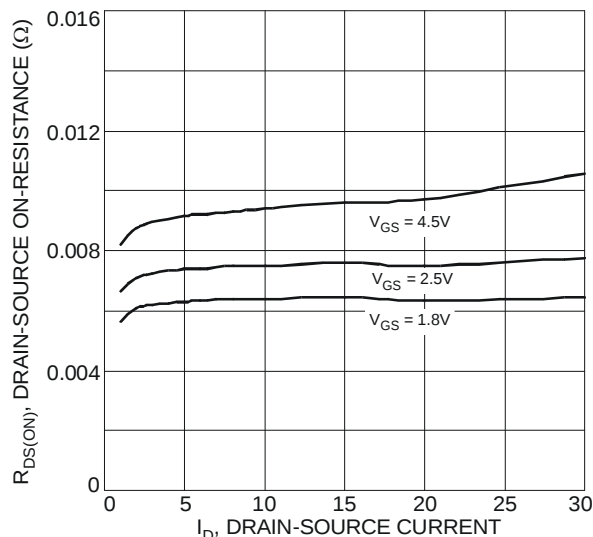


Fig. 6 Typical On-Resistance vs. Drain Current and Gate Voltage

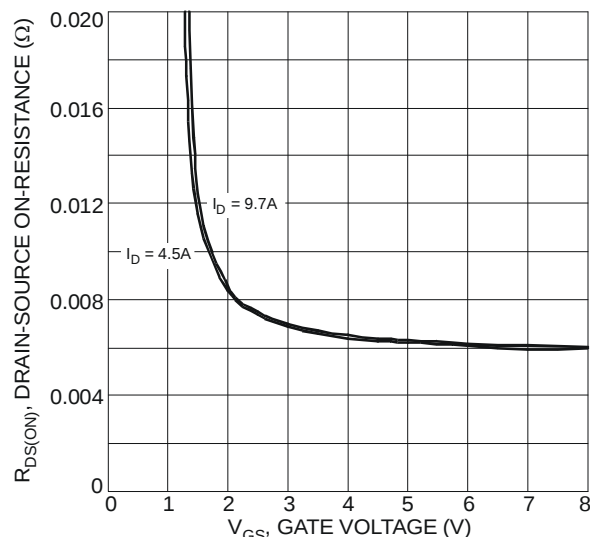


Fig. 7 Typical On-Resistance vs. Gate Voltage

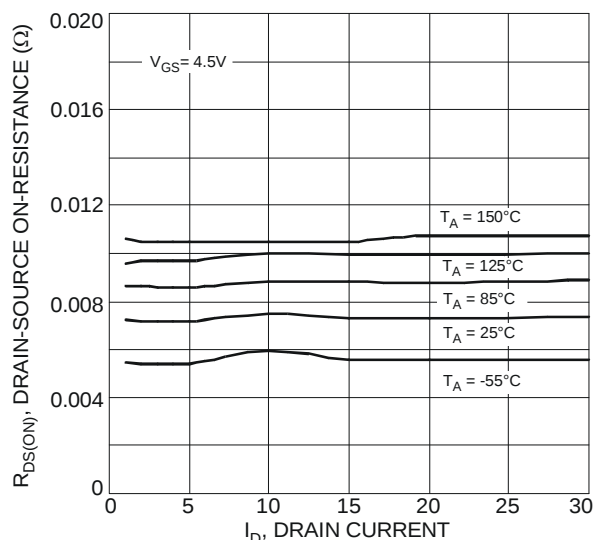


Fig. 8 Typical On-Resistance vs. Drain Current and Temperature

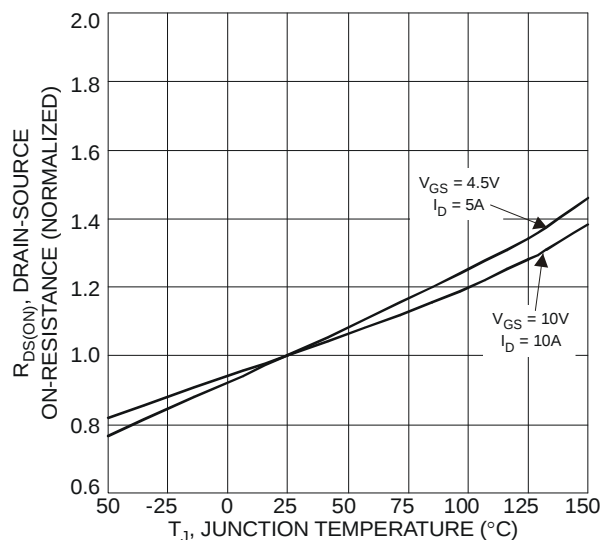


Fig. 9 On-Resistance Variation with Temperature

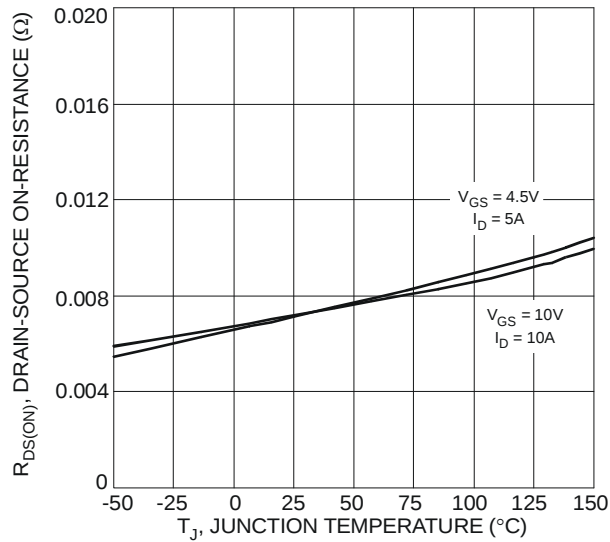


Fig. 10 On-Resistance Variation with Temperature

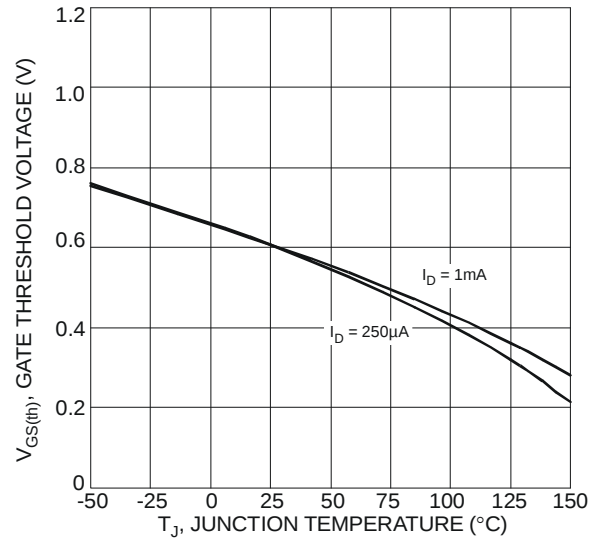


Fig. 11 Gate Threshold Variation vs. Ambient Temperature

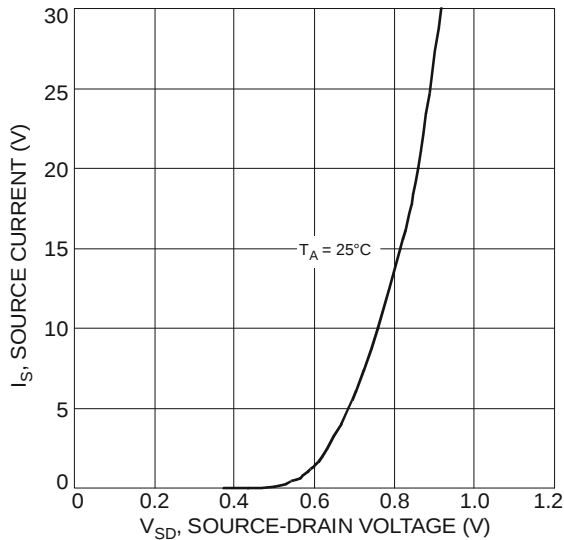


Fig. 12 Diode Forward Voltage vs. Current

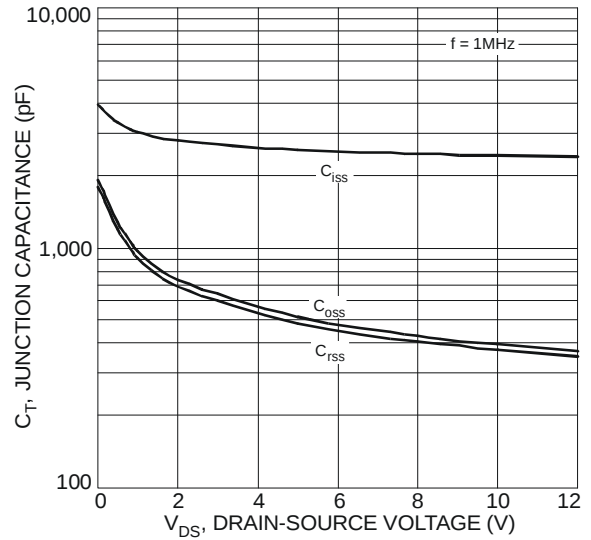


Fig. 13 Typical Junction Capacitance

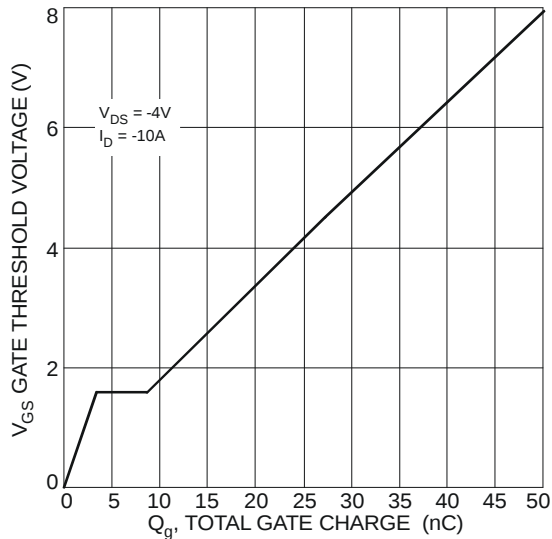
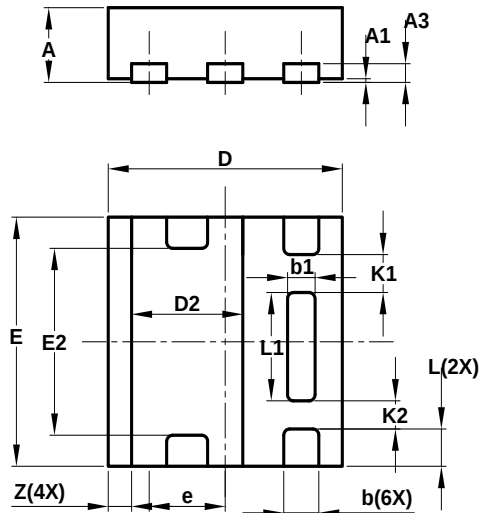


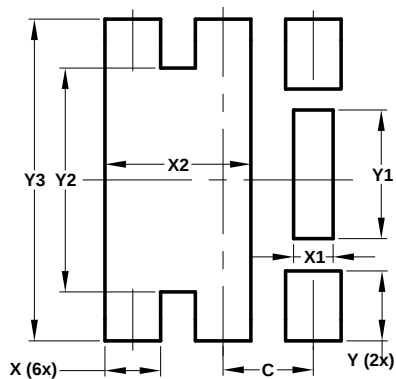
Fig. 14 Gate Charge

Package Outline Dimensions



U-DFN2020-6 Type E			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0	0.05	0.03
A3	—	—	0.15
b	0.25	0.35	0.30
b1	0.185	0.285	0.235
D	1.95	2.05	2.00
D2	0.85	1.05	0.95
E	1.95	2.05	2.00
E2	1.40	1.60	1.50
e	—	—	0.65
L	0.25	0.35	0.30
L1	0.82	0.92	0.87
K1	—	—	0.305
K2	—	—	0.225
Z	—	—	0.20
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
C	0.650
X	0.400
X1	0.285
X2	1.050
Y	0.500
Y1	0.920
Y2	1.600
Y3	2.300

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