XRT8001

WAN Clock for T1 and E1 Systems

October 2001-1

GENERAL DESCRIPTION

The XRT8001 WAN Clock is a dual-phase-locked loop chip that generates two very low jitter output clock signals that can be used for synchronization clocks in wide area networking systems. The XRT8001 has pre-programmed multipliers and dividers that are selected via the serial port. It generates two integer multiples of 8kHz, 56kHz, and 64kHz while locked onto an incoming reference of 1.54MHz (T1), 2.048MHz (E1), 8kHz, 56kHz, or 64kHz

The XRT8001 WAN Clock can be configured to operate in one of six modes:

1. The Forward/Master Mode
2. The Reverse/Master Mode
3. The “Fractional T1/E1" Reverse/Master Mode
4. The “E1 to T1 - Forward/Master" Mode
5. The “High Speed - Reverse" Mode
6. The “Slave” Mode

FEATURES

- Dual Phased Locked Loops with Pre-Programmed Multipliers and Dividers
- Pre-Programmed with Popular Frequency Conversions for Communications Systems
- Generates Output Clock Frequencies Ranging From 8kHz up to 16.384MHz
- Serial Port Control for Optimal Performance
- Sync Output: 8kHz or 64kHz
- Low Jitter
- Cascadable (Master / Slave Modes)
- No External Components Needed
- Pin Compatible with the XRT8000
- Low Power (3.3V or 5V): 40 - 100mW
- - 40°C to +85°C Temperature Range
- 18-Lead PDIP or SOIC Packages

APPLICATIONS

- T1/E1 Access Equipment (DSU/CSU)
- Frame Relay Access Devices (FRAD)
- Basic Rate and Primary Rate ISDN Equipment
  - ISDN Routers
  - Terminals
- Remote Access Servers
- T1/E1 Concentrators
- T1/E1 Multiplexers
- T1/E1 Clock Rate Converters
- Internal Timing Generators
- System Synchronizers

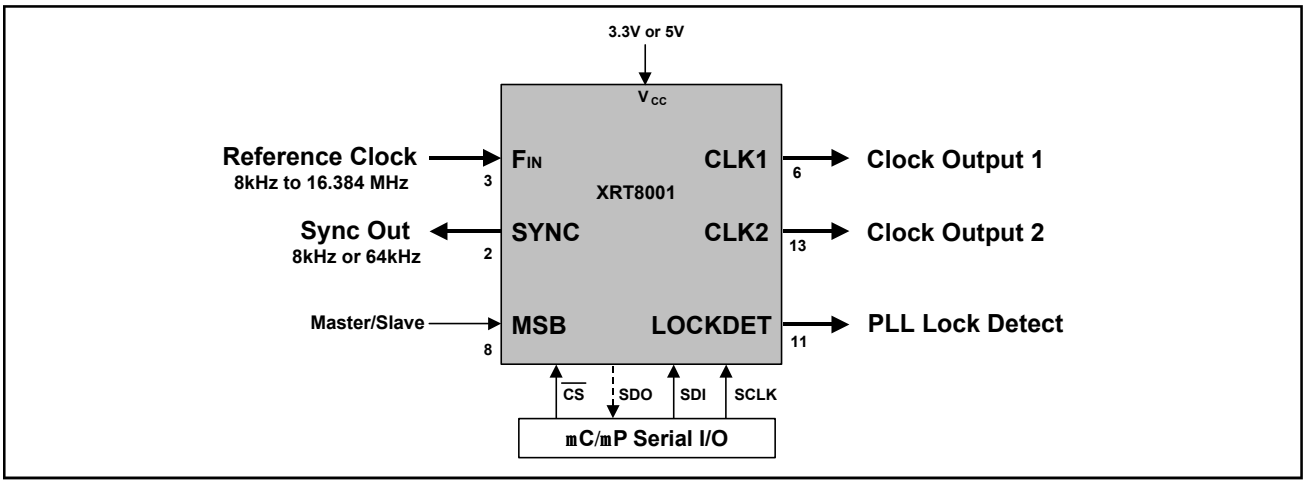

Figure 1. System Diagram

ORDERING INFORMATION

Part Number	Package	Operating Temperature Range
XRT8001IP	18-Lead 300 Mil PDIP	-40°C to +85°C
XRT8001ID	18-Lead 300 Mil JEDEC SOIC	-40°C to +85°C

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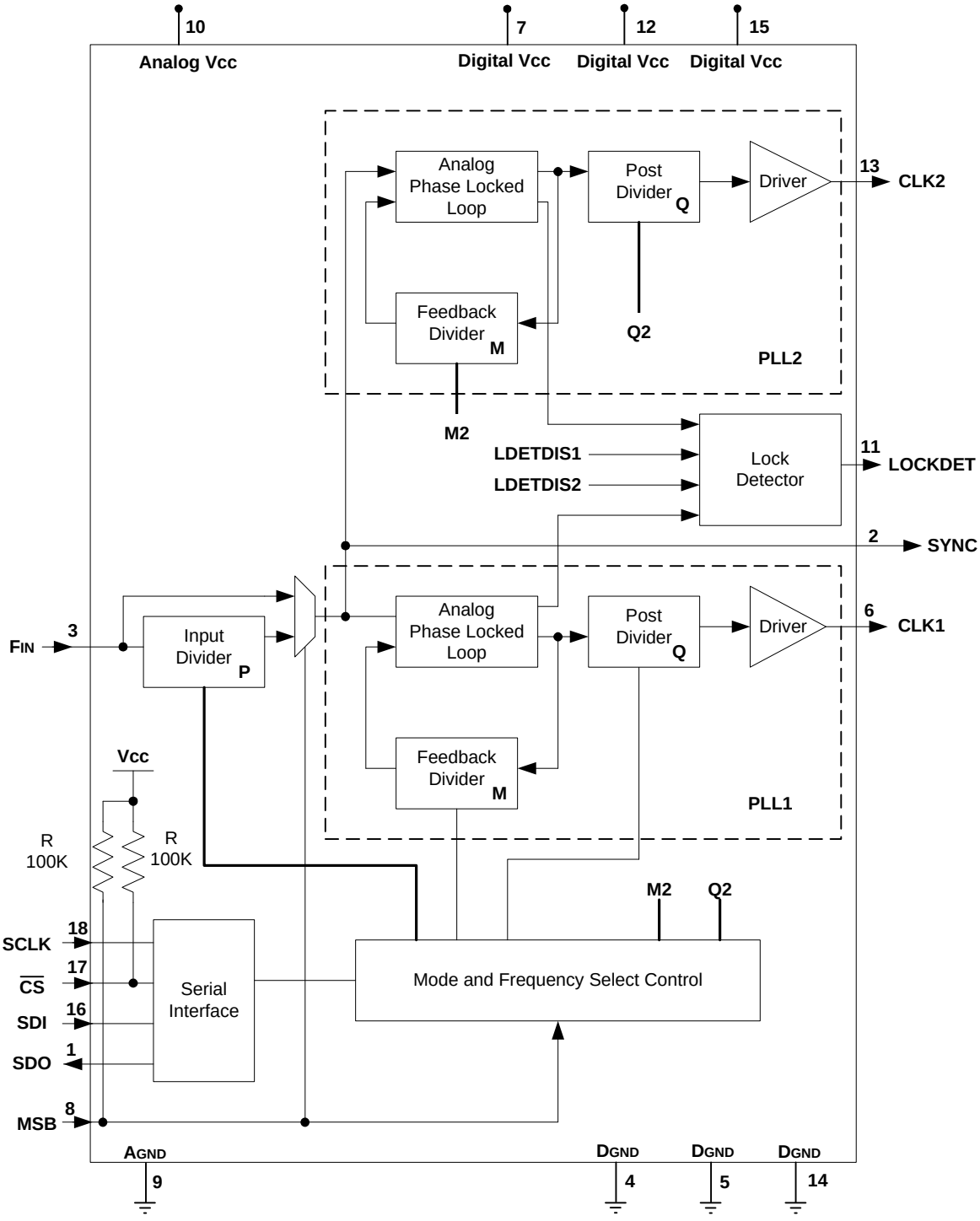


Figure 2. XRT8001 Block Diagram

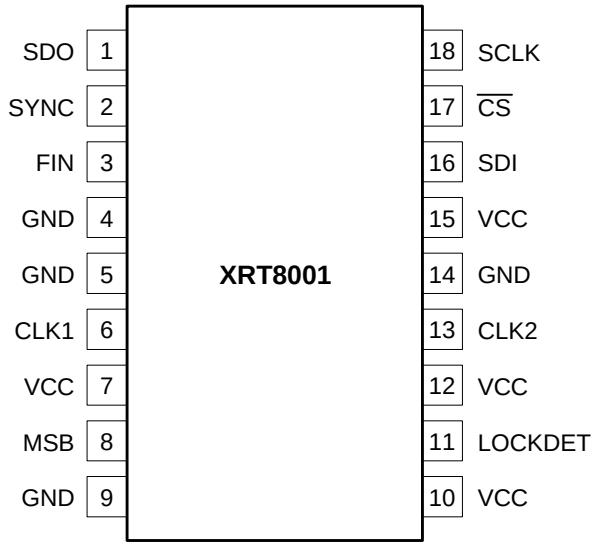


Figure 3. XRT8001 PIN OUT

PIN DESCRIPTION

Pin #	Name	Type	Description
1	SDO	O	**Serial Data Output from the Microprocessor Serial Interface** This pin will serially output the contents of the specified Command Register, during "Read" Operations. The data, on this pin, will be updated on the falling edge of the SCLK input signal. This pin will be tri-stated upon completion of data transfer.
2	SYNC	O	**Sync Output -** The XRT8001 will typically output an 8kHz clock signal via this output pin. However, when the XRT8001 is operating in the "High Speed - Reverse" Mode, then this device will simply output a 64kHz clock signal.
3	FIN	I	**Reference Clock Input -** The Reference Timing signal (from which the CLK1 and CLK2 output signals are derived) is to be input via this pin.
4	GND	-	**Digital Ground**
5	GND	-	**Digital Ground**
6	CLK1	O	**Clock Output 1 -** The XRT8001 will drive the desired "synthesized" signal via this output pin. This output signal will have a 50±5% duty cycle. ***Note:*** *This output pin is tri-stated unless the "CLK1EN" bit-field (within Command Register CR4) has been set to "1".*
7	V_{cc}	-	**Digital Power Supply**

PIN DESCRIPTION (CONT'D)

Pin #	Name	Type	Description
8	MSB	I	**Master/Slave Mode Select Input -** Setting this input pin "HIGH" configures the XRT8001 to operate in the "MASTER" Mode. Conversely, setting this input pin "LOW" configures the XRT8001 to operate in the "SLAVE" Mode.
9	GND	-	**Analog Ground**
10	VCC	-	**Analog Power Supply**
11	LOCKDET	O	**Lock Detect Output -** This output indicates whether or not the "selected" internal PLL(s) are "in-lock" or are "out-of-lock". By default, this output pin is "high" when both PLLs are in-lock" and will go toggle "low" if either one of the PLLs is "out-of-lock". However, the XRT8001 also permits the user to configure this output pin to reflect the state of any one of the PLLs within the chip. (See Table 3.)
12	VCC	-	**Digital Power Supply**
13	CLK2	O	**Clock Output 2 -** The XRT8001 will drive the desired "synthesized" signal via this output pin. This output signal will have a 50±5% duty cycle. ***Note:*** *This output pin is tri-stated unless the "CLK1EN" bit-field (within Command Register CR4) has been set to "1".*
14	GND	-	**Digital Ground**
15	VCC	-	**Digital Power Supply**
16	SDI	I	**Microprocessor Serial Interface – Serial Data Input** Whenever, the user wishes to read or write data into the Command Registers, over the Microprocessor Serial Interface, the user is expected to apply the "Read/Write" bit, the Address Values (of the Command Registers) and Data Value to be written (during "Write" Operations) to this pin. This input will be sampled on the rising edge of the SCLK pin (pin 18).
17	$\overline{CS}$	I	**Microprocessor Serial Interface – Chip Select Input:** The Local Microprocessor must assert this pin (e.g., set it to "0") in order to enable communication with the XRT8001 via the Microprocessor Serial Interface. ***Note:*** *This pin is internally pulled "high".*
18	SCLK	I	**Microprocessor Serial Interface-Clock Signal** This signal will be used to sample the data, on the SDI pin, on the rising edge of this signal. Additionally, during "Read" operations, the Microprocessor Serial Interface will update the SDO output on the falling edge of this signal.

ABSOLUTE MAXIMUM RATINGS

Supply Range 7V
Voltage at any Pin ..... GND -0.3V to Vcc+0.3V
Operating Temperature..... - 40°C to +85°C
Storage Temperature ..... - 40°C to +85°C
Package Dissipation 500mW

DC ELECTRICAL CHARACTERISTICS (Except Microprocessor Serial Interface)[1]

Symbol	Parameter	Min.	Typ.	Max.	Units	Condition
V_{IL}	Input Low Level			0.8	V	
V_{IH}	Input High Level	2.0			V	
V_{OL}	Output Low Level (CLK1, CLK2)			0.4	V	I_{OL} = -6.0mA
V_{OH}	Output High Level (CLK1, CLK2)	2.4			V	I_{OL} = 6.0mA
V_{OL}	Output Low Level (LOCKDET, SYNC)			0.4	V	I_{OL} = -3.0mA
V_{OH}	Output High Level (LOCKDET, SYNC)	2.4			V	I_{OL} = 3.0mA
I_{IL}	Input Low Current (CSB, MSB)			-150	mA	
I_{IH}	Input High Current (CSB, MSB)			10	mA	$V_{IN} = V_{CC}$
I_{IL}	Input Low Current (except CSB, MSB)	-10			mA	
I_{IH}	Input High Current (except CSB, MSB)			10	mA	$V_{IN} = V_{CC}$
I_{CC}	Operating Current		11 20	30 35	mA mA	3.3V, No Load, CLk1, CLK2 = 8 x 2.048MHz 5V, No Load, CLk1, CLK2 = 8 x 2.048MHz
R_{IN}	Internal Pull-up Resistance (CSB, MSB)	50	100	150	kW	

Note:
1. 5V tolerant input considerations when operating from 3.3V:

When the XRT8001 is powered at 3.3V, it can tolerate 5V-level signals via its inputs. However, the user should be aware the XRT8001 contains a "Factory-Test" Mode. This mode is enabled whenever the MSB (Master-Slave select) input pin is pulled to about 2V above VDD.

Therefore, if the user is powering the XRT8001 at 3.3V but is applying a 5.25V signal to the MSB input pin, then it is possible that the XRT8001 could be configured to operate in this "Factory-Test" Mode. Since all "Factory-Test" Mode registers are reset to "0", upon chip power, this should not be a problem for the user.

However, if the user performs write operations to "non-defined" address locations within the XRT8001, then the user may observe strange operation from the XRT8001. The user must make sure that when the Microcontroller performs WRITE operations to the XRT8001, it is only performing these WRITE operations to the Address Locations defined in the XRT8001 Data Sheet.

AC ELECTRICAL CHARACTERISTICS (See Figure 4.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t1	Input Frequency	0.008 0.008		32.7 32.7	MHz MHz	3.3V 5V
t2	Minimum Input Signal "High" to "Low" Duration	12			ns	
t3	Output Frequency	56		16,384	kHz	
t6[1]	Duty Cycle	47.5	50	52.5	%	VCC/2 switch point, 30pF Load
t7[4]	Jitter Added 8kHz – 40kHz		0.01 0.01	0.02 0.02	UI UI	3.3V, Output = 1.544MHz (0.025 UI)[3] 5V, Output = 1.544MHz (0.025 UI)[3]
t7[4]	Jitter Added 10Hz – 40kHz		0.03 0.03	 –	UI UI	3.3V, Output = 1.544MHz (0.025 UI)[3] 5V, Output = 1.544MHz (0.025 UI)[3]
t7[4]	Broadband Jitter		0.03 0.035	0.05 0.05	UI UI	3.3V, Output = 1.544MHz (0.05 UI)[3] 5V, Output = 1.544MHz (0.05 UI)[3]
t7[4]	Jitter Added 20Hz – 100kHz		 0.01	0.07 0.07	UI UI	3.3V, Output = 2.048MHz (1.5 UI)[3] 5V, Output = 2.048MHz (1.5 UI)[3]
t7[4]	Jitter Added 18kHz – 100kHz		 0.007	0.03 0.03	UI UI	3.3V, Output = 2.048MHz (0.2 UI)[3] 5V, Output = 2.048MHz (0.2 UI)[3]
t8	Capture Time			40 40	ms ms	3.3V 5V
t9	Clock Output Rise Time			10ns	ns	30pF load measured at 20/80%
t10	Clock Output Fall Time			10ns	ns	30pF load measured at 20/80%
t11[2]	SYNC Output Signal Duty Cycle	40		60	%	VCC/2 switch point
t12	SYNC Ouput Signal + ½ Cycle					
t13	SYNC Output Signal – ½ Cycle					
t14	Delay Time between the rising edge of of SYNC and the Rising edge of CLK1 and CLK2	t-20		t+20	ns	See Table 8 for values of "t"
t21	CSB Low to Rising Edge of SCLK Setup Time	50			ns	
t22	CSB High to Rising Edge of SCLK Hold Time	20			ns	
t23	SDI to Rising Edge of SCLK Setup Time	50			ns	
t24	SDI to Rising Edge of SCLK Hold Time	50			ns	
t25	SCLK "Low" Time	240			ns	
t26	SCLK "High" Time	240			ns	
t27	SCLK Period	500			ns	
t28	CSB Low to Rising Edge of SCLK Hold Time	50			ns	
t29	CSB "Inactive" Time	250			ns	
t30	Falling Edge of SCLK to SDO Valid Time			200	ns	
t31	Falling Edge of SCLK to SDO Invalid Time			100	ns	
t32	Falling Edge of SCLK, or rising edge of CSB to High Z		100		ns	
t33	Rise/Fall time of SDO Output			40	ns	
PW_{MIN}	F_{IN} Duty Cycle	12			ns	

Notes:

[1] $t6 = \frac{t4}{(t4 + t5)}$

[2] $t11 = \frac{t12}{(t12 + t13)}$

[3] *Specifications from AT&T Publication 62411 and ITU-T Recommendations G-823 (for 1.544MHz and (2.048MHz).*

[4] *t7 is guaranteed by characterization, not tested.*

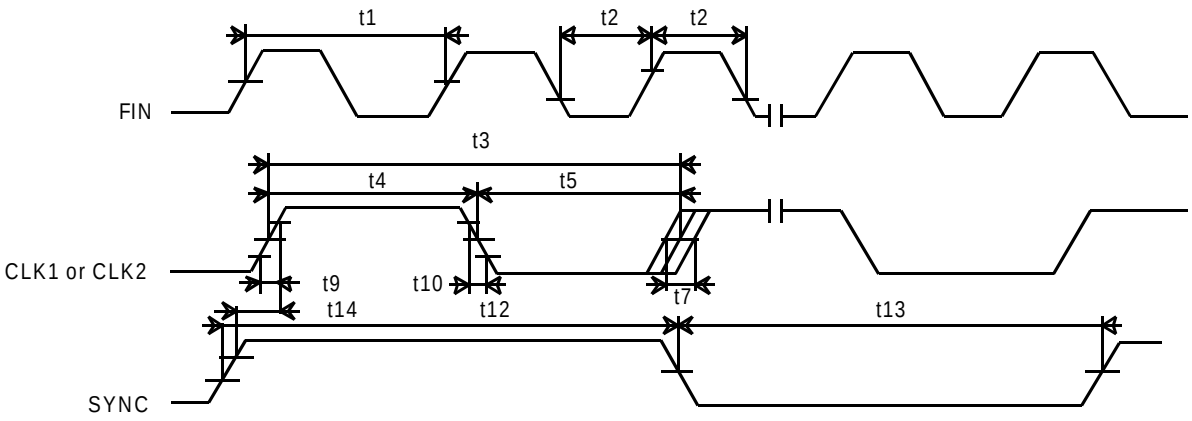


Figure 4. Timing Diagram for Clocks

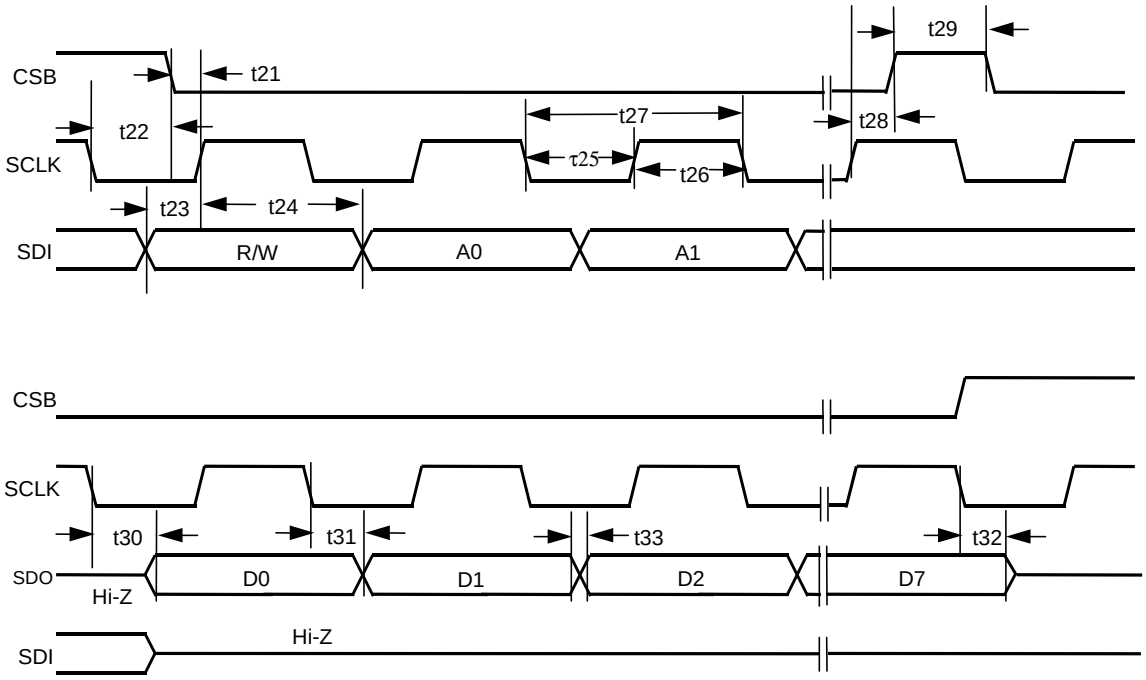


Figure 5. Timing Diagram for the Microprocessor Serial Interface

1.0 Operating the Microprocessor Serial Interface

The XRT8001 Serial Interface is a simple four-wire interface that is compatible with many of the microcontrollers available in the market. This interface consists of the following signals:

CSB - Chip Select (Active Low)
SCLK - Serial Clock
SDI - Serial Data Input
SDO - Serial Data Output

Using the Microprocessor Serial Interface

The following instructions, for using the Microprocessor Serial Interface, are best understood by referring to the diagram in Figure 19.

In order to use the Microprocessor Serial Interface the user must first provide a clock signal to the SCLK input pin. Afterwards, the user will initiate a "Read" or "Write" operation by asserting the "active-low" Chip Select input pin (CSB). It is important to assert the CSB pin (e.g., toggle it "low") at least 50ns prior to the very first rising edge of the clock signal.

Once the CSB input pin has been asserted, the type of operation and the target register address must now be specified by the user. The user provides this information to the Microprocessor Serial Interface by writing eight serial bits of data into the SDI input. Note: each of these bits will be "clocked" into the SDI input on the rising edge of SCLK. These eight bits are identified and described below.

Bit 1 - "R/W" (Read/Write) Bit

This bit will be clocked into the SDI input on the first rising edge of SCLK (after CSB has been asserted). This bit indicates whether the current operation is a "Read" or "Write" operation. A "1" in this bit specifies a "Read" operation; whereas, a "0" in this bit specifies a "Write" operation.

Bits 2 Through 5: The Four (4) Bit Address Values (Labeled A0, A1, A2 and A3)

The next four rising edges of the SCLK signal will clock in the 4-bit address value for this particular Read (or Write) operation. The address selects the Command Register, within the XRT8001, that the user will either be reading data from, or writing data to. The user must supply the address bits to the SDI input pin in ascending order with the LSB (least significant bit) first.

Bits 6 and 7:

The next two bits, A4 and A5, must be set to "0", as shown in Figure 19.

Bit 8 - A6

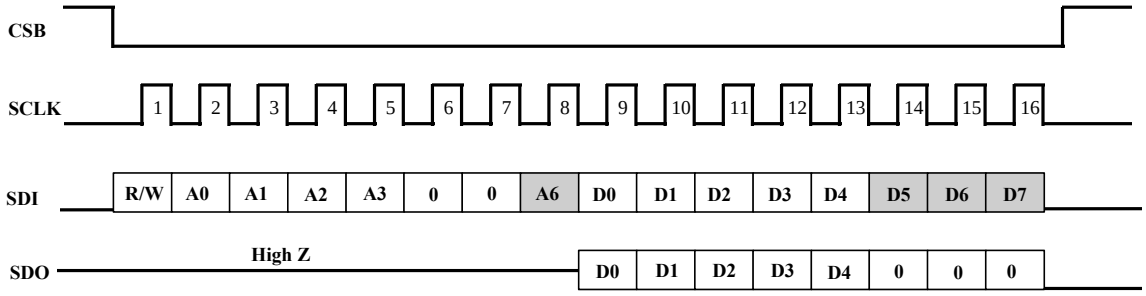
The value of "A6" is a "don't care". Once these first eight bits have been written into the Microprocessor Serial Interface, the subsequent action depends upon whether the current operation is a "Read" or "Write" operation.

Read Operation

Once the last address bit (A3) has been clocked into the SDI input, the "Read" operation will proceed through an idle period, lasting three SCLK periods. On the falling edge of SCLK Cycle #8 (see Figure 19) the serial data output signal (SDO) becomes active. At this point the user can begin reading the data contents of the addressed Command Register (at Address [A3, A2, A1, A0]) via the SDO output pin. The Microprocessor Serial Interface will output this 5-bit data word (D0 through D4) in ascending order (with the LSB first), on the falling edges of the SCLK pin. As a consequence, the data (on the SDO output pin) will be sufficiently stable for reading (by the Microprocessor), on the very next rising edge of the SCLK pin.

Write Operation

Once the last address bit (A3) has been clocked into the SDI input, the "Write" operation will proceed through an idle period, lasting three SCLK periods. Prior to the rising edge of SCLK Cycle # 9 (see Figure 6) the user must begin to apply the 8-bit data word, that he/she wishes to write to the Microprocessor Serial Interface, onto the SDI input pin. The Microprocessor Serial Interface will latch the value on the SDI input pin, on the rising edge of SCLK. The user must apply this word (D0 through D7) serially, in ascending order with the LSB first.



Notes:

A4 and A5 are always "0".

R/W = "1" for "Read" Operations

R/W = "0" for "Write" Operations

- Denotes a "don't care" value

Figure 6. Microprocessor Serial Interface Data Structure

Simplified Interface Option

The user can simplify the design of the circuitry connecting to the Microprocessor Serial Interface by tying both the SDO and SDI pins together, and reading data from and/or writing data to this "combined" signal. This simplification is possible because only one of these signals are active at any given time. The inactive signal will be tri-stated.

2.1 The Forward/Master Mode

In the Forward/Master Mode, the XRT8001 will accept either an “N x 1.544MHz” or an “N x 2.048MHz” clock signal via the FIN input pin (where: $1 \leq N \leq 16$). From this “reference signal” the XRT8001 will generate either a “K x 56kHz” or a “K x 64kHz” clock signal (where: $1 \leq K \leq 32$).

Figure 7, presents a simple illustration of the XRT8001 WAN Clock operating in the “Forward Master/Mode.”

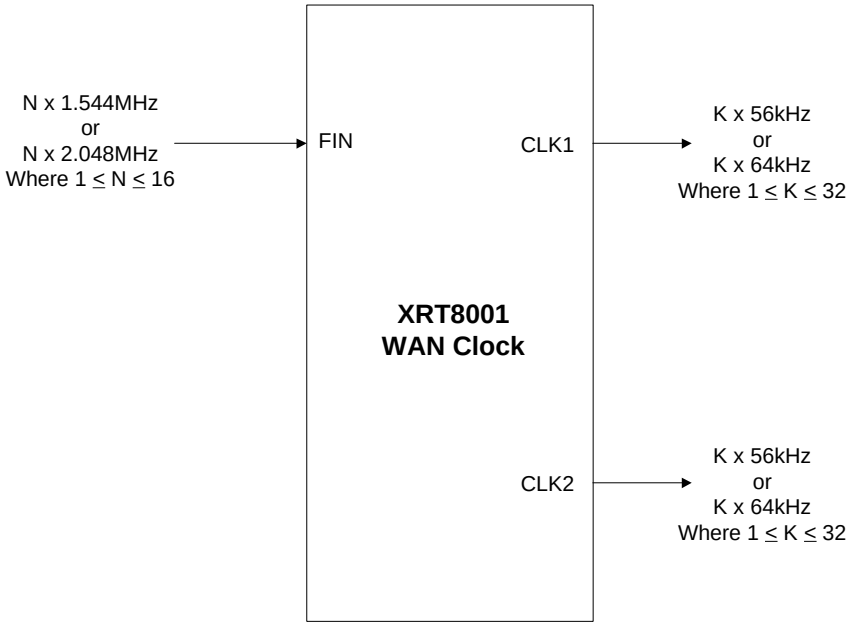


Figure 7. Illustration of the XRT8001 WAN Clock Operating in the Forward/Master Mode

2.2 The Reverse/Master Mode

In the Reverse/Master Mode, the XRT8001 will accept either a 56kHz or a 64kHz clock signal via the FIN input pin, and will generate either a 1.544MHz or a 2.048MHz clock signal via the Clock Output signals.

Figure 8, presents a simple illustration of the XRT8001 WAN Clock operating in the "Reverse/Master Mode."

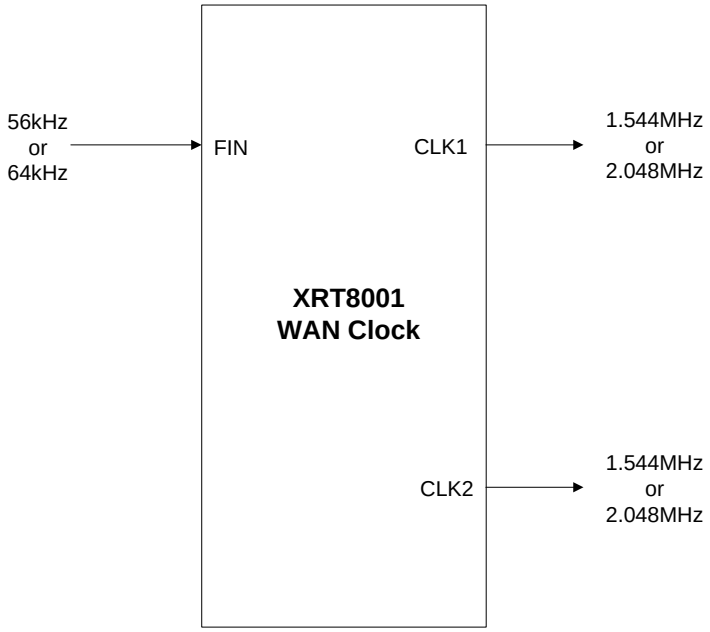


Figure 8. Illustration of the XRT8001 WAN Clock Operating in the Reverse/Master Mode

2.3 The Fractional T1/E1 Reverse/Master Mode

In the Fractional T1/E1 Reverse/Master Mode, the XRT8001 will accept either a “P x 56kHz” or a “P x 64kHz” clock signal via the FIN input pin (where: $1 \leq P \leq 32$). From this “reference signal” the XRT8001 will generate either a 1.544MHz or a 2.048MHz clock signal.

Figure 9, presents a simple illustration of the XRT8001 WAN Clock operating in the “Fractional T1/E1 Reverse/Master" Mode.

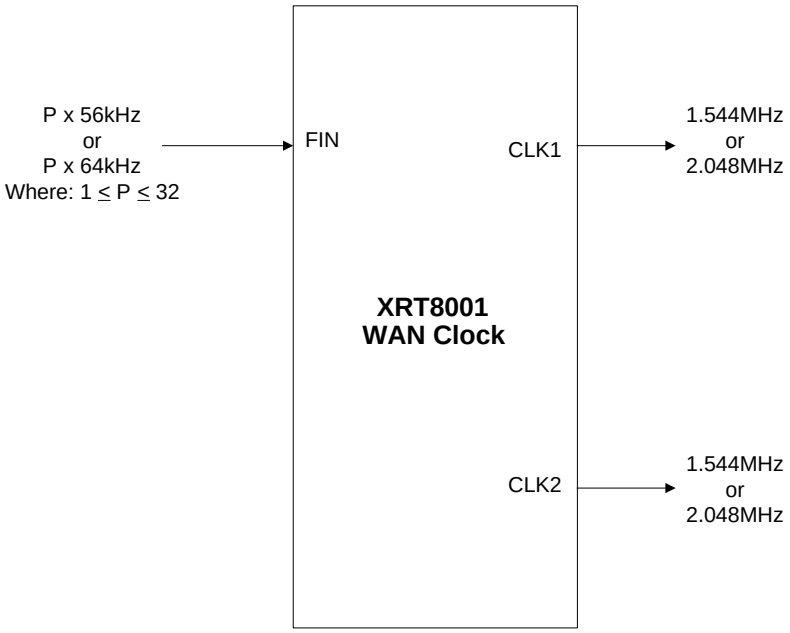


Figure 9. Illustration of the XRT8001 WAN Clock Operating in the “Fractional T1/E1 Reverse/Master” Mode

2.4 The "E1 to T1 Forward/Master" Mode

In the "E1 to T1 Forward/Master" Mode, the XRT8001 will accept a "Q x 2.048MHz" clock signal via the "Reference Clock Input" (FIN), and will output a "1.544MHz" clock signal via the CLK1 and/or CLK2 output pins.

Note: *The value of "Q" can range between 1 and 16.*

Figure 10, presents a simple illustration of the XRT8001 WAN Clock operating in the "E1 to T1 Forward/Master" Mode.

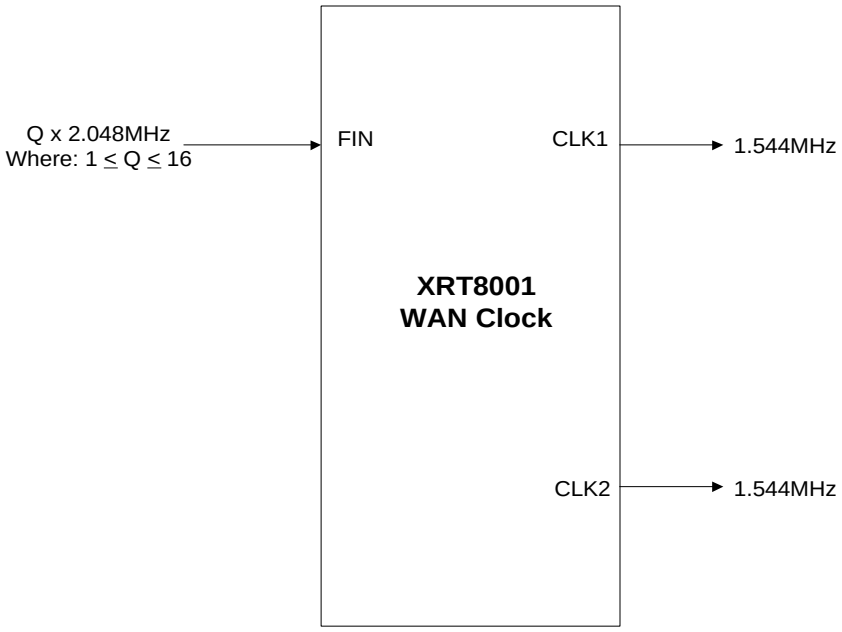


Figure 10. Illustration of the XRT8001 WAN Clock Operating in the "E1 to T1 Forward/Master" Mode

2.5 The "High Speed – Reverse" Mode

In the "High Speed - Reverse" Mode, the XRT8001 will accept a 64kHz clock signal via the "Reference Clock Input" (FIN), and will output a "M x 2.048MHz" clock signal (where M can be equal to 1, 2, 4 or 8) via the CLK1 and/or CLK2 output pins.

Note: The XRT8001 will accept and sythesze these clock frequencies independent of whether it has been configured to operate in the "Master" or "Slave" Modes.

Figure 11, presents a simple illustration of the XRT8001 WAN Clock operating in the "High Speed - Reverse" Mode.

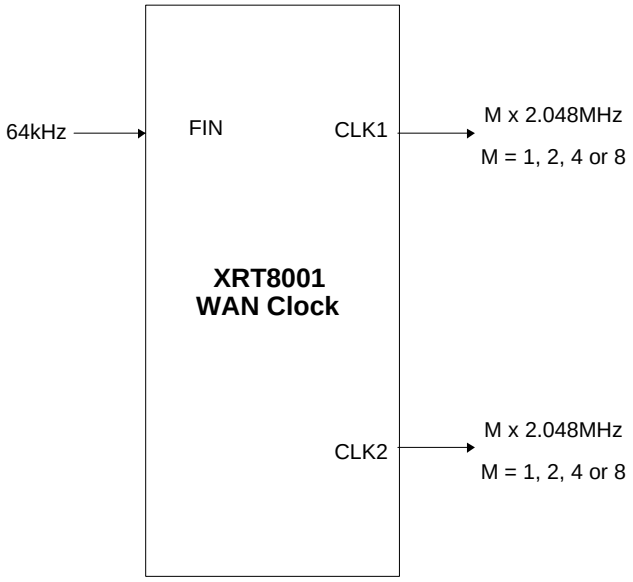


Figure 11. Illustration of the XRT8001 WAN Clock Operating in the "High Speed – Reverse" Mode

2.6 The "Forward/Slave" Mode

In the "Forward/Slave" Mode, the XRT8001 will accept an 8kHz clock signal via the Reference Clock Input (FIN), and will output a "L x 64kHz or L x 56kHz" clock signal (where L can range from 1 to 32) via the CLK1 and CLK2 output pins.

Figure 12 presents a simple illustration of the XRT8001 WAN Clock operating in the "Forward/Slave" Mode.

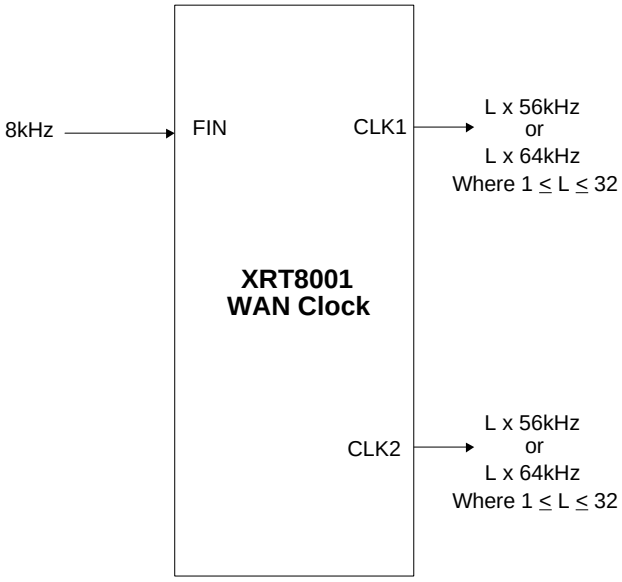


Figure 12. Illustration of the XRT8001 WAN Clock Operating in the "Forward/Slave" Mode

3.0 Description of the Command Registers

3.1 Address Map of the "On-Chip" Command Registers

			Register Bit-Format				
Address	**Command Register**	**Type**	**D4**	**D3**	**D2**	**D1**	**D0**
0x00	CR0	R/W	IOC4	IOC3	IOC2	IOC1	PL1EN
0x01	CR1	R/W	M4	M3	M2	M1	PL2EN
0x02	CR2	R/W	SEL14	SEL13	SEL12	SEL11	SEL10
0x03	CR3	R/W	SEL24	SEL23	SEL22	SEL21	SEL20
0x04	CR4	R/W	SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
0x05	CR5	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x06	CR6	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x07	CR7	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

3.2 Command Register Description

3.2.1 Command Register CR0 (Address = 0x00)

D4 – D1 (Configuration Mode Select Bits)

These four-bit fields permit the user to select which mode the XRT8001 will operate in. Specifically, these four bit-fields make the following configuration selections:

1. Whether the XRT8001 will be operating in the “Forward/Master”, “Reverse/Master”, “Fractional T1/E1 Reverse/Master”, "E1 to T1 - Forward/Master" and “High Speed - Reverse” odes.
2. What kind of input signals are to be applied to the Reference Clock Input (FIN).
3. What kind of signals will be output via the CLK1 and CLK2 output pins.

Table 2A relates the value of these four bit-fields to the four Master Modes and Table 2B relates to the three Slave Modes of the XRT8001.

D[4:1]	Mode	Input Frequency (at the FIN input)	CLK1 Output Signal	CLK2 Output Signal
0000	Forward/Master	N x 1.544MHz	K x 56kHz	K x 56kHz
0001	Forward/Master	N x 1.544MHz	K x 56kHz	K x 64kHz
0010	Forward/Master	N x 1.544MHz	K x 64kHz	K x 64kHz
0011	Reverse/Master	56kHz	1.544MHz	2.048MHz
0100	Forward/Master	N x 2.048MHz	K x 56kHz	K x 56kHz
0101	Forward/Master	N x 2.048MHz	K x 56kHz	K x 64kHz
0110	Forward/Master	N x 2.048MHz	K x 64kHz	K x 64kHz
0111	Reverse/Master	64kHz	1.544MHz	2.048MHz
1000	E1 to T1 – Forward/Master	Q x 2.048MHz	1.544MHz	1.544MHz
1001	Fract. T1/E1 Reverse/Master	P x 56kHz	1.544MHz	2.048MHz
1010	Fract. T1/E1 Reverse/Master	P x 56kHz	1.544MHz	1.544MHz
1011	Fract. T1/E1 Reverse/Master	P x 64kHz	2.048MHz	1.544MHz
1100	Fract. T1/E1 Reverse/Master	P x 64kHz	2.048MHz	2.048MHz
1101	High Speed - Reverse	64 kHz	M x 2.048MHz	M x 2.048MHz
1110	Reserved	Reserved	Reserved	Reserved
1111	Reserved	Reserved	Reserved	Reserved

Table 1. Relationship between the value of "D4 – D1 (within Command Register CR0) and the Operating Modes of the XRT8001 WAN Clock - Master Modes

D[4:1]	Mode	Input Frequency (at the FIN input)	CLK1 Output Signal	CLK2 Output Signal
0000	Forward/Slave	8kHz	K x 56kHz	K x 56kHz
0001	Forward/Slave	8kHz	K x 56kHz	K x 64kHz
0010	Forward/Slave	8kHz	K x 64kHz	K x 64kHz
0011	Reverse/Slave	8kHz	1.544MHz	2.048MHz
0100	Forward/Slave	8kHz	K x 56kHz	K x 56kHz
0101	Forward/Slave	8kHz	K x 56kHz	K x 64kHz
0110	Forward/Slave	8kHz	K x 64kHz	K x 64kHz
0111	Reverse/Slave	8kHz	1.544MHz	2.048MHz
1000	Reverse/Slave	8kHz	K x 56KHz	K x 64KHz
1001	Reverse/Slave	8kHz	1.544MHz	2.048MHz
1010	Reverse/Slave	8kHz	1.544MHz	1.554MHz
1011	Reverse/Slave	8kHz	2.048MHz	1.544MHz
1100	Reverse/Slave	8kHz	2.048MHz	2.048MHz
1101	High Speed – Reverse	64kHz	M x 2.048MHz	M x 2.048MHz
1110	Reserved	Reserved	Reserved	Reserved
1111	Reserved	Reserved	Reserved	Reserved

Table 2. Relationship between the value of "D4 – D1" (within Command Register CR0) and the Operating Modes of the XRT8001 WAN Clock – Slave Modes

D0 – PL1EN (PLL # 1 Enable Select)

This bit-field permits the user to enable or disable PLL # 1, within the XRT8001 WAN Clock. Setting this bit-field to "1" enables PLL # 1 for Frequency Synthesis. Conversely, setting this bit-field to "0" disables PLL # 1 for Frequency Synthesis.

3.2.2 Command Register CR1 (Address = 0x01)

D4 – D1: (M4 – M1)

These bit-fields are used to support configuration implementation for both the "Forward/Master" and "E1 to T1 - Forward/Master" Modes. In both the "Forward/Master" and "E1 to T1 - Forward/Master" Modes, the XRT8001 WAN Clock will be receiving either a "N x 1.544MHz" or a "N x 2.048MHz" clock signal. The M4 through M1 bit-fields, within this register, permit the user to specify the value of "N". As a consequence, the XRT8001 can be configured to accept a maximum frequency of "16 x 1.544MHz" or "16 x 2.048MHz".

D0 – PL2EN (PLL # 2 Enable Select)

This bit-field permits the user to enable or disable PLL # 2, within the XRT8001 WAN Clock. Setting this bit-field to "1" enables PLL # 2 for Frequency Synthesis. Conversely, setting this bit-field to "0" disables PLL # 2 for Frequency Synthesis.

3.2.3 Command Register CR2 (Address = 0x02)

D4 – D0 (SEL1[4:0])

These bit-fields are used to support configuration implementation for both the "Forward/Master", "Fractional T1/E1 Reverse/Master" and "High Speed – Reverse" Modes.

In the Forward/Master Mode

In the "Forward/Master" Mode, the XRT8001 WAN Clock will output either a "K x 56kHz" or a "K x 64kHz" clock signal via the CLK1 output pin. These five (5) bit-fields within Command Register CR2 are used to define the value of "K" for the CLK1 Output. As a consequence, the XRT8001 can be configured to generate a maximum frequency of "32 x 56kHz" or "32 x 64kHz" via the CLK1 output pin.

In the "Fractional T1/E1 Reverse/Master" Mode

In the "Fractional T1/E1 Reverse/Master" Mode, the XRT8001 WAN Clock will be receiving either a "P x 56kHz" or a "P x 64kHz" clock signal via the "FIN" input pin. The XRT8001 WAN Clock will, in response, generate either a 1.544MHz or a 2.048MHz clock signal via the CLK1 and/or CLK2 output pins. These five (5) bit-fields are used to define the value of "P". As a consequence, the XRT8001 can be configured to accept a maximum frequency of "32 x 56kHz" or "32 x 64kHz".

In the "High Speed – Reverse" Mode

In the "High Speed – Reverse" Mode, the XRT8001 WAN Clock will be receiving a 64kHz clock signal via the "FIN" input pin. The XRT8001 WAN Clock will, in response, generate an "M x 2.048MHz" clock via the CLK1 and CLK2 output pins. These five (5) bit-fields within Command Register CR2 are used to define the value "M" for the CLK1 output.

Note: *The only acceptable values for "M" are 1, 2, 4, or 8.*

3.2.4 Command Register CR3 (Address = 0x03)

D4 – D0 (SEL2[4:0])

These bit-fields are used to support configuration implementation for the "Forward/Master" and the "High Speed – Reverse" Modes of operation.

In the "Forward/Master" Mode

In the "Forward/Master" Mode, the XRT8001 WAN Clock will output either a "K x 56kHz" or a "K x 64kHz" clock signal via the CLK2 output pin. These five (5) bit-fields within Command Register CR3 are used to define the value of "K" for the CLK2 Output. As a consequence, the XRT8001 can be configured to generate a maximum frequency of "32 x 56kHz" or "32 x 64kHz" via the CLK2 output pin.

In the "High Speed – Reverse" Mode

In the "High Speed – Reverse" Mode, the XRT8001 WAN Clock will be receiving a 64kHz clock signal via the "FIN" input pin. The XRT8001 WAN Clock will, in response, generate an "M x 2.048MHz" clock via the CLK1 and CLK2 output pins. These five (5) bit-fields within Command Register CR3 are used to define the value "M" for the CLK2 output.

Note: *The only acceptable values for "M" are 1, 2, 4, or 8.*

3.2.5 Command Register CR4 (Address = 0x04)

D4 – SYNCEN (SYNC Output Driver Enable Select)

This "read/write" bit-field permits the user to enable or disable the Driver associated with the SYNC output pin. Setting this bit-field to "1" enables this Driver. Setting this bit-field to "0" disables this Driver.

D3 – CLK1EN (CLK1 Output Driver Enable Select)

This "read/write" bit-field permits the user to enable or disable the Driver associated with the CLK1 output pin. Setting this bit-field to "1" enables this Driver. Setting this bit-field to "0" disables this Driver.

D2 – CLK2EN (CLK2 Output Driver Enable Select)

This "read/write" bit-field permits the user to enable or disable the Driver associated with the CLK2 output pin. Setting this bit-field to "1" enables this Driver. Setting this bit-field to "0" disables this Driver.

D1, D0 – LDETDIS[2:1] – Lock Detector Output Control

The combination of these two bit-fields permit the user to specify the signal that will be output via the LOCKDET output pin. The user's options are shown in Table 3.

LDETDIS[2:1]	Signal output via the LOCKDET Signal
00	**The LOCK Condition of PLL1 AND PLL2** With this selection, the LOCKDET output pin will be "high" if either one of the following conditions are true. a. If both PLL1 and PLL2 are in the "LOCK" condition, (**applies if both PLL1 and PLL2 are enabled**) or b. If the only enabled PLL is in the "LOCK" condition (**applies only if one of the PLLs are enabled**).
01	**The LOCK Condition of PLL2 Only** With this selection, only the "LOCK" state of PLL2 will be reflected in the LOCKDET output pin. LOCKDET = "high" if PLL2 is in "LOCK". LOCKDET = "low" if PLL2 is out of "LOCK".
10	**The LOCK Condition of PLL1 Only** With this selection, only the "LOCK" state of PLL1 will be reflected in the LOCKDET output pin. LOCKDET = "high" if PLL1 is in "LOCK". LOCKDET = "low" if PLL1 is out of "LOCK".
11	LOCKDET will be unconditionally pulled to "LOW"

Table 3. Relationship Between the Values of the LDETDIS[2:1] Bit-Fields and the Meaning of the LOCKDET Output Signal

4.0 Instructions for Configuring the XRT8001 WAN Clock

As mentioned earlier, the XRT8001 WAN Clock can be configured to operate in the following modes:

- The "Forward/Master" Mode
- The "Reverse/Master" Mode
- The "Fractional T1/E1 Reverse/Master" Mode
- The "E1 to T1 – Forward/Master" Mode
- The "High Speed – Reverse" Mode
- The "Forward/Slave" Mode

A detailed description of the operation and the configuration steps for each of these configurations follows.

4.1 The "Forward/Master" Mode.

When the XRT8001 WAN Clock has been configured to operate in the "Forward/Master" Mode, then it will accept an "N x 1.544MHz" or an "N x 2.048MHz" clock signal via the "Reference Clock" input at FIN (pin 3); where "N" can range anywhere between 1 and 16. In response to this clock signal, the XRT8001 WAN Clock will output either a "K x 56kHz" or a "K x 64kHz" clock signal, via the Clock Output pins (CLK1 and/or CLK2).

A simple illustration of the XRT8001 WAN Clock, operating in the "Forward/Master" Mode is shown in figure 13.

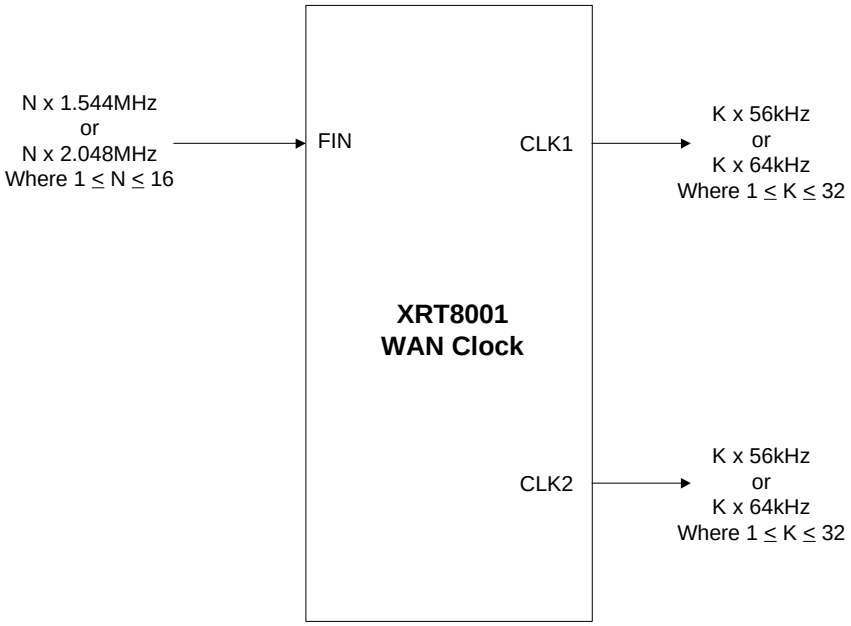


Figure 13. Illustration of the XRT8001 WAN Clock Device Operating in the "Forward/Master" Mode

5.0 Configuring the XRT8001 WAN Clock into the "Forward/Master" Mode

The user can configure the XRT8001 WAN Clock to operate in the "Forward/Master" Mode, by executing the following steps:

Step 1 *– Configure the XRT8001 to operate in the "MASTER" Mode, by pulling the MSB pin (pin 8) to VDD.*

Step 2 *– Review Table 4, and determine which combination of "Input Frequency" and "Output Frequencies" (via PLL1 and PLL2) correlate with the desired configuration.*

Input Frequency	PLL1 Output Frequency	PLL2 Output Frequency	Value to Write to D4-D1 in CR0
N x 1.544MHz	K x 56kHz	K x 56kHz	0000
N x 1.544MHz	K x 56kHz	K x 64kHz	0001
N x 1.544MHz	K x 64kHz	K x 64kHz	0010
N x 2.048MHz	K x 56kHz	K x 56kHz	0100
N x 2.048MHz	K x 56kHz	K x 64kHz	0101
N x 2.048MHz	K x 64kHz	K x 64kHz	0110

Table 4. Listing of "Input Frequency and "Output Frequency" Cases for "Forward/Master" Mode Operation

Step 3 *– Upon reviewing Table 4, write the listed value (under the "Value to Write to D4 – D1 in CR0" Register Column) into the D4 through D1 bit-fields within Command Register CR0, as illustrated below.*

Command Register CR0 (Address = 0x00)

D4	D3	D2	D1	D0
IOC4	IOC3	IOC2	IOC1	PL1EN
Value to Write to D4 – D1 in CR0				X

Note: *If the user wishes to output a clock signal via the CLK1 output signal, then he/she should also write a "1" into the "PL1EN" bit-field within Command Register CR0.*

This step configures the XRT8001 to operate in the "Forward/Master" Mode.

Step 4 *– Next, you need to specify the value for "N" (e.g., as in the "N x 1.544MHz" or "N x 2.048MHz" clock signal which is to be applied to the "FIN" input pin.)*

In order to specify the value for "N", one needs to write the value of "N - 1" (in binary format) into the "D4 through D1" bits within Command Register CR1, as illustrated below.

Command Register, CR1 (Address = 0x01)

D4	D3	D2	D1	D0
M4	M3	M2	M1	PL2EN
Value of "N - 1" (in Binary Format)				X

For example, if the user wishes to configure the XRT8001 to accept a 1.544MHz clock signal, via the "FIN" input pin (e.g., N = 1), then the user should write in the value "0", into Command Register CR1.

Note: *If the user wishes to output a clock signal via the CLK2 output signal, then he/she should also write a "1" into the "PL2EN" bit-field within Command Register CR1.*

Step 5 *– Specify the value of "K" (e.g., as in the "K x 56kHz" or "K x 64kHz" clock signal which is to be output via the CLK1 output signal).*

In order to specify the value for "K", one needs to write the value of "K - 1" (in binary format) into Command Register CR2, as illustrated below.

Command Register, CR2 (Address = 0x02)

D4	D3	D2	D1	D0
SEL14	SEL13	SEL12	SEL11	SEL10
Value of "K - 1" (in Binary Format).				

For example, if one wishes to configure the XRT8001 to output a clock signal of either "56kHz" or "64kHz" (e.g., where "K" = 1) via the CLK1 output pin, then he/she should write the value "0", into Command Register CR2.

Step 6 *– Specify the value of "K" (e.g., as in the "K x 56kHz" or "K x 64kHz" clock signal which is to be output via the CLK2 output signal).*

In order to specify the value for "K", one needs to write the value of "K - 1" (binary format) into Command Register CR3, as illustrated below.

Command Register, CR3 (Address = 0x03)

D4	D3	D2	D1	D0
SEL24	SEL23	SEL22	SEL21	SEL20
Value of "K - 1" (in Binary Format).				

For example, if one wishes to configure the XRT8001 to output a clock signal of either "1.792MHz" or "2.048MHz" (e.g., where "K" = 32) via the CLK2 output pin, then he/she should write the value "31" (or "1 1 1 1 1" in binary format) into Command Register CR3.

Step 7 *– Enable any of the following output signals as appropriate: "SYNC", "CLK1", "CLK2" and "LOCKDET".*

This is accomplished by writing a "1" into the corresponding bit-fields, within Command Register CR4, as illustrated below.

Command Register CR4, (Address = 0x04)

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
1	1	1	0	0

Note: *For information on the "LDETDIS1" and "LDETDIS2" bit-fields, please see Table 3.*

6.0 The "Reverse/Master" Mode

When the XRT8001 WAN Clock has been configured to operate in the "Reverse/Master" Mode, then it will accept either a "56kHz" or a "64kHz" clock signal via the "Reference Clock" input at FIN (pin 3). In response to this clock signal, the XRT8001 WAN Clock will output either a "1.544MHz" or a "2.048MHz" clock signal, via the Clock Output pins (CLK1 and/or CLK2).

A simple illustration of the XRT8001 WAN Clock, operating in the "Reverse/Master" Mode is presented in Figure 14.

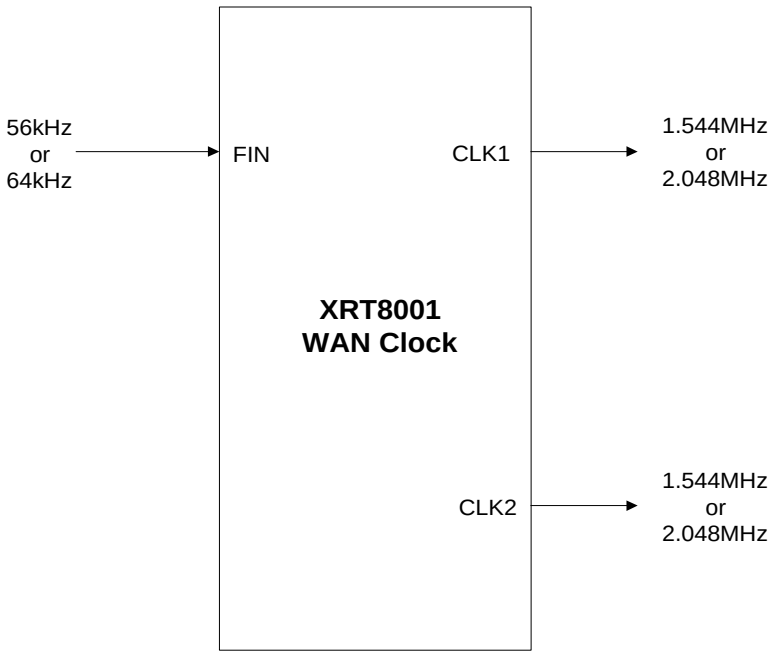


Figure 14. Illustration of the XRT8001 WAN Clock Operating in the "Reverse/Master" Mode

6.1 Configuring the XRT8001 WAN Clock Device into the "Reverse/Master" Mode

The user can configure the XRT8001 WAN Clock to operate in the "Reverse/Master" Mode, by executing the following steps:

Step 1 *– Configure the XRT8001 to operate in the "MASTER" Mode by pulling the "MSB" pin (pin 8) to VDD.*

Step 2 *– Review Table 5, and determine which combination of "Input Frequency" and "Output Frequencies" (via PLL1 and PLL2) correlate with the desired configuration.*

Input Frequency	PLL1 Output Frequency	PLL2 Output Frequency	Value to Write to D4 – D1 in CR0
56kHz	1.544MHz	2.048MHz	0011
64kHz	1.544MHz	2.048MHz	0111

Table 5. Listing of "Input Frequency" and "Output Frequency" Cases for "Reverse/Master" Mode Operation

Step 3 *– Upon reviewing Table 5, write the listed value (under the "Value to Write to D4 – D1 in CR0" register) into the D4 through D1 bit-fields within Command Register CR0, as illustrated below:*

Command Register CR0 (Address = 0x00)

D4	D3	D2	D1	D0
IOC4	IOC3	IOC2	IOC1	PL1EN
Value to Write to D4 – D1 in CR0				X

Note: *If the user wishes to output a clock signal via the CLK1 output signal, then he/she should also write a "1" into the "PL1EN" bit-field within Command Register CR0.*

This step configures the XRT8001 to operate in the "Reverse/Master" Mode.

Step 4 *– Write a "1" into the "PL2EN" bit-field within Command Register CR1 (if you wish to output a clock signal via the "CLK2" output pin), as illustrated below:*

Command Register, CR1 (Address = 0x01)

D4	D3	D2	D1	D0
M4	M3	M2	M1	PL2EN
Don't Care				1

Notes:

1. *The value of the "D4 through D1" bit-fields within Command Register, CR1 are "Don't Care".*
2. *The contents of Command Registers CR2 and CR3 are "Don't Care".*

Step 5 *– Enable any of the following output signals as appropriate: SYNC", CLK1, CLK2 and LOCKDET.*

This is accomplished by writing a "1" into the corresponding bit-fields, within Command Register CR4, as illustrated below:

Command Register CR4, (Address = 0x04)

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
1	1	1	0	0

Note: *For information on the "LDETDIS1" and "LDETDIS2" bit-fields, please see Table 3.*

6.2 The "Fractional T1/E1 Reverse/Master" Mode

When the XRT8001 WAN Clock has been configured to operate in the "Fractional T1/E1 Reverse/Master" Mode, then it will accept either a "P x 56kHz" or a "P x 64kHz" clock signal via the "FIN" input pin (pin 3). In response, the XRT8001 will output either a 1.544MHz or a 2.048MHz clock signal via the CLK1 and/or CLK2 outputs.

A simple illustration of the XRT8001 WAN Clock, operating in the "Fractional T1/E1 Reverse/Master" Mode is presented in Figure 15.

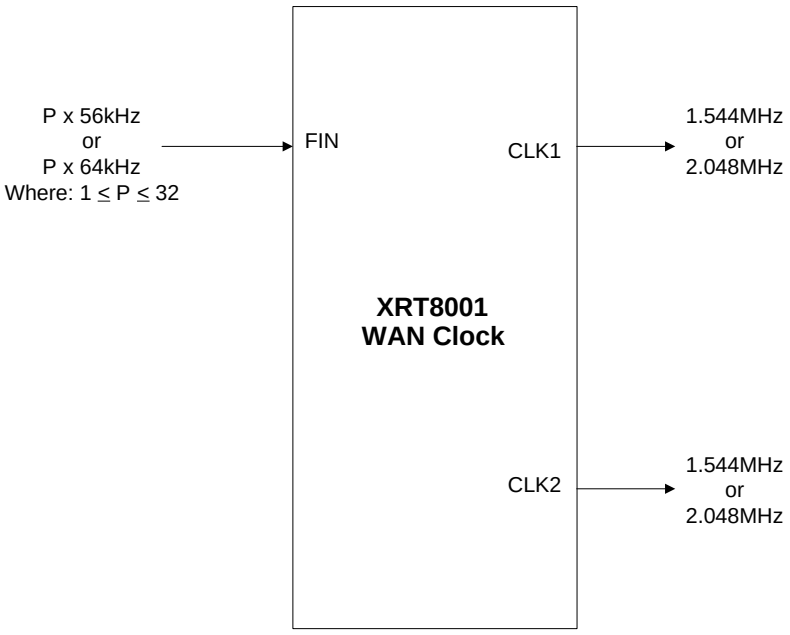


Figure 15. Illustration of the XRT8001 WAN Clock Operating in the "Fractional T1/E1 Reverse/Master" Mode

6.3 Configuring the XRT8001 WAN Clock into the "Fractional T1/E1 Reverse/Master" Mode

The user can configure the XRT8001 WAN Clock to operate in the "Fractional T1/E1 Reverse/Master" Mode by executing the following steps.

Step 1 *– Configure the XRT8001 to operate in the "MASTER" Mode, by pulling the "MSB" input pin (pin 8) to VDD.*

Step 2 *– Review Table 6, and determine which combination of "Input Frequency" and "Output Frequencies" (via PLL1 and PLL2) correlate with the desired configuration.*

Input Frequency	PLL1 Output Frequency	PLL2 Output Frequency	Value to Write to D4 – D1 in CR0
P x 56kHz	1.544MHz	2.048MHz	1001
P x 56kHz	1.544MHz	1.544MHz	1010
P x 64kHz	2.048MHz	1.544MHz	1011
P x 64kHz	2.048MHz	2.048MHz	1100

Table 6. Listing of "Input Frequency" and "Output Frequency" Cases for "Fractional T1/E1 Reverse/ Master" Mode Operation

Step 3 *– Upon reviewing Table 6, write the listed value (under the "Value to Write to D4 – D1 in CR0" register) into the D4 through D1 bit-fields within Command Register CR0, as illustrated below:*

Command Register CR0 (Address = 0x00)

D4	D3	D2	D1	D0
IOC4	IOC3	IOC2	IOC1	PL1EN
Value to Write to D4 – D1 in CR0				X

Notes:

1. *If the user wishes to output a clock signal via the CLK1 output signal, then he/she should also write a "1" into the "PL1EN" bit-field within Command Register CR0.*
2. *The contents of bit-fields D4 through D1 (within Command Register CR1) are "Don't Care"*
3. *If the user wishes to output a clock signal via the CLK2 output signal, then he/she should also write a "1" into the "PL2EN" bit-field within Command Register CR1.*

This step configures the XRT8001 to operate in the "Fractional T1/E1 Reverse/Master" Mode.

Step 4 *– Specify the value of "P" (e.g., as in the "P x 56kHz" or "P x 64kHz" clock signal which is to be input via the FIN Reference Clock input).*

In order to specify the value for "P", one needs to write in the value of "P - 1" (binary format) into Command Register CR2, as illustrated below:

Command Register, CR2 (Address = 0x02)

D4	D3	D2	D1	D0
SEL14	SEL13	SEL12	SEL11	SEL10
Value of "P - 1" (in Binary Format).				

In other words, if one intends to input either a "56kHz" or "64kHz" clock signal via the "FIN" input pin (e.g., where P = 1), then he/she should write a "0" into Command Register CR2.

Step 5 *– Write the binary expression "11111" into Command Register CR3.*

This step is necessary in order to insure proper operation of the XRT8001. This step is also illustrated below:

Command Register, CR3 (Address = 0x03)

D4	D3	D2	D1	D0
SEL24	SEL23	SEL22	SEL21	SEL20
1	1	1	1	1

Step 6 *– Enable any of the following output signals as appropriate: "SYNC", "CLK1", "CLK2" and "LOCKDET".*

This is accomplished by writing a "1" into the corresponding bit-fields, within Command Register CR4, as illustrated below:

Command Register CR4, (Address = 0x04)

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
1	1	1	0	0

6.4 The "E1 to T1 –Forward/Master" Mode

When the XRT8001 WAN Clock has been configured to operate in the "E1 to T1 – Forward/Master" Mode, then it will accept a "Q x 2.048MHz" clock signal via the "Reference Clock" input at FIN (pin 3), where "Q" can range anywhere between 1 - 16. In response to this clock signal, the XRT8001 WAN Clock will output a 1.544MHz clock signal via the Clock Output pins (CLK1 and/or CLK2).

A simple illustration of the XRT8001 WAN Clock, operating in the "E1 to T1 - Forward/Master" Mode is presented in Figure 16.

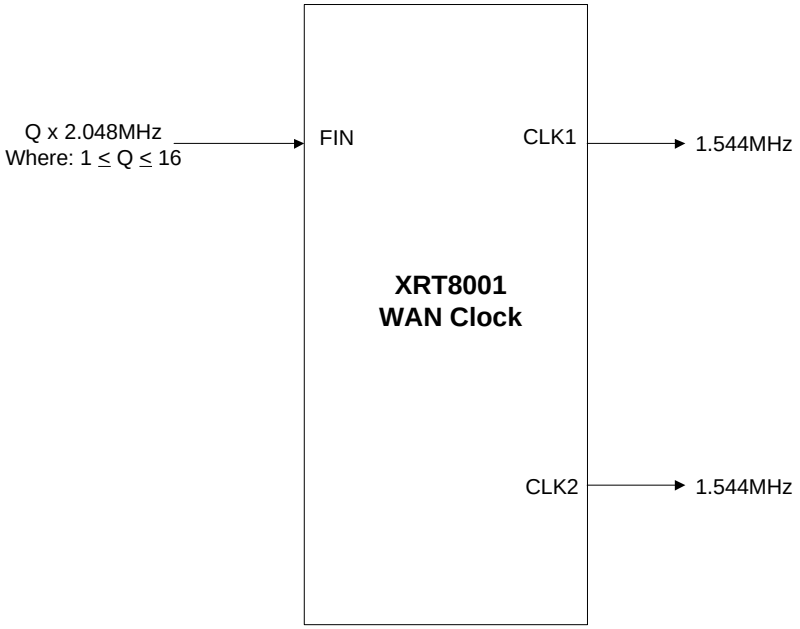


Figure 16. Illustration of the XRT8001 WAN Clock Operating in the "E1 to T1 – Forward/Master" Mode

6.5 Configuring the XRT8001 WAN Clock into the "E1 to T1 – Forward/Master" Mode

The user can configure the XRT8001 WAN Clock to operate in the "E1 to T1 – Forward/Master" Mode by executing the following steps:

Step 1 *– Configure the XRT8001 to operate in the "MASTER" Mode, by pulling the "MSB" input pin (pin 8) to VDD.*

Step 2 *– Write the binary value "1000" into Command Register CR0, as illustrated below:*

Command Register CR0 (Address = 0x00)

D4	D3	D2	D1	D0
IOC4	IOC3	IOC2	IOC1	PL1EN
1	0	0	0	X

This step configures the XRT8001 WAN Clock to operate in the "E1 to T1 – Forward/Master" Mode.

Note: *If the user wishes to output a clock signal via the CLK1 output signal, then he/she should also write a "1" into the "PL1EN" bit-field within Command Register, CR0.*

Step 3 *– Next, you need to specify the value for "Q" *(e.g., as in the "Q x 2.048MHz" clock signal which will be applied to the "FIN" input pin).*

The user accomplishes this writing the binary expression for "Q - 1" into Command Register, CR1, as illustrated below.

Command Register, CR1 (Address = 0x01)

D4	D3	D2	D1	D0
M4	M3	M2	M1	PL2EN
Value of "Q - 1" (in Binary Format)				X

For example, if the user wishes to input a clock signal of 2.048MHz, to the "FIN" input pin (e.g., where Q = 1), then he/she should write a "0" into Command Register CR1.

Note: *If the user wishes to output a clock signal via the CLK2 output signal, then he/she should also write a "1" into the "PL2EN" bit-field within Command Register CR1.*

Step 4 *– Write the binary expression "11111" into Command Register CR2, as illustrated below.*

This step is necessary in order to insure proper operation of the XRT8001.

Command Register, CR2 (Address = 0x02)

D4	D3	D2	D1	D0
SEL14	SEL13	SEL12	SEL11	SEL10
1	1	1	1	1

Step 5 *– Write the binary expression "11111" into Command Register CR3, as illustrated below.*

This step is necessary in order to insure proper operation of the XRT8001. This step is also illustrated below.

Command Register, CR3 (Address = 0x03)

D4	D3	D2	D1	D0
SEL24	SEL23	SEL22	SEL21	SEL20
1	1	1	1	1

Step 6 *– Enable any of the following output signals as appropriate: "SYNC", "CLK1", "CLK2" and "LOCKDET".*

This is accomplished by writing a "1" into the corresponding bit-fields, within Command Register CR4, as illustrated below.

Command Register CR4, (Address = 0x04)

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
1	1	1	0	0

6.6 The "High Speed – Reverse" Mode

When the XRT8001 WAN Clock has been configured to operate in the "High Speed – Reverse" Modes, its operation is independent of whether it has been configured in the "Master" or "Slave" Mode.

When the XRT8001 WAN Clock has been configured to operate in the "High Speed – Reverse" Modes, then it will accept a "64kHz" clock signal via the "Reference Clock" input at FIN (pin 3). In response, to this clock signal, the XRT8001 WAN Clock will output an "M x 2.048MHz" clock signal via the Clock Output pins (CLK1 and/or CLK2); where M can only have the values 1, 2,4 or 8.

A simple illustration of the XRT8001 WAN Clock, operating in the "High Speed – Reverse" Mode is presented in Figure 17.

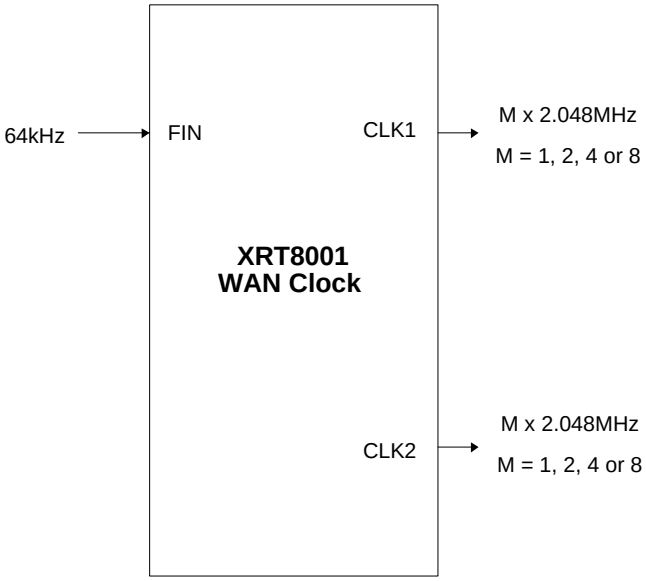


Figure 17. Illustration of the XRT8001 WAN Clock Operating in the "High Speed – Reverse" Mode

6.7 Configuring the XRT8001 WAN Clock into the "High Speed – Reverse" Mode.

The user can configure the XRT8001 WAN Clock to operate in the "High Speed – Reverse" Mode, by executing the following steps.

Step 1 *– Configure the XRT8001 to operate in the "SLAVE" Mode, by pulling the "MSB" input pin (pin 8) to GND.*

Step 2 *- Write the value "1101" into bts D4-D1 within command register CR0*

Command Register CR0 (Address = 0x00)

D4	D3	D2	D1	D0
IOC4	IOC3	IOC2	IOC1	PL1EN
1	1	0	1	X

Note: *If the user wishes to output a clock signal via the CLK1 output signal, then he/she should also write a "1" into the "PL1EN" bit-field within Command Register CR0.*

This step configures the XRT8001 to operate in the "High Speed – Reverse" Mode.

Step 3 *– Write the binary expression "0000" into bit-fields "D4 through D1" within Command Register, CR1, as illustrated below.*

Command Register, CR1 (Address = 0x01)

D4	D3	D2	D1	D0
M4	M3	M2	M1	PL2EN
0	0	0	0	1

Note: *If the user wishes to output a clock signal via the CLK2 output signal, then he/she should also write a "1" into the "PL2EN" bit-field within Command Register CR1.*

Step 4 *– Specify the value for "M" (e.g., as in the "M x 2.048MHz" clock signal) which is to be output via the "CLK1" output pin.*

This is accomplished by reviewing Table 7, and determining the 5 bit binary value which corresponds with the desired value of "M". Afterwards, the user should write this value into Command Register CR2.

Value of "M"	Value to be Written into Command Register CR2
1	0000X
2	0001X
4	001XX
8	X1XX or 1XXX

Table 7. Relationship Between the Value of "M" and the Value to Be Written into Command Register CR2 (in Order to Configure the "CLK1" Output Frequency)

Note: *The expression "X" indicates a "Don't Care" value for that particular bit-field.*

Command Register, CR2 (Address = 0x02)

D4	D3	D2	D1	D0
SEL14	SEL13	SEL12	SEL11	SEL10
Value from Table 7				

Step 5 *– Specify the value for "M" (e.g., as in the "M x 2.048MHz" clock signal) which is to be the output on the "CLK2" output pin.*

This is accomplished by reviewing Table 8, and determining the 5-bit binary value which corresponds with the desired value of "M". Afterwards, the user should write this value into Command Register, CR3.

Value of "M"	Value to be Written into Command Register CR3
1	0000X
2	0001X
4	001XX
8	X1XXX or 1XXXX

Table 8. Relationship Between the Value of "M" and the Value to Be Written into Command Register CR3 (in Order to Configure the "CLK2" Output Frequency)

Note: *The expression "X" indicates a "Don't Care" value for that particular bit-field.*

Command Register, CR3 (Address = 0x03)

D4	D3	D2	D1	D0
SEL24	SEL23	SEL22	SEL21	SEL20
Value from Table 8				

Step 6 *– Enable any of the following output signals as appropriate: "SYNC", "CLK1", "CLK2" and "LOCKDET".*

This is accomplished by writing a "1" into the corresponding bit-fields, within Command Register CR4, as illustrated below:

Command Register CR4, (Address = 0x04)

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
1	1	1	0	0

6.8 The "Forward/Slave" Mode

When the XRT8001 WAN Clock has been configured to operate in the "Forward/Slave" Mode, then it will accept an 8kHz clock signal via the "Reference Clock" input at FIN (pin 3). In response to this clock signal, the XRT8001 WAN Clock will output either a "L x 56kHz" or "L x 64kHz" clock signal via the "Clock Output pins" (CLK1 and CLK2); where L can range in value from 1 to 32.

A simple illustration of the XRT8001 WAN Clock operating in the "Forward/Slave" Mode" is presented in Figure 18.

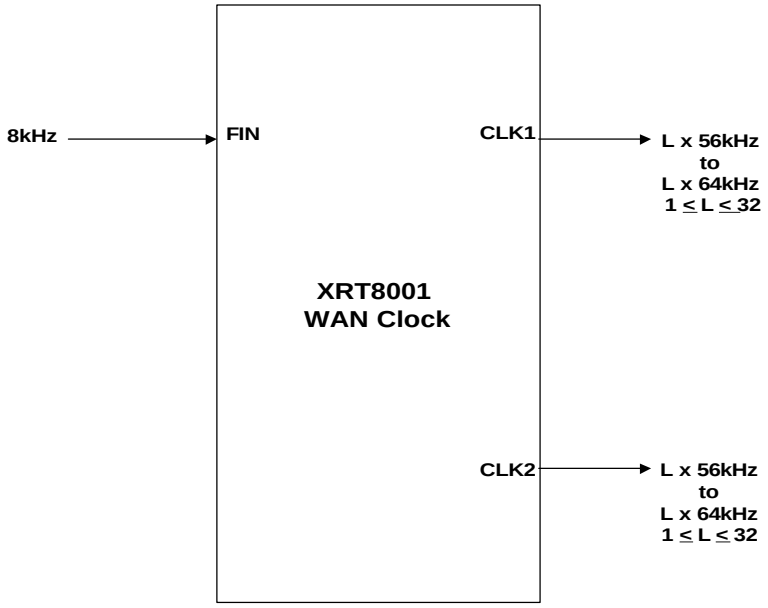


Figure 18. Illustration of the XRT8001 WAN Clock operating in the "Forward/Slave" Mode

6.9 Configuring the XRT8001 WAN Clock into the "Forward/Slave" Mode.

The user can configure the XRT8001 WAN Clock to operate in the "Forward/Slave Mode" by executing the following steps:

Step 1 *– Configure the XRT8001 to operate in the "SLAVE" Mode by pulling the MSB input pin (pin 8) to GND.*

Step 2 *– Refer to Table 2B and write the value that corresponds to the desired "Forward/Slave" Mode into Bits D[4:1] within Command Register CR0.*

Step 3 *– Define the values for L, for the CLK1 output by writing the appropriate value into the CR2 register. This is achieved by writing the value "L – 1" into this register.*

Notes:

1. *For example, if the user writes "00000" into this register, then the XRT8001 device will output a 64kHz signal via the CLK1 output pin.*
2. *If the user intends to output data via CLK1, then he/she must ensure that the PL1EN bit-field within Command Register CR0 is set to "1".*

Step 4- Define the value for L, for the CLK2 output by writing the appropriate value into the CR3 register. This is achieved by writing the value "L – 1" into this register.

Note: *If the user intends to output data via CLK2, then he/she must ensure that the PL2EN bit-field within Command Register CR1 is set to "1".*

Step 5 – Set the CLK1EN and CLK2EN bit-fields, within Command Register CR4 to 1 in order to enable the output drivers for CLK1 and CLK2, as illustrated below.

Command Register CR4

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	X	X
x	1	1	0	0

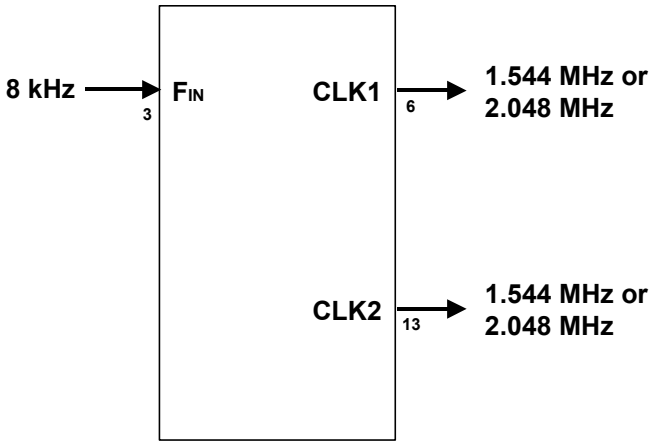


Figure 19. XRT8001 Reverse/Slave Mode

6.10 Phase relationship between the "FIN" input and the "CLK1 and CLK2" outputs

The Phase relationship depends upon whether the XRT8001 is operating in the "Slave" or "Master" Mode.

6.11 Slave Mode:

If the XRT8001 is operating in the "Slave" Mode, then there is a specific phase relationship between the "FIN" and the "CLK1, CLK2" outputs. The reasons are as follows.

For Slave Mode Operation, the XRT8001 accepts a 8kHz clock signal (which it will also synthesize and output via the SYNC output signal). Each of the two PLLs (within the XRT8001) will be configured to generate either a "K x 56kHz" or a "K x 64kHz" clock signal.

Hence, in the "Slave Mode", the "SYNC" output, is simply a buffered version of the "FIN" input. Therefore, *generate a "K x 56kHz" clock signal.*

the "SYNC" signal is approximately 4ns delayed from the "FIN" input signal.

Each of the two PLLs "lock" onto the "SYNC" signal, for frequency synthesis.

This timing relationship (between FIN and the CLK1, CLK2 signals) depends upon the "CLK1" and "CLK2" signal frequencies and as listed in the following tables.

NOTES:

1. Table 9 presents the timing relationship between the "FIN" and the "CLK1, CLK2" if the PLLs are configured generate a "K x 64kHz" clock signal.

2. Table 10 presents the timing relationship between the "FIN" and the "CLK1, CLK2" if the PLLs are configured to generate a "K x 56kHz" clock signal.

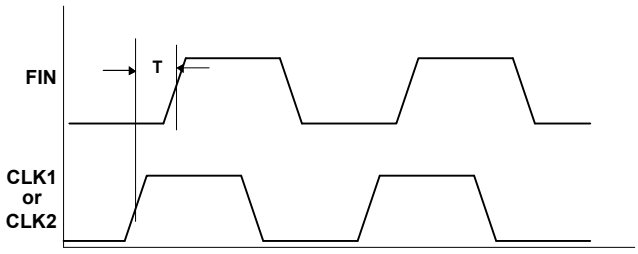


Figure 20: Timing Relationship between the FIN and the "CLK1/CLK2" outputs

Values written into	Value for K "SEL1[4:0]	CLK1/CLK2 (K x 64kHz)	T (ns) Output Frequency
00000	1	64kHz	330
00001	2	128kHz	330
00010	3	192kHz	330
00011	4	256kHz	330
00100	5	320kHz	395
00101	6	384kHz	330
00110	7	448kHz	283
00111	8	512kHz	247
01000	9	576kHz	438
01001	10	640kHz	305
01010	11	704kHz	359
01011	12	768kHz	330
01100	13	832kHz	305
01101	14	896kHz	283
01110	15	960kHz	264
01111	16	1.024MHz	248
10000	17	1.088Mhz	464
10001	18	1.152MHz	438
10010	19	1.214MHz	415
10011	20	1.280MHz	395
10100	21	1.344MHz	376
10101	22	1.408MHz	359
10110	23	1.472MHz	344
10111	24	1.536MHz	330
11000	25	1.600MHz	316
11001	26	1.664MHz	305
11010	27	1.728MHz	293
11011	28	1.792MHz	283
11100	29	1.856MHz	283
11101	30	1.920MHz	264
11110	31	1.984MHz	256
11111	32	2.048MHz	248

Table 9: Timing Relationship (T), from the rising edge of "CLK1/CLK2" to the rising edge of "FIN" with the XRT8001 in Slave Mode, and FIN = 8kHz

Values written into	Value for K "SEL1[4:0]	CLK1/CLK2 (K x 56kHz)	T (ns) Output Frequency
00000	1	56kHz	376
00001	2	112kHz	376
00010	3	168kHz	376
00011	4	224kHz	376
00100	5	280kHz	450
00101	6	336kHz	376
00110	7	392kHz	323
00111	8	448kHz	283
01000	9	504kHz	500
01001	10	560kHz	450
01010	11	616kHz	410
01011	12	672kHz	376
01100	13	728kHz	347
01101	14	784kHz	323
01110	15	840kHz	302
01111	16	896kHz	283
10000	17	952kHz	529
10001	18	1.008MHz	500
10010	19	1.064MHz	474
10011	20	1.120MHz	450
10100	21	1.176MHz	429
10101	22	1.232MHz	410
10110	23	1.288MHz	392
10111	24	1.344MHz	376
11000	25	1.400MHz	361
11001	26	1.456MHz	347
11010	27	1.512MHz	335
11011	28	1.568MHz	323
11100	29	1.624MHz	312
11101	30	1.680MHz	302
11110	31	1.756MHz	292
11111	32	1.812MHz	283

Table 10: Timing Relationship (T), from the rising edge of "CLK1/CLK2" to the rising edge of "FIN" with the XRT8001 in Slave Mode, and FIN = 8kHz

6.12 Master Mode:

If the XRT8001 is operating in the "Master" Mode, then the timing relationship between the "Reference signal" (e.g., a signal applied to the "FIN" and the "CLK1" or "CLK2" output is not readily available. This is because the "FIN" signal is internally divided down, via a Programmable Divider, which generates the "SYNC" signal. The internal Phase Locked Loops (within the XRT8001) are "locked" onto the "SYNC" signal. Hence, there is definitely a phase relationship between the "SYNC" and the "CLK1, CLK2" outputs.

7.0 Phase Relationship Between SYNC and CLK1 0r CLK2

Table 11, presents information on the delay between the rising edge of SYNC and CLK1 or CLK2 output signals. It is important to Note that this delay behaves as a function of the settings within the CR3 register.

t Values (nS)			
SEL14~SEL10	K	Kx56 MODE	Kx64 MODE
00000	1	372	326
00001	2	372	326
00010	3	372	326
00011	4	372	326
00100	5	446	391
00101	6	372	326
00110	7	319	279
00111	8	279	244
01000	9	496	434
01001	10	446	301
01010	11	406	355
01011	12	372	326
01100	13	343	301
01101	14	319	279
01110	15	298	260
01111	16	279	244
10000	17	525	460
10001	18	496	434
10010	19	470	411
10011	20	446	391
10100	21	425	372
10101	22	406	355
10110	23	388	340
10111	24	372	326
11000	25	357	312
11001	26	343	301
11010	27	331	289
11011	28	319	279
11100	29	308	279
11101	30	298	260
11110	31	288	252
11111	32	279	244

Table 11. Delay Time Between SYNC and CLK1 or CLK2

Note:
This table only applies when the XRT8001 is configured to operate in the "Forward/Master" or "Forward/Slave" Modes.

7.1 Synthesizing an "M x 2.048MHz" clock signal, such that "M" can take on the value of "1", "2", "4", or "8" with a clock signal of 2.048MHz

Figure 21 presents a possible approach that can be used. In this example, the user takes the 2.048MHz clock signal, and runs it through an external "Divide-by-32" counter (which is realized with two 74AHCT193). This "Divide-by-32" counter generates a 64kHz clock signal, which is applied to the "FIN" input pin of the XRT8001.

If the user configures the XRT8001 WAN Clock to operate in the "**High Speed – Reverse**" Mode, then it will accepts a 64kHz clock signal (via the FIN input) and generates an "M x 2.048MHz" clock signal via both the CLK1 and CLK2 outputs.

NOTES:

1. In this configuration, "M" can be configured to be of value "1", "2", "4" or "8".

2. The steps required to configure the XRT8001 into the "High Speed – Reverse" Mode are presented below.

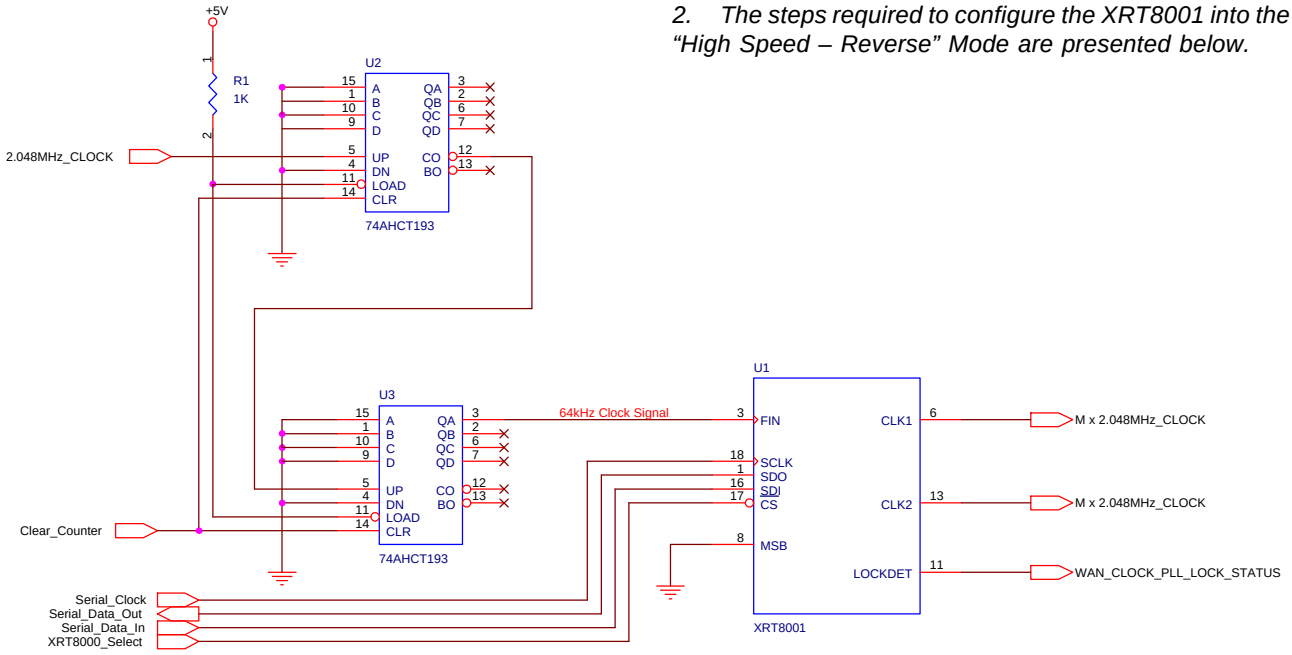


Figure 21: Circuit that inputs a 2.048MHz clock and generates a "M" x 2.048MHz clock

7.2 Configuring the XRT8001 WAN Clock to operate in the "High Speed – Reverse" Mode.

The following is a "six-step" procedure to configure the XRT8001 WAN Clock into the "High Speed – Reverse" Mode.

***STEP 1** – Configure the XRT8001 to operate in the "SLAVE" Mode, by pulling the "MSB" input pin (pin 8) to GND (low).*

***STEP 2** – Write the binary expression "1101" into bit-fields D4 through D1, within Command Register, CR0, as indicated below.*

Command Register, CR1 (Address = 0x01)

D4	D3	D2	D1	D0
M4	M3	M2	M1	PL2EN
1	1	0	1	X

This step configures the XRT8001 to operate in the "High Speed – Reverse" Mode.

NOTE: *If the user wishes to output a clock signal via the "CLK1" output pin, then he/she should also write a "1" into the "PL1EN" bit-field within Command Register, CR0.*

STEP 3 *– Write the binary expression "0000" into bit-fields D4 through D1, within Command Register, CR1, as illustrated below.*

Command Register, CR1 (Address = 0x01)

D4	D3	D2	D1	D0
M4	M3	M2	M1	PL2EN
0	0	0	0	X

NOTE: *If the user wishes to output a clock signal via the CLK2 output pin, then he/she should also write a "1" into the "PL2EN" bit-field within Command Register*

STEP 4 *– Specify the value for "M" (e.g., as in the "M x 2.048MHz" clock signal) which is to output via the "CLK1" output pin.*

This is accomplished by reviewing Table 3 to determine the 5 bit binary value which corresponds with the desired value of "M". Afterwards, the user should write this value into Command Register, CR2.

Value of "M"	Value to be written into the Command Register, CR2
1	0000x
2	0001x
4	001xx
8	x1xx or 1xxx

Table 12: Relationship between the value of "M", and Value to be written into Command Register, CR2 to configure the "CLK1" output frequency

STEP 5 *– Specify the value for "M" (e.g., as in the "M x 2.048MHz" clock signal) which is to output via the "CLK2" output pin.*

This is accomplished by reviewing Table 4 to determine the 5 bit binary value corresponding with the desired value of "M". Afterwards, the user should write this value into Command Register, CR3.

Value of "M"	Value to be written into the Command Register, CR3
1	0000x
2	0001x
4	001xx
8	x1xx or 1xxx

Table 13, The Relationship between the value of "M", and Value to be written into Command Register, CR2 to configure the "CLK2" output frequency

STEP 6 – Enable the desired output signals: *"SYNC", "CLK1", "CLK2" and "LOCKDET".*

This is accomplished by writing a "1" into the corresponding bit-fields, within Command Register CR4, as illustrated below.

Command Register, CR4 (Address = 0x04)

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
1	1	1	0	0

8.0 Generating 2.048MHz from 1.55MHz

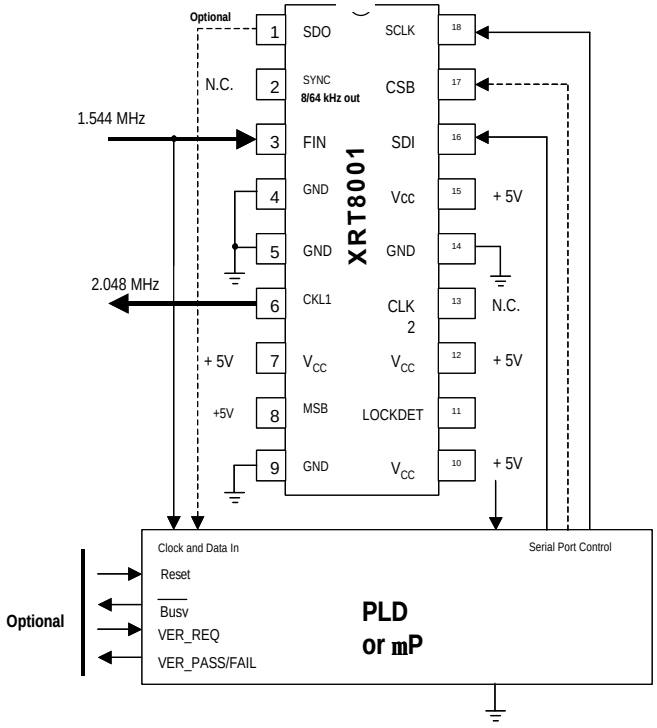


Figure 22. Typical Application Example: Generating 2.048MHz from 1.544MHz

Serial Port Programming in Four Steps

Step	Procedure	Result
1	Set the "MSB_OUT" output pin to "high"	Configures XRT8001 to operate in "Master" mode
2	Write the value "00101" into Command Register CR0 (located at 0x00)	Configures XRT8001 to accept an "N x 1.544MHz clock signal via the "FIN" input pin., and output a "K x 64kHz" clock signal via the "CLK1" output pin. (For this application N = 1 and K = 32). This step also enables "PLL #1" within the XRT8001
3	Write the value "00000" into Command Register CR1 (located at 0x01)	Sets "N" (as in "N x 1.544MHz") to be "1"
4	Write the value "11111" into Command Register CR2 (located at 0x02)	Sets "K" (as in "K x 64kHz") to be "32"
5	Write the value "01000" into Command Register CR4 (located at 0x04)	Enables the output driver for CLK1

9.0 Generating a 1.544MHz clock signal via the "CLK1/CLK2" outputs from either a 1.544MHz, or a 2.048MHz clock signal

When approaching this problem, be aware that the XRT8001 WAN Clock can be configured to accept a 2.048MHz clock signal via the "FIN" input pin and generate a 1.544MHz clock signal. However, the XRT8001 WAN Clock cannot be configured to accept a 1.544MHz clock signal, and generate a 1.544MHz clock signal.

Also, note the XRT8001 WAN Clock can be configured to accept a 2.048MHz clock signal (via the "FIN" input) and generate a 1.544MHz clock signal if it configured to operate in the "E1 to T1 Forward/Master" Mode. The XRT8001 can similarly be configured to accept an 8kHz clock signal (via the same "FIN" input pin) and generate a 1.544MHz clock signal if it is configured to operate in the "Reverse/Slave" Mode.

Based upon these two points, the necessary circuitry (in order to synthesize a 1.544MHz clock signal, from either a 1.544MHz or a 2.048MHz clock signal) can be achieved by the approach shown below in a block diagram.

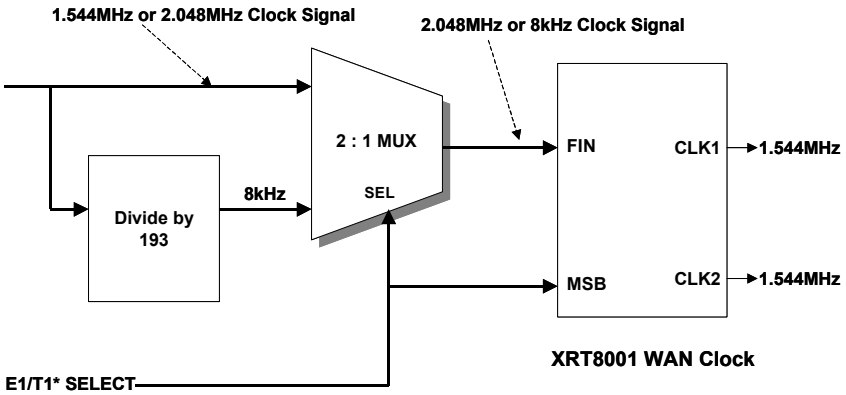


Figure 23: Synthesizing a 1.544MHz clock signal from a 1.544MHz or 2.048MHz clock

In Figure 23, the 1.544MHz or 2.048MHz input clock signal is routed to two locations.

- One of the inputs of a "2:1 MUX".
- The "CU" input of a "Divide-by-193" Block.

Figure 23 also includes a digital "E1/T1* SELECT" signal. This signal is connected to both the "SEL" input of the "2:1 MUX" and the "MSB" input of the XRT8001 WAN Clock. The basic idea behind this schematic is as follows:

1. If the incoming clock signal (from the T1/E1 LIU for example) is a 1.544MHz clock signal, then this signal will be divided by 193. As it passes through the "Divide-by-193" block a 8kHz clock signal is generated. This 8kHz clock signal will be applied to one of the inputs to the "2:1 MUX". *(**NOTE:** A 1.544MHz clock signal is applied to the other input to the "2:1 MUX").*

In this case, the user must set the "E1/T1* SELECT" signal to "LOW", order to select "T1 rates" (1.544MHz). By doing this, the 8kHz output from the "Divide-by-193" block is selected and will be applied to the "FIN" input of the XRT8001; and the XRT8001 will be configured to operate in the "Slave" Mode.

At this point, the user will need to execute the appropriate steps in order to configure the XRT8001 into the "Reverse-Slave" Mode.

2. If the incoming clock signal (from the T1/E1 LIU) is a 2.048MHz clock signal, then this signal will also be divided by 193. As it passes through the "Divide-by-193" block, it generates a clock signal of a strange (and undesirable frequency). This clock signal will be applied to one of the inputs to the "2:1 MUX" (***NOTE**: The 2.048MHz clock will also be applied to the other input of the "2:1 MUX*).

In this case, the user must set the "E1/T1* SELECT" signal to "HIGH", order to select "E1 rates" (2.048MHz). By doing this, the 2.048MHz clock signal (from the T1/E1 LIU) is selected and will be applied to the "FIN" input of the XRT8001, and the XRT8001 will configured to operate in the "Master" Mode.

At this point, the user will need to execute the appropriate steps in order to configure the XRT8001 into the "E1 to T1 Forward/Master" Mode.

9.1 Hardware and Software Implementation Details

Figure x presents a simple block diagram of a design that can accept either a 1.544MHz or a 2.048MHz clock signal, and synthesize a 1.544MHz clock signal. Now we need to provide some details. Hence, Figure 24 presents a circuit schematic which realizes the function, depicted in Figure 23.

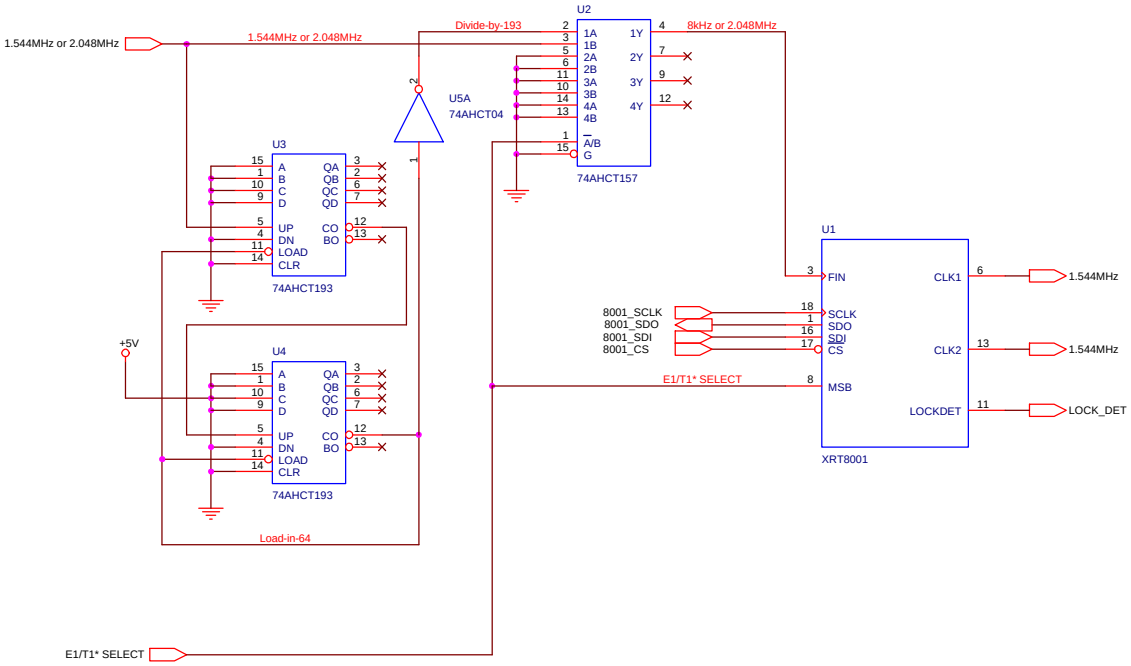


Figure 24: Hardware Design Implementation of Figure 23.

Next, we describe how to configure the circuitry in Figure 24 to accept a 2.048MHz clock signal, and configure it to synthesize a 1.544MHz clock signal by executing five steps. We also describe how to accept a 1.544MHz clock signal and configure it to synthesize a 1.544MHz clock.

9.2 Configuring the Circuitry in Figure 6 to accept a 2.048MHz clock in order to synthesize a 1.544MHz output clock.

STEP 1 *– Drive the "E1/T1* SELECT" input pin to "HIGH". This step configures the "2:1 MUX" to select and apply the 2.048MHz clock to the "FIN" input of the XRT8001 WAN Clock, as well as configuring the XRT8001 WAN Clock into the "Master Mode".*

NOTE: *The next steps are devoted to configuring the XRT8001 WAN Clock into the "E1 to T1 Forward/Master" Mode.*

STEP 2 *– Write the binary value "1000" into Command Register CR0 (within the XRT8001 WAN Clock) as indicated below.*

Command Register, CR0 (Address = 0x00)

D4	D3	D2	D1	D0
IOC4	IOC3	IOC2	IOC1	PL1EN
1	0	0	0	1

NOTE: *In order to synthesize and output a clock signal via the "CLK1" output pin, the user must write a "1" into the D0 (PL1EN) bit-field within Command Register, CR0, as indicated above.*

This step configures the XRT8001 WAN to operate in the "E1 to T1 Forward/Master" Mode. In this mode, the XRT8001 WAN Clock will be configured to accept a "Q x 2.048MHz" clock signal via the "FIN" input and will synthesize a 1.544MHz clock signal via both the "CLK1" and "CLK2" output pins.

STEP 3 *– Next specify the value for "Q" (e.g., as in "Q x 2.048MHz" clock signal, which will be applied to the "FIN" input).*

In this application, the value for "Q" is "1". Hence, the user must configure the XRT8001 WAN Clock to use this value for "Q", by writing the binary value for "Q – 1" into Command Register, CR1. In this application, the user should write "0000" into the Command Register, as indicated below.

Command Register, CR1 (Address = 0x01)

D4	D3	D2	D1	D0
M4	M3	M2	M1	PL2EN
0	0	0	0	1

NOTE: *In order to synthesize and output a clock signal via the "CLK2" output pin, the user must write a "1" into the "D0 (PL2EN) bit-field within Command Register, CR1, as indicated above.*

STEP 4 *– Write the binary value "11111" into both Command Registers CR2 and CR3. This is necessary in order to ensure proper operation of the XRT8001 WAN Clock.*

STEP 5 *– Enable the desired output signals: SYNC, CLK1, CLK2, and LOCKDET. This is accomplished by writing a "1" into the corresponding bit-field, within Command Register, CR4, as illustrated below.*

Command Register, CR4 (Address = 0x04)

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
1	1	1	1	1

Once the user has executed these five steps, then the circuitry (in Figure 6) is now configured to accept a 2.048MHz clock signal (from the T1/E1 LIU) and synthesize a 1.544MHz clock signal.

Configuring the Circuitry in Figure 24 to accept a 1.544MHz clock signal and synthesize a 1.544MHz clock signal.

The user can configure the circuitry (within Figure 6) to accept a 1.544MHz clock signal, and synthesize a 1.544MHz clock signal, by executing the following four (4) steps.

STEP 1 *– Drive the "E1/T1* SELECT" input pin to "LOW". This step configures the "2:1 MUX" to select and apply the 8kHz clock signal to the "FIN" input of the XRT8001 WAN Clock, and configures the XRT8001 WAN Clock into the "Slave" Mode.*

NOTE: *The next few steps will be devoted to configuring the XRT8001 WAN Clock into the "Reverse/Slave" Mode.*

STEP 2 *– Write the binary value "1000" into Command Register CR0, within the XRT8001 WAN Clock, as indicated below.*

Command Register, CR0 (Address = 0x00)

D4	D3	D2	D1	D0
IOC4	IOC3	IOC2	IOC1	PL1EN
1	0	0	0	1

NOTE: *In order to synthesize and output a clock signal via the "CLK1" output pin, the user must write a "1" into the "D0 (PL1EN) bit-field within Command Register, CR0, as indicated above.*

This step configures the XRT8001 WAN to operate in the "Reverse/Slave" Mode. In this mode, the XRT8001 WAN Clock will be configured to accept an 8kHz clock signal via the "FIN" input and will synthesize a 1.544MHz clock signal via both the "CLK1" and "CLK2" output pins.

STEP 3 *– Write the binary expression "0000" into bit-fields D4 through D1, within Command Register CR1, as illustrated below.*

Command Register, CR1 (Address = 0x01)

D4	D3	D2	D1	D0
M4	M3	M2	M1	PL2EN
0	0	0	0	1

NOTE: *In order to synthesize and output a clock signal via the "CLK2" output, the user must write a "1" into the "D0 (PL2EN) bit-field within Command Register, CR1, as illustrated above.*

The values within Command Registers CR2 and CR3 are "don't care".

STEP 4 *– Enable the desired output signals: SYNC, CLK1, CLK2, and LOCKDET.*

This is accomplished by writing a "1" into the corresponding bit-field, within Command Register, CR4, as illustrated below.

Command Register, CR4 (Address = 0x04)

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
1	1	1	1	1

Once the user has executed these four (4) steps, then the circuitry in Figure 24 is configured to accept a 1.544MHz clock signal (from the T1/E1 LIU) and synthesize a 1.544MHz clock signal.

10.0 Jitter Transfer Characteristics of the XRT8001

The definition of "Jitter Transfer Characteristics" (of the XRT8001) is the amount of "output" jitter that the XRT8001 produces (at the "CLK1" and "CLK2" outputs), when provided with a certain amount of jitter at the FIN input pin.

The "Jitter Transfer Characteristics" of the XRT8001 are presented in Figure 25 (for 3.3V applications) and Figure 26(for 5.0V applications).

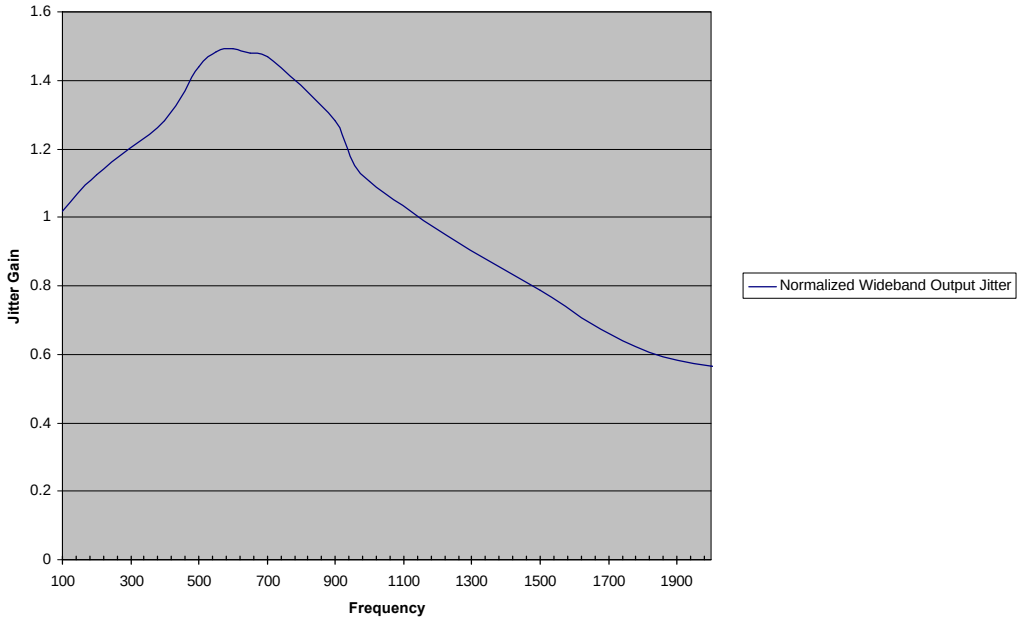


Figure 25: Jitter Transfer Characteristics of the XRT8001 WAN Clock for 3.3V Applications

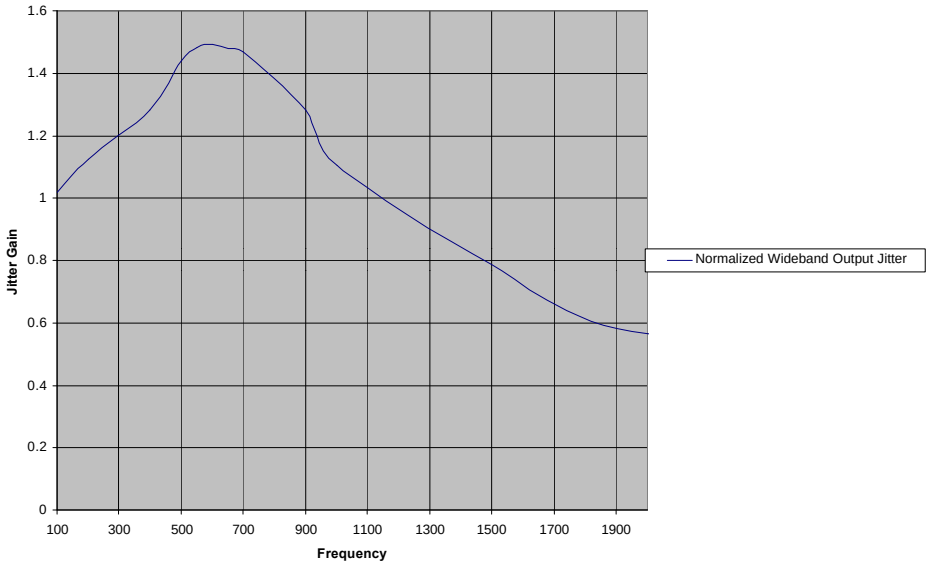


Figure 26: Jitter Transfer Characteristics of the XRT8001 WAN Clock for 5V Applications

10.1 Reading Figures 25 and 26

Figures 25 and 26 are linear (as opposed to logarithmic) plots. The Jitter Gain is computed via the following equation.

Jitter Gain (at Jitter Frequency f) = (Jitter_Amplitude_CLK)/(Jitter_Amplitude_FIN)

Where:

- Jitter_Amplitude_FIN = The Jitter Amplitude applied to the "FIN" input (at Jitter Frequency f).
- Jitter_Amplitude_CLK = The Jitter Amplitude measured at the "CLK1" or "CLK2" output, when "Jitter_Amplitude_FIN" is applied to the FIN input in of the XRT8001.

Hence, the Jitter Gain is not expressed in terms of dB, but simply a ratio of two numbers.

Wherever the Jitter Gain exceeds "1.0" in value, then, for those "Jitter Frequencies" the XRT8001 amplifies Jitter (e.g., the amplitude of the jitter, as it propagates from the "FIN" input to the "CLK1" or CLK2" output, increases).

Conversely, wherever the Jitter Gain falls below "1.0" in value, then for those "Jitter Frequencies" the XRT8001 attenuates jitter (e.g., the amplitude of the jitter, as it propagates from the "FIN" input to the "CLK1" or "CLK2" output, decreases).

Figures 25 and 26 indicate that for Jitter Frequencies, ranging between 100Hz and 1100Hz, the XRT8001 amplifies Jitter. Further, these figures also indicate that for Jitter Frequencies greater than 1100Hz, that the XRT8001 attenuates Jitter.

10.2 Test Conditions for Measurements associated with Figures 25 and 26

- Power Supply voltage either 3.3V or 5.V
- Input Clock Frequency = 2.048MHz
- Output Clock Frequency = 2.048MHz
- Input Jitter Amplitude = 0.25Upp.
- Ambient Temperature = 25°C.

11.0 PCB layout guidelines for the XRT8001

- Use a multi-layer circuit board with separate plane layers for "+5V" (or 3.3V) and "Ground" .
- Bypass the Analog VDD pin to ground with a 6.9mF "ceramic" capacitor.
- Use large "vias" located close to the IC package to ensure that Digital VDD (e.g., pins 7, 12 and 15) and Digital Ground (e.g., pins 4, 5 and 14) have a low inductance path to the +5V (+3.3V) and Ground Planes, respectively.
- Bypass the Digital VDD pins (pin 10) to ground with a 0.1mF ceramic capacitors that are located as close as possible to the IC package.

12.0 Comparing the XRT8001 with the earlier pin-compatible XRT8000

The XRT8001 is pin-to-pin compatible with the XRT8000. However, there are some functional differences between these two products. These differences are summarized below.

1) The XRT8001 can be configured to generate frequencies up to 2.048MHz, 4.096MHz, 8.192MHz or 16.384MHz.

The Maximum Frequency that the XRT8000 can generate is either 2.048MHz or 1.544MHz

2) The XRT8001 can be configured to accept an E1 rate clock signal and synthesize a T1 rate clock signal. The XRT8001 can also synthesize an E1 rate clock signal, when provided with a T1 rate clock signal

The XRT8000 can be configured to accept a T1 rate clock signal (e.g., 1.544MHz) and can be easily configured to synthesize an E1 rate clock signal (e.g., 2.048MHz).

However, the XRT8000 cannot be configured to accept an E1 rate clock signal and synthesize a T1 rate clock signal.

3) Both the XRT8001 and XRT8000 can be configured to accept "Fractional T1/E1" rate clock signals (e.g., K x 64kHz) and synthesize either a 1.544MHz or 2.048MHz clock signal.

However, the XRT8001 can also synthesize "Fractional T1/E1" rate clock signals, when provided with either a 1.544MHz or 2.048MHz clock signal

4) The XRT8001 permits the user to determine the exact role of the LOCKDET output pin. The on-chip Command Register (within the XRT8001) permits the user to configure the LOCKDET output pin to have the functions listed below.

In the XRT8000, the LOCKDET output pin is pulled HIGH only when both XRT8000 PLLs are "in-lock".

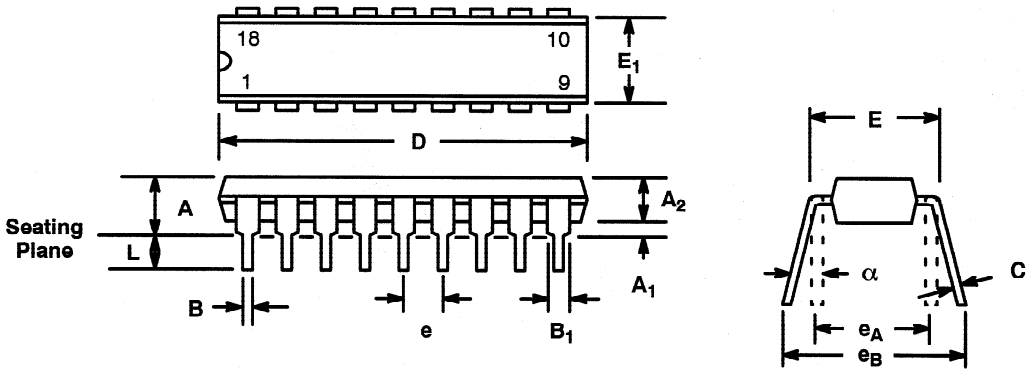
LOCKDET Pin Function	Description of LOCKDET pin's role
LOCK Condition of both PLL1 AND PLL2	The LOCKDET output pin toggles "HIGH" only if both (of if the only enabled) PLLs are "In-LOCK". The LOCKDET output pin will toggle "LOW" if any one of the PLLs are out of LOCK. ***NOTE:*** *In this case, the LOCKDET output of the XRT8001 behaves identical to that of the XRT8000.*
LOCK Condition of PLL1 Only	The LOCKDET output pin toggles "HIGH" only if PLL1 is in the "In-LOCK" condition.
LOCK Condition of PLL2 Only	The LOCKDET output pin toggles "HIGH" only if PLL2 is in the "In-LOCK" condition.
Forced to "LOW"	The LOCKDET output pin is pulled "LOW" regardless of the "Lock" condition of the two PLLs.

NOTE: *The XRT8000 has an additional divide by 8 block which is not included in the XRT8001.*

Table 15: Selectable Functions of the LOCKDET Output Pin in the XRT8001

18 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

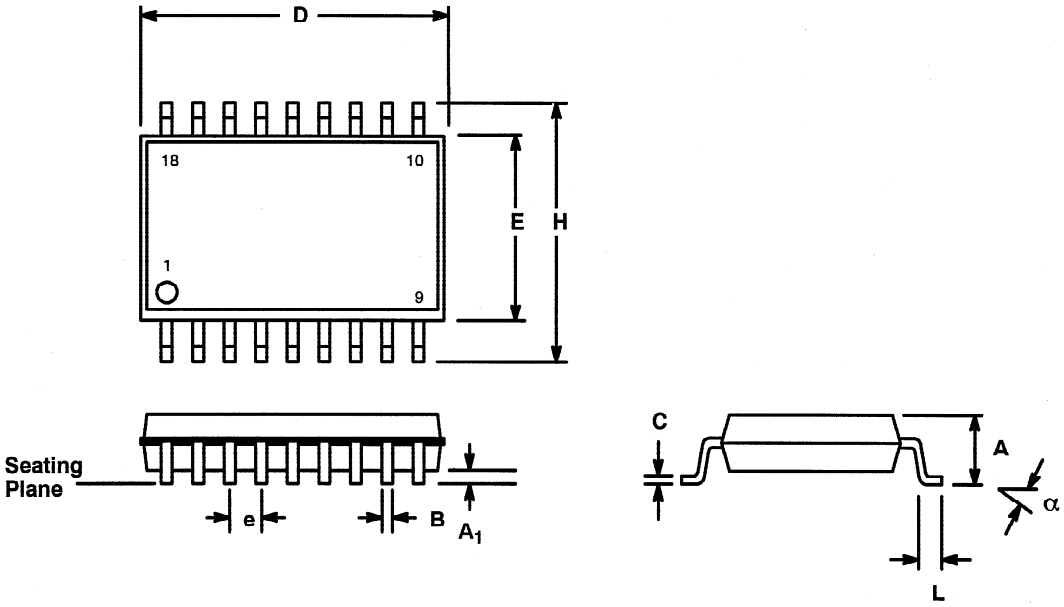


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.845	0.925	21.46	23.50
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

18 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A_1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.447	0.463	11.35	11.75
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

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