

OT407

Four-quadrant triac, enhanced noise immunity

Rev. 01 — 19 May 2008

Product data sheet

1. Product profile

1.1 General description

Passivated sensitive gate triac in a SOT54A (wide pitch) plastic package

1.2 Features

- Sensitive gate
- Direct interfacing to logic level ICs
- Enhanced immunity to voltage transients and noise
- Gate triggering in four quadrants
- Direct interfacing to low power gate drive circuits
- High blocking voltage to 800 V

1.3 Applications

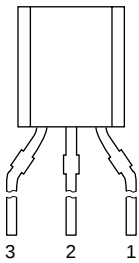
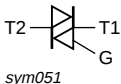
- Home appliances
- Low power AC fan speed controllers
- Low power motor control
- Low power loads in industrial process control

1.4 Quick reference data

- $V_{\text{DRM}} \leq 800 \text{ V}$
- $I_{\text{TSM}} \leq 12.5 \text{ A}$ ($t = 20 \text{ ms}$)
- $I_{\text{T(RMS)}} \leq 1 \text{ A}$
- $I_{\text{GT}} \leq 5 \text{ mA}$
- $I_{\text{GT}} \leq 7 \text{ mA}$ (T2– G+)

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	main terminal 2 (T2)		 sym051
2	gate (G)		
3	main terminal 1 (T1)		

SOT54A

3. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
OT407	-	plastic single-ended leaded (through hole) package; 3 leads (wide pitch)	SOT54A

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
V_{RRM}	repetitive peak reverse voltage		-	800	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{lead}} \leq 38\text{ °C}$; see Figure 4 and 5	-	1	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{j}} = 25\text{ °C}$ prior to surge; see Figure 2 and 3			
		$t = 20\text{ ms}$	-	12.5	A
		$t = 16.7\text{ ms}$	-	13.8	A
I^2t	I^2t for fusing	$t_{\text{p}} = 10\text{ ms}$	-	1.28	A ² s
di_{T}/dt	rate of rise of on-state current	$I_{\text{TM}} = 1\text{ A}$; $I_{\text{G}} = 20\text{ mA}$; $di_{\text{G}}/dt = 0.2\text{ A}/\mu\text{s}$			
		T2+ G+	-	50	A/ μs
		T2+ G-	-	50	A/ μs
		T2- G-	-	50	A/ μs
		T2- G+	-	10	A/ μs
I_{GM}	peak gate current		-	1	A
P_{GM}	peak gate power		-	2	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	+150	°C
T_{j}	junction temperature		-	125	°C

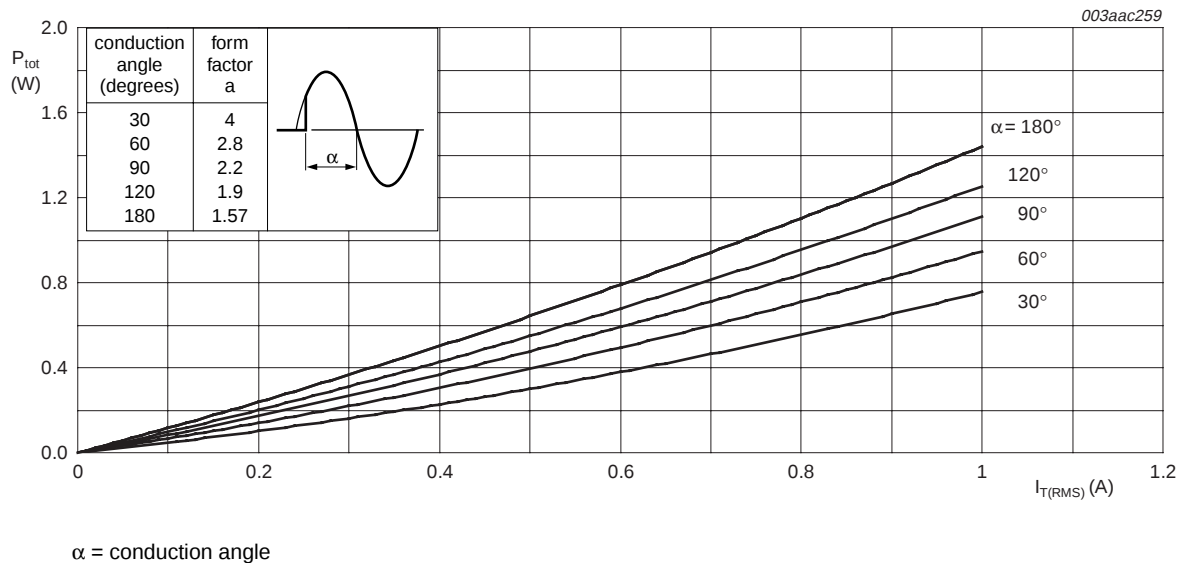


Fig 1. Total power dissipation as a function of RMS on-state current; maximum values

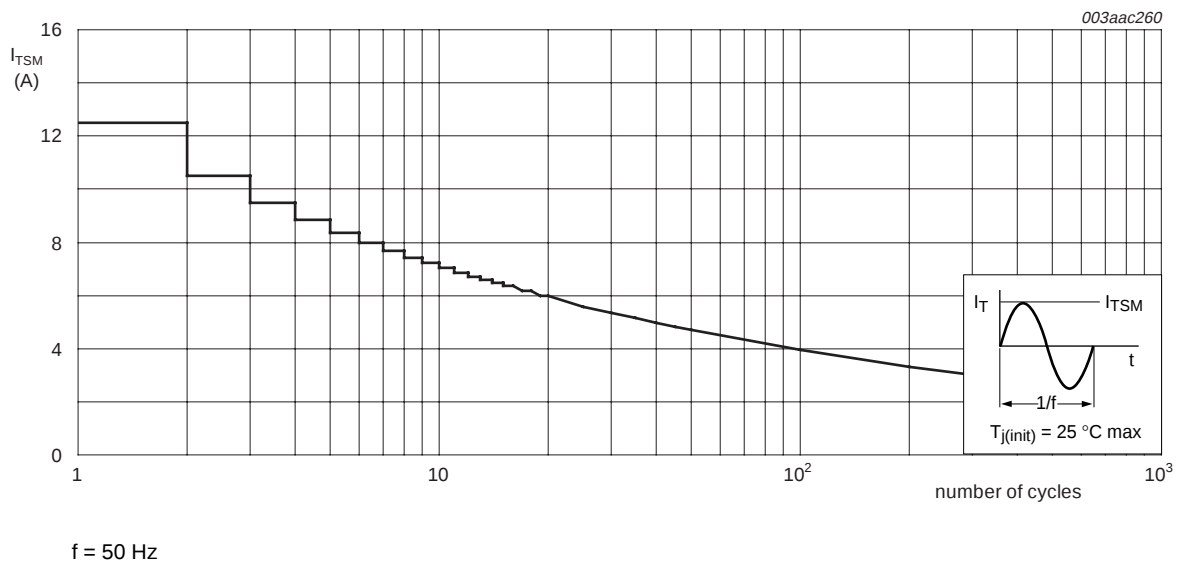
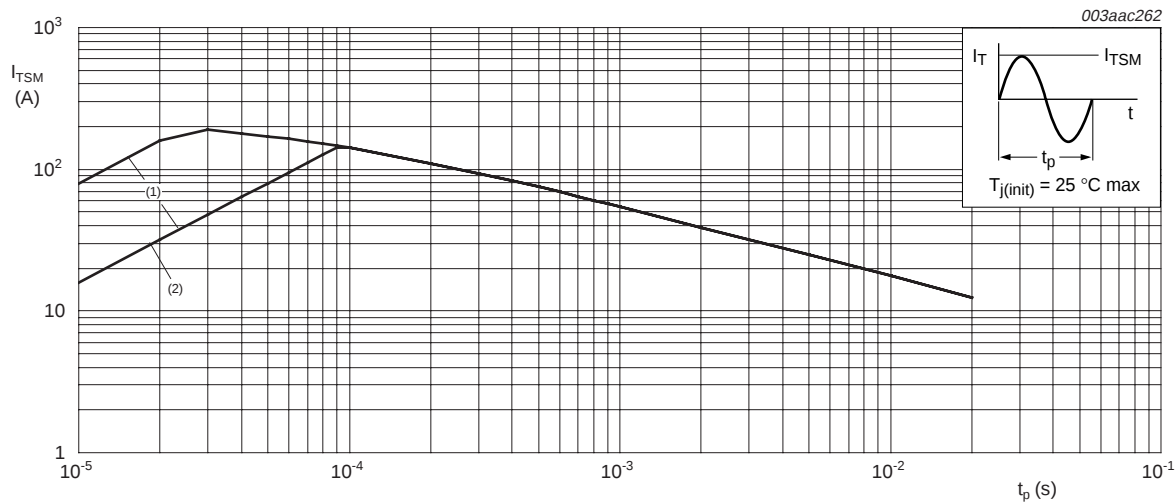
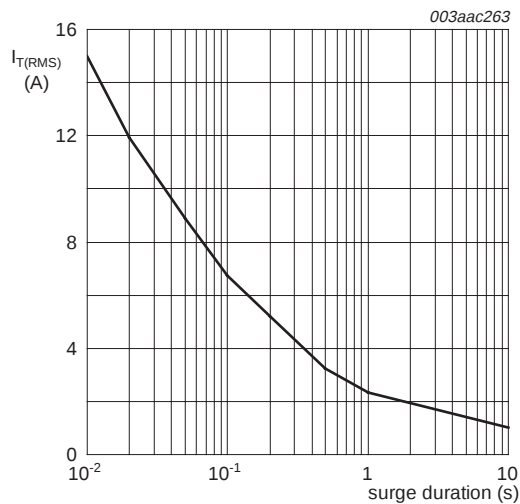


Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20\text{ ms}$
(1) dI_T/dt limit
(2) T2- G+ quadrant limit

Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values



$f = 50\text{ Hz}$
 $T_{lead} = 38\text{ }^{\circ}\text{C}$

Fig 4. RMS on-state current as a function of surge duration; maximum values

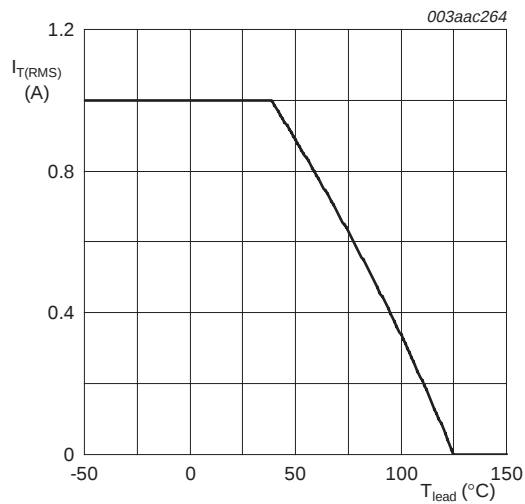
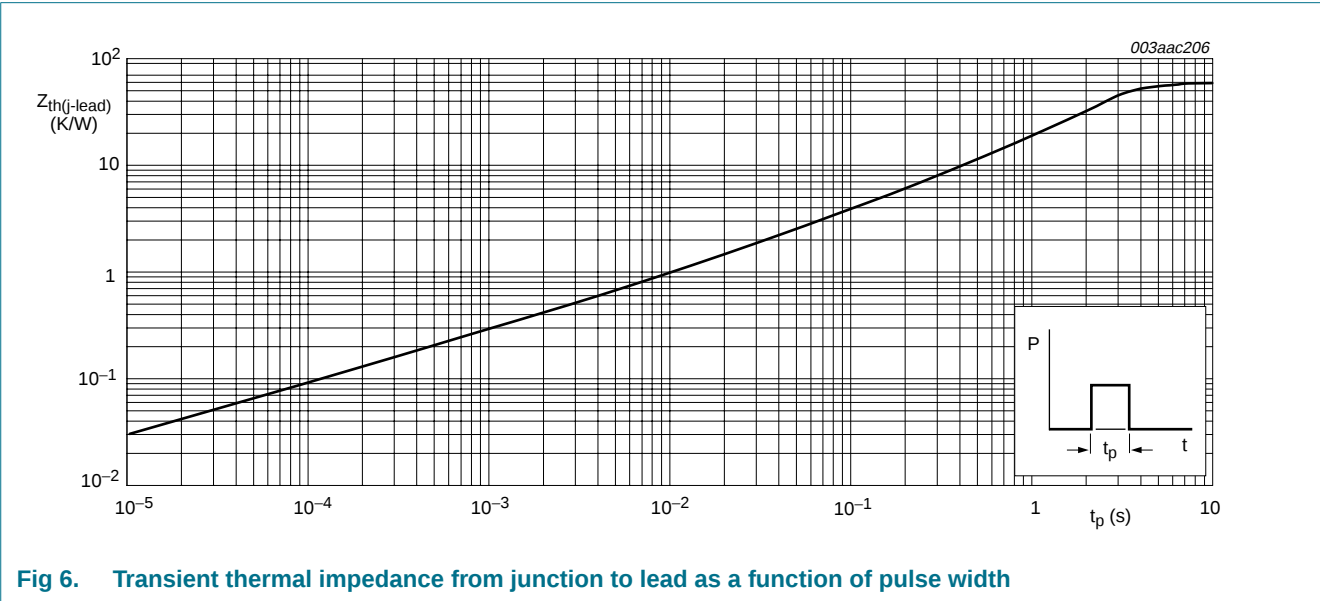


Fig 5. RMS on-state current as a function of solder point temperature; maximum values

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle; see Figure 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	full cycle; printed-circuit board mounted; lead length = 4 mm	-	150	-	K/W



6. Static characteristics

Table 5. Static characteristics

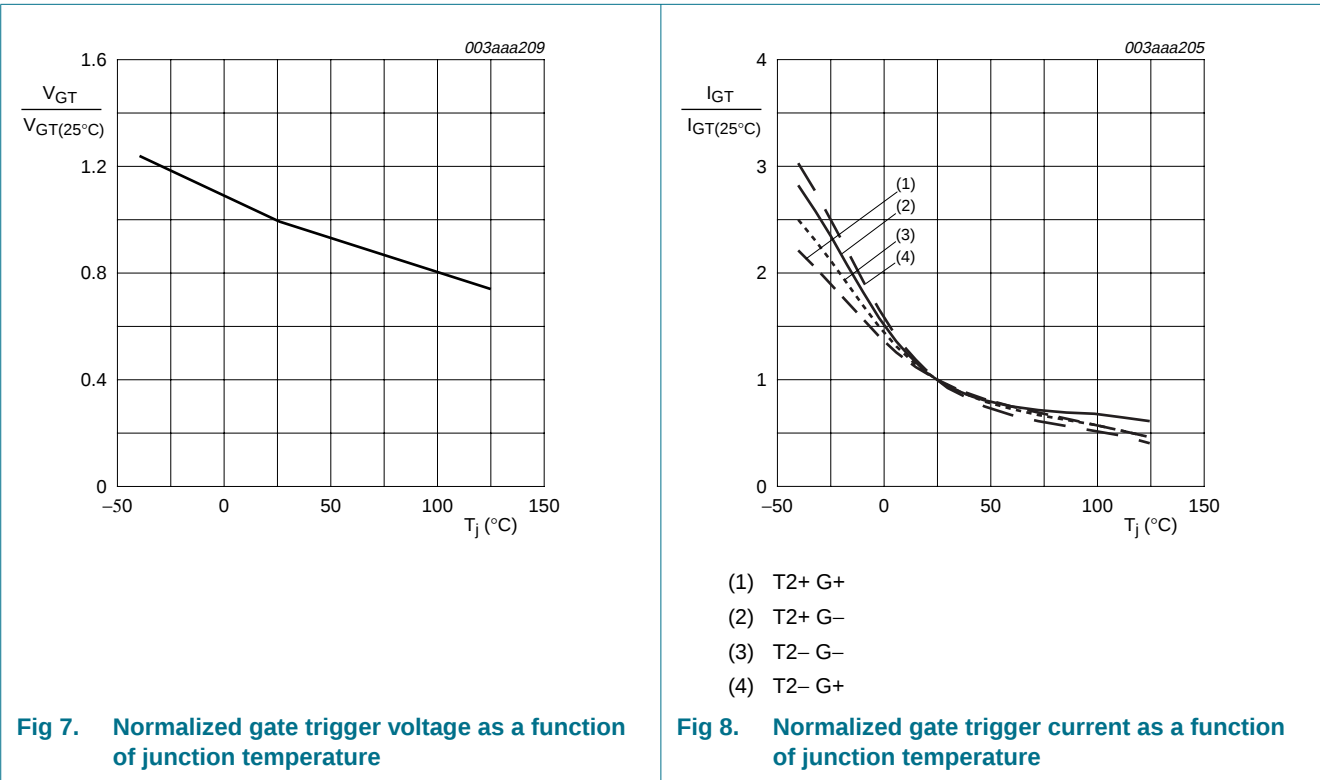
$T_j = 25\text{ °C}$ unless otherwise specified.

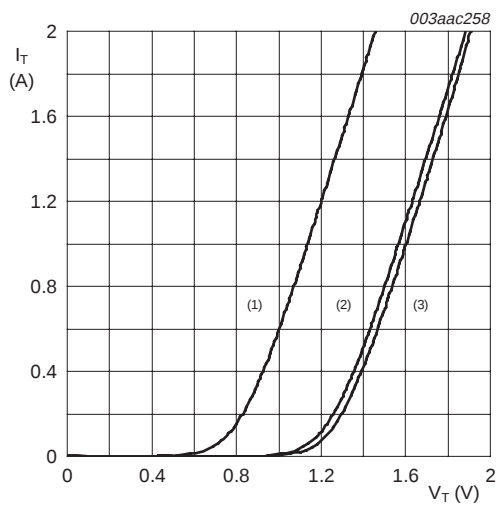
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; see Figure 8				
		T2+ G+	0.25	-	5	mA
		T2+ G-	0.25	-	5	mA
		T2- G-	0.25	-	5	mA
		T2- G+	0.35	-	7	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; see Figure 10				
		T2+ G+	-	-	10	mA
		T2+ G-	-	-	25	mA
		T2- G-	-	-	10	mA
		T2- G+	-	-	10	mA
I_H	holding current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; see Figure 11	-	-	10	mA
V_T	on-state voltage	$I_T = 1\text{ A}$; see Figure 9	-	1.3	1.6	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; see Figure 7	-	-	1.3	V
		$V_D = V_{DRM}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ °C}$	0.2	-	-	V
I_D	off-state current	$V_D = V_{DRM(max)}$; $T_j = 125\text{ °C}$	-	-	0.5	mA

7. Dynamic characteristics

Table 6. Dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 0.67V_{DRM(max)}$; $T_j = 110\text{ }^{\circ}\text{C}$; exponential waveform; gate open circuit	20	-	-	$\text{V}/\mu\text{s}$
dV_{com}/dt	rate of change of commutating voltage	$V_{DM} = 400\text{ V}$; $T_j = 110\text{ }^{\circ}\text{C}$; $I_{TM} = 1\text{ A}$; $di_{com}/dt = 0.44\text{ A/ms}$	1	-	-	$\text{V}/\mu\text{s}$





- $V_0 = 1.254 \text{ V}$; $R_S = 0.31 \text{ } \Omega$
- (1) $T_j = 125 \text{ } ^\circ\text{C}$; typical values
 - (2) $T_j = 125 \text{ } ^\circ\text{C}$; maximum values
 - (3) $T_j = 25 \text{ } ^\circ\text{C}$; maximum values

Fig 9. On-state current as a function of on-state voltage

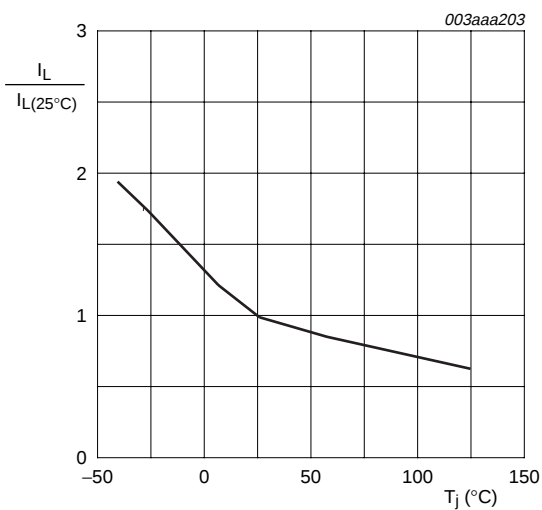


Fig 10. Normalized latching current as a function of junction temperature

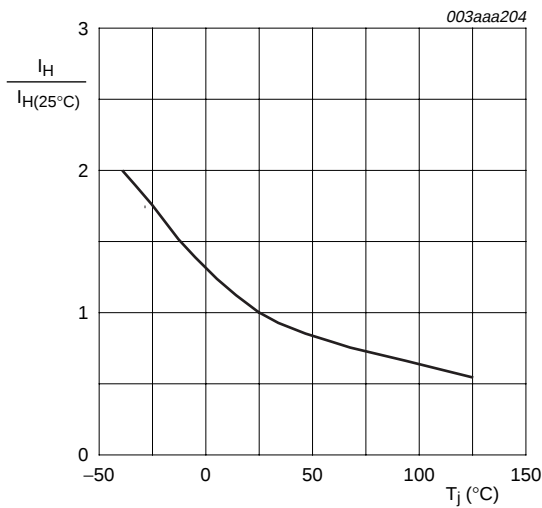


Fig 11. Normalized holding current as a function of junction temperature

8. Package outline

Plastic single-ended leaded (through hole) package; 3 leads (wide pitch) SOT54A

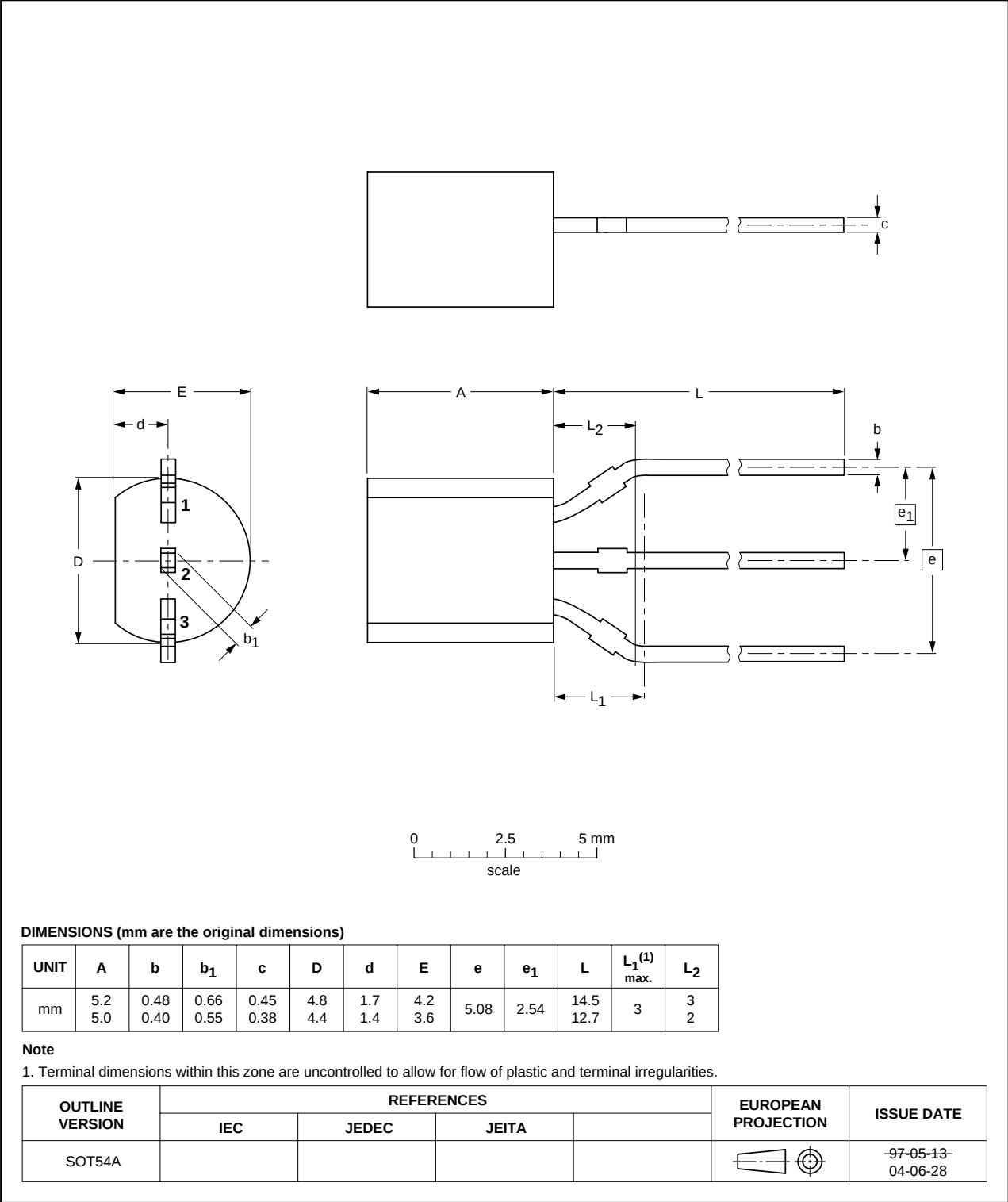


Fig 12. Package outline SOT54A

9. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
OT407_1	20080519	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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12. Contents

1 Product profile 1

1.1 General description..... 1

1.2 Features 1

1.3 Applications 1

1.4 Quick reference data..... 1

2 Pinning information..... 1

3 Ordering information..... 2

4 Limiting values..... 2

5 Thermal characteristics..... 5

6 Static characteristics..... 6

7 Dynamic characteristics 7

8 Package outline 9

9 Revision history..... 10

10 Legal information..... 11

10.1 Data sheet status 11

10.2 Definitions..... 11

10.3 Disclaimers..... 11

10.4 Trademarks..... 11

11 Contact information..... 11

12 Contents 12



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