

# IDC Low Inductance Capacitors (RoHS)

## 0306/0612/0508 IDC (InterDigitated Capacitors)

### GENERAL DESCRIPTION

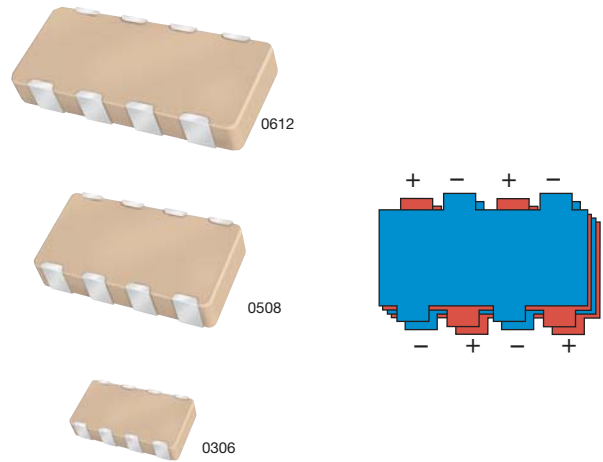
Inter-Digitated Capacitors (IDCs) are used for both semiconductor package and board level decoupling. The equivalent series inductance (ESL) of a single capacitor or an array of capacitors in parallel determines the response time of a Power Delivery Network (PDN). The lower the ESL of a PDN, the faster the response time. A designer can use many standard MLCCs in parallel to reduce ESL or a low ESL Inter-Digitated Capacitor (IDC) device. These IDC devices are available in versions with a maximum height of 0.95mm or 0.55mm.

IDCs are typically used on packages of semiconductor products with power levels of 15 watts or greater. Inter-Digitated Capacitors are used on CPU, GPU, ASIC, and ASSP devices produced on 0.13μ, 90nm, 65nm, and 45nm processes. IDC devices are used on both ceramic and organic package substrates. These low ESL surface mount capacitors can be placed on the bottom side or the top side of a package substrate. The low profile 0.55mm maximum height IDCs can easily be used on the bottom side of BGA packages or on the die side of packages under a heat spreader.

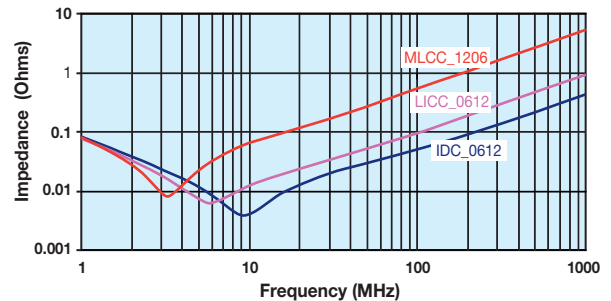
IDCs are used for board level decoupling of systems with speeds of 300MHz or greater. Low ESL IDCs free up valuable board space by reducing the number of capacitors required versus standard MLCCs. There are additional benefits to reducing the number of capacitors beyond saving board space including higher reliability from a reduction in the number of components and lower placement costs based on the need for fewer capacitors.

The Inter-Digitated Capacitor (IDC) technology was developed by AVX. This is the second family of Low Inductance MLCC products created by AVX. IDCs are a cost effective alternative to AVX's first generation low ESL family for high-reliability applications known as LICA (Low Inductance Chip Array).

AVX IDC products are available with a lead-free finish of plated Nickel/Tin.



### TYPICAL IMPEDANCE



### HOW TO ORDER

W	3	L	1	6	D	225	M	A	T	3	A
Style	IDC Case Size	Low Inductance	Number of Terminals	Voltage	Dielectric	Capacitance Code (In pF)	Capacitance Tolerance	Failure Rate	Termination	Packaging	Thickness
	2 = 0508 3 = 0612 4 = 0306		1 = 8 Terminals	4 = 4V 6 = 6.3V Z = 10V Y = 16V 3 = 25V	C = X7R D = X5R Z = X7S	2 Sig. Digits + Number of Zeros	M = ±20%	A = N/A	T = Plated Ni and Sn	Available 1=7" Reel 3=13" Reel	Max. Thickness mm (in.) A=Standard S=0.55 (0.022)

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

### PERFORMANCE CHARACTERISTICS

<b>Capacitance Tolerance</b>	±20% Preferred
<b>Operation Temperature Range</b>	X7R = -55°C to +125°C X5R = -55°C to +85°C X7S = -55°C to +125°C
<b>Temperature Coefficient</b>	±15% (OVDC), ±22% (X7S)
<b>Voltage Ratings</b>	4, 6.3, 10, 16, 25 VDC
<b>Dissipation Factor</b>	≤ 6.3V = 6.5% max; 10V = 5.0% max; ≥ 16V = 3.5% max
<b>Insulation Resistance (@+25°C, RVDC)</b>	100,000MΩ min, or 1,000MΩ per μF min., whichever is less

<b>Dielectric Strength</b>	No problems observed after 2.5 x RVDC for 5 seconds at 50mA max current
<b>CTE (ppm/C)</b>	12.0
<b>Thermal Conductivity</b>	4-5W/M K
<b>Terminations Available</b>	Plated Nickel and Solder

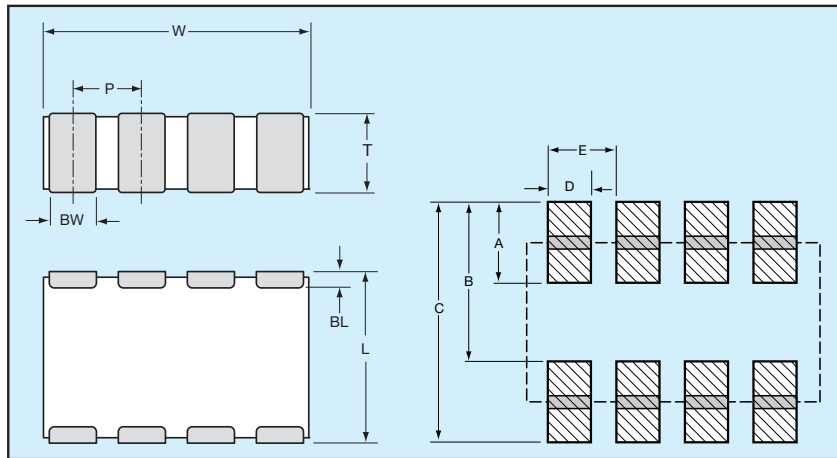
# IDC Low Inductance Capacitors (RoHS)

## 0306/0612/0508 IDC (InterDigitated Capacitors)

SIZE	0306		Thin 0508			0508			Thin 0612			0612			THICK 0612						
Max. Thickness	0.55 (0.022)		0.55 (0.022)			0.95 (0.037)			0.55 (0.022)			0.95 (0.037)			1.22 (0.048)						
WVDC	4	6.3	4	6.3	10	16	25	4	6.3	10	16	25	4	6.3	10	16	25	4	6.3	10	16
Cap (μF)	0.010																				
	0.022																				
	0.033																				
	0.047																				
	0.068																				
	0.10																				
	0.22																				
	0.33																				
	0.47																				
	0.68																				
	1.0																				
	1.5																				
	2.2																				
	3.3																				

### PHYSICAL DIMENSIONS AND PAD LAYOUT

Consult factory for additional requirements



- = X7R
- = X5R
- = X7S

### PHYSICAL CHIP DIMENSIONS millimeters (inches)

SIZE	W	L	BW	BL	P
<b>0306</b>	1.60 ± 0.20 (0.063 ± 0.008)	0.82 ± 0.10 (0.032 ± 0.006)	0.25 ± 0.10 (0.010 ± 0.004)	0.20 ± 0.10 (0.008 ± 0.004)	0.40 ± 0.05 (0.015 ± 0.002)
<b>0508</b>	2.03 ± 0.20 (0.080 ± 0.008)	1.27 ± 0.20 (0.050 ± 0.008)	0.30 ± 0.10 (0.012 ± 0.004)	0.25 ± 0.15 (0.010 ± 0.006)	0.50 ± 0.05 (0.020 ± 0.002)
<b>0612</b>	3.20 ± 0.20 (0.126 ± 0.008)	1.60 ± 0.20 (0.063 ± 0.008)	0.50 ± 0.10 (0.020 ± 0.004)	0.25 ± 0.15 (0.010 ± 0.006)	0.80 ± 0.10 (0.031 ± 0.004)

### PAD LAYOUT DIMENSIONS

SIZE	A	B	C	D	E
<b>0306</b>	0.38 (0.015)	0.89 (0.035)	1.27 (0.050)	0.20 (0.008)	0.40 (0.015)
<b>0508</b>	0.64 (0.025)	1.27 (0.050)	1.91 (0.075)	0.28 (0.011)	0.50 (0.020)
<b>0612</b>	0.89 (0.035)	1.65 (0.065)	2.54 (0.100)	0.45 (0.018)	0.80 (0.031)

# IDC Low Inductance Capacitors (SnPb)

## 0306/0612/0508 IDC with Sn/Pb Termination

### GENERAL DESCRIPTION

Inter-Digitated Capacitors (IDCs) are used for both semiconductor package and board level decoupling. The equivalent series inductance (ESL) of a single capacitor or an array of capacitors in parallel determines the response time of a Power Delivery Network (PDN). The lower the ESL of a PDN, the faster the response time. A designer can use many standard MLCCs in parallel to reduce ESL or a low ESL Inter-Digitated Capacitor (IDC) device. These IDC devices are available in versions with a maximum height of 0.95mm or 0.55mm.

IDCs are typically used on packages of semiconductor products with power levels of 15 watts or greater. Inter-Digitated Capacitors are used on CPU, GPU, ASIC, and ASSP devices produced on 0.13 $\mu$ m, 90nm, 65nm, and 45nm processes. IDC devices are used on both ceramic and organic package substrates. These low ESL surface mount capacitors can be placed on the bottom side or the top side of a package substrate. The low profile 0.55mm maximum height IDCs can easily be used on the bottom side of BGA packages or on the die side of packages under a heat spreader.

IDCs are used for board level decoupling of systems with speeds of 300MHz or greater. Low ESL IDCs free up valuable board space by reducing the number of capacitors required versus standard MLCCs. There are additional benefits to reducing the number of capacitors beyond saving board space including higher reliability from a reduction in the number of components and lower placement costs based on the need for fewer capacitors.

The Inter-Digitated Capacitor (IDC) technology was developed by AVX. This is the second family of Low Inductance MLCC products created by AVX. IDCs are a cost effective alternative to AVX's first generation low ESL family for high-reliability applications known as LICA (Low Inductance Chip Array).

AVX IDC products are available with a lead termination for high reliability military and aerospace applications that must avoid tin whisker reliability issues.



### TYPICAL IMPEDANCE



**Not RoHS Compliant**

### HOW TO ORDER

<b>L</b>	<b>3</b>	<b>L</b>	<b>1</b>	<b>6</b>	<b>D</b>	<b>225</b>	<b>M</b>	<b>A</b>	<b>B</b>	<b>3</b>	<b>A</b>
<b>Style</b>	<b>IDC Case Size</b>	<b>Low Inductance</b>	<b>Number of Terminals</b>	<b>Voltage</b>	<b>Dielectric</b>	<b>Capacitance Code (In pF)</b>	<b>Capacitance Tolerance</b>	<b>Failure Rate</b>	<b>Termination</b>	<b>Packaging Available</b>	<b>Thickness</b>
	2 = 0508 3 = 0612 4 = 0306		1 = 8 Terminals	4 = 4V 6 = 6.3V Z = 10V Y = 16V 3 = 25V	C = X7R D = X5R Z = X7S	2 Sig. Digits + Number of Zeros	M = $\pm 20\%$	A = N/A	B = 5% min. Lead	1=7" Reel 3=13" Reel	Max. Thickness mm (in.) A=Standard S=0.55 (0.022)

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

### PERFORMANCE CHARACTERISTICS

<b>Capacitance Tolerance</b>	$\pm 20\%$ Preferred
<b>Operation Temperature Range</b>	X7R = -55°C to +125°C X5R = -55°C to +85°C X7S = -55°C to +125°C
<b>Temperature Coefficient</b>	$\pm 15\%$ (0VDC), $\pm 22\%$ (X7S)
<b>Voltage Ratings</b>	4, 6.3, 10, 16, 25 VDC
<b>Dissipation Factor</b>	$\leq 6.3V = 6.5\%$ max; 10V = 5.0% max; $\geq 16V = 3.5\%$ max
<b>Insulation Resistance (@+25°C, RVDC)</b>	100,000M $\Omega$ min, or 1,000M $\Omega$ per $\mu F$ min., whichever is less

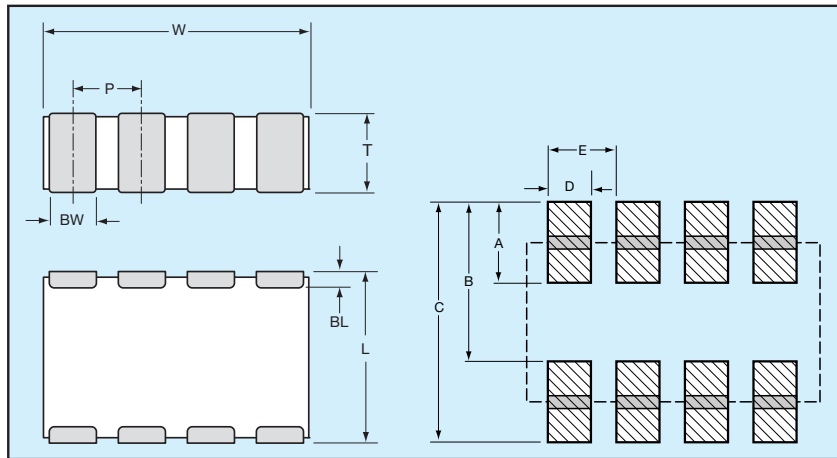
<b>Dielectric Strength</b>	No problems observed after 2.5 x RVDC for 5 seconds at 50mA max current
<b>CTE (ppm/C)</b>	12.0
<b>Thermal Conductivity</b>	4-5W/M K
<b>Terminations Available</b>	Plated Nickel and Solder

# IDC Low Inductance Capacitors (SnPb)

## 0306/0612/0508 IDC with Sn/Pb Termination

SIZE	0306		Thin 0508			0508			Thin 0612				0612					THICK 0612										
Max. Thickness	0.55 (0.022)		0.55 (0.022)			0.95 (0.037)			0.55 (0.022)				0.95 (0.037)					1.22 (0.048)										
WVDC	4	6.3	4	6.3	10	16	25	4	6.3	10	16	25	4	6.3	10	16	25	4	6.3	10	16	25	4	6.3	10	16		
Cap (μF)	Grid content representing availability of capacitor values across different sizes and WVDC ratings.																											

### PHYSICAL DIMENSIONS AND PAD LAYOUT



Consult factory for additional requirements

- = X7R
- = X5R
- = X7S

### PHYSICAL CHIP DIMENSIONS millimeters (inches)

SIZE	W	L	BW	BL	P
<b>0306</b>	1.60 ± 0.20 (0.063 ± 0.008)	0.82 ± 0.10 (0.032 ± 0.006)	0.25 ± 0.10 (0.010 ± 0.004)	0.20 ± 0.10 (0.008 ± 0.004)	0.40 ± 0.05 (0.015 ± 0.002)
<b>0508</b>	2.03 ± 0.20 (0.080 ± 0.008)	1.27 ± 0.20 (0.050 ± 0.008)	0.30 ± 0.10 (0.012 ± 0.004)	0.25 ± 0.15 (0.010 ± 0.006)	0.50 ± 0.05 (0.020 ± 0.002)
<b>0612</b>	3.20 ± 0.20 (0.126 ± 0.008)	1.60 ± 0.20 (0.063 ± 0.008)	0.50 ± 0.10 (0.020 ± 0.004)	0.25 ± 0.15 (0.010 ± 0.006)	0.80 ± 0.10 (0.031 ± 0.004)

### PAD LAYOUT DIMENSIONS

SIZE	A	B	C	D	E
<b>0306</b>	0.38 (0.015)	0.89 (0.035)	1.27 (0.050)	0.20 (0.008)	0.40 (0.015)
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<b>0612</b>	0.89 (0.035)	1.65 (0.065)	2.54 (0.100)	0.45 (0.018)	0.80 (0.031)



**Стандарт  
Электрон  
Связь**

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**Наши контакты:**

**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331