



Low-Power Audio/Video Interface for Single SCART Connectors

MAX9597

General Description

The MAX9597 single SCART interface routes audio and video signals between a set-top box decoder chip and an external SCART connector under I²C control. Operating from a 3.3V supply and a 12V supply, the MAX9597 consumes 53mW during quiescent operation and 254mW during average operation when driving typical signals into typical loads.

The MAX9597 audio section contains left and right audio paths with an independent operational amplifier at the inputs. The DirectDrive[®] output amplifiers create a 2VRMS full-scale audio signal biased around ground, eliminating the need for bulky output capacitors and reducing click-and-pop noise. The zero-cross detection circuitry also further reduces clicks and pops by enabling audio sources to switch only during a zero-crossing.

The MAX9597 video section contains 4 channels of video filter amplifiers. The standard-definition video signals from the set-top box decoder chip are lowpass filtered to remove out-of-bandwidth artifacts. The MAX9597 also supports slow-switching and fast-switching signals.

The MAX9597 is available in a compact 28-pin thin QFN package and is specified over the 0°C to +70°C commercial temperature range.

Features

- ◆ 53mW Quiescent Power Consumption
- ◆ 5μW Shutdown Consumption
- ◆ Audio Operational Amplifiers to Create Input Filters
- ◆ Clickless/Popless, DirectDrive Audio
- ◆ Video Reconstruction Filter with 10MHz Passband and 43dB Attenuation at 27MHz
- ◆ 3.3V and 12V Supply Voltages

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|-------------|--------------|-------------|
| MAX9597CTI+ | 0°C to +70°C | 28 TQFN-EP* |

+Denotes a lead-free/RoHS-compliant package.

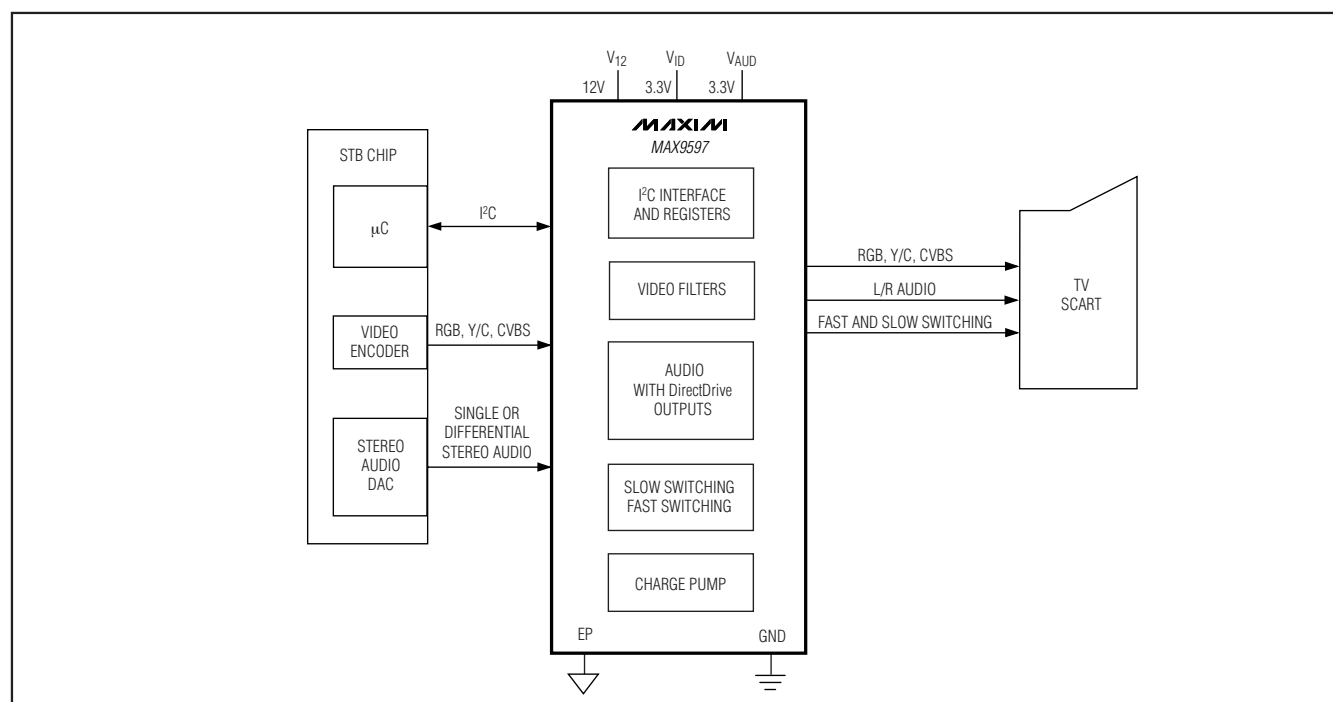
*EP = Exposed pad.

Applications

| | |
|---------------|-------------|
| Set-Top Boxes | TVs |
| AV Receivers | DVD Players |

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System Block Diagram



Low-Power Audio/Video Interface for Single SCART Connectors

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)

| | |
|------------------------------|--|
| V _{VID} | -0.3V to +4V |
| V ₁₂ to EP | -0.3V to +14V |
| V _{AUD} to EP | -0.3V to +4V |
| EP to GND | -0.1V to +0.1V |
| All Video Inputs | -0.3V to +4V |
| All Audio Inputs to EP | (V _{EP} - 1)V to (V _{EP} + 1)V |
| SDA, SCL, DEV_ADDR | -0.3V to +4V |
| TV_SS_OUT | -0.3V to (V ₁₂ + 0.3V) |
| Current | |
| All Video/Audio Inputs | ±20mA |
| C1P, C1N, CPVSS | ±50mA |

Output Short-Circuit Current Duration

| | |
|--|-----------------|
| All Video Outputs, TV_FS_OUT to V _{VID} , GND | Continuous |
| Audio Outputs to V _{AUD} , EP | Continuous |
| TV_SS_OUT to V ₁₂ , EP | Continuous |
| Continuous Power Dissipation (T _A = +70°C) | |
| 28-Pin Thin QFN | |
| (derate 21.3mW/°C above +70°C) | 1702mW |
| Operating Temperature Range | 0°C to +70°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{VID} = V_{AUD} = 3.3V, V₁₂ = 12V, GND = EP = 0, no load, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------------|---|------|------|------|-------|
| Video Supply Voltage Range | V _{VID} | Inferred from video PSRR test at 3.0V and 3.6V | 3.0 | 3.3 | 3.6 | V |
| Audio Supply Voltage Range | V _{AUD} | Inferred from audio PSRR tests at 3.0V and 3.6V | 3.0 | 3.3 | 3.6 | V |
| Slow-Switching Supply Voltage Range | V ₁₂ | Inferred from slow-switching levels | 11.4 | 12 | 12.6 | V |
| V _{VID} Quiescent Supply Current | I _{VID_Q} | Normal operation, all video output amplifiers are enabled | | 13 | 20 | mA |
| | | Shutdown | | 1 | 10 | μA |
| V _{AUD} Quiescent Supply Current | I _{AUD_Q} | Normal operation | | 3 | 4.1 | mA |
| | | Shutdown | | 0.01 | 10 | μA |
| V ₁₂ Quiescent Supply Current | I _{12_Q} | Normal operation | | 1.5 | 100 | μA |
| | | Shutdown | | 0.1 | 10 | μA |

VIDEO CHARACTERISTICS

DC-COUPLED INPUT

| | | | | | |
|---------------------|-----------------|---|---------------------------|----------|------------------|
| Input Voltage Range | V _{IN} | R _L = 75Ω to GND or 150Ω to V _{VID} /2, inferred from gain test | V _{VID} = 3V | 1.15 | V _{P-P} |
| | | | V _{VID} = 3.135V | 1.2 | |
| | | | V _{VID} = 3.3V | 1.3 | |
| Input Current | I _{IN} | V _{IN} = GND | | 2 3 | μA |
| Input Resistance | R _{IN} | | | 300 | kΩ |

AC-COUPLED INPUT

| | | | | | | |
|------------------------|------------------|---|----|---|-----|----|
| Sync-Tip Clamp Level | V _{CLP} | Sync-tip clamp | -5 | 0 | 6.1 | mV |
| Sync Crush | | Sync-tip clamp; percentage reduction in sync pulse (0.3V _{P-P}); guaranteed by input clamping current measurement | | | 2 | % |
| Input Clamping Current | | Sync-tip clamp | | 2 | 3 | μA |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{VID} = V_{AUD} = 3.3V$, $V_{I2} = 12V$, $GND = EP = 0$, no load, $T_A = 0^{\circ}C$ to $+70^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------|------------|---|--|------|----------------------|------------------|
| Max Input Source Resistance | | | | 300 | | Ω |
| Bias Voltage | V_{BIAS} | Bias circuit | 0.57 | 0.6 | 0.63 | V |
| Input Resistance | | Bias circuit | | 10 | | k Ω |
| DC CHARACTERISTICS | | | | | | |
| DC Voltage Gain | A_V | $R_L = 75\Omega$ to GND or $R_L = 150\Omega$ to $V_{VID}/2$ | $V_{VID} = 3V$, $V_{IN} = V_{CLP}$ to $(V_{CLP} + 1.15V)$ | | 2 | V/V |
| | | | $V_{VID} = 3.135V$, $V_{IN} = V_{CLP}$ to $(V_{CLP} + 1.2V)$ | | 1.93 2 2.05 | |
| | | | $V_{VID} = 3V$, $V_{IN} = (V_{BIAS} - 0.575V)$ to $(V_{BIAS} + 0.575V)$ | | 2 | |
| | | | $V_{VID} = 3.135V$, $V_{IN} = (V_{BIAS} - 0.6V)$ to $(V_{BIAS} + 0.6V)$ | | 1.93 2 2.05 | |
| DC Gain Mismatch | | Guaranteed by DC voltage gain | -2 | | +2 | % |
| Output Level | | Sync-tip clamp | 0.2 | 0.30 | 0.4 | V |
| | | Bias circuit | 1.38 | 1.5 | 1.62 | |
| Output Voltage Swing | | Guaranteed by DC voltage gain | Sync-tip clamp, measured at output, $V_{VID} = 3V$, $V_{IN} = V_{CLP}$ to $(V_{CLP} + 1.15V)$, $R_L = 75\Omega$ to GND or $R_L = 150\Omega$ to $V_{VID}/2$ | | 2.3 | V _{P-P} |
| | | | Measured at output, $V_{VID} = 3.135V$, $V_{IN} = V_{CLP}$ to $(V_{CLP} + 1.2V)$, $R_L = 75\Omega$ to GND or $R_L = 150\Omega$ to $V_{VID}/2$ | | 2.316 2.4 2.46 | |
| | | | Bias circuit, measured at output, $V_{VID} = 3V$, $V_{IN} = (V_{BIAS} - 0.575V)$ to $(V_{BIAS} + 0.575V)$, $R_L = 75\Omega$ to GND or $R_L = 150\Omega$ to $V_{VID}/2$ | | 2.3 | |
| | | | Measured at output, $V_{VID} = 3.135V$, $V_{IN} = (V_{BIAS} - 0.6V)$ to $(V_{BIAS} + 0.6V)$, $R_L = 75\Omega$ to GND or $R_L = 150\Omega$ to $V_{VID}/2$ | | 2.316 2.4 2.46 | |
| Output Short-Circuit Current | | | | 100 | | mA |
| Output Leakage Current | | Output disabled | | 0.02 | 10 | μA |
| Power-Supply Rejection Ratio | | $3.0V \leq V_{VID} \leq 3.6V$ | 50 | 75 | | dB |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{ID} = V_{AUD} = 3.3V$, $V_{12} = 12V$, $GND = EP = 0$, no load, $T_A = 0^\circ C$ to $+70^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------|--|---------------------|--------|------|-----------|
| AC CHARACTERISTICS | | | | | | |
| Filter Passband Flatness | | $V_{OUT} = 2V_{P-P}$, $f = 100kHz$ to $10MHz$ | | 1 | | dB |
| Filter Attenuation | | $V_{OUT} = 2V_{P-P}$, attenuation is referred to $100kHz$ | $f = 11MHz$ | 3 | | dB |
| | | | $f = 27MHz$ | 43 | | |
| | | | $f = 54MHz$ | 63 | | |
| Differential Gain | DG | 5-step modulated staircase, $f = 4.43MHz$ | | 0.2 | | % |
| Differential Phase | DP | 5-step modulated staircase, $f = 4.43MHz$ | | 0.3 | | Degrees |
| 2T Pulse-to-Bar K Rating | | $2T = 200ns$; bar time is $18\mu s$; the beginning 2.5% and the ending 2.5% of the bar time is ignored | | 0.5 | | K% |
| 2T Pulse Response | | $2T = 200ns$ | | 0.5 | | K% |
| 2T Bar Response | | $2T = 200ns$; bar time is $18\mu s$; the beginning 2.5% and the ending 2.5% of the bar time is ignored | | 0.5 | | K% |
| Nonlinearity | | 5-step staircase | | 0.5 | | % |
| Group Delay Distortion | | $100kHz \leq f \leq 5MHz$, outputs are $2V_{P-P}$ | | 3.5 | | ns |
| Peak Signal to RMS Noise | | $100kHz \leq f \leq 5MHz$ | | 60 | | dB |
| Power-Supply Rejection Ratio | | $f = 100kHz$, $100mV_{P-P}$ | | 47 | | dB |
| Output Impedance | | $f = 5MHz$ | | 5.5 | | Ω |
| Video Crosstalk | | $f = 4.43MHz$ | | -68.5 | | dB |
| AUDIO CHARACTERISTICS OUTPUT AMPLIFIER (Note 2) | | | | | | |
| Voltage Gain | | | 3.95 | 4 | 4.05 | V/V |
| Gain Mismatch | | | -1.5 | | +1.5 | % |
| Flatness | | $f = 20Hz$ to $20kHz$, $0.25V_{RMS}$ input | | 0.01 | | dB |
| Frequency Bandwidth | | $0.25V_{RMS}$ input, frequency where output is -3dB referenced to $1kHz$ | | 205 | | kHz |
| Capacitive Drive | | No sustained oscillations, 75Ω series resistor on output | | 300 | | pF |
| Input Signal Amplitude | | $f = 1kHz$, THD < 1% | | 0.5 | | V_{RMS} |
| Output DC Level | | No input signal, $V_{IN} = 0V$ | -3 | | +3 | mV |
| Power-Supply Rejection Ratio | | DC | 75 | 110 | | dB |
| | | $f = 1kHz$ | | 91 | | |
| Signal-to-Noise Ratio | | $f = 1kHz$, $0.25V_{RMS}$ input, $20Hz$ to $20kHz$ | | 97 | | dB |
| Total Harmonic Distortion Plus Noise | | $R_L = 3.3k\Omega$, $f = 1kHz$ | $0.25V_{RMS}$ input | 0.0011 | | % |
| | | | $0.5V_{RMS}$ input | 0.0021 | | |
| Output Impedance | | $f = 1kHz$ | | 0.28 | | Ω |
| Mute Suppression | | $f = 1kHz$, $0.25V_{RMS}$ input | | 101 | | dB |
| Audio Crosstalk | | $f = 1kHz$, $0.25V_{RMS}$ input | | 100 | | dB |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{VID} = V_{AUD} = 3.3V$, $V_{12} = 12V$, $GND = EP = 0$, no load, $T_A = 0^\circ C$ to $+70^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|------------------|--|-------------------------------|------------------------|--------------------------|--------|------------------|
| VIDEO TO AUDIO INTERACTION | | | | | | | |
| Crosstalk | | Video input: f = 15kHz, 1V _{P-P} signal | | 100 | | dB | |
| | | Audio input: f = 15kHz, 0.1V _{RMS} signal | | 102 | | | |
| INPUT AMPLIFIER OPEN-LOOP CHARACTERISTICS | | | | | | | |
| Input Offset Voltage | V _{OS} | V _{CM} = 0V | T _A = +25°C | 25 | 100 | μV | |
| | | | T _A = 0°C to +70°C | 225 | | | |
| Input Bias Current | I _B | V _{CM} = 0V | | 100 | 550 | nA | |
| Input Offset Current | I _{OS} | V _{CM} = 0V | | 1.5 | 30 | nA | |
| Common-Mode Input Voltage Range | V _{CM} | Inferred from CMRR test | | -0.707 | +0.707 | | V |
| Common-Mode Rejection Ratio | CMRR | | | 80 | 100 | dB | |
| Power-Supply Rejection Ratio | PSRR | V _{CM} = 0V | | 90 | 125 | dB | |
| Large-Signal Voltage Gain | A _{VOL} | V _{CM} = 0V, -0.8V ≤ V _{OUT} ≤ +0.8V | | 60 | 80 | dB | |
| Output Voltage Swing | V _{OUT} | R _L = 124Ω, inferred from A _{VOL} test | | 1.6 | | | V _{P-P} |
| Gain-Bandwidth Product | GBWP | | | 8.25 | | MHz | |
| Slew Rate | SR | | | 1.24 | | V/μs | |
| Input Voltage-Noise Density | V _N | f = 1kHz | | 13.5 | | nV/√Hz | |
| Input Current-Noise Density | I _N | f = 1kHz | | 0.2 | | pA/√Hz | |
| Capacitive Load Stability | | A _{VCL} = 1V/V, no sustained oscillation | | 20 | | pF | |
| CHARGE PUMP | | | | | | | |
| Switching Frequency | | | | 580 | | kHz | |
| FAST SWITCHING | | | | | | | |
| Output Low Voltage | | I _{OL} = 0.5mA | | 0.003 | 0.1 | V | |
| Output High Voltage | | I _{OH} = 0.5mA | | V _{VID} - 0.1 | V _{VID} - 0.003 | V | |
| Output Resistance | | | | 5.5 | | Ω | |
| Rise Time | | R _L = 143Ω to GND | | 2 | | ns | |
| Fall Time | | R _L = 143Ω to GND | | 2 | | ns | |
| SLOW SWITCHING | | | | | | | |
| Output Low Voltage | | 10kΩ to EP, 11.4V ≤ V _{I2} ≤ 12.6V | | 1.5 | | V | |
| Output Medium Voltage | | 10kΩ to EP, 11.4V ≤ V _{I2} ≤ 12.6V | | 5 | 6.5 | V | |
| Output High Voltage | | 10kΩ to EP, 11.4V ≤ V _{I2} ≤ 12.6V | | 10 | V | | |
| Input Current | | | | -1 | +1 | μA | |
| DIGITAL INTERFACE (SDA, SCL) | | | | | | | |
| Input High Voltage | V _{IH} | | | 0.7 x V _{VID} | | V | |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{VID} = V_{AUD} = 3.3V$, $V_{12} = 12V$, $GND = EP = 0$, no load, $T_A = 0^\circ C$ to $+70^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------------|---|-----------------------|-----|----------------------|---------|
| Input Low Voltage | V_{IL} | | | | $0.3 \times V_{VID}$ | V |
| Input Hysteresis | V_{HYS} | | $0.05 \times V_{VID}$ | | | V |
| Input Leakage Current | I_{IH}, I_{IL} | SCL and SDA have $40k\Omega$ pullup resistors to V_{VID} | -1 | | +1 | μA |
| Input Capacitance | | | | 10 | | pF |
| Input Current | | $V_{VIDMAX} = 3.6V$ $0.1V_{VID} < SDA < 0.9V_{VIDMAX}$ $0.1V_{VID} < SCL < 0.9V_{VIDMAX}$ I/O pins of fast-mode devices must not obstruct the SDA and SCL lines if V_{VID} is switched off | -10 | | +10 | μA |
| Output Low Voltage SDA | V_{OL} | $I_{SINK} = 6mA$ | | | 0.4 | V |
| Serial-Clock Frequency | f_{SCL} | | 0 | | 400 | kHz |
| Bus Free Time Between a STOP and a START Condition | t_{BUF} | | 1.3 | | | μs |
| Hold Time, (REPEATED) START Condition | $t_{HD, STA}$ | | 0.6 | | | μs |
| Low Period of the SCL Clock | t_{LOW} | | 1.3 | | | μs |
| High Period of the SCL Clock | t_{HIGH} | | 0.6 | | | μs |
| Setup Time for a REPEATED START Condition | $t_{SU, STA}$ | | 0.6 | | | μs |
| Data Hold Time | $t_{HD, DAT}$ | A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge | 0 | | 0.9 | μs |
| Data Setup Time | $t_{HD, DAT}$ | | 100 | | | ns |
| Fall Time of SDA Transmitting | t_F | C_B = total capacitance of one bus line in pF < 400pF; t_R and t_F measured between $0.3V_{VID}$ and $0.7V_{VID}$ (C_B is in pF) | | 250 | | ns |
| Setup Time for STOP Condition | $t_{SU, STO}$ | | 0.6 | | | μs |
| Pulse Width of Spike Suppressed | t_{SP} | Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns | 0 | | 50 | ns |
| OTHER DIGITAL I/O | | | | | | |
| DEV_ADDR Low Level | | | | | $0.3 \times V_{VID}$ | V |
| DEV_ADDR High Level | | | $0.7 \times V_{VID}$ | | | V |
| DEV_ADDR Input Current | | | -1 | | +1 | μA |

Note 1: All devices are 100% production tested at $T_A = +25^\circ C$ and are guaranteed by design for $T_A = 0^\circ C$ to $+70^\circ C$ as specified.

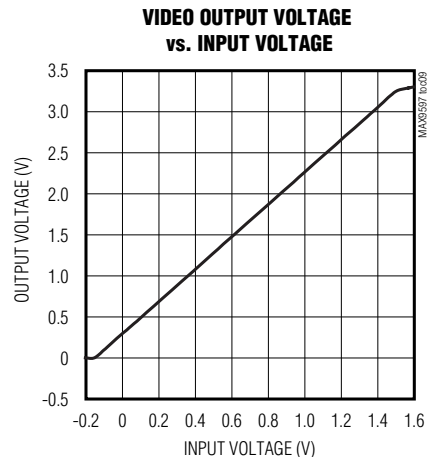
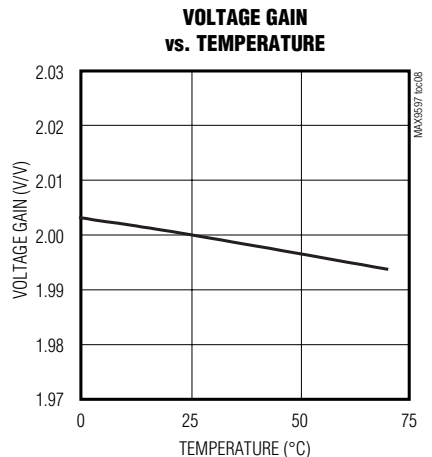
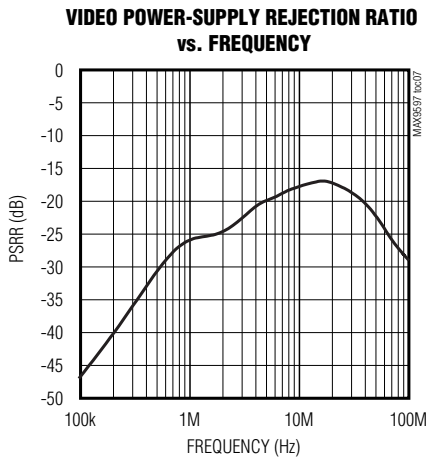
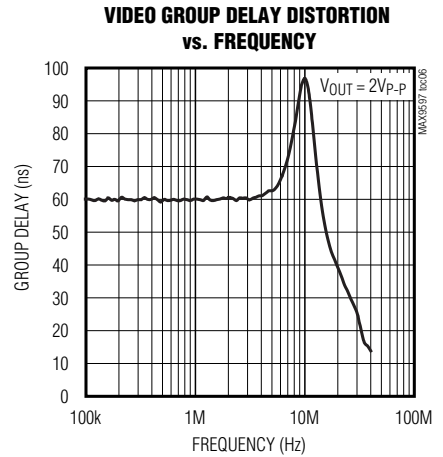
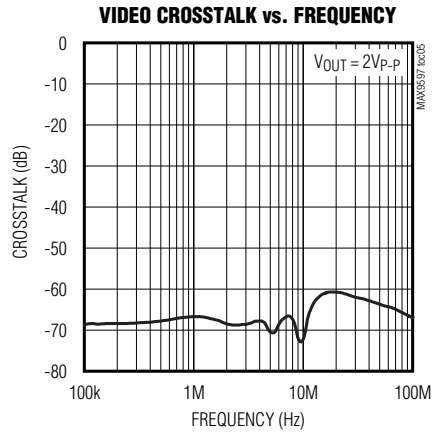
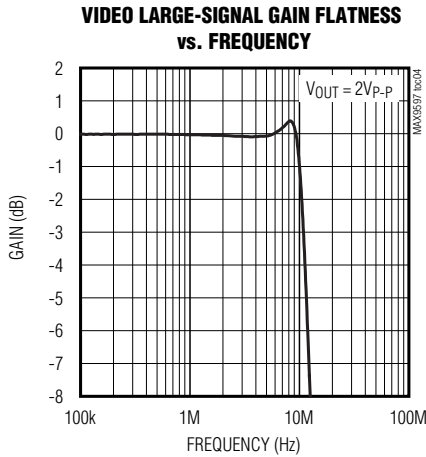
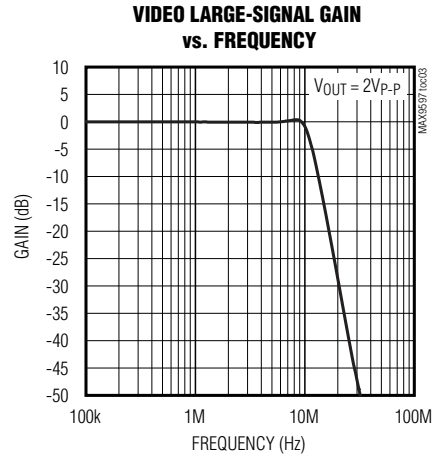
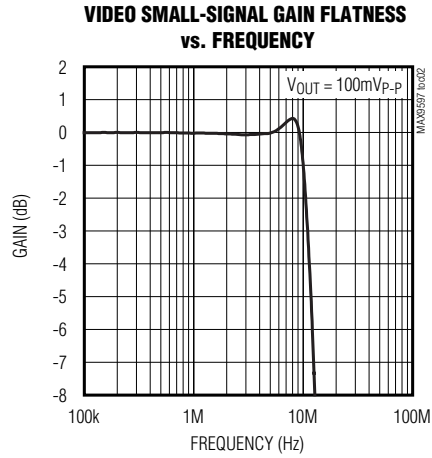
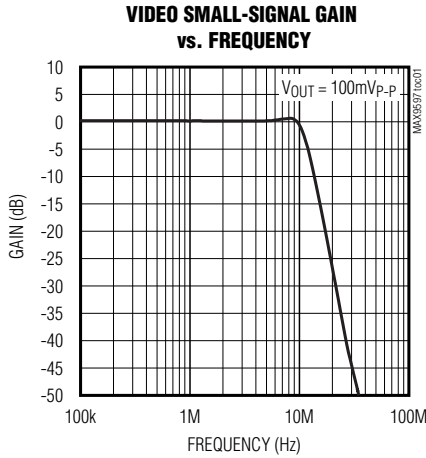
Note 2: Input operational amplifier configured in voltage follower configuration, unless otherwise noted.

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Typical Operating Characteristics

($V_{VID} = V_{AUD} = 3.3V$, $V_{I2} = 12V$, $GND = EP = 0$, video load is 150Ω to GND , audio load is $10k\Omega$ to GND , $T_A = +25^\circ C$, unless otherwise noted.)

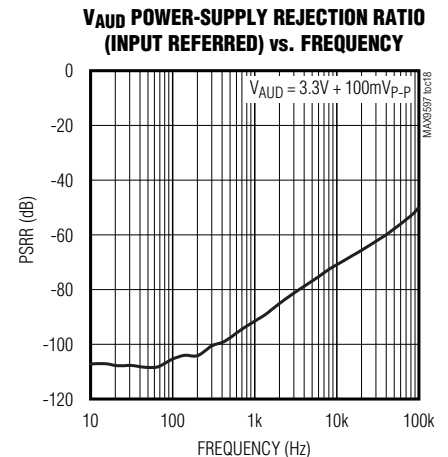
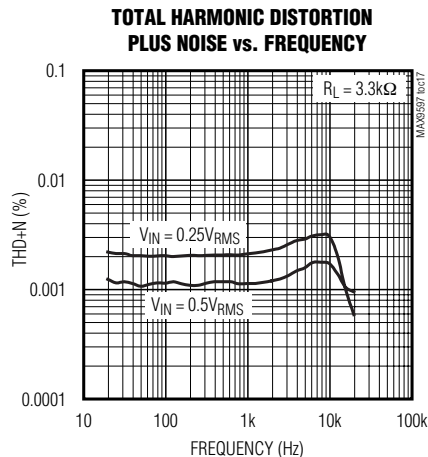
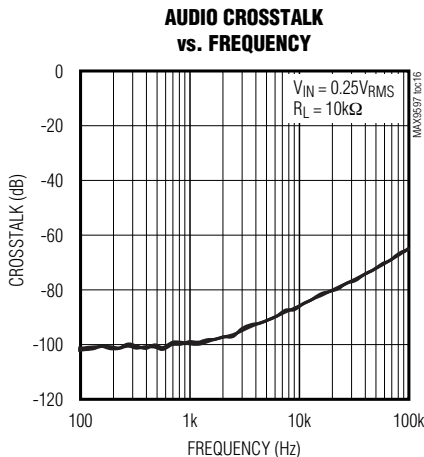
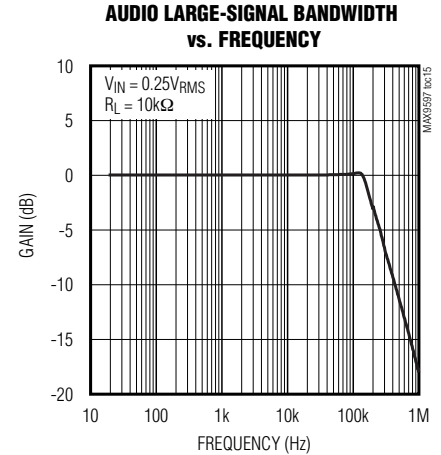
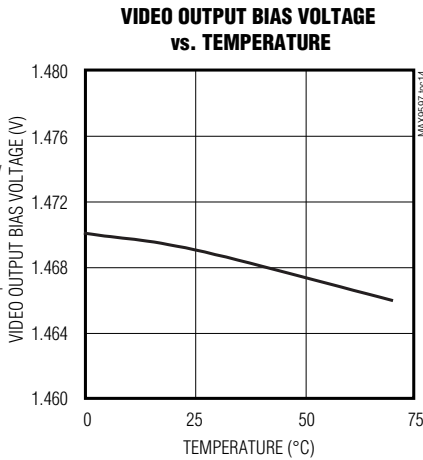
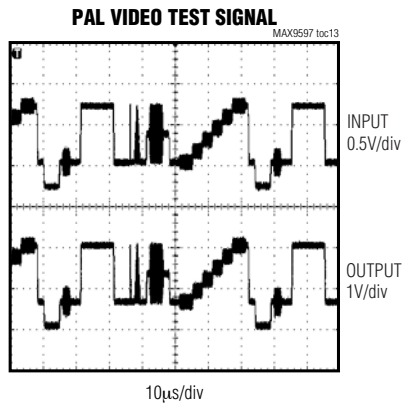
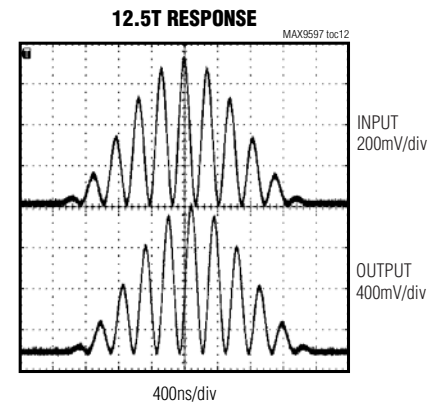
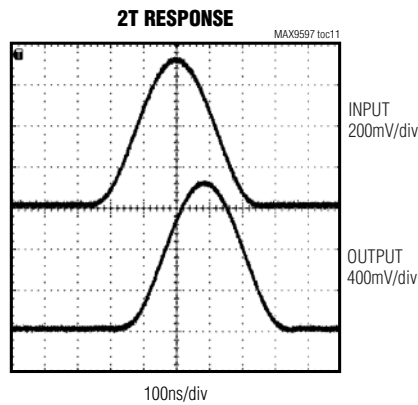
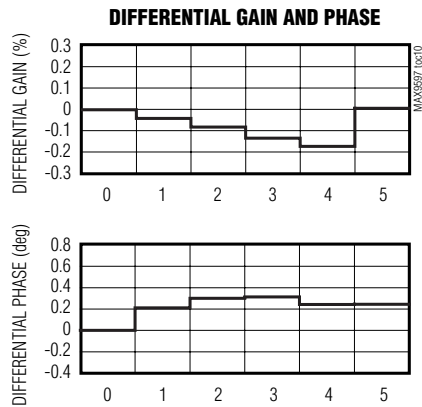
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Typical Operating Characteristics (continued)

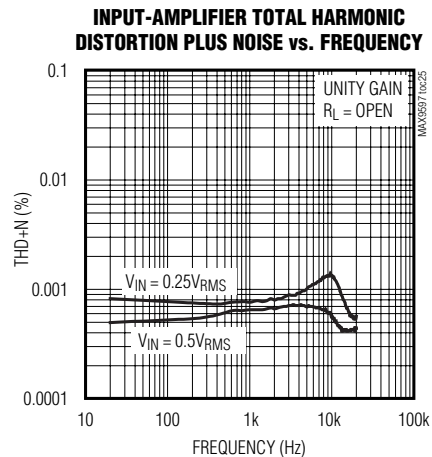
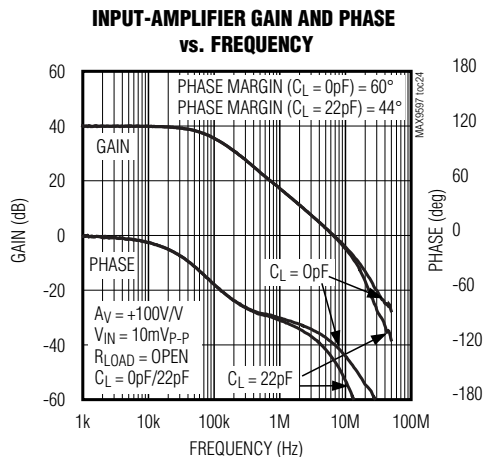
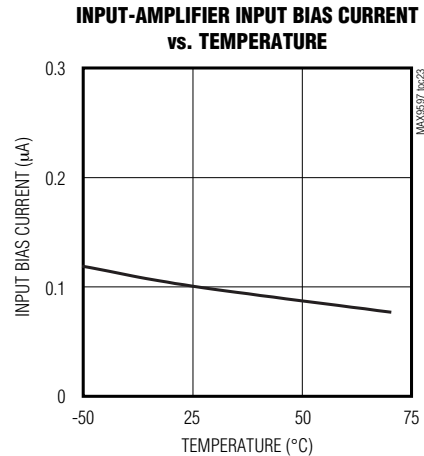
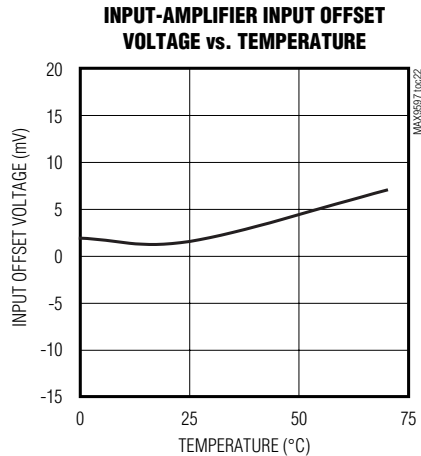
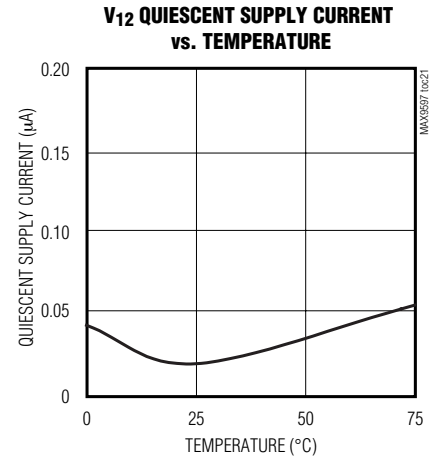
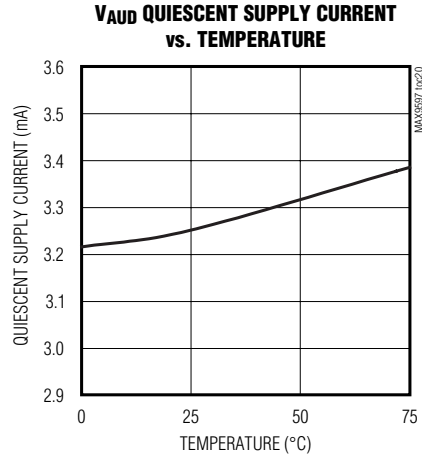
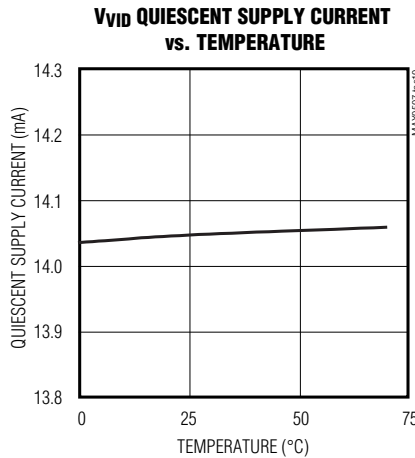
($V_{VID} = V_{AUD} = 3.3V$, $V_{12} = 12V$, GND = EP = 0, video load is 150Ω to GND, audio load is $10k\Omega$ to GND, $T_A = +25^\circ C$, unless otherwise noted.)



Low-Power Audio/Video Interface for Single SCART Connectors

Typical Operating Characteristics (continued)

($V_{VID} = V_{AUD} = 3.3V$, $V_{12} = 12V$, GND = EP = 0, video load is 150Ω to GND, audio load is $10k\Omega$ to GND, $T_A = +25^\circ C$, unless otherwise noted.)

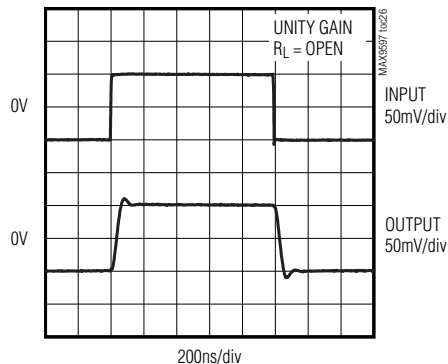


Low-Power Audio/Video Interface for Single SCART Connectors

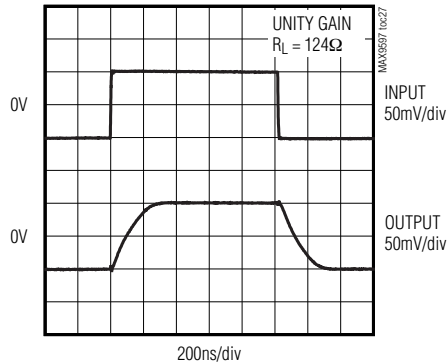
Typical Operating Characteristics (continued)

($V_{VID} = V_{AUD} = 3.3V$, $V_{12} = 12V$, $GND = EP = 0$, video load is 150Ω to GND , audio load is $10k\Omega$ to GND , $T_A = +25^\circ C$, unless otherwise noted.)

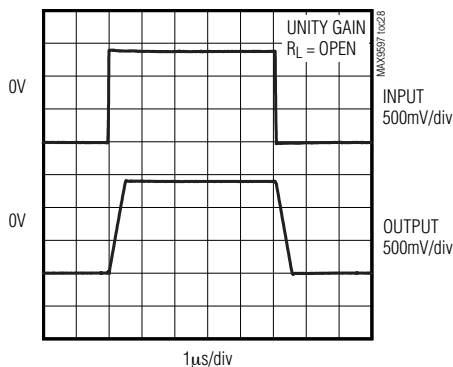
**INPUT-AMPLIFIER SMALL-SIGNAL
TRANSIENT RESPONSE**



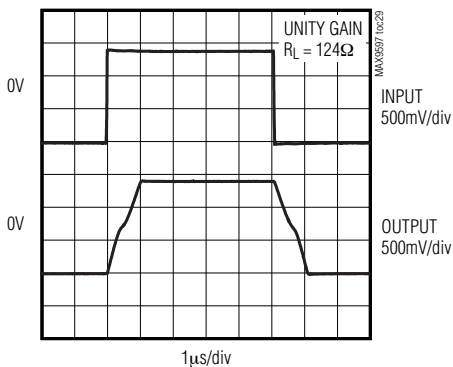
**INPUT-AMPLIFIER SMALL-SIGNAL
TRANSIENT RESPONSE**



**INPUT-AMPLIFIER LARGE-SIGNAL
TRANSIENT RESPONSE**



**INPUT-AMPLIFIER LARGE-SIGNAL
TRANSIENT RESPONSE**



Low-Power Audio/Video Interface for Single SCART Connectors

Pin Description

| PIN | NAME | FUNCTION |
|-----|------------------|--|
| 1 | V _{AUD} | Audio Supply. Connect to a 3.3V supply. Bypass with a 10μF aluminum electrolytic capacitor in parallel with a 0.1μF ceramic capacitor to EP. |
| 2 | C1P | Charge-Pump Flying Capacitor Positive Terminal. Connect a 1μF capacitor from C1P to C1N. |
| 3 | C1N | Charge-Pump Flying Capacitor Negative Terminal. Connect a 1μF capacitor from C1P to C1N. |
| 4 | CPVSS | Charge-Pump Negative Power Supply. Bypass with a 10μF aluminum electrolytic capacitor in parallel with a 1μF ceramic capacitor to EP. |
| 5 | DEV_ADDR | Device Address Set Input. Connect DEV_ADDR to GND, V _{VID} , SDA, or SCL. See Table 3. |
| 6 | SDA | Bidirectional, I ² C Data I/O. Output is open drain and tolerates up to 3.6V. |
| 7 | SCL | I ² C Clock Input |
| 8 | ENC_B_IN | Encoder Blue Video Input |
| 9 | ENC_G_IN | Encoder Green Video Input |
| 10 | ENC_R/C_IN | Encoder Red/Chroma Video Input |
| 11 | ENC_CVBS_IN | Encoder Composite Video Input |
| 12 | TV_CVBS_OUT | TV SCART Composite Video Output. The sync tip is biased at 0.3V. |
| 13 | V _{VID} | Video and Digital Supply. Connect to a +3.3V supply. Bypass with a parallel 1μF and 0.1μF ceramic capacitor to GND. V _{VID} also serves as a digital supply for the I ² C interface. |
| 14 | TV_FS_OUT | TV SCART Fast-Switching Logic Output. This signal drives a back-terminated, 75Ω transmission line. |
| 15 | GND | Video Ground |
| 16 | TV_R/C_OUT | TV SCART Red/Chroma Video Output. The black level of the red signal is set to 0.3V and the blank level of the chroma signal is 1.5V. |
| 17 | TV_G_OUT | TV SCART Green Video Output. The black level of the green signal is set to 0.3V. |
| 18 | TV_B_OUT | TV SCART Blue Video Output. The black level of the blue signal is set to 0.3V. |
| 19 | V ₁₂ | +12V Supply. Bypass V ₁₂ with a 0.1μF capacitor to EP. |
| 20 | TV_SS_OUT | TV SCART Slow-Switch Signal Output |
| 21 | TV_OUTL | TV SCART Left-Channel Audio Output |
| 22 | ENC_INL+ | Left Input-Amplifier Noninverting Terminal |
| 23 | ENC_INL- | Left Input-Amplifier Inverting Terminal |
| 24 | ENC_INLOUT | Left Input-Amplifier Output |
| 25 | ENC_INROUT | Right Input-Amplifier Output |
| 26 | ENC_INR- | Right Input-Amplifier Inverting Terminal |
| 27 | ENC_INR+ | Right Input-Amplifier Noninverting Terminal |
| 28 | TV_OUTR | TV SCART Right-Channel Audio Output |
| — | EP | Exposed Pad. The exposed pad is the internal ground for the audio amplifiers and charge pump. A low-impedance connection to EP is required for proper isolation. |

MAX9597

Low-Power Audio/Video Interface for Single SCART Connectors

Detailed Description

The MAX9597 represents Maxim's third generation of SCART audio/video (A/V) switches. Under I²C control, these devices route audio, video, and control information between the set-top box decoder chip and a SCART connector. The audio signals are left audio and right audio. The video signals are composite video with blanking and sync (CVBS) and component video (red, green, blue). S-video (Y/C) can be transported across the SCART interface if CVBS is reassigned to luma (Y) and red is reassigned to chroma (C). Support for S-video is optional. The slow-switch signal and the fast-switch signal carry control information. The slow-switch signal is a 12V, trilevel signal that indicates whether the picture aspect ratio is 4:3, 16:9, or causes the television to use an internal A/V source, such as an antenna. The fast-switch signal indicates whether the television should display CVBS or RGB signals.

CVBS, left audio, and right audio are full duplex. All the other signals are half duplex. Therefore, one device on the link must be designated as the transmitter, and the other device must be designated as the receiver.

The low power consumption of the MAX9597 enables the creation of lower power set-top boxes, televisions, and DVD players. Unlike competing SCART ICs, the audio and video circuits of the MAX9597 operate entirely from 3.3V rather than from 5V and 12V. Only the slow-switch circuit of the MAX9597 requires a 12V supply.

The MAX9597 features DirectDrive audio circuitry to eliminate click-and-pop noise. With DirectDrive, the DC bias of the audio line outputs is always at ground when the MAX9597 is being powered up or powered down. Conventional audio line output drivers that operate from a single supply require series AC-coupling capacitors. During power-up, the DC bias on the AC-coupling capacitor moves from ground to a positive voltage, and during power-down, the opposite occurs. The changing DC bias usually causes an audible transient.

Audio Section

The audio circuit consists of a left and right audio path, each with an independent operational amplifier followed by a gain-of-4 amplifier. The encoder (stereo audio DAC) is the input source, and the output goes to the TV SCART connector. See Figure 1.

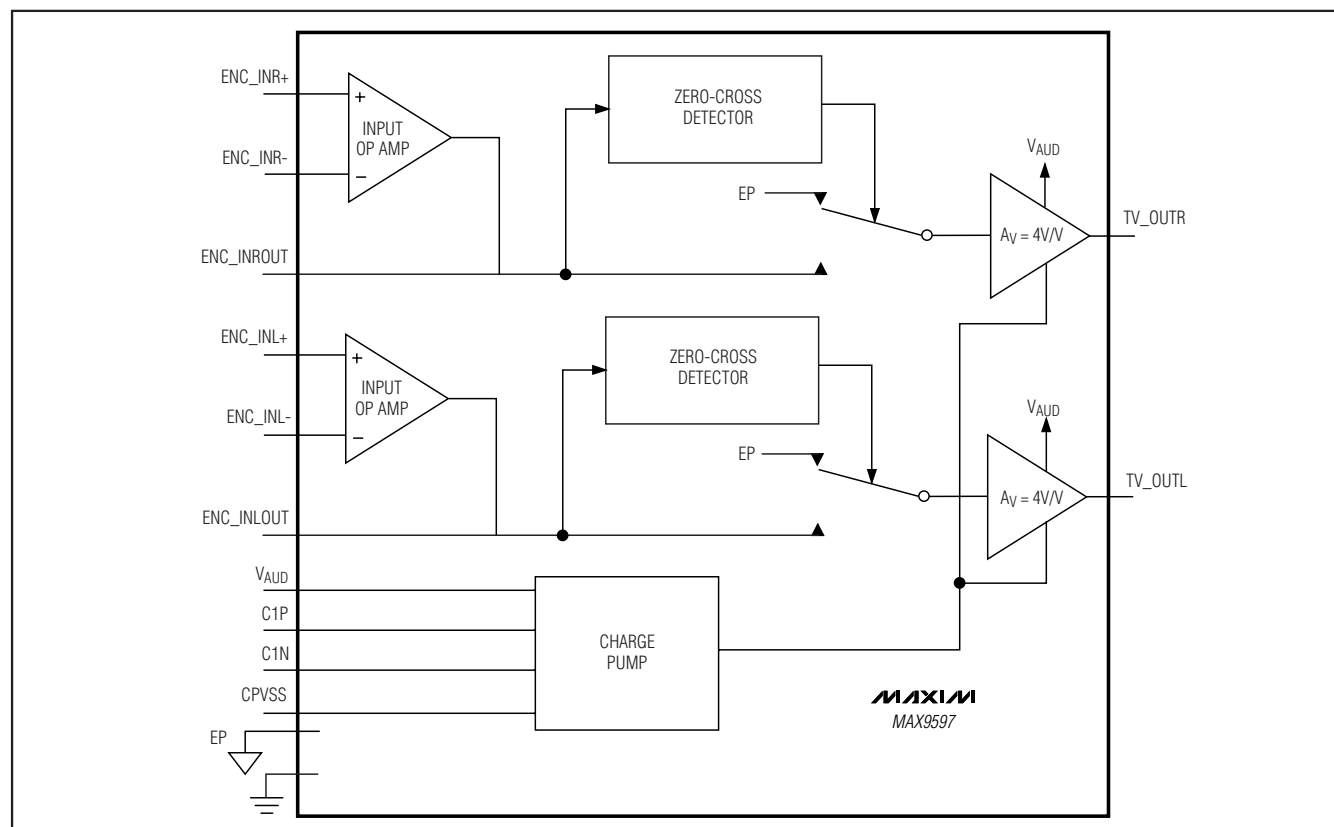


Figure 1. MAX9597 Audio Section Functional Diagram

Low-Power Audio/Video Interface for Single SCART Connectors

The full-scale output of the independent operational amplifiers is $0.5V_{RMS}$. The closed-loop gain of the operational amplifier circuit should be designed such that the resulting full-scale output is $0.5V_{RMS}$. The fixed, gain-of-4 amplifiers that follow the independent operational amplifiers amplify the $0.5V_{RMS}$ to $2V_{RMS}$, which complies with the SCART standard.

An integrated charge pump inverts the $+3.3V$ supply (V_{AUD}) to create a $-3.3V$ supply ($CPVSS$), enabling the audio circuit to operate from bipolar supplies. The audio signal from the beginning to the end of the signal path is always biased at ground.

Clickless Muting and Unmuting

The TV audio channel incorporates a zero-crossing detect (ZCD) circuit that minimizes click noise due to abrupt signal level changes that occur when entering or coming out of a mute condition at an arbitrary moment.

To implement the zero-crossing function when switching audio signals, set ZCD (register 00h, bit 6) high. The MAX9597 switches the signal in or out of mute at the next zero crossing after the mute or unmute request occurs. See Table 8.

Audio Outputs

The MAX9597 audio output amplifiers feature Maxim's DirectDrive architecture, eliminating the need for output-coupling capacitors required by conventional single-supply audio line drivers. Conventional single-supply audio line drivers have their outputs biased about a nominal DC voltage (typically half the supply) for maximum dynamic range. Large coupling capacitors are needed to block this DC bias. Clicks and pops are created when the coupling capacitors are charged during power-up and discharged during power-down.

An internal charge pump inverts the positive supply (V_{AUD}), creating a negative supply ($CPVSS$). The audio output amplifiers operate from the bipolar supplies with the outputs biased about audio ground (Figure 2). The benefit of this audio ground bias is that the amplifier outputs do not have a DC component. The DC-blocking capacitors required with conventional audio line drivers are unnecessary, conserving board space, reducing system cost, and improving frequency response.

The MAX9597 features a low-noise charge pump that requires only two small ceramic capacitors. The 580kHz switching frequency is well beyond the audio range and does not interfere with audio signals. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. The di/dt noise caused by the parasitic bond

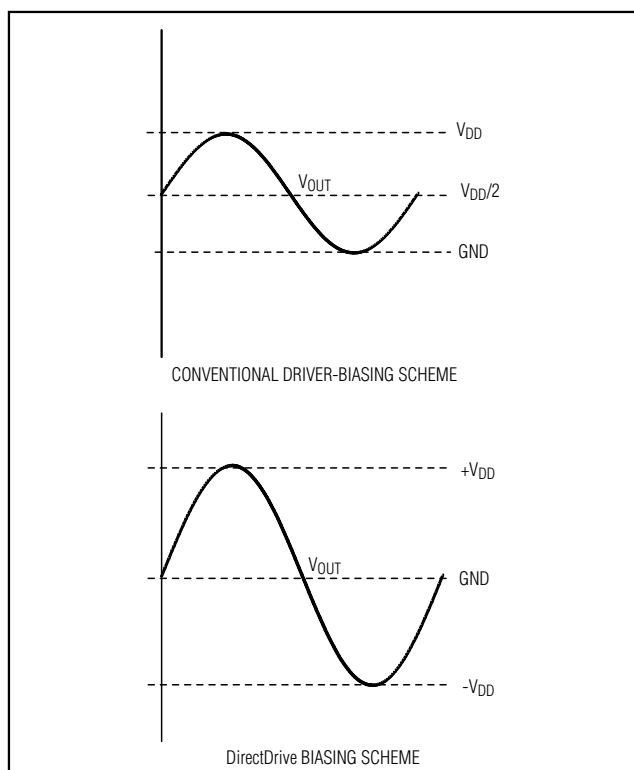


Figure 2. Conventional Driver Output Waveform vs. MAX9597 Output Waveform

wire and trace inductance is minimized by limiting the switching speed of the charge pump.

The SCART standard specifies $2V_{RMS}$ as the full-scale for audio signals. As the audio circuits process $0.5V_{RMS}$ full-scale audio signals internal to the MAX9597, the gain-of-4 output amplifiers restore the audio signals to a full scale of $2V_{RMS}$.

Video Section

The video circuit routes different video formats between the set-top box decoder and the TV SCART connector. It also routes slow-switch and fast-switch control information as shown in Figure 3.

Video Inputs

Whether the incoming video input signal is AC-coupled or DC-coupled into the MAX9597 depends upon the origin, format, and voltage range of the video signal. Table 1 below shows the recommended connections. Always AC-couple an external video signal through a $0.1\mu F$ capacitor because its voltage range is not well defined (see the *Typical Application Circuit*). For example, the

Low-Power Audio/Video Interface for Single SCART Connectors

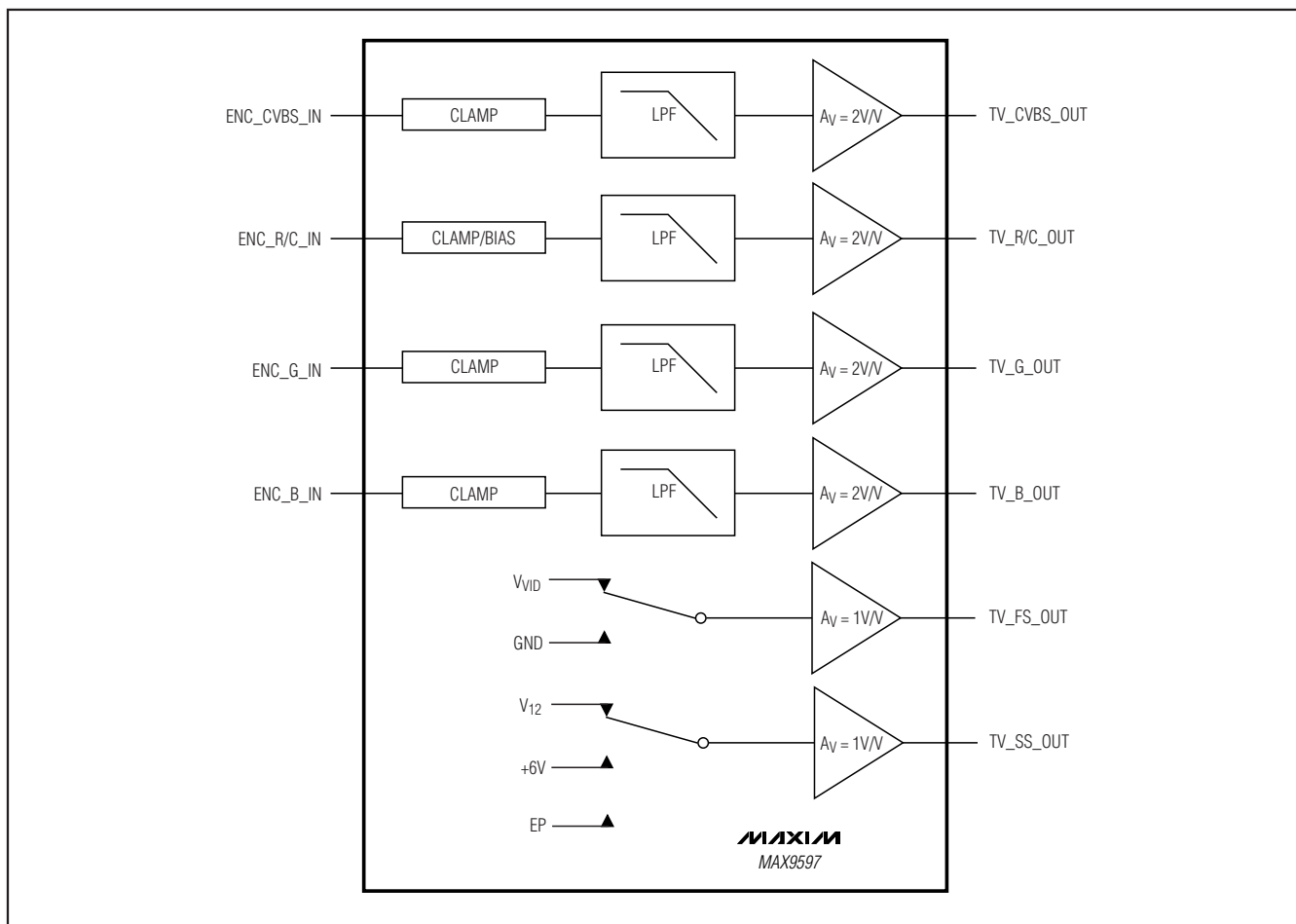


Figure 3. MAX9597 Video Section Function Diagram

video transmitter circuit might have a different ground than the video receiver, thereby level shifting the DC bias. The 50Hz power line hum might cause the video signal to change DC bias slowly.

Internal video signals that are between 0V and 1V can be DC-coupled. Most video DACs generate video signals between 0V and 1V because the video DAC sources current into a ground-referenced resistor. For the minority of video DACs that generate video signals between 2.3V and 3.3V because the video DAC sinks current from a V_{DD} -referenced resistor, AC-couple the video signal to the MAX9597.

The MAX9597 restores the DC level of incoming, AC-coupled video signals with either transparent sync-tip clamps or bias circuits. When using an AC-coupled input, the transparent sync-tip clamp automatically clamps the input signal minimum to ground, preventing it

from going lower. A small current of 2 μ A pulls down on the input to prevent an AC-coupled signal from drifting outside the input range of the part. The transparent sync-tip clamp is used with CVBS, RGB, and luma signals.

The transparent sync-tip clamp is transparent when the incoming video signal is DC-coupled and at ground or above. Under such conditions, the clamp never activates. Therefore, the outputs of video DACs that generate signals between 0V and 1V can be directly connected to the MAX9597 inputs.

The bias circuit accepts AC-coupled chroma, which is a subcarrier with the color information modulated onto it. The bias voltage of the bias circuits is around 600mV.

ENC_R/C_IN can receive either a red video signal or a chroma video signal. Set the input configuration by writing to bit 3 of register 08h. See Table 10.

Low-Power Audio/Video Interface for Single SCART Connectors

Table 1. Recommended Coupling for Incoming Video Signals and Input Circuit Configuration**

| VIDEO ORIGIN | FORMAT | VOLTAGE RANGE (V) | COUPLING | INPUT CIRCUIT CONFIGURATION |
|--------------|-----------|-------------------|----------|-----------------------------|
| External | CVBS | Unknown | AC | Transparent sync-tip clamp |
| External | RGB | Unknown | AC | Transparent sync-tip clamp |
| External | Y | Unknown | AC | Transparent sync-tip clamp |
| External | C | Unknown | AC | Bias circuit |
| Internal | CVBS | 0 to 1 | DC | Transparent sync-tip clamp |
| Internal | R, G, B | 0 to 1 | DC | Transparent sync-tip clamp |
| Internal | Y, C | 0 to 1 | DC | Transparent sync-tip clamp |
| Internal | Y, Pb, Pr | 0 to 1 | DC | Transparent sync-tip clamp |
| Internal | CVBS | 2.3 to 3.3 | AC | Transparent sync-tip clamp |
| Internal | R, G, B | 2.3 to 3.3 | AC | Transparent sync-tip clamp |
| Internal | Y | 2.3 to 3.3 | AC | Transparent sync-tip clamp |
| Internal | C | 2.3 to 3.3 | AC | Bias circuit |

**Use a 0.1 μ F capacitor to AC-couple a video signal into the MAX9597.

Video Reconstruction Filter

The video DAC outputs of the set-top box decoder chip need to be lowpass-filtered to reject the out-of-band noise. The MAX9597 integrates sixth-order, Butterworth filters. The filter passband (± 1 dB) is typically 10MHz, and the attenuation at 27MHz is 43dB. The filters are suited for standard-definition video.

Video Outputs

The video output amplifiers can both source and sink load current, allowing output loads to be DC- or AC-coupled. The amplifier output stage needs approximately 300mV of headroom from either supply rail.

If the supply voltage is greater than 3.135V (5% below a 3.3V supply), each amplifier can drive two DC-coupled video loads to ground. If the supply is less than 3.135V, each amplifier can drive only one DC-coupled or AC-coupled video load.

The SCART standard allows for video signals to have a superimposed DC component within 0V and 2V. Therefore, most video signals are DC-coupled at the output. In the unlikely event that the video signal needs to be AC-coupled, the coupling capacitors should be 220 μ F or greater to keep the highpass filter formed by the 37.5 Ω equivalent resistance of the video transmission line to a corner frequency of 4.8Hz or below to keep it well below the 25Hz frame rate of the PAL standard.

The video outputs can be enabled or disabled by bits 1 to 5 of register 0Dh. See Table 11.

Slow Switching

The MAX9597 supports the IEC 933-1, Amendment 1, trilevel slow-switching standard that selects the aspect ratio for the display (TV). Under I²C control, the MAX9597 sets the slow-switching output voltage level. Table 2 shows the valid input levels of the slow-switching signal and the corresponding operating modes of the display device.

One port is available for slow-switching signals for the TV. The slow-switching outputs can be set to a logic level or high impedance by writing to bit 0 and 1 of register 07h. See Table 9.

Table 2. Slow-Switching Modes

| SLOW-SWITCHING SIGNAL VOLTAGE (V) | MODE |
|-----------------------------------|--|
| 0 to 2 | Display device uses an internal source such as a built-in tuner to provide a video signal. |
| 4.5 to 7.0 | Display device uses a video signal from the SCART connector and sets the display to a 16:9 aspect ratio. |
| 9.5 to 12.6 | Display device uses a signal from the SCART connector and sets the display to a 4:3 aspect ratio. |

Low-Power Audio/Video Interface for Single SCART Connectors

Table 3. Slave Address

| DEV_ADDR | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | WRITE ADDRESS (HEX) | READ ADDRESS (HEX) |
|------------------|----|----|----|----|----|----|----|-----|---------------------|--------------------|
| GND | 1 | 0 | 0 | 1 | 0 | 1 | 0 | R/W | 94h | 95h |
| V _{VID} | 1 | 0 | 0 | 1 | 0 | 1 | 1 | R/W | 96h | 97h |
| SCL | 1 | 0 | 0 | 1 | 1 | 0 | 0 | R/W | 98h | 99h |
| SDA | 1 | 0 | 0 | 1 | 1 | 0 | 1 | R/W | 9Ah | 9Bh |

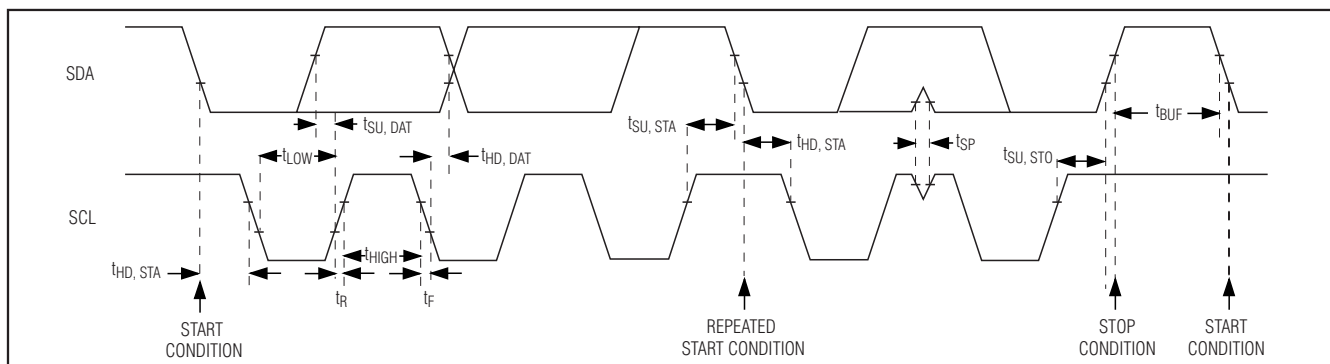


Figure 4. I²C Serial-Interface Timing Diagram

Fast Switching

The fast-switching signal was originally used to switch between CVBS and RGB signals on a pixel-by-pixel basis so that on-screen display (OSD) information could be inserted. Since modern set-top box decoder chips have integrated OSD circuitry, there is no need to create OSD information using the older technique. Now, the fast-switching signal is just used to switch between CVBS and RGB signal sources.

Set the source of the fast-switching signal by writing to bits 4 and 3 of register 07h. The fast-switching signal to the TV SCART connector can be enabled or disabled by bit 1 of register 0Dh. See Tables 9 and 11.

I²C Serial Interface

The MAX9597 features an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX9597 and the master at clock rates up to 400kHz. Figure 4 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. A master device writes data to the MAX9597 by transmitting a START (S) condition, the proper slave address with the R/W bit set to 0, followed by the register address and then the data word. Each transmit sequence is framed by a START and a STOP (P) condition. Each word transmitted to the MAX9597 is 8 bits long and is followed by

an acknowledge clock pulse. A master reads from the MAX9597 by transmitting the slave address with the R/W bit set to 1, followed by a series of SCL pulses. The MAX9597 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, an acknowledge or a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on the SDA bus. SCL operates as only an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9597 from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP*

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Conditions section). SDA and SCL idle high when the I²C bus is not busy.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 5). A START condition from the master signals the beginning of a transmission to the MAX9597. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early STOP Conditions

The MAX9597 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the 7 most significant bits (MSBs) followed by the read/write (R/W) bit. Set the R/W bit to 1 to configure the MAX9597 to read mode. Set the R/W bit to 0 to configure the MAX9597 to write mode. The slave address is always the first byte of information sent to the MAX9597 after a START or a REPEATED START condition. The MAX9597 slave address is configurable with DEV_ADDR. Table 3 shows the possible slave addresses for the MAX9597.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9597 uses to handshake receipt of each byte of data when in write mode (see Figure 6). The MAX9597 pulls down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may retry communication. The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the MAX9597 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the MAX9597, followed by a STOP condition.

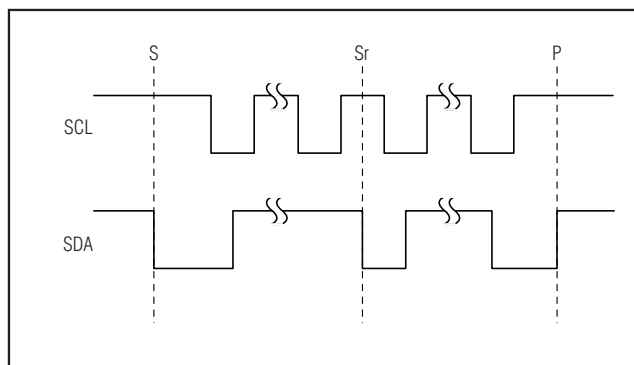


Figure 5. START, STOP, and REPEATED START Conditions

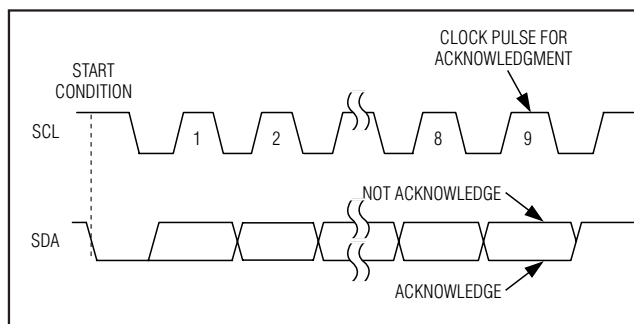


Figure 6. Acknowledge

Write Data Format

A write to the MAX9597 consists of transmitting a START condition, the slave address with the R/W bit set to 0, one data byte to configure the internal register address pointer, one or more data bytes, and a STOP condition. Figure 7 illustrates the proper frame format for writing one byte of data to the MAX9597. Figure 8 illustrates the frame format for writing n-bytes of data to the MAX9597.

The slave address with the R/W bit set to 0 indicates that the master intends to write data to the MAX9597. The MAX9597 acknowledges receipt of the address byte during the master-generated ninth SCL pulse.

The second byte transmitted from the master configures the MAX9597's internal register address pointer. The pointer tells the MAX9597 where to write the next byte of data. An acknowledge pulse is sent by the MAX9597 upon receipt of the address pointer data.

The third byte sent to the MAX9597 contains the data that is written to the chosen register. An acknowledge pulse from the MAX9597 signals receipt of the data byte. The address pointer autoincrements to the next

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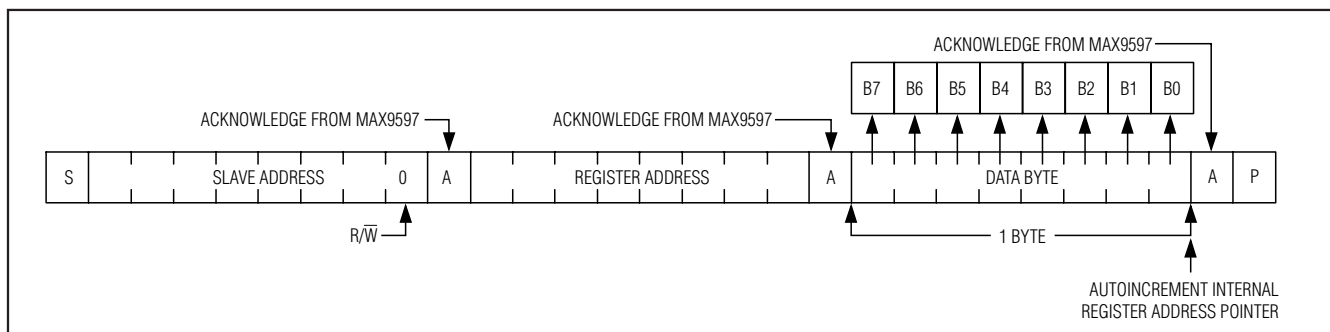


Figure 7. Writing a Byte of Data to the MAX9597

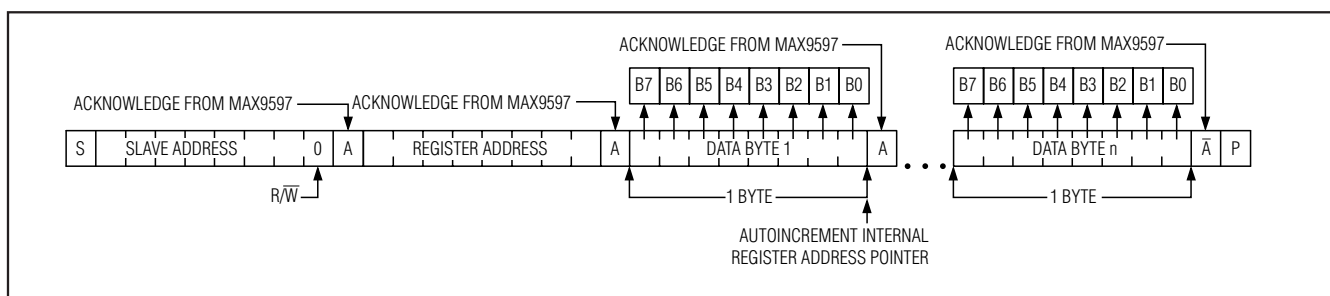


Figure 8. Writing n-Bytes of Data to the MAX9597

register address after each received data byte. This autoincrement feature allows a master to write to sequential register address locations within one continuous frame. The master signals the end of transmission by issuing a STOP condition.

Read Data Format

The master presets the address pointer by first sending the MAX9597's slave address with the R/W bit set to 0 followed by the register address after a START condition. The MAX9597 acknowledges receipt of its slave address and the register address by pulling SDA low during the ninth SCL clock pulse. A REPEATED START condition is then sent followed by the slave address with the R/W bit set to 1. The MAX9597 transmits the contents of the specified register. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from the register address location set by the previous transaction and not 00h and subsequent reads autoincrement the address pointer

until the next STOP condition. Attempting to read from register addresses higher than 01h results in repeated reads from a dummy register containing FFh data. The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figures 9 and 10 illustrate the frame format for reading data from the MAX9597.

Applications Information

Operating Modes

The MAX9597 has two operating modes: full power and shutdown. The operations can be set by writing to bit 7 of register 10h. See Table 12.

In shutdown mode, all circuitry is shut down except for the I²C interface, which is designed with static CMOS logic. If the I²C bus is quiet, the I²C interface draws only leakage current.

Power Consumption

With a low 3.3V supply, the quiescent power consumption and average power consumption of the MAX9597 is very low. Quiescent power consumption is defined

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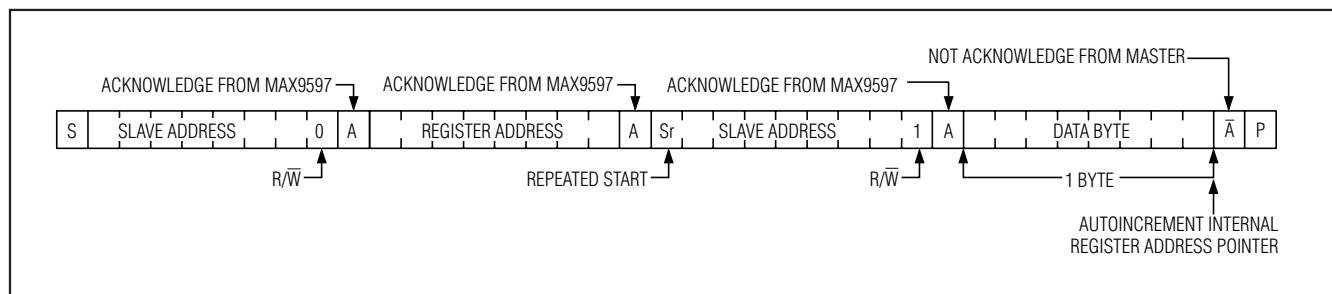


Figure 9. Reading One Indexed Byte of Data from the MAX9597

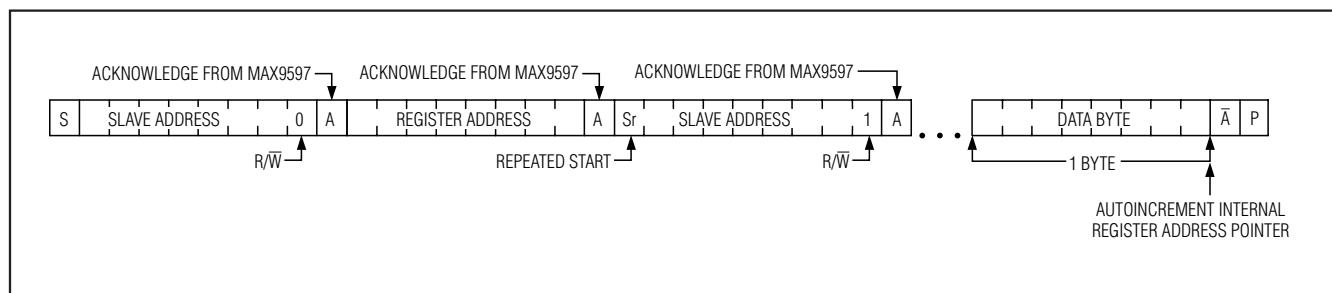


Figure 10. Reading n-Bytes of Indexed Data from the MAX9597

when the MAX9597 is operating without loads and without any audio or video signals. Table 4 shows the quiescent power consumption in both operating modes.

Average power consumption is defined when the MAX9597 drives typical signals into typical loads. Table 5 shows the average power consumption in full-power mode, and Table 6 shows the input and output conditions.

Interfacing to an RF Modulator

If the set-top box modulates CVBS and mono audio onto an RF carrier (for example, channel 3), a simple application circuit can provide the needed signals (see Figure 11). A 10k Ω resistor summer circuit between TV_OUTR and TV_OUTL creates the mono audio signal. The resistor-divider to ground on TV_CVBS_OUT creates a video signal with normal amplitude. The unique feature of the MAX9597 that facilitates this application circuit is that the audio and video output amplifiers of the MAX9597 can drive multiple loads if V_{AUD} and V_{VID} are both greater than 3.135V.

Table 4. Quiescent Power Consumption

| OPERATING MODE | POWER CONSUMPTION (mW) |
|----------------|------------------------|
| Shutdown | 0.005 |
| Full power | 53 |

Table 5. Average Power Consumption

| OPERATING MODE | POWER CONSUMPTION (mW) |
|----------------|------------------------|
| Full power | 254 |

Floating-Chassis Discharge Protection and ESD

Some set-top boxes have a floating chassis problem in which the chassis is not connected to earth ground. As a result, the chassis can charge up to 500V. When a SCART cable is connected to the SCART connector, the charged chassis can discharge through a signal pin. The equivalent circuit is a 2200pF capacitor charged to 311V connected through less than 0.1 Ω to a signal pin. The MAX9597 is soldered on the PCB when it experiences such a discharge. Therefore, the current spike flows through both external and internal ESD protection devices and is absorbed by the supply bypass capacitors, which have high capacitance and low ESR.

Low-Power Audio/Video Interface for Single SCART Connectors

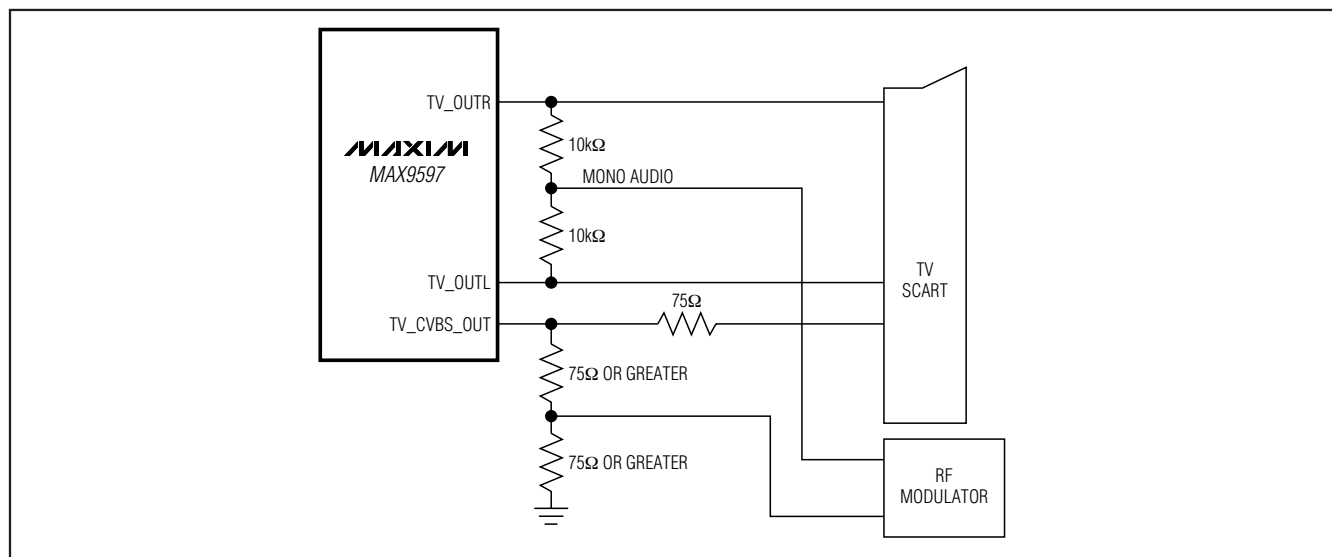


Figure 11. Application Circuit to Connect CVBS and Mono Audio from TV SCART to RF Modulator

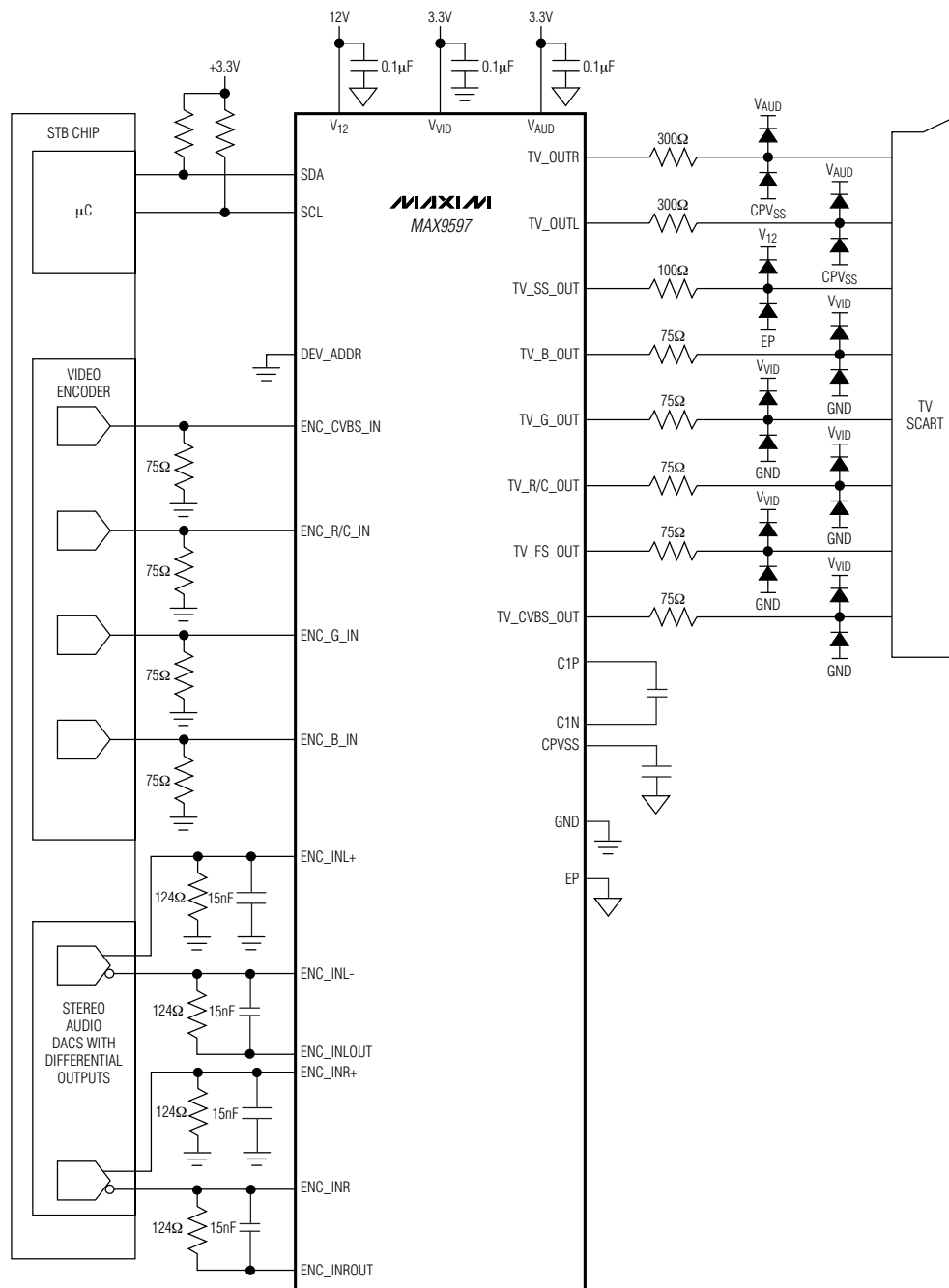
Table 6. Conditions for Average Power Consumption Measurement

| PIN | NAME | TYPE | SIGNAL | LOAD |
|-----|------------------|--------|-----------------------------|----------------|
| 1 | V _{AUD} | Supply | 3.3V | N/A |
| 8 | ENC_B_IN | Input | 50% flat field | N/A |
| 9 | ENC_G_IN | Input | 50% flat field | N/A |
| 10 | ENC_R/C_IN | Input | 50% flat field | N/A |
| 11 | ENC_CVBS_IN | Input | 50% flat field | N/A |
| 12 | TV_CVBS_OUT | Output | 50% flat field | 150Ω to ground |
| 13 | V _{VID} | Supply | 3.3V | N/A |
| 14 | TV_FS_OUT | Output | 3.3V | 150Ω to ground |
| 15 | GND | Supply | 0 | N/A |
| 16 | TV_R/C_OUT | Output | 50% flat field | 150Ω to ground |
| 17 | TV_G_OUT | Output | 50% flat field | 150Ω to ground |
| 18 | TV_B_OUT | Output | 50% flat field | 150Ω to ground |
| 19 | V ₁₂ | Supply | 12V | N/A |
| 20 | TV_SS_OUT | Output | 12V | 10kΩ to ground |
| 21 | TV_OUTL | Output | 1V _{RMS} , 1kHz | 10kΩ to ground |
| 22 | ENC_INL+ | Input | 0.25V _{RMS} , 1kHz | N/A |
| 23 | ENC_INL- | Input | N/A | N/A |
| 24 | ENC_INLOUT | Output | N/A | 1kΩ to ground |
| 25 | ENC_INROUT | Output | N/A | 1kΩ to ground |
| 26 | ENC_INR- | Input | N/A | N/A |
| 27 | ENC_INR+ | Input | 0.25V _{RMS} , 1kHz | N/A |
| 28 | TV_OUTR | Output | 1V _{RMS} , 1kHz | 10kΩ to ground |

Note: Input operational amplifiers set to unity-gain configuration.

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NOTE: OPTIONAL RESISTOR CAN BE PLACED FROM AUDIO DAC OUTPUTS TO GROUND TO DECREASE SWING AT AUDIO DAC OUTPUTS.

⬆ BAV99, SMALL-SIGNAL DIODE

Figure 12. Application Circuit to Connect Series Resistors and External ESD Protection Diodes at MAX9597 Outputs

Low-Power Audio/Video Interface for Single SCART Connectors

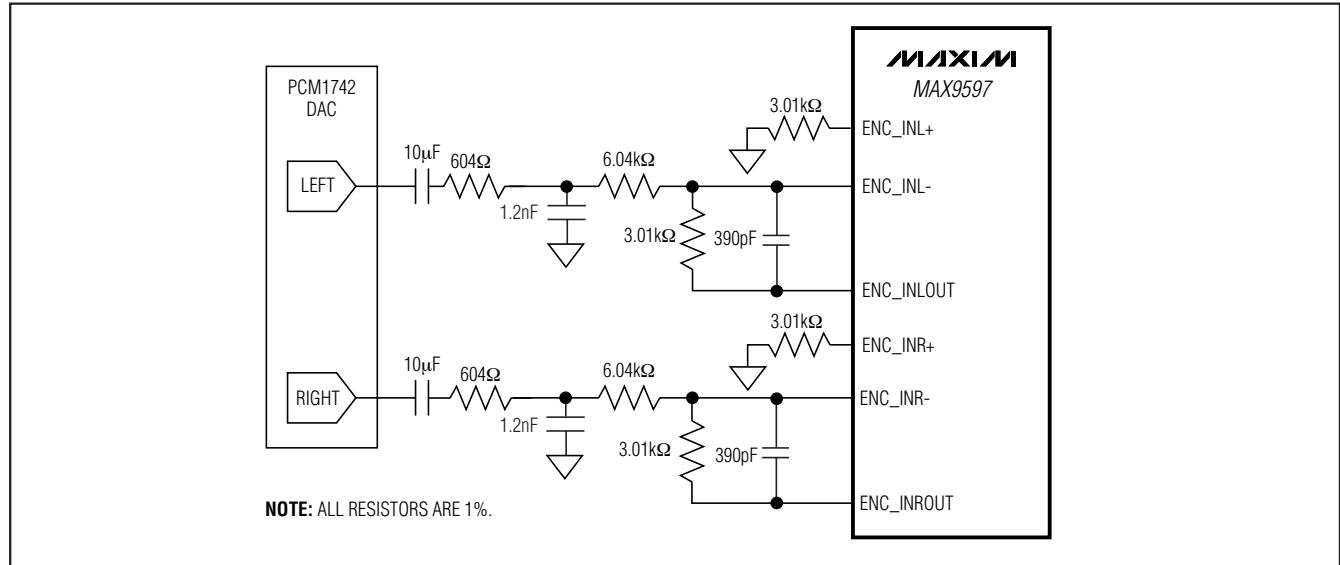


Figure 13. Lowpass Filter Configuration for the Burr-Brown PCM1742

To better protect the MAX9597 against excess voltages during the cable discharge condition or ESD events, add series resistors to all inputs and outputs to the SCART connector if series resistors are not already present in the application circuit. Also add external ESD protection diodes (for example, BAV99) on all inputs and output to the SCART connector.

Lowpass Filter Configuration for PCM1742 and CS4334

The lowpass filter configurations shown in Figures 13 and 15 are recommended when connecting a stereo audio DAC to the audio preamplifier (input amplifier) of the MAX9597. The filter configuration helps eliminate the switching noise caused by the audio DAC. The corner frequency of the filter configuration should be set above the maximum audio frequency (20kHz) and below the sampling frequency of the DAC. The frequency response of the filter configurations is shown in Figures 14 and 16.

Differential to Single-Ended Conversion of Audio Signals

If the stereo audio DAC generates an analog, voltage mode, differential audio signal, the circuit shown in Figure 17 can be used to convert the signal to single ended.

The gain of the circuit is represented by this equation:

$$\text{GAIN} = \left(\frac{R2}{R1} \right) \times 4$$

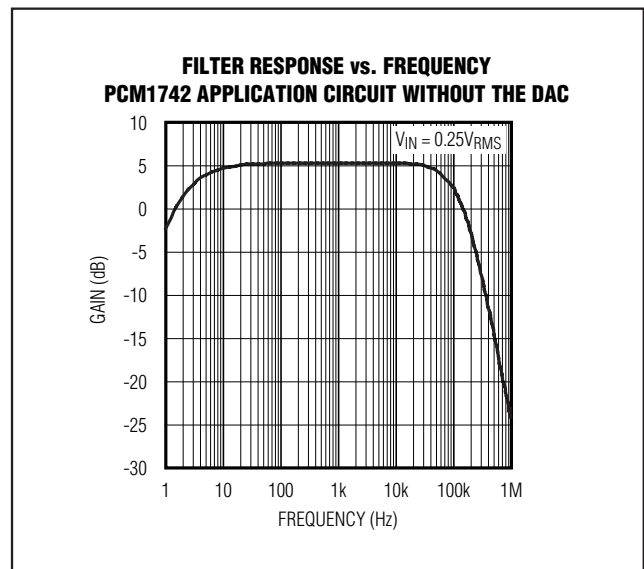


Figure 14. Filter Response of PCM1742 Filter Configuration

Low-Power Audio/Video Interface for Single SCART Connectors

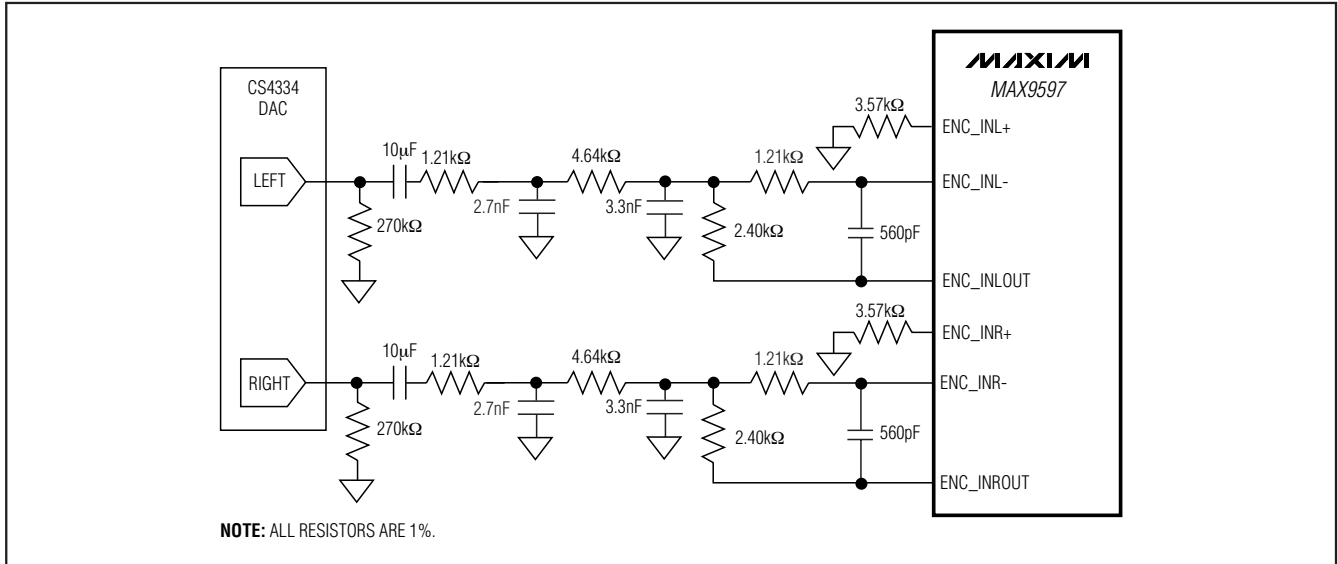


Figure 15. Lowpass Filter Configuration for the Cirrus CS4334

Keep the full-scale audio output of the preamplifiers to 0.5V_{RMS}. Capacitors C1 and C2 create a one-pole, lowpass filter to attenuate any high-frequency noise coming from the stereo audio DAC. The frequency of the lowpass pole is represented by this equation:

$$f_{-3dB} = \frac{1}{2\pi \left(\frac{R1 \times R2}{R1 + R2} \right) C1} \text{ or } f_{-3dB} = \frac{1}{2\pi \left(\frac{R1 \times R2}{R1 + R2} \right) C2}$$

If the stereo audio DAC generates an analog, current mode, and differential audio signal, the *Typical Application Circuit* can be used to convert the signal to single ended. The transresistance of the circuit is represented by this equation:

$$V_{OUT} = I_{DIFF} \times R_F$$

Keep the full-scale audio output of the preamplifiers to 0.5V_{RMS}. Capacitors C1 and C2 create a one-pole, lowpass filter to attenuate any high-frequency noise coming from the stereo audio DAC. The frequency of the lowpass pole is represented by this equation:

$$f_{-3dB} = \frac{1}{2\pi(R_F)C1} \text{ or } f_{-3dB} = \frac{1}{2\pi(R_F)C2}$$

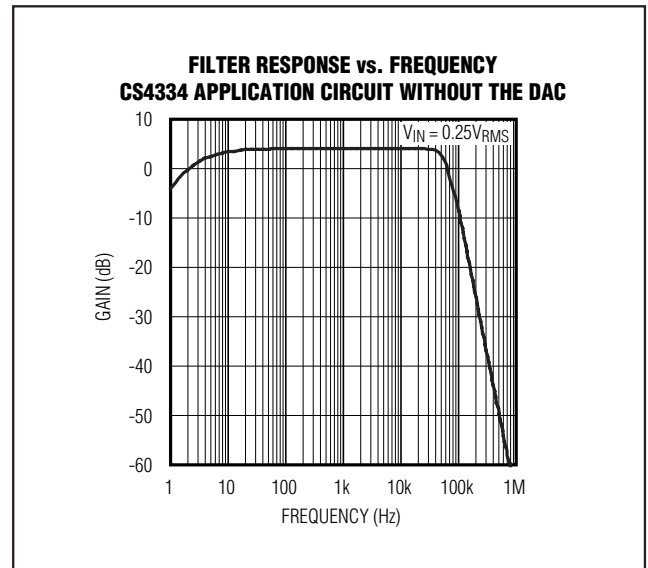


Figure 16. Filter Response of CS4334 Filter Configuration

Low-Power Audio/Video Interface for Single SCART Connectors

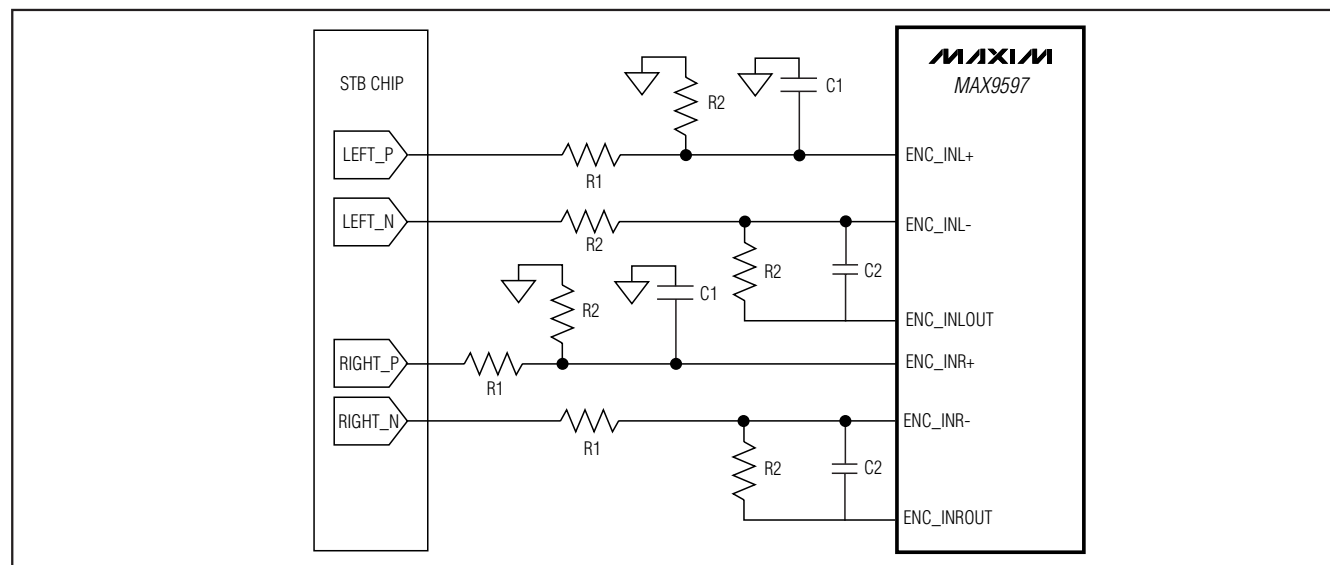


Figure 17. Differential to Single-Ended Conversion Circuit for Voltage Mode, Differential Audio Signals

Stand-Alone Operational Amplifier Applications

The input amplifier of the audio section can be utilized for stand-alone operational amplifier applications by configuring ENC_INR+ and ENC_INL+ input as the noninverting input, ENC_INR- and ENC_INL- input as the inverting input and ENC_INROUT and ENC_INLOUT output as the output of the stand-alone operational amplifier. The gain-bandwidth product of the amplifier is 7MHz (typ).

Applications That Do Not Need the Slow-Switch Signal

V₁₂ should be left unconnected if the MAX9597 is used in an application that does not require the slow-switch output signal. See Figure 18.

Power-Supply Bypassing

The MAX9597 features single 3.3V and 12V supply operation and requires no negative supply. The 12V supply V₁₂ is for the SCART slow-switching function. For pin V₁₂, place a 0.1μF bypass capacitor as close to it as possible. Connect V_{AUD} to 3.3V and bypass with a

10μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor to audio ground. Bypass V_{VID} to GND with a 0.1μF ceramic capacitor.

Using a Digital Supply

The MAX9597 was designed to operate from noisy digital supplies. The high video PSRR (47dB at 100kHz) allows the MAX9597 to reject the noise from the digital power supplies (see the *Typical Operating Characteristics*). If the digital power supply is very noisy and stripes appear on the television screen, increase the supply bypass capacitance. An additional, smaller capacitor in parallel with the main bypass capacitor can reduce digital supply noise because the smaller capacitor has lower equivalent series resistance (ESR) and equivalent series inductance (ESL).

Layout and Grounding

For optimal performance, use controlled-impedance traces for video signal paths and place input termination resistors and output back-termination resistors close to the MAX9597. Avoid routing video traces parallel to high-speed data lines.

Low-Power Audio/Video Interface for Single SCART Connectors

MAX9597

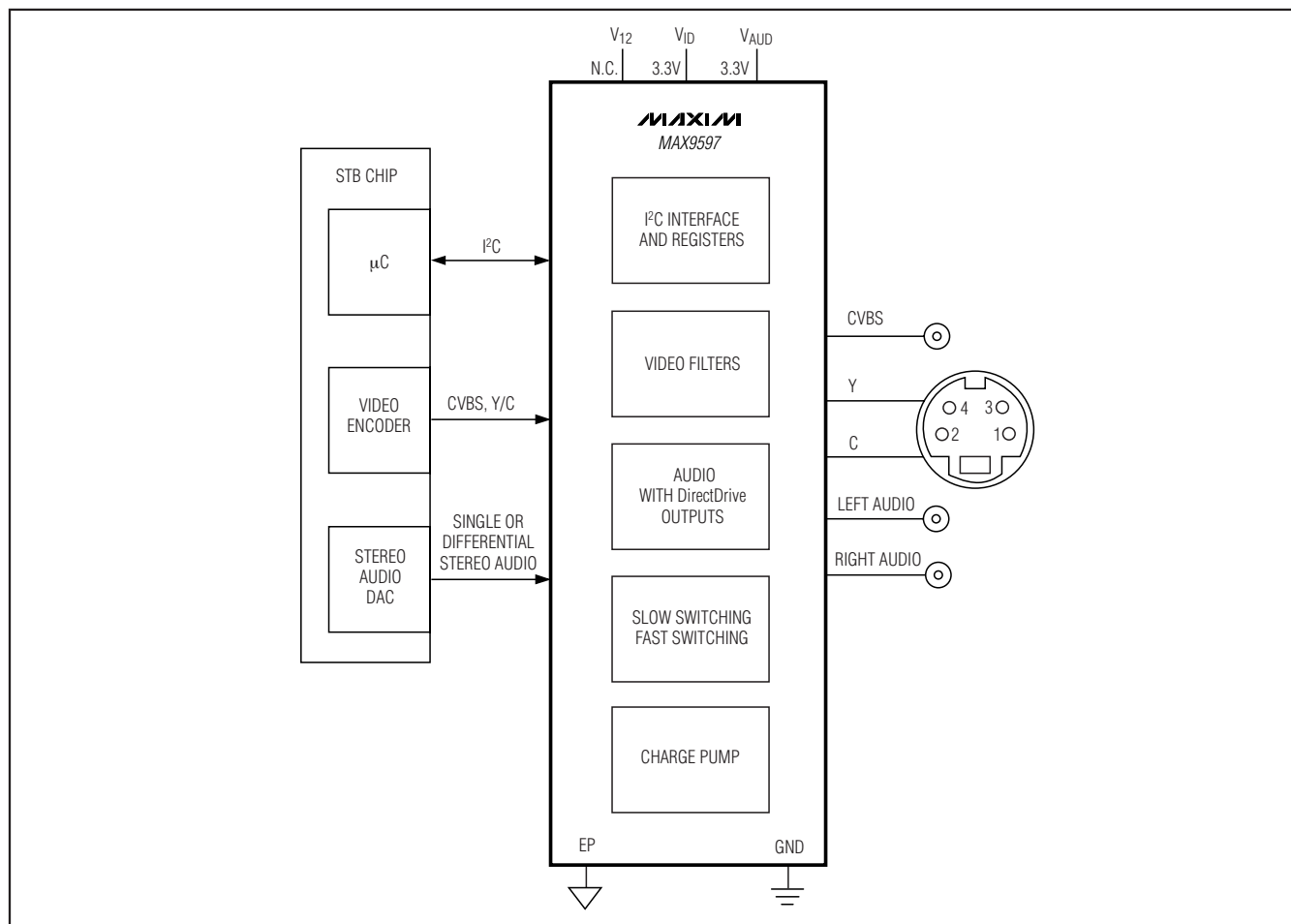


Figure 18. Set-Top Box with CVBS Output, S-Video Output, and Stereo Audio Outputs

The MAX9597 provides separate ground connections for video and audio supplies. For best performance, use separate ground planes for each of the ground returns and connect all ground planes together at a single point. Refer to the MAX9597 Evaluation Kit for a proven circuit board layout example.

If the MAX9597 is mounted using flow soldering or wave soldering, the ground via(s) for the exposed pad should have a finished hole size of at least 14mil to ensure adequate wicking of soldering onto the exposed pad. If the MAX9597 is mounted using the solder mask technique, the via requirement does not apply. In either case, a good connection between the exposed pad and ground is required to minimize noise from coupling onto the outputs.

Low-Power Audio/Video Interface for Single SCART Connectors

Register Tables

Table 7. Data Format for Write Mode

| REGISTER ADDRESS (HEXADECIMAL) | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|--------------------------------|----------------|----------|------------|-----------------------|------------------|-------------|-----------------------|---------------|
| 0x00 | Not used | ZCD | Not used | | | | | TV audio mute |
| 0x01 | Not used | | | | | | | |
| 0x02 | Not used | | | | | | | |
| 0x03 | Not used | | | | | | | |
| 0x04 | Not used | | | | | | | |
| 0x05 | Not used | | | | | | | |
| 0x06 | Not used | | | | | | | |
| 0x07 | Not used | Not used | Not used | Set TV fast switching | | Not used | Set TV slow switching | |
| 0x08 | Not used | Not used | Not used | Not used | ENC_R/C_IN clamp | Not used | Not used | Not used |
| 0x09 | Not used | | | | | | | |
| 0x0A | Not used | | | | | | | |
| 0x0B | Not used | | | | | | | |
| 0x0C | Not used | | | | | | | |
| 0x0D | Not used | Not used | TV_R/C_OUT | TV_G_OUT | TV_B_OUT | TV_CVBS_OUT | TV_FS_OUT | Not used |
| 0x10 | Operating mode | Not used | Not used | Not used | Not used | Not used | Not used | Not used |

Low-Power Audio/Video Interface for Single SCART Connectors

Table 8. Register 00h: Audio Control

| DESCRIPTION | BIT | | | | | | | | COMMENTS |
|------------------------|-----|---|---|---|---|---|---|---|-----------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| TV audio mute | — | — | — | — | — | — | — | 0 | Off |
| | — | — | — | — | — | — | — | 1 | On (power-on default) |
| Zero-crossing detector | — | 0 | — | — | — | — | — | — | Off |
| | — | 1 | — | — | — | — | — | — | On (power-on default) |

Table 9. Register 07h: TV Video Output Control

| DESCRIPTION | BIT | | | | | | | | COMMENTS |
|-----------------------|-----|---|---|---|---|---|---|---|--|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Set TV slow switching | — | — | — | — | — | — | 0 | 0 | Low (< 2V) internal source (power-on default) |
| | — | — | — | — | — | — | 0 | 1 | Medium (4.5V to 7V) external SCART source with 16:9 aspect ratio |
| | — | — | — | — | — | — | 1 | 0 | High impedance |
| | — | — | — | — | — | — | 1 | 1 | High (> 9.5V) external SCART source with 4:3 aspect ratio |
| Set TV fast switching | — | — | — | 0 | 0 | — | — | — | GND (power-on default) |
| | — | — | — | 0 | 1 | — | — | — | Not used |
| | — | — | — | 1 | 0 | — | — | — | Same level as VCR_FB_IN |
| | — | — | — | 1 | 1 | — | — | — | V _{VID} |

Table 10. Register 08h: VCR Video Input Control

| DESCRIPTION | BIT | | | | | | | | COMMENTS |
|-----------------------|-----|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| ENC_R/C_IN clamp/bias | — | — | — | — | 0 | — | — | — | DC restore clamp active at input (power-on default) |
| | — | — | — | — | 1 | — | — | — | Chrominance bias applied at input |

Low-Power Audio/Video Interface for Single SCART Connectors

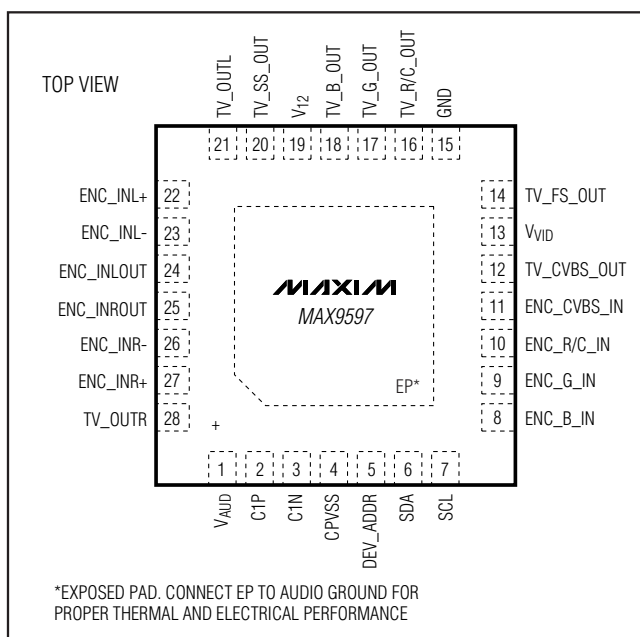
Table 11. Register 0Dh: Output Enable

| DESCRIPTION | BIT | | | | | | | | COMMENTS |
|--------------------|-----|---|---|---|---|---|---|---|------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| TV_FS_OUT enable | — | — | — | — | — | — | 0 | — | Off (power-on default) |
| | — | — | — | — | — | — | 1 | — | On |
| TV_CVBS_OUT enable | — | — | — | — | — | 0 | — | — | Off (power-on default) |
| | — | — | — | — | — | 1 | — | — | On |
| TV_B_OUT enable | — | — | — | — | 0 | — | — | — | Off (power-on default) |
| | — | — | — | — | 1 | — | — | — | On |
| TV_G_OUT enable | — | — | — | 0 | — | — | — | — | Off (power-on default) |
| | — | — | — | 1 | — | — | — | — | On |
| TV_R/C_OUT enable | — | — | 0 | — | — | — | — | — | Off (power-on default) |
| | — | — | 1 | — | — | — | — | — | On |

Table 12. Register 10h: Operating Modes

| DESCRIPTION | BIT | | | | | | | | COMMENTS |
|----------------|-----|---|---|---|---|---|---|---|------------------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Operating mode | 0 | — | — | — | — | — | — | — | Shutdown |
| | 1 | — | — | — | — | — | — | — | Full-power mode (power-on default) |

Pin Configuration



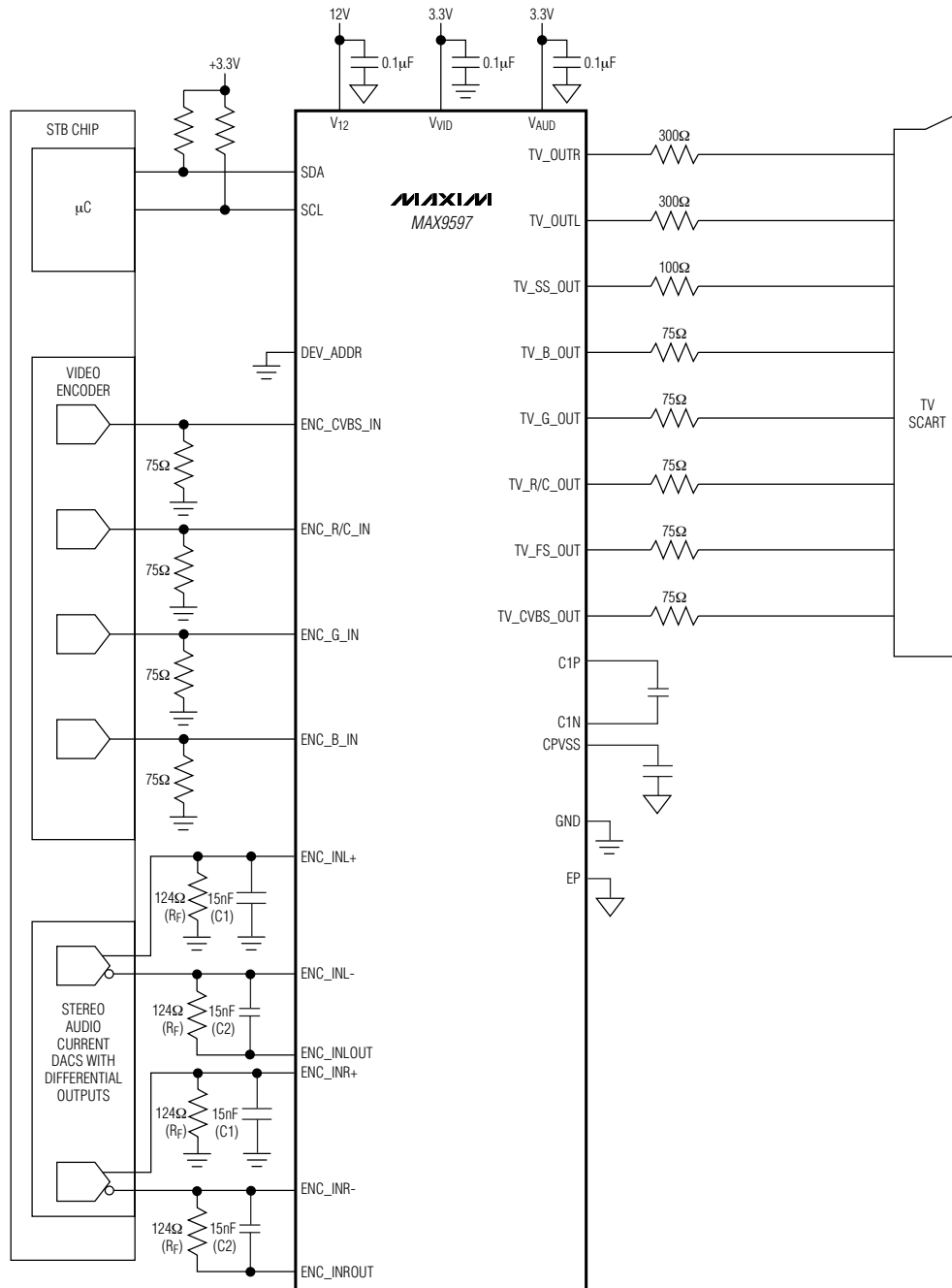
Chip Information

PROCESS: BiCMOS

Low-Power Audio/Video Interface for Single SCART Connectors

Typical Application Circuit

MAX9597



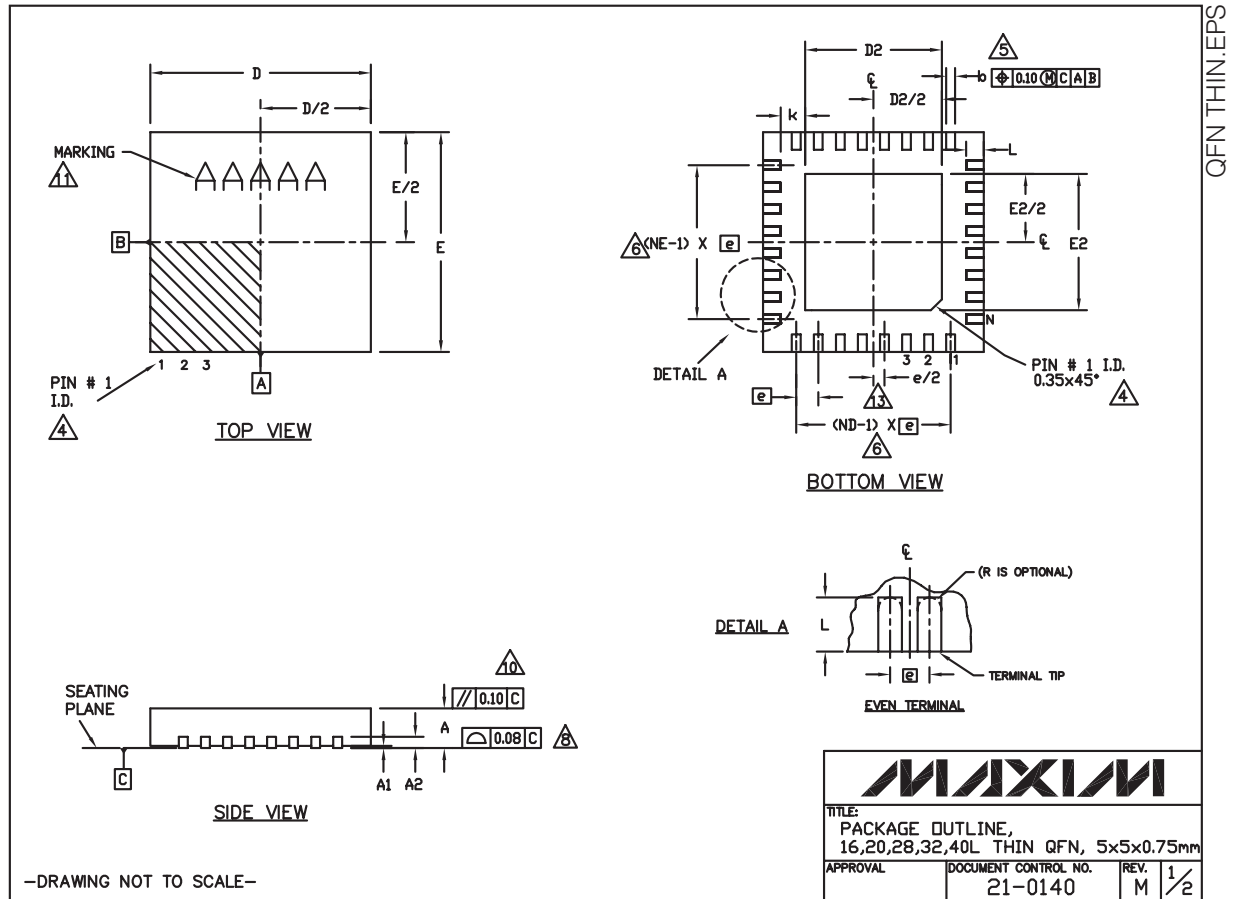
NOTE: OPTIONAL RESISTOR CAN BE PLACED FROM AUDIO DAC OUTPUTS TO GROUND TO DECREASE SWING AT AUDIO DAC OUTPUTS.

Low-Power Audio/Video Interface for Single SCART Connectors

_Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|--------------|--------------|-------------------------|
| 28 TQFN-EP | T2855-8 | 21-0140 |



Low-Power Audio/Video Interface for Single SCART Connectors

Package Information (continued)

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

MAX9597

| COMMON DIMENSIONS | | | | | | | | | | | | | | | |
|-------------------|-----------|------|------|-----------|------|------|-----------|------|------|-----------|------|------|-----------|------|------|
| PKG. | 16L 5x5 | | | 20L 5x5 | | | 28L 5x5 | | | 32L 5x5 | | | 40L 5x5 | | |
| SYMBOL | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 |
| A2 | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | |
| b | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 | 0.15 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 |
| E | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 |
| e | 0.80 BSC. | | | 0.65 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | | 0.40 BSC. | | |
| k | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - |
| L | 0.30 | 0.40 | 0.50 | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 | 0.30 | 0.40 | 0.50 |
| N | 16 | | | 20 | | | 28 | | | 32 | | | 40 | | |
| ND | 4 | | | 5 | | | 7 | | | 8 | | | 10 | | |
| NE | 4 | | | 5 | | | 7 | | | 8 | | | 10 | | |
| JEDEC | WHHB | | | WHHC | | | WHHD-1 | | | WHHD-2 | | | ----- | | |

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

| EXPOSED PAD VARIATIONS | | | | | | |
|------------------------|------|------|------|------|------|------|
| PKG. CODES | D2 | | | E2 | | |
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T1655-2 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T1655-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T1655-4 | 2.19 | 2.29 | 2.39 | 2.19 | 2.29 | 2.39 |
| T165N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-5 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2055MN-5 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-3 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-4 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-5 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-6 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-7 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-8 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855N-1 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T3255-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255N-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255-5 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T4055-1 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |
| T4055-2 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |
| T4055N-1 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |
| T4055MN-1 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |

MAXIM

| | | |
|--|---------------------------------|------------|
| TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.75mm | | |
| APPROVAL | DOCUMENT CONTROL NO. 21-0140 | REV. M 2/2 |

Low-Power Audio/Video Interface for Single SCART Connectors

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|--------------------|---------------|---------------------------------------|---------------|
| 0 | 6/08 | Initial release | — |
| 1 | 10/08 | Corrected resistor value in Figure 13 | 22 |

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помещение 100-Н Офис 331