19-2851; Rev 7; 4/12

EVALUATION KIT AVAILABLE

12-Bit 300ksps ADCs with FIFO, Temp Sensor, Internal Reference

General Description

The MAX1227/MAX1229/MAX1231 are serial 12-bit analog-to-digital converters (ADCs) with an internal reference and an internal temperature sensor. These devices feature an on-chip FIFO, scan mode, internal clock mode, internal averaging, and AutoShutdown™. The maximum sampling rate is 300ksps using an external clock. The MAX1231 has 16 input channels, the MAX1229 has 12 input channels, and the MAX1227 has 8 input channels. All input channels are configurable for single-ended or differential inputs in unipolar or bipolar mode. All three devices operate from a +3V supply and contain a 10MHz SPI™-/QSPI™-/MICROWIRE™-compatible serial port.

The MAX1231 is available in 28-pin 5mm x 5mm TQFN with exposed pad and 24-pin QSOP packages. The MAX1227/MAX1229 are only available in QSOP packages. All three devices are specified over the extended -40°C to +85°C temperature range.

Applications

System Supervision

Data-Acquisition Systems

Industrial Control Systems

Patient Monitoring

Data Logging

Instrumentation

AutoShutdown is a trademark of Maxim Integrated Products, Inc.
SPI/QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

Features

- **Internal Temperature Sensor (±0.7°C Accuracy)**
- **16-Entry First-In/First-Out (FIFO)**
- **Analog Multiplexer with True Differential Track/Hold**
  - **16-, 12-, 8-Channel Single Ended**
  - **8-, 6-, 4-Channel True Differential (Unipolar or Bipolar)**
- **Accuracy: ±1 LSB INL, ±1 LSB DNL, No Missing Codes Overtemperature**
- **Scan Mode, Internal Averaging, and Internal Clock**
- **Low-Power Single +3V Operation**
  - **1mA at 300ksps**
- **Internal 2.5V Reference or External Differential Reference**
- **10MHz 3-Wire SPI-/QSPI-/MICROWIRE-Compatible Interface**
- **Space-Saving 28-Pin 5mm x 5mm TQFN Package**

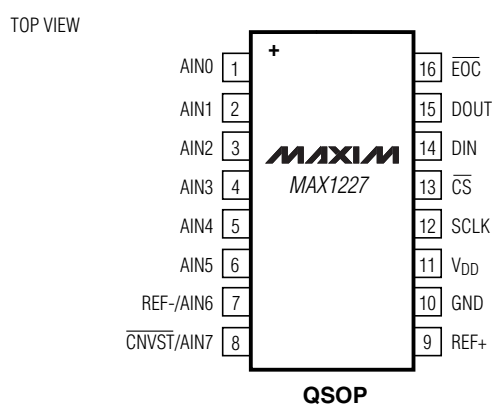
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1227BCEE+	0°C to +70°C	16 QSOP
MAX1227BEEE+	-40°C to +85°C	16 QSOP
MAX1229BCEP+	0°C to +70°C	20 QSOP
MAX1229BEEP+	-40°C to +85°C	20 QSOP

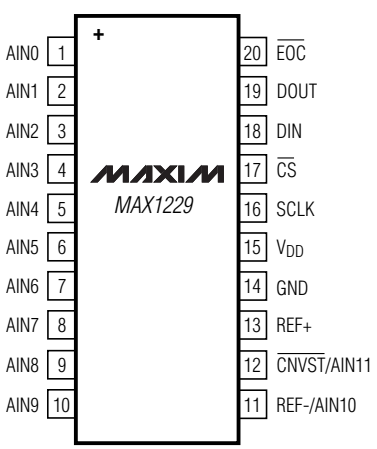
Ordering Information continued at end of data sheet.

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad (TQFN only). Connect to GND.*

Pin Configurations



QSOP



QSOP

Pin Configurations continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

12-Bit 300ksps ADCs with FIFO, Temp Sensor, Internal Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
$\overline{CS}$, SCLK, DIN, $\overline{EOC}$, DOUT to GND .....-0.3V to (V_{DD} + 0.3V)
AIN0–AIN13, REF-/AIN_, $\overline{CNVST}$/AIN_,
REF+ to GND .....-0.3V to (V_{DD} + 0.3V)
Maximum Current into Any Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C) 667mW
20-Pin QSOP (derate 9.1mW/°C above +70°C) 727mW
24-Pin QSOP (derate 9.5mW/°C above +70°C) 762mW
28-Pin TQFN 5mm x 5mm
(derate 20.8mW/°C above +70°C) 1667mW

Operating Temperature Ranges
MAX12__C__ .....0°C to +70°C
MAX12__E__ .....-40°C to +85°C
Storage Temperature Range .....-60°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V, f_{SAMPLE} = 300kHz, f_{SCLK} = 4.8MHz (50% duty cycle), V_{REF} = 2.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (NOTE 1)						
Resolution	RES		12			Bits
Integral Nonlinearity	INL				±1.0	LSB
Differential Nonlinearity	DNL	No missing codes over temperature			±1.0	LSB
Offset Error				±0.5	±4.0	LSB
Gain Error		(Note 2)		±0.5	±4.0	LSB
Offset Error Temperature Coefficient				±2		ppm/°C FSR
Gain Temperature Coefficient				±0.8		ppm/°C
Channel-to-Channel Offset Matching				±0.1		LSB
DYNAMIC SPECIFICATIONS (30kHz sine wave input, 2.5V_{P-P}, 300ksps, f_{SCLK} = 4.8MHz)						
Signal-to-Noise Plus Distortion	SINAD			71		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-80		dBc
Spurious-Free Dynamic Range	SFDR			81		dBc
Intermodulation Distortion	IMD	f_{IN1} = 29.9kHz, f_{IN2} = 30.2kHz		76		dBc
Full-Power Bandwidth		-3dB point		1		MHz
Full-Linear Bandwidth		S/(N + D) > 68dB		100		kHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V, f_{SAMPLE} = 300kHz, f_{SCLK} = 4.8MHz (50% duty cycle), V_{REF} = 2.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONVERSION RATE						
Power-Up Time	t_{PU}	External reference		0.8		µs
		Internal reference (Note 3)		65		
Acquisition Time	t_{ACQ}				0.6	µs
Conversion Time	t_{CONV}	Internally clocked		3.5		µs
		Externally clocked (Note 4)	2.7			
External Clock Frequency	f_{SCLK}	Externally clocked conversion	0.1		4.8	MHz
		Data I/O			10	
SCLK Duty Cycle			40		60	%
Aperture Delay				30		ns
Aperture Jitter				<50		ps
ANALOG INPUT						
Input Voltage Range		Unipolar	0		V_{REF}	V
		Bipolar (Note 5)	$-V_{REF}/2$		$V_{REF}/2$	
Input Leakage Current		V_{IN} = V_{DD}		±0.01	±1	µA
Input Capacitance		During acquisition time (Note 6)		24		pF
INTERNAL TEMPERATURE SENSOR						
Measurement Error (Note 7)		T_A = +25°C		±0.7		°C
		T_A = T_{MIN} to T_{MAX}		±1.2	±2.5	
Temperature Measurement Noise				0.4		$°C_{RMS}$
Temperature Resolution				1/8		°C
Power-Supply Rejection				0.3		°C/V
INTERNAL REFERENCE						
REF Output Voltage			2.48	2.50	2.52	V
REF Temperature Coefficient	TC_{REF}			±30		ppm/°C
Output Resistance				6.5		kΩ
REF Output Noise				200		$µV_{RMS}$
REF Power-Supply Rejection	PSRR			-70		dB
EXTERNAL REFERENCE INPUT						
REF- Input Voltage Range	V_{REF-}		0		500	mV
REF+ Input Voltage Range	V_{REF+}		1.0		V_{DD} + 50mV	V
REF+ Input Current	I_{REF+}	V_{REF+} = 2.5V, f_{SAMPLE} = 300ksps		40	100	µA
		V_{REF+} = 2.5V, f_{SAMPLE} = 0		±0.1	±5	

12-Bit 300ksps ADCs with FIFO, Temp Sensor, Internal Reference

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V, f_{SAMPLE} = 300kHz, f_{SCLK} = 4.8MHz (50% duty cycle), V_{REF} = 2.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{CNVST}$) (Note 8)							
Input Voltage Low	V_{IL}					V_{DD} x 0.3	V
Input Voltage High	V_{IH}			V_{DD} x 0.7			V
Input Hysteresis	V_{HYST}				200		mV
Input Leakage Current	I_{IN}	V_{IN} = 0 or V_{DD}			±0.01	±1.0	µA
Input Capacitance	C_{IN}				15		pF
DIGITAL OUTPUTS (DOUT, $\overline{EOC}$)							
Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
		I_{SINK} = 4mA				0.8	
Output Voltage High	V_{OH}	I_{SOURCE} = 1.5mA		V_{DD} - 0.5			V
Tri-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}			±0.05	±1	µA
Tri-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD}			15		pF
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			2.7		3.6	V
Supply Current (Note 9)	I_{DD}	Internal reference	During temp sense		2400	2700	µA
			f_{SAMPLE} = 300ksps		1750	2000	
			f_{SAMPLE} = 0, REF on		1000	1200	
			Shutdown		0.2	5	
		External reference	During temp sense		1550	2000	
			f_{SAMPLE} = 300ksps		1050	1200	
			Shutdown		0.2	5	
Power-Supply Rejection	PSR	V_{DD} = 2.7V to 3.6V; full-scale input			±0.2	±1	mV

Note 1: Tested at V_{DD} = +2.7V, unipolar input mode.
Note 2: Offset nulled.
Note 3: Time for reference to power up and settle to within 1 LSB.
Note 4: Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 5: The operational input voltage range for each individual input of a differentially configured pair is from GND to V_{DD}. The operational input voltage difference is from -V_{REF}/2 to +V_{REF}/2.
Note 6: See Figure 3 (Input Equivalent Circuit) and the Typical Operating Curve in the *Sampling Error vs. Source Impedance* section.
Note 7: Fast automated test, excludes self-heating effects.
Note 8: When CNVST is configured as a digital input, do not apply a voltage between V_{IL} and V_{IN}.
Note 9: Supply current is specified depending on whether an internal or external reference is used for voltage conversions. Temperature measurements always use the internal reference.

TIMING CHARACTERISTICS (Figure 1)

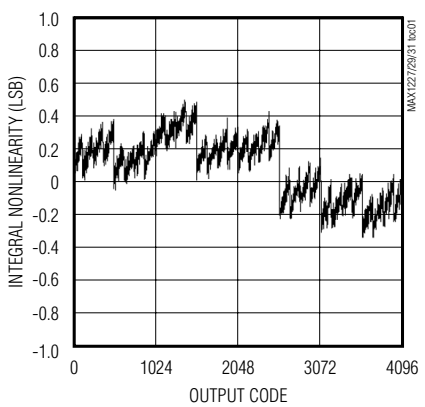
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t_{CP}	Externally clocked conversion	208			ns
		Data I/O	100			
SCLK Duty Cycle	t_{CH}		40		60	%
SCLK Fall to DOUT Transition	t_{DOT}	C_{LOAD} = 30pF			40	ns
$\overline{CS}$ Rise to DOUT Disable	t_{DOD}	C_{LOAD} = 30pF			40	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DOE}	C_{LOAD} = 30pF			40	ns
DIN to SCLK Rise Setup	t_{DS}				40	ns
SCLK Rise to DIN Hold	t_{DH}		0			ns
$\overline{CS}$ Rise-to-SCLK Rise Setup Time	t_{CSS1}		40			ns
$\overline{CS}$ Fall-to-SCLK Hold Time	T_{CSH0}		0			ns
$\overline{CNVST}$ Pulse Width	t_{CSW}	CKSEL = 00, CKSEL = 01 (temp sense)	40			ns
		CKSEL = 01 (voltage conversion)	1.4			µs
$\overline{CS}$ or $\overline{CNVST}$ Rise to $\overline{EOC}$ Low (Note 10)	t_{TS}	Temp sense			55	µs
		Voltage conversion			7	
		Reference power-up			65	

Note 10: This time is defined as the number of clock cycles needed for conversion multiplied by the clock period. If the internal ref erence needs to be powered up, the total time is additive. The internal reference is always used for temperature measure ments.

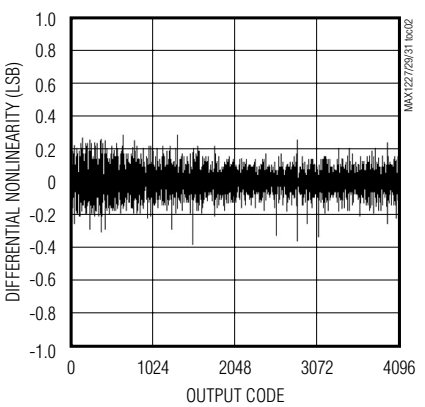
Typical Operating Characteristics

(V_{DD} = +3V, V_{REF} = +2.5V, f_{SCLK} = 4.8MHz, C_{LOAD} = 30pF, T_A = +25°C, unless otherwise noted.)

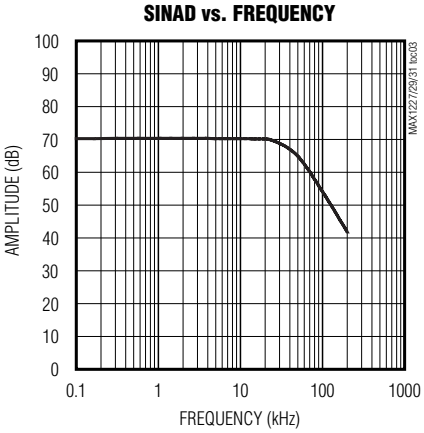
INTEGRAL NONLINEARITY vs. OUTPUT CODE



DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



SINAD vs. FREQUENCY

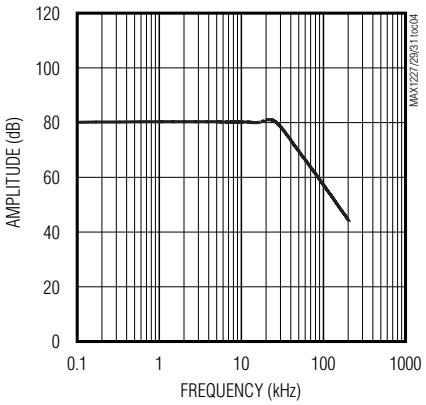


12-Bit 300ksps ADCs with FIFO, Temp Sensor, Internal Reference

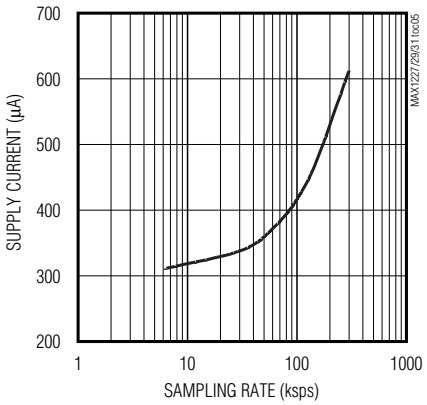
Typical Operating Characteristics (continued)

(V_{DD} = +3V, V_{REF} = +2.5V, f_{SCLK} = 4.8MHz, C_{LOAD} = 30pF, T_A = +25°C, unless otherwise noted.)

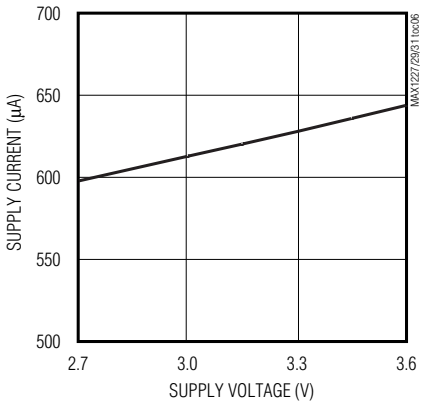
SFDR vs. FREQUENCY



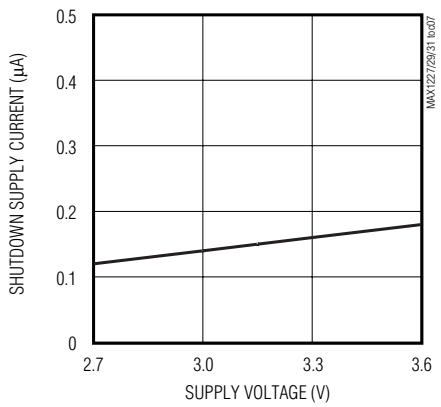
SUPPLY CURRENT vs. SAMPLING RATE



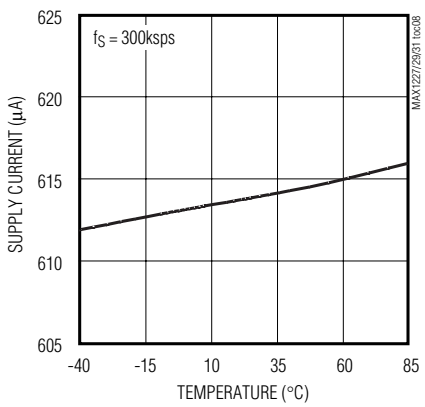
SUPPLY CURRENT vs. SUPPLY VOLTAGE



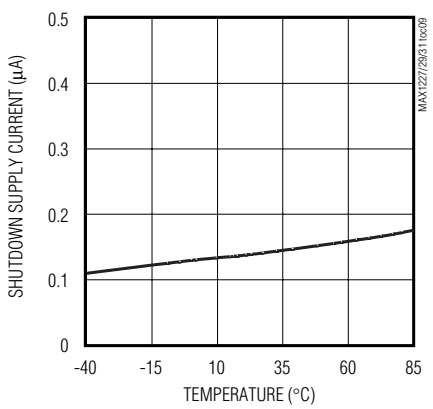
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



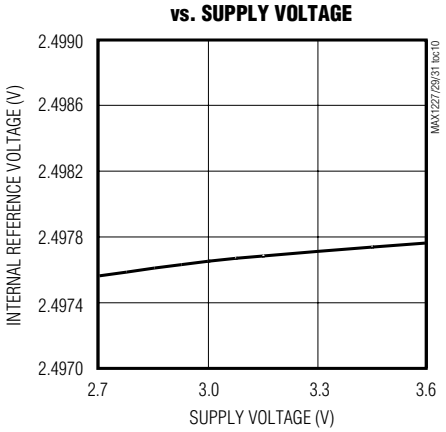
SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



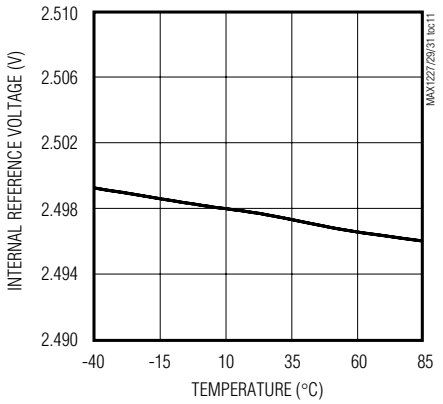
INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



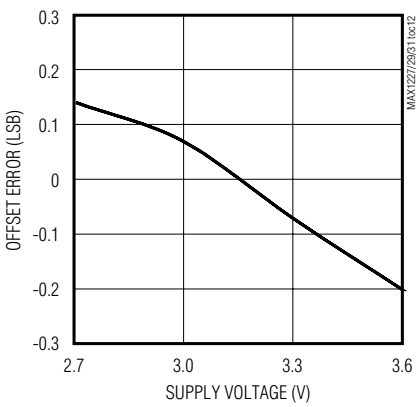
Typical Operating Characteristics (continued)

(V_{DD} = +3V, V_{REF} = +2.5V, f_{SCLK} = 4.8MHz, C_{LOAD} = 30pF, T_A = +25°C, unless otherwise noted.)

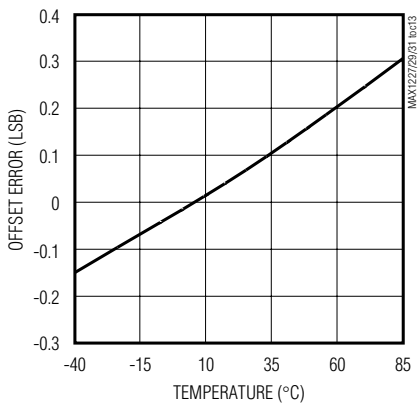
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



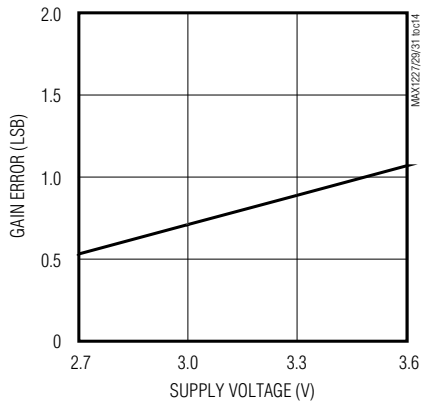
OFFSET ERROR vs. SUPPLY VOLTAGE



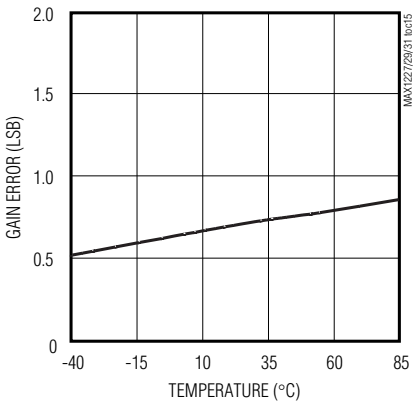
OFFSET ERROR vs. TEMPERATURE



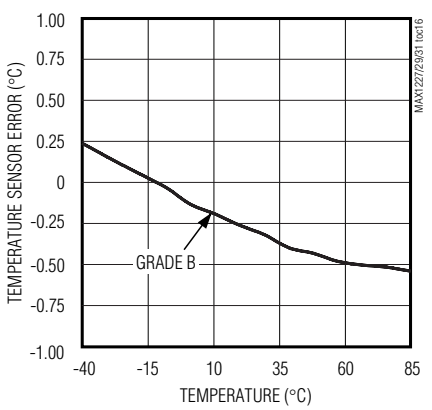
GAIN ERROR vs. SUPPLY VOLTAGE



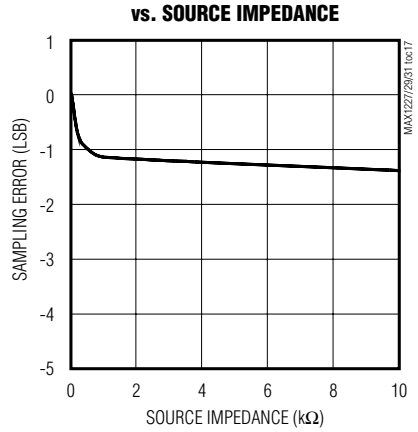
GAIN ERROR vs. TEMPERATURE



TEMPERATURE SENSOR ERROR vs. TEMPERATURE



SAMPLING ERROR vs. SOURCE IMPEDANCE



12-Bit 300ksps ADCs with FIFO, Temp Sensor, Internal Reference

Pin Description

PIN				NAME	FUNCTION
MAX1231 TQFN-EP	MAX1231 QSOP	MAX1229	MAX1227		
2–12, 26, 27, 28,	1–14	—	—	AIN0–13	Analog Inputs
—	—	1–10	—	AIN0–9	Analog Inputs
—	—	—	1–6	AIN0–5	Analog Inputs
13	15	—	—	REF-/AIN14	Negative Input for External Differential Reference/Analog Input 14. See Table 3 for details on programming the setup register.
—	—	11	—	REF-/AIN10	Negative Input for External Differential Reference/Analog Input 10. See Table 3 for details on programming the setup register.
—	—	—	7	REF-/AIN6	Negative Input for External Differential Reference/Analog Input 6. See Table 3 for details on programming the setup register.
14	16	—	—	$\overline{\text{CNVST}}$/ AIN15	Active-Low Conversion Start Input/Analog Input 15. See Table 3 for details on programming the setup register.
—	—	12	—	$\overline{\text{CNVST}}$/ AIN11	Active-Low Conversion Start Input/Analog Input 11. See Table 3 for details on programming the setup register.
—	—	—	8	$\overline{\text{CNVST}}$/ AIN7	Active-Low Conversion Start Input/Analog Input 7. See Table 3 for details on programming the setup register.
15	17	13	9	REF+	Positive Reference Input. Bypass to GND with a 0.1µF capacitor.
16	18	14	10	GND	Ground
18	19	15	11	V_{DD}	Power Input. Bypass to GND with a 0.1µF capacitor.
20	20	16	12	SCLK	Serial Clock Input. Clocks data in and out of the serial interface. (Duty cycle must be 40% to 60%.) See Table 3 for details on programming the clock mode.
21	21	17	13	$\overline{\text{CS}}$	Active-Low Chip Select Input. When $\overline{\text{CS}}$ is low, the serial interface is enabled. When $\overline{\text{CS}}$ is high, DOUT is high impedance.
22	22	18	14	DIN	Serial Data Input. DIN data is latched into the serial interface on the rising edge of SCLK.
23	23	19	15	DOUT	Serial Data Output. Data is clocked out on the falling edge of SCLK. High impedance when $\overline{\text{CS}}$ is connected to V_{DD}.
24	24	20	16	$\overline{\text{EOC}}$	End of Conversion Output. Data is valid after $\overline{\text{EOC}}$ pulls low.
1, 17, 19, 25	—	—	—	N.C.	No Connection. Not internally connected.
—	—	—	—	EP	Exposed Pad (TQFN Only). Connect to GND.

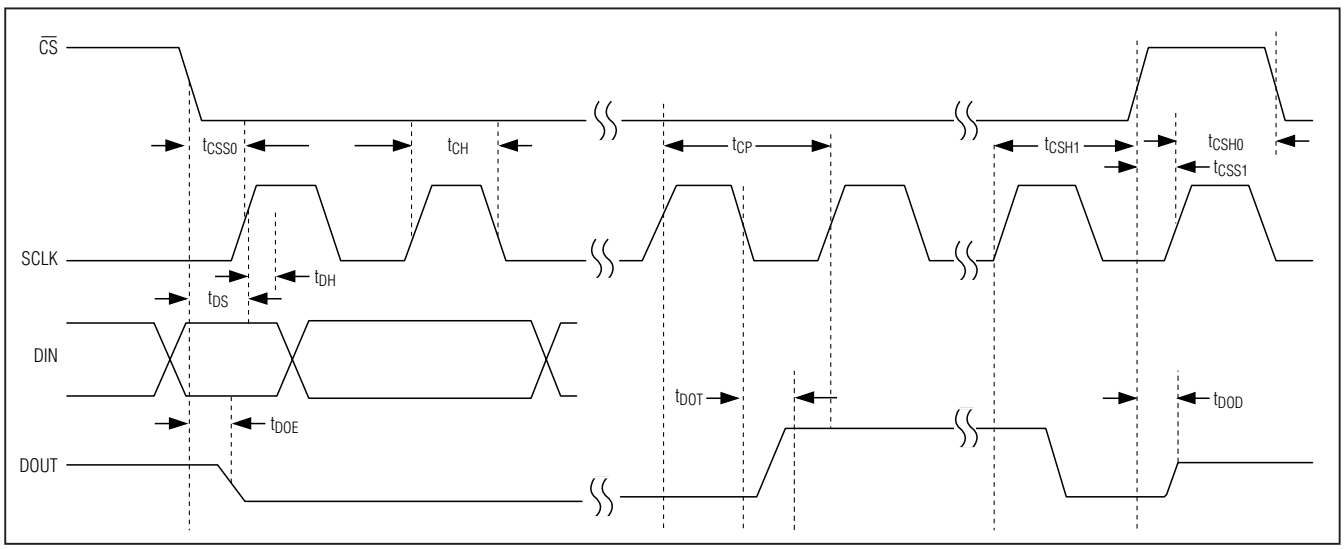


Figure 1. Detailed Serial-Interface Timing Diagram

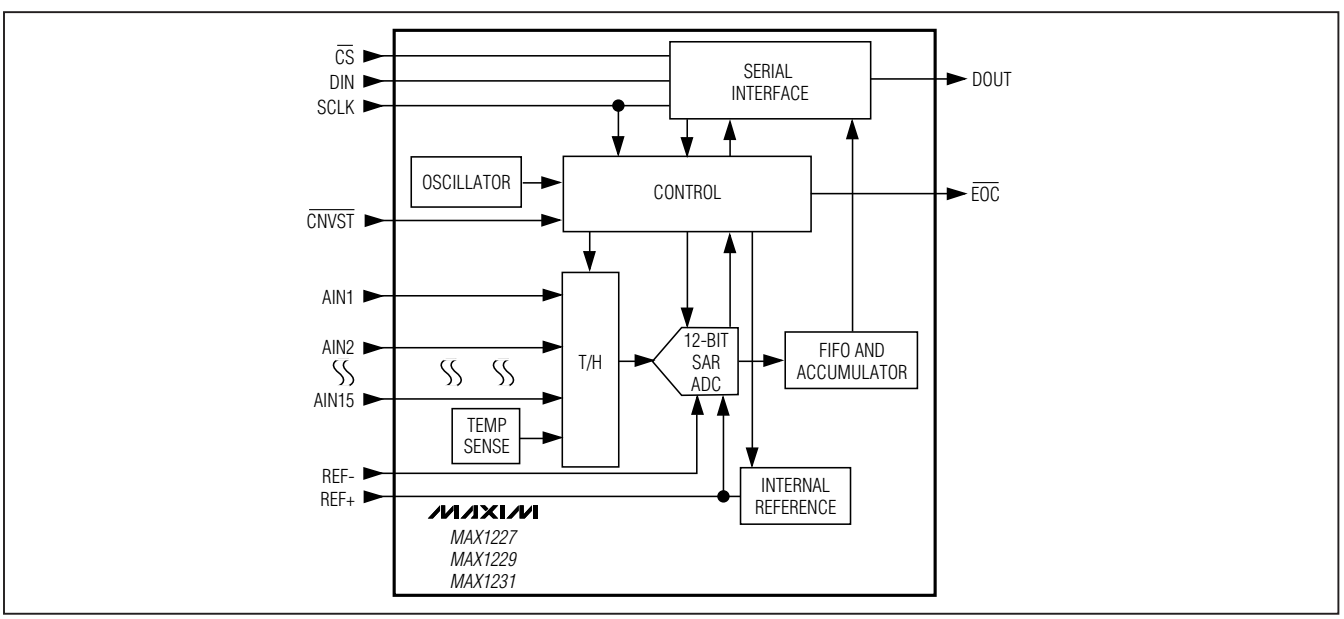


Figure 2. Functional Diagram

Detailed Description

The MAX1227/MAX1229/MAX1231 are low-power, serial-output, multichannel ADCs with temperature-sensing capability for temperature-control, process-control, and monitoring applications. These 12-bit ADCs have internal track and hold (T/H) circuitry that supports single-ended and fully differential inputs. Data is converted from an internal temperature sensor or analog voltage sources in a variety of channel and data-acquisition configurations. Microprocessor (µP) control is made easy through a 3-wire SPI-/QSPI/ MICROWIRE-compatible serial interface.

Figure 2 shows a simplified functional diagram of the MAX1227/MAX1229/MAX1231 internal architecture. The MAX1227 has eight single-ended analog input channels or four differential channels. The MAX1229 has 12 single-ended analog input channels or six differential channels. The MAX1231 has 16 single-ended analog input channels or eight differential channels.

12-Bit 300ksps ADCs with FIFO, Temp Sensor, Internal Reference

Converter Operation

The MAX1227/MAX1229/MAX1231 ADCs use a fully differential, successive-approximation register (SAR) conversion technique and an on-chip T/H block to convert temperature and voltage signals into a 12-bit digital result. Both single-ended and differential configurations are supported, with a unipolar signal range for single-ended mode and bipolar or unipolar ranges for differential mode.

Input Bandwidth

The ADC's input-tracking circuitry has a 1MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. Anti-alias prefiltering of the input signals is necessary to avoid high-frequency signals aliasing into the frequency band of interest.

Analog Input Protection

Internal ESD protection diodes clamp all pins to V_{DD} and GND, allowing the inputs to swing from (GND - 0.3V) to (V_{DD} + 0.3V) without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than GND by 50mV. If an off-channel analog input voltage exceeds the supplies, limit the input current to 2mA.

3-Wire Serial Interface

The MAX1227/MAX1229/MAX1231 feature a serial interface compatible with SPI/QSPI and MICROWIRE devices. For SPI/QSPI, ensure the CPU serial interface runs in master mode so it generates the serial clock signal. Select the SCLK frequency of 10MHz or less, and set clock polarity (CPOL) and phase (CPHA) in the µP control registers to the same value. The MAX1227/MAX1229/MAX1231 operate with SCLK idling high or low, and thus operate with CPOL = CPHA = 0 or CPOL = CPHA = 1. Set $\overline{CS}$ low to latch input data at DIN on the rising edge of SCLK. Output data at DOUT is updated on the falling edge of SCLK. Bipolar true differential results and temperature sensor results are available in two's complement format, while all others are in binary.

Serial communication always begins with an 8-bit input data byte (MSB first) loaded from DIN. Use a second byte, immediately following the setup byte, to write to the unipolar mode or bipolar mode registers (see Tables 1, 3, 4, and 5). A high-to-low transition on $\overline{CS}$ initiates the data input operation. The input data byte and the subsequent data bytes are clocked from DIN into the serial interface on the rising edge of SCLK.

Tables 1–7 detail the register descriptions. Bits 5 and 4, CKSEL1 and CKSEL0, respectively, control the clock modes in the setup register (see Table 3). Choose between four different clock modes for various ways to start a conversion and determine whether the acquisitions are internally or externally timed. Select clock mode 00 to configure $\overline{CNVST}$/AIN_ to act as a conversion start and use it to request the programmed, internally timed conversions without tying up the serial bus. In clock mode 01, use $\overline{CNVST}$ to request conversions one channel at a time, controlling the sampling speed without tying up the serial bus. Request and start internally timed conversions through the serial interface by writing to the conversion register in the default clock mode 10. Use clock mode 11 with SCLK up to 4.8MHz for externally timed acquisitions to achieve sampling rates up to 300ksps. Clock mode 11 disables scanning and averaging. See Figures 4–7 for timing specifications and how to begin a conversion.

These devices feature an active-low, end-of-conversion output. $\overline{EOC}$ goes low when the ADC completes the last-requested operation and is waiting for the next input data byte (for clock modes 00 and 10). In clock mode 01, $\overline{EOC}$ goes low after the ADC completes each requested operation. $\overline{EOC}$ goes high when $\overline{CS}$ or $\overline{CNVST}$ goes low. $\overline{EOC}$ is always high in clock mode 11.

Single-Ended/Differential Input

The MAX1227/MAX1229/MAX1231 use a fully differential ADC for all conversions. The analog inputs can be configured for either differential or single-ended conversions by writing to the setup register (see Table 3). Single-ended conversions are internally referenced to GND (see Figure 3).

In differential mode, the T/H samples the difference between two analog inputs, eliminating common-mode DC offsets and noise. IN+ and IN- are selected from the following pairs: AIN0/AIN1, AIN2/AIN3, AIN4/AIN5, AIN6/AIN7, AIN8/AIN9, AIN10/AIN11, AIN12/AIN13, and AIN14/AIN15. AIN0–AIN7 are available on the MAX1227, MAX1229, and MAX1231. AIN8–AIN11 are only available on the MAX1229 and MAX1231. AIN12–AIN15 are only available on the MAX1231. See Tables 2–5 for more details on configuring the inputs. For the inputs that can be configured as $\overline{CNVST}$ or an analog input, only one can be used at a time. For the inputs that can be configured as REF- or an analog input, the REF- configuration excludes the analog input.

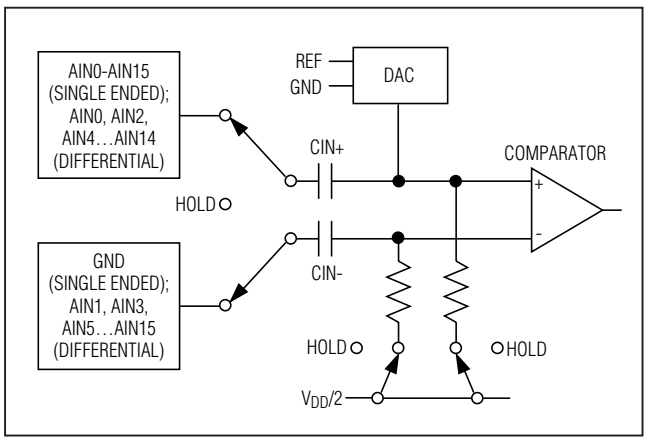


Figure 3. Equivalent Input Circuit

Unipolar/Bipolar

Address the unipolar and bipolar registers through the setup register (bits 1 and 0). Program a pair of analog channels for differential operation by writing a 1 to the appropriate bit of the bipolar or unipolar register. Unipolar mode sets the differential input range from 0 to V_{REF}. A negative differential analog input in unipolar mode causes the digital output code to be zero. Selecting bipolar mode sets the differential input range to $\pm V_{REF}/2$. The digital output code is binary in unipolar mode and two's complement in bipolar mode (Figures 8 and 9).

In single-ended mode, the MAX1227/MAX1229/MAX1231 always operate in unipolar mode. The analog inputs are internally referenced to GND with a full-scale input range from 0 to V_{REF}.

True Differential Analog Input T/H

The equivalent circuit of Figure 3 shows the MAX1227/MAX1229/MAX1231s' input architecture. In track mode, a positive input capacitor is connected to AIN0–AIN15 in single-ended mode (and AIN0, AIN2, AIN4…AIN14 in differential mode). A negative input capacitor is connected to GND in single-ended mode (or AIN1, AIN3, AIN5…AIN15 in differential mode). For external T/H timing, use clock mode 01. After the T/H enters hold mode, the difference between the sampled positive and negative input voltages is converted. The time required for the T/H to acquire an input signal is determined by how quickly its input capacitance is charged. If the input signal's source impedance is high, the required acquisition time lengthens. The acquisition time, t_{ACQ}, is the maximum time needed for a signal to be acquired, plus the power-up time. It is calculated by the following equation:

$$t_{ACQ} = 9 \times (R_S + R_{IN}) \times 24pF + t_{PWR}$$

where $R_{IN} = 1.5k\Omega$, R_S is the source impedance of the input signal, and $t_{PWR} = 1\mu s$, the power-up time of the device. The varying power-up times are detailed in the explanation of the clock mode conversions.

t_{ACQ} is never less than 1.4µs, and any source impedance below 300Ω does not significantly affect the ADC's AC performance. A high-impedance source can be accommodated either by lengthening t_{ACQ} or by placing a 1µF capacitor between the positive and negative analog inputs.

Internal FIFO

The MAX1227/MAX1229/MAX1231 contain a FIFO buffer that can hold up to 16 ADC results plus one temperature result. This allows the ADC to handle multiple internally clocked conversions and a temperature measurement, without tying up the serial bus.

If the FIFO is filled and further conversions are requested without reading from the FIFO, the oldest ADC results are overwritten by the new ADC results. Each result contains 2 bytes, with the MSB preceded by four leading zeros. After each falling edge of $\overline{CS}$, the oldest available byte of data is available at DOUT, MSB first. When the FIFO is empty, DOUT is zero.

The first 2 bytes of data read out after a temperature measurement always contain the temperature result preceded by four leading zeros, MSB first. If another temperature measurement is performed before the first temperature result is read out, the old measurement is overwritten by the new result. Temperature results are in degrees Celsius (two's complement) at a resolution of 1/8 of a degree. See the *Temperature Measurements* section for details on converting the digital code to a temperature.

Internal Clock

The MAX1227/MAX1229/MAX1231 operate from an internal oscillator, which is accurate within 10% of the 4.4MHz nominal clock rate. The internal oscillator is active in clock modes 00, 01, and 10. Read out the data at clock speeds up to 10MHz. See Figures 4–7 for details on timing specifications and starting a conversion.

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Applications Information

Register Descriptions

The MAX1227/MAX1229/MAX1231 communicate between the internal registers and the external circuitry through the SPI-/QSPI-compatible serial interface. Table 1 details the registers and the bit names. Tables 2–7 show the various functions within the conversion register, setup register, averaging register, reset register, unipolar register, and bipolar register.

Conversion Time Calculations

The conversion time for each scan is based on a number of different factors: conversion time per sample, samples per result, results per scan, if a temperature measurement is requested, and if the external reference is in use.

Use the following formula to calculate the total conversion time for an internally timed conversion in clock modes 00 and 10 (see the *Electrical Characteristics* section as applicable):

total conversion time = $t_{CNV} \times n_{AVG} \times n_{RESULT} + t_{TS} + t_{RP}$

where:

$t_{CNV} = t_{ACQ}(max) + t_{CONV}(max)$

n_{AVG} = samples per result (amount of averaging)

n_{RESULT} = number of FIFO results requested; determined by number of channels being scanned or by NSCAN1, NSCAN0

t_{TS} = time required for temperature measurement; set to zero if temp measurement is not requested

t_{RP} = internal reference wake up; set to zero if internal reference is already powered up or external reference is being used

In clock mode 01, the total conversion time depends on how long $\overline{CNVST}$ is held low or high, including any time required to turn on the internal reference. Conversion time in externally clocked mode (CKSEL1, CKSEL0 = 11) depends on the SCLK period and how long $\overline{CS}$ is held high between each set of eight SCLK cycles. In clock mode 01, the total conversion time does not include the time required to turn on the internal reference.

Conversion Register

Select active analog input channels, scan modes, and a single temperature measurement per scan by writing to the conversion register. Table 2 details channel selection, the four scan modes, and how to request a temperature measurement. Request a scan by writing to the conversion register when in clock mode 10 or 11, or by applying a low pulse to the $\overline{CNVST}$ pin when in clock mode 00 or 01.

A conversion is not performed if it is requested on a channel that has been configured as $\overline{CNVST}$ or REF-. Do not request conversions on channels 8–15 on the MAX1227 and channels 12–15 on the MAX1229. Set CHSEL3:CHSELO to the lower channel's binary value. If the last two channels are configured as a differential pair and one of them has been reconfigured as $\overline{CNVST}$ or REF-, the pair is ignored.

Select scan mode 00 or 01 to return one result per single-ended channel and one result per differential pair within the requested range, plus one temperature result if selected. Select scan mode 10 to scan a single input channel numerous times, depending on NSCAN1 and NSCAN0 in the averaging register (Table 6). Select scan mode 11 to return only one result from a single channel.

Setup Register

Write a byte to the setup register to configure the clock, reference, and power-down modes. Table 3 details the

Table 1. Input Data Byte (MSB First)

REGISTER NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Conversion	1	CHSEL3	CHSEL2	CHSEL1	CHSEL0	SCAN1	SCAN0	TEMP
Setup	0	1	CKSEL1	CKSEL0	REFSEL1	REFSEL0	DIFFSEL1	DIFFSEL0
Averaging	0	0	1	AVGON	NAVG1	NAVG0	NSCAN1	NSCAN0
Reset	0	0	0	1	$\overline{RESET}$	X	X	X
Unipolar mode (setup)	UCH0/1	UCH2/3	UCH4/5	UCH6/7	UCH8/9*	UCH10/11	UCH12/138**	UCH14/15**
Bipolar mode (setup)	BCH0/1	BCH1/2	BCH4/5	BCH6/7	BCH8/9*	BCH10/11	BCH12/13**	BCH14/15**

*Unipolar/bipolar channels 8–15 are only valid on the MAX1229 and MAX1231.
*Unipolar/bipolar channels 12–15 are only valid on the MAX1231.
X = Don't care.

Table 2. Conversion Register

BIT NAME	BIT	FUNCTION
—	7 (MSB)	Set to 1 to select conversion register.
CHSEL3	6	Analog input channel select.
CHSEL2	5	Analog input channel select.
CHSEL1	4	Analog input channel select.
CHSEL0	3	Analog input channel select.
SCAN1	2	Scan mode select.
SCAN0	1	Scan mode select.
TEMP	0 (LSB)	Set to 1 to take a single temperature measurement. The first conversion result of a scan contains temperature information.

* See below for bit details.

CHSEL3	CHSEL2	CHSEL1	CHSEL0	SELECTED CHANNEL (N)
0	0	0	0	AIN0
0	0	0	1	AIN1
0	0	1	0	AIN2
0	0	1	1	AIN3
0	1	0	0	AIN4
0	1	0	1	AIN5
0	1	1	0	AIN6
0	1	1	1	AIN7
1	0	0	0	AIN8
1	0	0	1	AIN9
1	0	1	0	AIN10
1	0	1	1	AIN11
1	1	0	0	AIN12
1	1	0	1	AIN13
1	1	1	0	AIN14
1	1	1	1	AIN15

SCAN1	SCAN0	SCAN MODE (CHANNEL N IS SELECTED BY BITS CHSEL3–CHSEL0)
0	0	Scans channels 0 through N.
0	1	Scans channels N through the highest numbered channel.
1	0	Scans channel N repeatedly. The averaging register sets the number of results.
1	1	No scan. Converts channel N once only.

bits in the setup register. Bits 5 and 4 (CKSEL1 and CKSEL0) control the clock mode, acquisition and sampling, and the conversion start. Bits 3 and 2 (REFSEL1 and REFSEL0) control internal or external reference use. Bits 1 and 0 (DIFFSEL1 and DIFFSEL0) address the unipolar mode and bipolar mode registers and configure the analog input channels for differential operation.

Unipolar/Bipolar Registers

The final 2 bits (LSBs) of the setup register control the unipolar/bipolar mode address registers. Set bits 1 and 0 (DIFFSEL1 and DIFFSEL0) to 10 to write to the unipolar mode register. Set bits 1 and 0 to 11 to write to the bipolar mode register. In both cases, the setup byte must be followed immediately by 1 byte of data written to the unipolar register or bipolar register. Hold $\overline{CS}$ low and run 16 SCLK cycles before pulling $\overline{CS}$ high. If the last 2 bits of the setup register are 00 or 01, neither the unipolar mode register nor the bipolar mode register is written. Any subsequent byte is recognized as a new input data byte. See Tables 4 and 5 to program the unipolar and bipolar mode registers.

If a channel is configured as both unipolar and bipolar, the unipolar setting takes precedence. In unipolar mode, AIN+ can exceed AIN- by up to V_{REF}. The output format in unipolar mode is binary. In bipolar mode, either input can exceed the other by up to $V_{REF}/2$. The output format in bipolar mode is two's complement.

Averaging Register

Write to the averaging register to configure the ADC to average up to 32 samples for each requested result, and to independently control the number of results requested for single-channel scans.

Table 2 details the four scan modes available in the conversion register. All four scan modes allow averaging as long as the AVGON bit, bit 4 in the averaging register, is set to 1. Select scan mode 10 to scan the same channel multiple times. Clock mode 11 disables averaging.

Reset Register

Write to the reset register (as shown in Table 7) to clear the FIFO or to reset all registers to their default states. Set the $\overline{RESET}$ bit to 1 to reset the FIFO. Set the reset bit to zero to return the MAX1227/MAX1229/MAX1231 to the default power-up state.

Power-Up Default State

The MAX1227/MAX1229/MAX1231 power up with all blocks in shutdown, including the reference. All registers power up in state 00000000, except for the setup register, which powers up in clock mode 10 (CKSEL1 = 1).

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Table 3. Setup Register

BIT NAME	BIT	FUNCTION
—	7 (MSB)	Set to zero to select setup register.
—	6	Set to 1 to select setup register.
CKSEL1	5	Clock mode and $\overline{\text{CNVST}}$ configuration. Resets to 1 at power-up.
CKSEL0	4	Clock mode and $\overline{\text{CNVST}}$ configuration.
REFSEL1	3	Reference mode configuration.
REFSEL0	2	Reference mode configuration.
DIFFSEL1	1	Unipolar/bipolar mode register configuration for differential mode.
DIFFSEL0	0 (LSB)	Unipolar/bipolar mode register configuration for differential mode.

* See below for bit details.

CKSEL1	CKSEL0	CONVERSION CLOCK	ACQUISITION/SAMPLING	$\overline{\text{CNVST}}$ CONFIGURATION
0	0	Internal	Internally timed	$\overline{\text{CNVST}}$
0	1	Internal	Externally timed through $\overline{\text{CNVST}}$	$\overline{\text{CNVST}}$
1	0	Internal	Internally timed	AIN15/11/7
1	1	External (4.8MHz max)	Externally timed through SCLK	AIN15/11/7

REFSEL1	REFSEL0	VOLTAGE REFERENCE	AutoShutdown	REF- CONFIGURATION
0	0	Internal	Reference off after scan; need wake-up delay.	AIN14/10/6
0	1	External single ended	Reference off; no wake-up delay.	AIN14/10/6
1	0	Internal	Reference always on; no wake-up delay.	AIN14/10/6
1	1	External differential	Reference off; no wake-up delay.	REF-

DIFFSEL1	DIFFSEL0	FUNCTION
0	0	No data follows the setup byte. Unipolar mode and bipolar mode registers remain unchanged.
0	1	No data follows the setup byte. Unipolar mode and bipolar mode registers remain unchanged.
1	0	One byte of data follows the setup byte and is written to the unipolar mode register.
1	1	One byte of data follows the setup byte and is written to the bipolar mode register.

Temperature Measurements

The MAX1227/MAX1229/MAX1231 perform temperature measurements with an internal diode-connected transistor. The diode bias current changes from 68µA to 4µA to produce a temperature-dependent bias voltage difference. The second conversion result at 4µA is subtracted from the first at 68µA to calculate a digital value that is proportional to absolute temperature. The output data appearing at DOUT is the above digital code minus an offset to adjust from Kelvin to Celsius.

The reference voltage used for the temperature measurements is derived from the internal reference source to ensure that 1 LSB corresponds to 1/8 of a degree.

Output Data Format

Figures 4–7 illustrate the conversion timing for the MAX1227/MAX1229/MAX1231. The 12-bit conversion result is output in MSB-first format with four leading zeros. DIN data is latched into the serial interface on the rising edge of SCLK. Data on DOUT transitions on the falling edge of SCLK. Conversions in clock modes 00 and 01 are initiated by $\overline{CNVST}$. Conversions in clock modes 10 and 11 are initiated by writing an input data byte to the conversion register. Data is binary for unipolar mode and two's complement for bipolar mode.

Table 4. Unipolar Mode Register (Addressed Through Setup Register)

BIT NAME	BIT	FUNCTION
UCH0/1	7 (MSB)	Set to 1 to configure AIN0 and AIN1 for unipolar differential conversion.
UCH2/3	6	Set to 1 to configure AIN2 and AIN3 for unipolar differential conversion.
UCH4/5	5	Set to 1 to configure AIN4 and AIN5 for unipolar differential conversion.
UCH6/7	4	Set to 1 to configure AIN6 and AIN7 for unipolar differential conversion.
UCH8/9	3	Set to 1 to configure AIN8 and AIN9 for unipolar differential conversion (MAX1229/MAX1231 only).
UCH10/11	2	Set to 1 to configure AIN10 and AIN11 for unipolar differential conversion (MAX1229/MAX1231 only).
UCH12/13	1	Set to 1 to configure AIN12 and AIN13 for unipolar differential conversion (MAX1231 only).
UCH14/15	0 (LSB)	Set to 1 to configure AIN14 and AIN15 for unipolar differential conversion (MAX1231 only).

Table 5. Bipolar Mode Register (Addressed Through Setup Register)

BIT NAME	BIT	FUNCTION
BCH0/1	7 (MSB)	Set to 1 to configure AIN0 and AIN1 for bipolar differential conversion.
BCH2/3	6	Set to 1 to configure AIN2 and AIN3 for bipolar differential conversion.
BCH4/5	5	Set to 1 to configure AIN4 and AIN5 for bipolar differential conversion.
BCH6/7	4	Set to 1 to configure AIN6 and AIN7 for bipolar differential conversion.
BCH8/9	3	Set to 1 to configure AIN8 and AIN9 for bipolar differential conversion (MAX1229/MAX1231 only).
BCH10/11	2	Set to 1 to configure AIN10 and AIN11 for bipolar differential conversion (MAX1229/MAX1231 only).
BCH12/13	1	Set to 1 to configure AIN12 and AIN13 for bipolar differential conversion (MAX1231 only).
BCH14/15	0 (LSB)	Set to 1 to configure AIN14 and AIN15 for bipolar differential conversion (MAX1231only).

Table 6. Averaging Register

BIT NAME	BIT	FUNCTION
—	7 (MSB)	Set to zero to select averaging register.
—	6	Set to zero to select averaging register.
—	5	Set to 1 to select averaging register.
AVGON	4	Set to 1 to turn averaging on. Set to zero to turn averaging off.
NAVG1	3	Configures the number of conversions for single-channel scans.
NAVG0	2	Configures the number of conversions for single-channel scans.
NSCAN1	1	Single-channel scan count. (Scan mode 10 only.)
NSCAN0	0 (LSB)	Single-channel scan count. (Scan mode 10 only.)

* See below for bit details.

AVGON	NAVG1	NAVG0	FUNCTION
0	x	x	Performs 1 conversion for each requested result.
1	0	0	Performs 4 conversions and returns the average for each requested result.
1	0	1	Performs 8 conversions and returns the average for each requested result.
1	1	0	Performs 16 conversions and returns the average for each requested result.
1	1	1	Performs 32 conversions and returns the average for each requested result.

NSCAN1	NSCAN0	FUNCTION (APPLIES ONLY IF SCAN MODE 10 IS SELECTED)
0	0	Scans channel N and returns 4 results.
0	1	Scans channel N and returns 8 results.
1	0	Scans channel N and returns 12 results.
1	1	Scans channel N and returns 16 results.

Table 7. Reset Register

BIT NAME	BIT	FUNCTION
—	7 (MSB)	Set to zero to select reset register.
—	6	Set to zero to select reset register.
—	5	Set to zero to select reset register.
—	4	Set to 1 to select reset register.
$\overline{\text{RESET}}$	3	Set to zero to reset all registers. Set to 1 to clear the FIFO only.
x	2	Reserved. Don't care.
x	1	Reserved. Don't care.
x	0 (LSB)	Reserved. Don't care.

Internally Timed Acquisitions and Conversions Using CNVST

Performing Conversions in Clock Mode 00

In clock mode 00, the wake-up, acquisition, conversion, and shutdown sequences are initiated through CNVST and performed automatically using the internal oscillator. Results are added to the internal FIFO to be read out later. See Figure 4 for clock mode 00 timing.

Initiate a scan by setting CNVST low for at least 40ns before pulling it high again. The MAX1227/MAX1229/MAX1231 then wake up, scan all requested channels, store the results in the FIFO, and shut down. After the scan is complete, EOC is pulled low and the results are available in the FIFO. Wait until EOC goes low before pulling CS low to communicate with the serial interface. EOC stays low until CS or CNVST is pulled low again. A temperature measurement result, if requested, precedes all other FIFO results.

Do not initiate a second CNVST before EOC goes low; otherwise, the FIFO can become corrupted.

Externally Timed Acquisitions and Internally Timed Conversions with CNVST

Performing Conversions in Clock Mode 01

In clock mode 01, conversions are requested one at a time using CNVST and performed automatically using the internal oscillator. See Figure 5 for clock mode 01 timing.

Setting CNVST low begins an acquisition, wakes up the ADC, and places it in track mode. Hold CNVST low for at least 1.4µs to complete the acquisition. If internal reference needs to wake up, an additional 65µs is required for the internal reference to power up. If a temperature measurement is being requested, reference power-up and temperature measurement are internally timed. In this case, hold CNVST low for at least 40ns.

Set CNVST high to begin a conversion. After the conversion is complete, the ADC shuts down and pulls EOC low. EOC stays low until CS or CNVST is pulled low again. Wait until EOC goes low before pulling CS or CNVST low.

If averaging is turned on, multiple CNVST pulses need to be performed before a result is written to the FIFO. Once the proper number of conversions has been performed to generate an averaged FIFO result, as specified by the averaging register, the scan logic automatically switches the analog input multiplexer to the next-requested channel. If a temperature measurement is programmed, it is performed after the first rising edge of CNVST following the input data byte written to the conversion register. The result is available on DOUT once EOC has been pulled low.

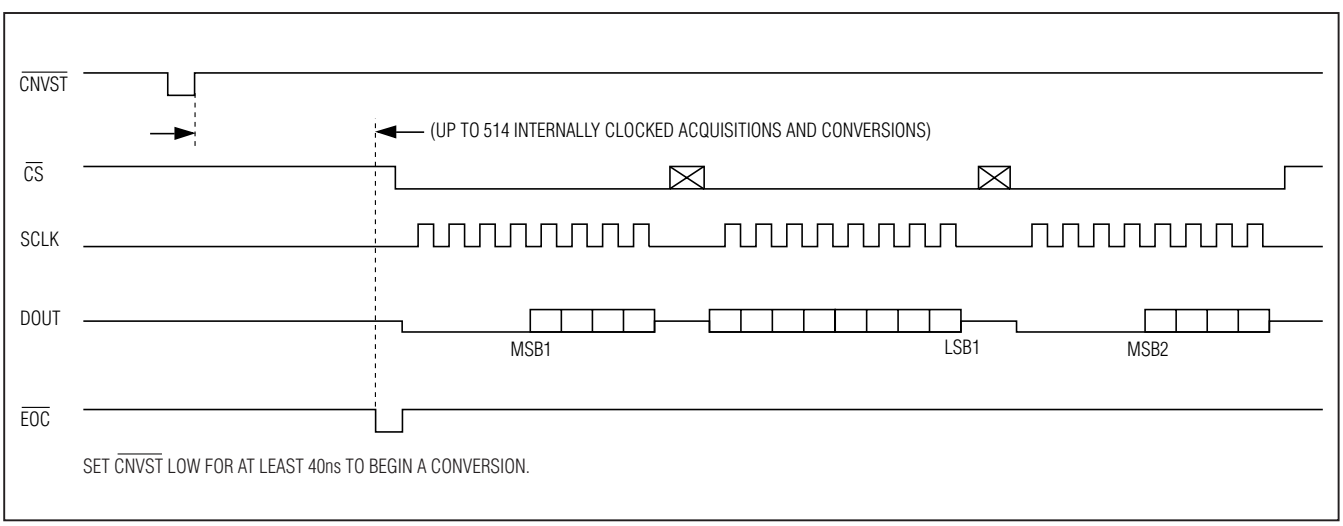

Figure 4. Clock Mode 00

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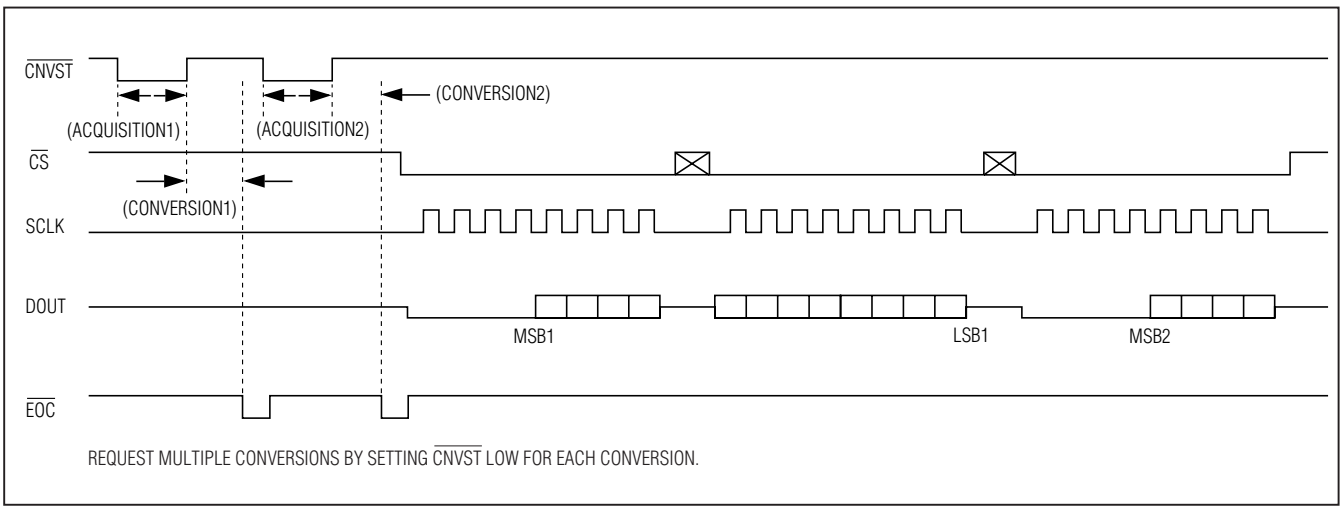


Figure 5. Clock Mode 01

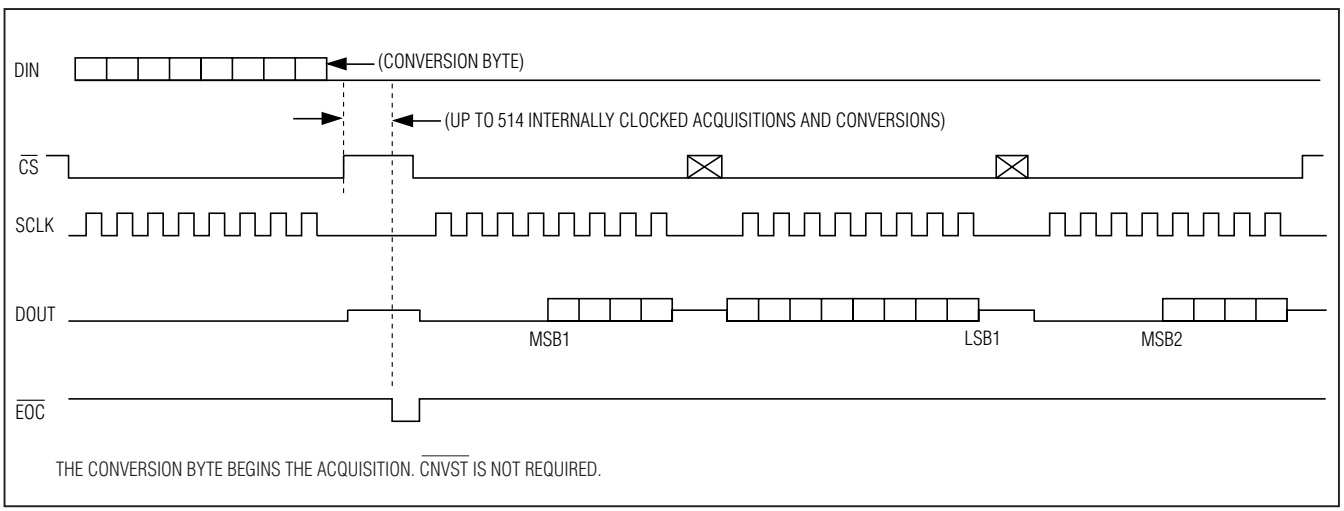


Figure 6. Clock Mode 10

Internally Timed Acquisitions and Conversions Using the Serial Interface

Performing Conversions in Clock Mode 10

In clock mode 10, the wake-up, acquisition, conversion, and shutdown sequences are initiated by writing an input data byte to the conversion register, and are performed automatically using the internal oscillator. This is the default clock mode upon power-up. See Figure 6 for clock mode 10 timing.

Initiate a scan by writing a byte to the conversion register. The MAX1227/MAX1229/MAX1231 then power up, scan all requested channels, store the results in the FIFO, and shut down. After the scan is complete, $\overline{EOC}$ is pulled low and the results are available in the FIFO. If a temperature measurement is requested, the temperature result precedes all other FIFO results. $\overline{EOC}$ stays low until $\overline{CS}$ is pulled low again.

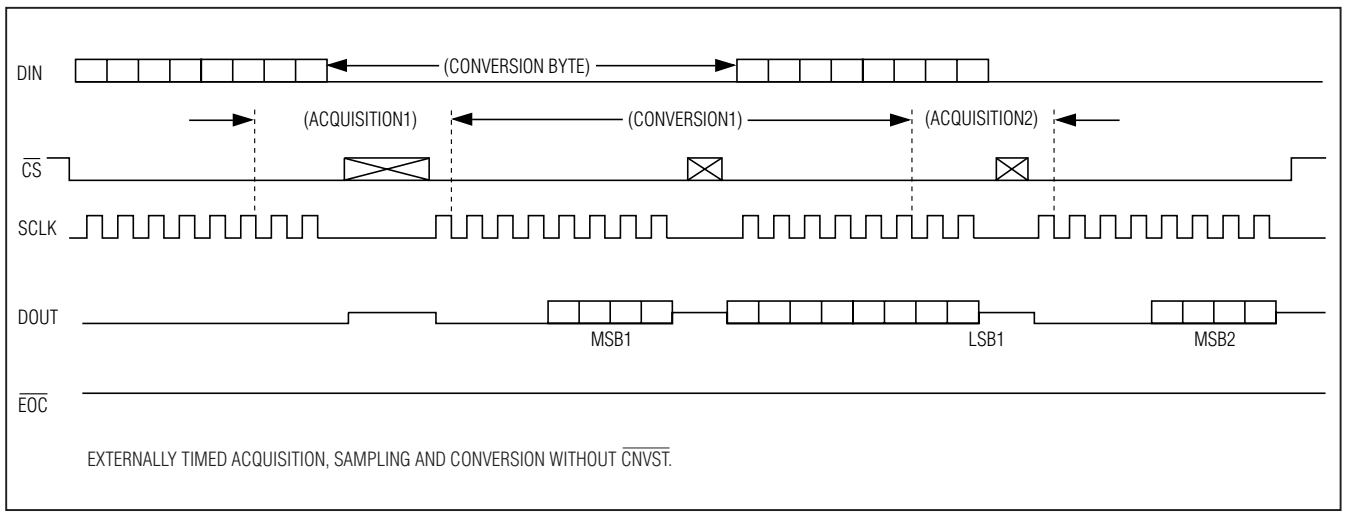


Figure 7. Clock Mode 11

Externally Clocked Acquisitions and Conversions Using the Serial Interface

Performing Conversions in Clock Mode 11

In clock mode 11, acquisitions and conversions are initiated by writing to the conversion register and are performed one at a time using the SCLK as the conversion clock. Scanning and averaging are disabled, and the conversion result is available at DOUT during the conversion. See Figure 7 for clock mode 11 timing.

Initiate a conversion by writing a byte to the conversion register followed by 16 SCLK cycles. If $\overline{CS}$ is pulsed high between the eighth and ninth cycles, the pulse width must be less than 100µs. To continuously convert at 16 cycles per conversion, alternate 1 byte of zeros between each conversion byte.

If reference mode 00 is requested, or if an external reference is selected but a temperature measurement is being requested, wait 65µs with $\overline{CS}$ high after writing the conversion byte to extend the acquisition and allow the internal reference to power up. To perform a temperature measurement, write 24 bytes (192 cycles) of zeros after the conversion byte. The temperature result appears on DOUT during the last 2 bytes of the 192 cycles.

Partial Reads and Partial Writes

If the first byte of an entry in the FIFO is partially read ($\overline{CS}$ is pulled high after fewer than eight SCLK cycles), the second byte of data that is read out contains the next 8 bits (not b7–b0). The remaining bits are lost for that entry. If the first byte of an entry in the FIFO is read out fully, but the second byte is read out partially, the rest of the entry is lost. The remaining data in the FIFO is uncorrupted and can be read out normally after taking $\overline{CS}$ low again, as long as the 4 leading bits (normally zeros) are ignored. Internal registers that are written partially through the SPI contain new values, starting at the MSB up to the point that the partial write is stopped. The part of the register that is not written contains previously written values. If $\overline{CS}$ is pulled low before $\overline{EOC}$ goes low, a conversion cannot be completed and the FIFO is corrupted.

Transfer Function

Figure 8 shows the unipolar transfer function for single-ended or differential inputs. Figure 9 shows the bipolar transfer function for differential inputs. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1 LSB = V_{REF} / 2.5V for unipolar and bipolar operation, and 1 LSB = 0.125°C for temperature measurements.

Layout, Grounding, and Bypassing

For best performance, use PC boards. Do not use wire-wrap boards. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) signals parallel to one another or run digital lines underneath the MAX1227/MAX1229/MAX1231 package. High-frequency noise in the V_{DD} power supply can affect performance. Bypass the V_{DD} supply with a 0.1µF capacitor to GND, close to the V_{DD} pin. Minimize capacitor lead lengths for best supply-noise rejection. If the power supply is very noisy, connect a 10Ω resistor in series with the supply to improve power-supply filtering. For the TQFN package, connect its exposed pad to ground.

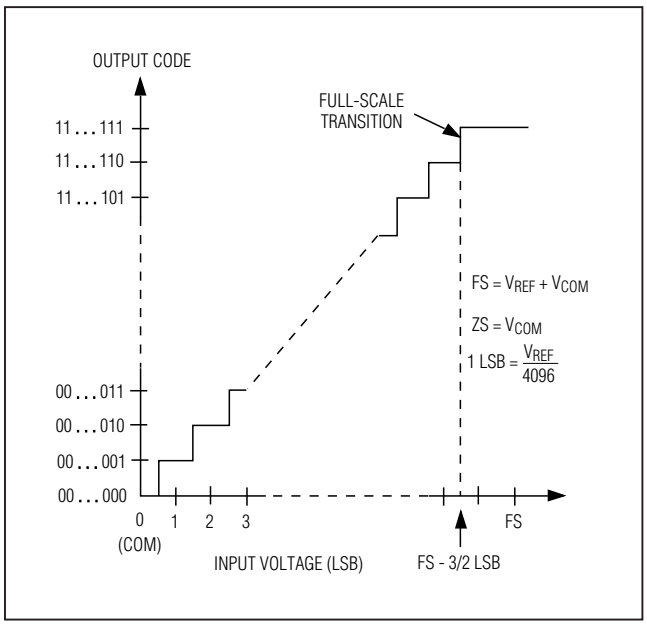


Figure 8. Unipolar Transfer Function, Full Scale (FS) = V_{REF}

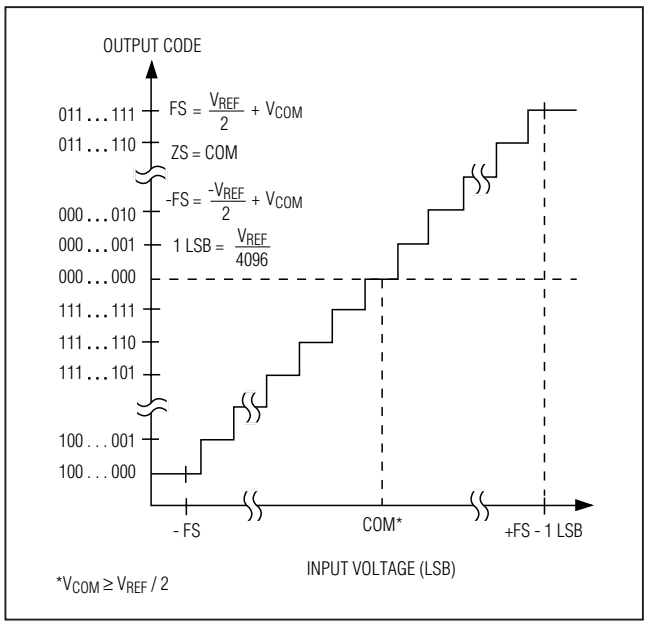


Figure 9. Bipolar Transfer Function, Full Scale (±FS) = ±V_{REF} / 2

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. INL for the MAX1227/MAX1229/MAX1231 is measured using the end-point method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples.

Aperture Delay

Aperture delay (t_{AD}) is the time between the rising edge of the sampling clock and the instant when an actual sample is taken.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise, including thermal noise, reference noise, clock jitter, etc. Therefore, SNR is calculated by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all other ADC output signals:

$$SINAD\ (dB) = 20 \times \log (Signal_{RMS} / Noise_{RMS})$$

Effective Number of Bits

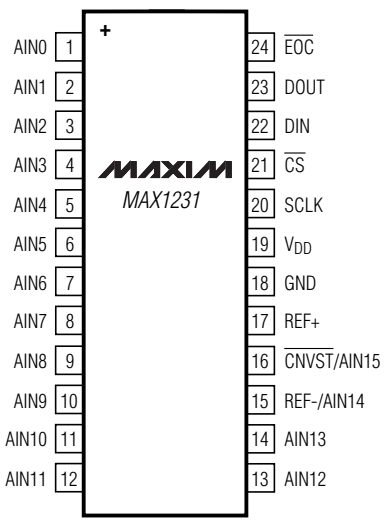
Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the effective number of bits as follows:

$$ENOB = (SINAD - 1.76) / 6.02$$

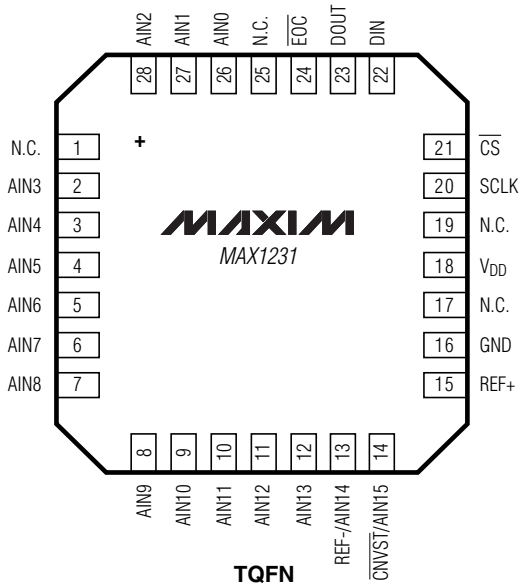
12-Bit 300ksps ADCs with FIFO, Temp Sensor, Internal Reference

Pin Configurations (continued)

TOP VIEW



QSOP



TQFN

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left[\frac{\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2\right)}}{V_1}\right]$$

where V1 is the fundamental amplitude, and V2–V5 are the amplitudes of the first five harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component.

Chip Information

PROCESS: BiCMOS

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX1231BCEG+	0°C to +70°C	24 QSOP
MAX1231BEEG+	-40°C to +85°C	24 QSOP
MAX1231BCTI+	0°C to +70°C	28 TQFN-EP*
MAX1231BETI+	-40°C to +85°C	28 TQFN-EP*

**EP = Exposed pad. (Connect to GND.)*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 QSOP	E16+1	21-0055	90-0167
20 QSOP	E20+1	21-0055	90-0168
24 QSOP	E24+1	21-0055	90-0172
28 TQFN-EP	T2855+6	21-0140	90-0026

12-Bit 300ksps ADCs with FIFO, Temp Sensor, Internal Reference

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	2/10	Removed the A grade products from the *Ordering Information* table and *Electrical Characteristics* table.	1, 3, 21
4	8/10	Added lead-free information to *Ordering Information* and *Package Information* sections	1, 21
5	12/10	Changed several data sheet specifications	1–5, 7, 9, 21
6	5/11	Revised *Ordering Information*	1
7	4/12	Corrected error in acquisition time formula	11

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