

# 74LVT16543A

## 3.3 V 16-bit registered transceiver; 3-state

Rev. 3 — 1 October 2018

Product data sheet

## 1. General description

The 74LVT16543A is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3 V. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74LVT16543A contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B enable ( $n\overline{EAB}$ ) input and the A-to-B latch enable ( $n\overline{LEAB}$ ) input are LOW, the A-to-B path is transparent.

A subsequent LOW-to-HIGH transition of the  $n\overline{LEAB}$  signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With  $n\overline{EAB}$  and  $n\overline{OEAB}$  both LOW, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the  $n\overline{EBA}$ ,  $n\overline{LEBA}$ , and  $n\overline{OEBA}$  inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

## 2. Features and benefits

- 16-bit universal bus interface
- 3-state buffers
- Input and output interface capability to systems at 5 V supply
- TTL input and output switching levels
- Output capability: +64 mA/-32 mA
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-state
- Power-up reset
- No bus current loading when output is tied to 5 V bus
- Latch-up protection:
  - JESD78B Class II exceeds 500 mA
- ESD protection:
  - HBM: JESD22-A114F exceeds 2000 V
  - MM: JESD22-A115-A exceeds 200 V

## 3. Ordering information

Table 1. Ordering information

| Type number    | Package           |         |                                                                        |          |
|----------------|-------------------|---------|------------------------------------------------------------------------|----------|
|                | Temperature range | Name    | Description                                                            | Version  |
| 74LVT16543ADL  | -40 °C to +85 °C  | SSOP56  | plastic shrink small outline package; 56 leads; body width 7.5 mm      | SOT371-1 |
| 74LVT16543ADGG | -40 °C to +85 °C  | TSSOP56 | plastic thin shrink small outline package; 56 leads; body width 6.1 mm | SOT364-1 |

4. Functional diagram

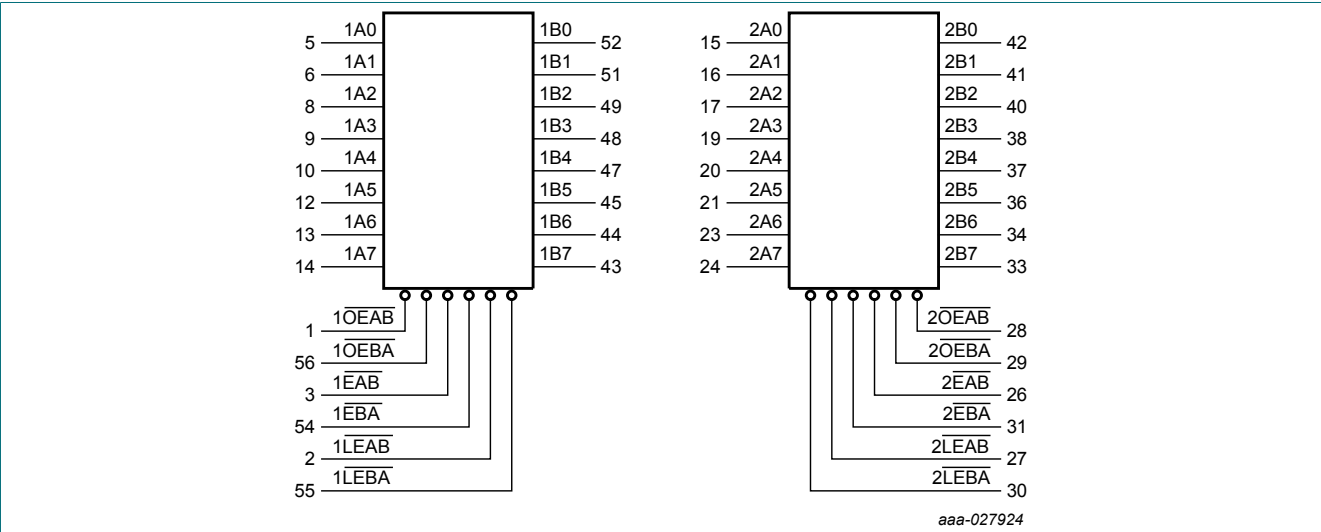


Fig. 1. Logic symbol

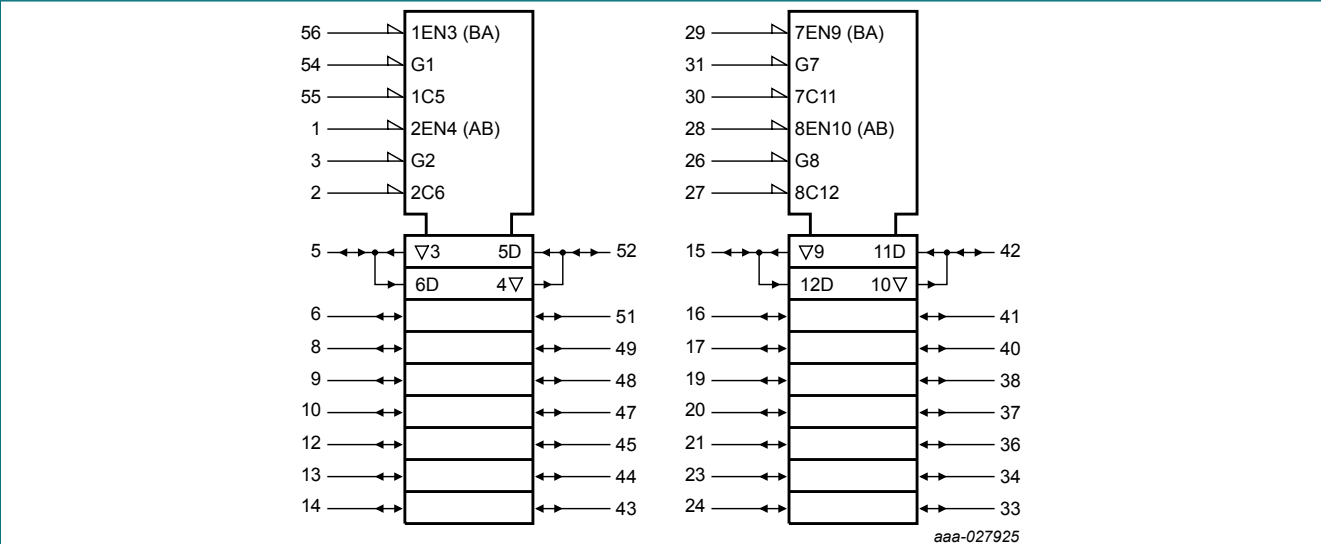


Fig. 2. IEC logic symbol

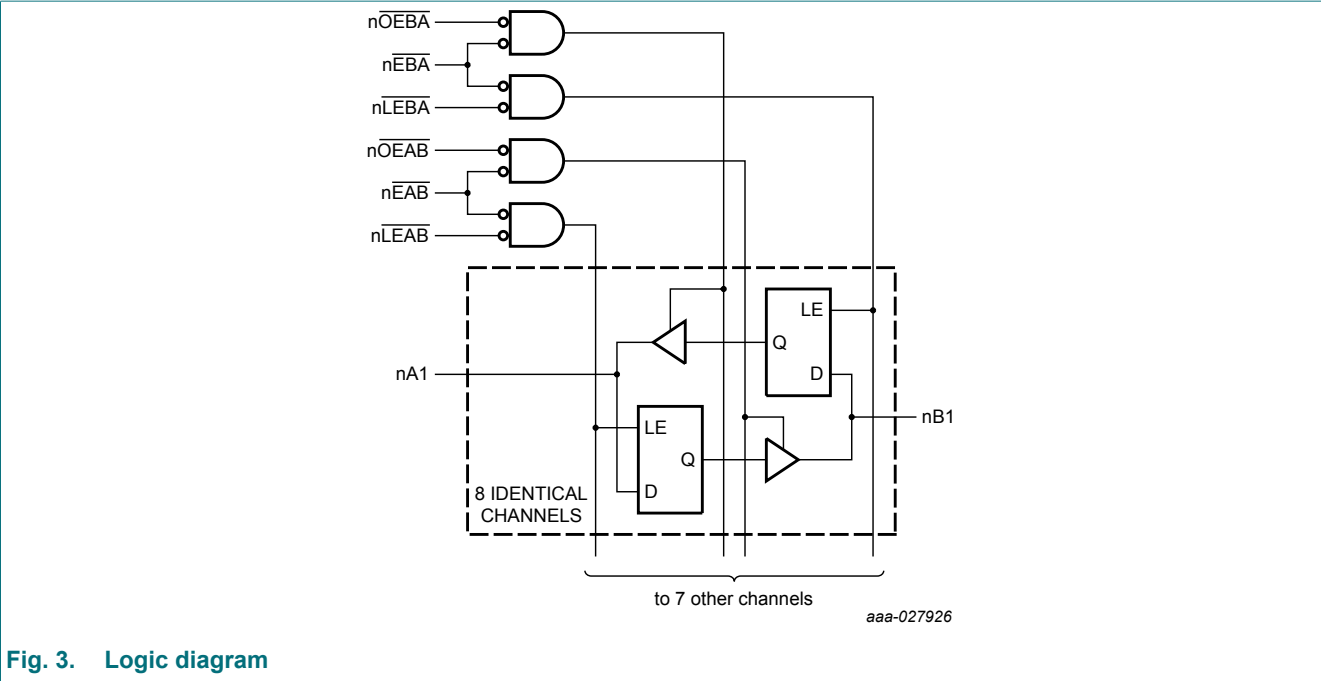


Fig. 3. Logic diagram

5. Pinning information

5.1. Pinning

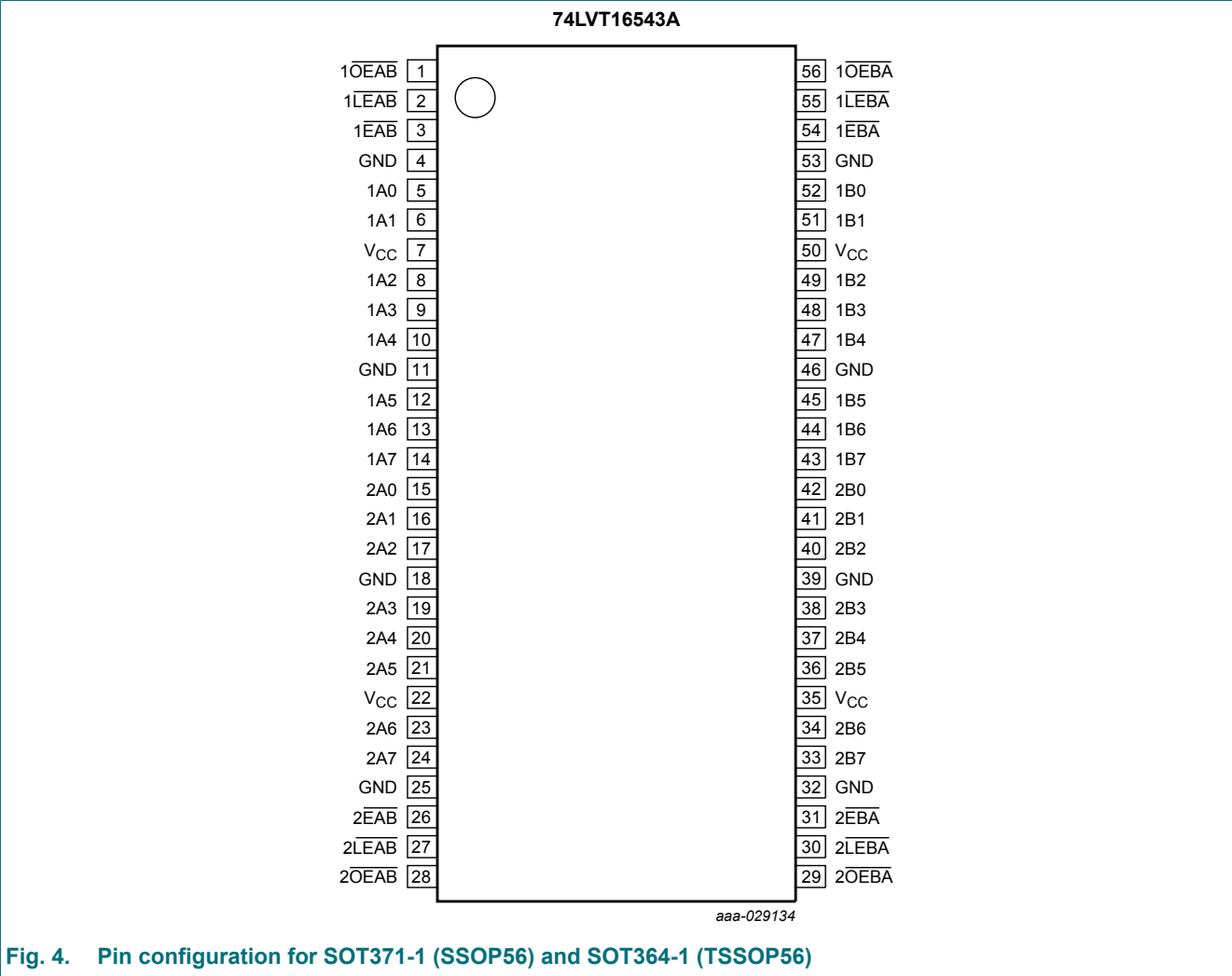


Fig. 4. Pin configuration for SOT371-1 (SSOP56) and SOT364-1 (TSSOP56)

## 5.2. Pin description

Table 2. Pin description

| Symbol                                 | Pin                            | Description                                       |
|----------------------------------------|--------------------------------|---------------------------------------------------|
| 1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7 | 5, 6, 8, 9, 10, 12, 13, 14     | data inputs/outputs                               |
| 2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7 | 15, 16, 17, 19, 20, 21, 23, 24 | data inputs/outputs                               |
| 1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7 | 52, 51, 49, 48, 47, 45, 44, 43 | data inputs/outputs                               |
| 2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7 | 42, 41, 40, 38, 37, 36, 34, 33 | data inputs/outputs                               |
| 1OEAB, 1OEBA, 2OEAB, 2OEBA             | 1, 56, 28, 29                  | A to B / B to A output enable inputs (active LOW) |
| 1EAB, 1EBA, 2EAB, 2EBA                 | 3, 54, 26, 31                  | A to B / B to A enable inputs (active LOW)        |
| 1LEAB, 1LEBA, 2LEAB, 2LEBA             | 2, 55, 27, 30                  | A to B / B to A latch enable inputs (active LOW)  |
| GND                                    | 4, 11, 18, 25, 32, 39, 46, 53  | ground (0 V)                                      |
| V <sub>CC</sub>                        | 7, 22, 35, 50                  | supply voltage                                    |

## 6. Functional description

Table 3. Function selection [1]

| Inputs         |              |                |            | Outputs    | Status           |
|----------------|--------------|----------------|------------|------------|------------------|
| nOEAB or nOEBA | nEAB or nEBA | nLEAB or nLEBA | nAn or nBn | nBn or nAn |                  |
| H              | X            | X              | X          | Z          | Disabled         |
| X              | H            | X              | X          | Z          | Disabled         |
| L              | ↑            | L              | h          | Z          | Disabled + Latch |
| L              | ↑            | L              | l          | Z          | Disabled + Latch |
| L              | L            | ↑              | h          | H          | Latch + Display  |
| L              | L            | ↑              | l          | L          | Latch + Display  |
| L              | L            | L              | H          | H          | Transparent      |
| L              | L            | L              | L          | L          | Transparent      |
| L              | L            | H              | X          | NC         | Hold             |

- [1] H = HIGH voltage level;  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH transition of nLEAB, nLEBA, nEAB and nEBA;  
L = LOW voltage level;  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH transition of nLEAB, nLEBA, nEAB and nEBA;  
X = don't care;  
↑ = LOW-to-HIGH transition of nLEAB, nLEBA, nEAB or nEBA;  
NC = no change;  
Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol    | Parameter               | Conditions                      | Min  | Max  | Unit |
|-----------|-------------------------|---------------------------------|------|------|------|
| $V_{CC}$  | supply voltage          |                                 | -0.5 | +4.6 | V    |
| $V_I$     | input voltage           | [1]                             | -0.5 | +7.0 | V    |
| $V_O$     | output voltage          | output in OFF or HIGH state [1] | -0.5 | +7.0 | V    |
| $I_{IK}$  | input clamping current  | $V_I < 0$                       | -50  | -    | mA   |
| $I_{OK}$  | output clamping current | $V_O < 0$                       | -50  | -    | mA   |
| $I_O$     | output current          | output in LOW state             | -    | 128  | mA   |
|           |                         | output in HIGH state            | -64  | -    | mA   |
| $T_{stg}$ | storage temperature     |                                 | -65  | +150 | °C   |
| $T_j$     | junction temperature    | [2]                             | -    | +150 | °C   |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol              | Parameter                           | Conditions      | Min | Max | Unit |
|---------------------|-------------------------------------|-----------------|-----|-----|------|
| $V_{CC}$            | supply voltage                      |                 | 2.7 | 3.6 | V    |
| $V_I$               | input voltage                       |                 | 0   | 5.5 | V    |
| $T_{amb}$           | ambient temperature                 | in free air     | -40 | +85 | °C   |
| $\Delta t/\Delta V$ | input transition rise and fall rate | outputs enabled | -   | 10  | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol   | Parameter                 | Conditions                                                                   | Min            | Typ [1]  | Max  | Unit |
|----------|---------------------------|------------------------------------------------------------------------------|----------------|----------|------|------|
| $V_{IK}$ | input clamping voltage    | $V_{CC} = 2.7\text{ V}$ ; $I_{IK} = -18\text{ mA}$                           | -              | -0.85    | -1.2 | V    |
| $V_{IH}$ | HIGH-level input voltage  |                                                                              | 2.0            | -        | -    | V    |
| $V_{IL}$ | LOW-level input voltage   |                                                                              | -              | -        | 0.8  | V    |
| $V_{OH}$ | HIGH-level output voltage | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ; $I_{OH} = -100\text{ }\mu\text{A}$ | $V_{CC} - 0.2$ | $V_{CC}$ | -    | V    |
|          |                           | $V_{CC} = 2.7\text{ V}$ ; $I_{OH} = -8\text{ mA}$                            | 2.4            | 2.54     | -    | V    |
|          |                           | $V_{CC} = 3.0\text{ V}$ ; $I_{OH} = -32\text{ mA}$                           | 2.0            | 2.36     | -    | V    |
| $V_{OL}$ | LOW-level output voltage  | $V_{CC} = 2.7\text{ V}$ ; $I_{OL} = 100\text{ }\mu\text{A}$                  | -              | 0.07     | 0.2  | V    |
|          |                           | $V_{CC} = 2.7\text{ V}$ ; $I_{OL} = 24\text{ mA}$                            | -              | 0.3      | 0.5  | V    |
|          |                           | $V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 16\text{ mA}$                            | -              | 0.2      | 0.4  | V    |
|          |                           | $V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 32\text{ mA}$                            | -              | 0.3      | 0.5  | V    |
|          |                           | $V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 64\text{ mA}$                            | -              | 0.35     | 0.55 | V    |
| $I_{OH}$ | HIGH-level output current |                                                                              | -              | -        | -32  | mA   |

## 3.3 V 16-bit registered transceiver; 3-state

| Symbol          | Parameter                          | Conditions                                                                                                     | Min | Typ [1] | Max       | Unit    |
|-----------------|------------------------------------|----------------------------------------------------------------------------------------------------------------|-----|---------|-----------|---------|
| $I_{OL}$        | LOW-level output current           |                                                                                                                | -   | -       | 32        | mA      |
|                 |                                    | current duty cycle $\leq 50\%$ ; $f_i \geq 1$ kHz                                                              | -   | -       | 64        | mA      |
| $V_{OL(pu)}$    | power-up LOW-level output voltage  | $V_{CC} = 3.6$ V; $I_O = 1$ mA; $V_I = V_{CC}$ or GND [2]                                                      | -   | 0.13    | 0.55      | V       |
| $I_I$           | input leakage current              | control pins                                                                                                   |     |         |           |         |
|                 |                                    | $V_{CC} = 0$ V or 3.6 V; $V_I = 5.5$ V                                                                         | -   | 0.1     | 10        | $\mu$ A |
|                 |                                    | $V_{CC} = 3.6$ V; $V_I = V_{CC}$ or GND                                                                        | -   | 0.1     | $\pm 1$   | $\mu$ A |
|                 |                                    | I/O data pins [3]                                                                                              |     |         |           |         |
|                 |                                    | $V_{CC} = 3.6$ V; $V_I = 5.5$ V                                                                                | -   | 0.5     | 20        | $\mu$ A |
|                 |                                    | $V_{CC} = 3.6$ V; $V_I = V_{CC}$                                                                               | -   | 0.5     | 10        | $\mu$ A |
|                 |                                    | $V_{CC} = 3.6$ V; $V_I = 0$ V                                                                                  | -   | 1       | -5        | $\mu$ A |
| $I_{OFF}$       | power-off leakage current          | $V_{CC} = 0$ V; $V_I$ or $V_O = 0$ V to 4.5 V                                                                  | -   | 1       | $\pm 100$ | $\mu$ A |
| $I_{BHL}$       | bus hold LOW current               | $V_{CC} = 3.0$ V; $V_I = 0.8$ V                                                                                | 75  | 130     | -         | $\mu$ A |
| $I_{BHH}$       | bus hold HIGH current              | $V_{CC} = 3.0$ V; $V_I = 2.0$ V                                                                                | -75 | -140    | -         | $\mu$ A |
| $I_{BHLO}$      | bus hold LOW overdrive current     | $V_{CC} = 3.6$ V; $V_I = 0$ V to 3.6 V [4]                                                                     | 500 | -       | -         | $\mu$ A |
| $I_{BHHO}$      | bus hold HIGH overdrive current    | $V_{CC} = 3.6$ V; $V_I = 0$ V to 3.6 V [4]                                                                     | -   | -       | -500      | $\mu$ A |
| $I_{CEX}$       | output high leakage current        | output in HIGH-state when $V_O > V_{CC}$ ; $V_O = 5.5$ V; $V_{CC} = 3.0$ V                                     | -   | 45      | 125       | $\mu$ A |
| $I_{O(pu/pd)}$  | power-up/power-down output current | $V_{CC} \leq 1.2$ V; $V_O = 0.5$ V to $V_{CC}$ ; $V_I = \text{GND or } V_{CC}$ ; $nOE = \text{don't care}$ [5] | -   | 35      | $\pm 100$ | $\mu$ A |
| $I_{CC}$        | supply current                     | $V_{CC} = 3.6$ V; $V_I = V_{CC}$ or GND; $I_O = 0$ A                                                           |     |         |           |         |
|                 |                                    | outputs HIGH                                                                                                   | -   | 0.07    | 0.12      | mA      |
|                 |                                    | outputs LOW                                                                                                    | -   | 4.5     | 6         | mA      |
|                 |                                    | outputs disabled [6]                                                                                           | -   | 0.07    | 0.12      | mA      |
| $\Delta I_{CC}$ | additional supply current          | per input pin; $V_{CC} = 3.0$ V to 3.6 V; one input = $V_{CC} - 0.6$ V; other inputs at $V_{CC}$ or GND [7]    | -   | 0.1     | 0.2       | mA      |
| $C_I$           | input capacitance                  | at control pins; $V_I = 0$ V or 3.0 V                                                                          | -   | 3       | -         | pF      |
| $C_{I/O}$       | input/output capacitance           | at input/output data pins, outputs disabled; $V_{I/O} = 0$ V or 3.0 V                                          | -   | 9       | -         | pF      |

[1] All typical values are measured at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C.

[2] For valid test results, data must not be loaded into the latches after applying power.

[3] Unused pins at  $V_{CC}$  or GND.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This parameter is valid for any  $V_{CC}$  between 0 V and 1.2 V with a transition time of up to 10 ms.

From  $V_{CC} = 1.2$  V to  $V_{CC} = 3.0$  V to 3.6 V a transition time of 100  $\mu$ s is permitted. This parameter is valid for  $T_{amb} = +25$  °C only.

[6]  $I_{CC}$  with the outputs disabled is measured with outputs pulled to  $V_{CC}$  or GND.

[7] This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 9.

| Symbol      | Parameter                           | Conditions                                 | Min | Typ [1] | Max | Unit |
|-------------|-------------------------------------|--------------------------------------------|-----|---------|-----|------|
| $t_{pd}$    | propagation delay                   | nAn to nBn or nBn to nAn; see Fig. 5 [2]   |     |         |     |      |
|             |                                     | $V_{CC} = 2.7\text{ V}$                    | -   | -       | 4.4 | ns   |
|             |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$   | 1.0 | 2.2     | 3.7 | ns   |
| $t_{pd}$    | propagation delay                   | nLEBA to nAn, nLEAB to nBn; see Fig. 6 [2] |     |         |     |      |
|             |                                     | $V_{CC} = 2.7\text{ V}$                    | -   | -       | 6.2 | ns   |
|             |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$   | 1.5 | 2.7     | 4.8 | ns   |
| $t_{PZH}$   | OFF-state to HIGH propagation delay | nOEBA to nAn, nOEAB to nBn; see Fig. 7     |     |         |     |      |
|             |                                     | $V_{CC} = 2.7\text{ V}$                    | -   | -       | 6.1 | ns   |
|             |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$   | 1.5 | 2.8     | 4.6 | ns   |
| $t_{PZL}$   | OFF-state to LOW propagation delay  | nOEBA to nAn, nOEAB to nBn; see Fig. 7     |     |         |     |      |
|             |                                     | $V_{CC} = 2.7\text{ V}$                    | -   | -       | 6.6 | ns   |
|             |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$   | 1.5 | 2.6     | 5.0 | ns   |
| $t_{PHZ}$   | HIGH to OFF-state propagation delay | nOEBA to nAn, nOEAB to nBn; see Fig. 7     |     |         |     |      |
|             |                                     | $V_{CC} = 2.7\text{ V}$                    | -   | -       | 5.7 | ns   |
|             |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$   | 2.0 | 3.1     | 5.2 | ns   |
| $t_{PLZ}$   | LOW to OFF-state propagation delay  | nOEBA to nAn, nOEAB to nBn; see Fig. 7     |     |         |     |      |
|             |                                     | $V_{CC} = 2.7\text{ V}$                    | -   | -       | 4.7 | ns   |
|             |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$   | 2.0 | 3.2     | 4.6 | ns   |
| $t_{PZH}$   | OFF-state to HIGH propagation delay | nEBA to nAn, nEAB to nBn; see Fig. 7       |     |         |     |      |
|             |                                     | $V_{CC} = 2.7\text{ V}$                    | -   | -       | 6.1 | ns   |
|             |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$   | 1.5 | 2.9     | 4.8 | ns   |
| $t_{PZL}$   | OFF-state to LOW propagation delay  | nEBA to nAn, nEAB to nBn; see Fig. 7       |     |         |     |      |
|             |                                     | $V_{CC} = 2.7\text{ V}$                    | -   | -       | 6.6 | ns   |
|             |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$   | 1.5 | 2.6     | 5.1 | ns   |
| $t_{PHZ}$   | HIGH to OFF-state propagation delay | nEBA to nAn, nEAB to nBn; see Fig. 7       |     |         |     |      |
|             |                                     | $V_{CC} = 2.7\text{ V}$                    | -   | -       | 5.7 | ns   |
|             |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$   | 2.0 | 3.1     | 5.1 | ns   |
| $t_{PLZ}$   | LOW to OFF-state propagation delay  | nEBA to nAn, nEAB to nBn; see Fig. 7       |     |         |     |      |
|             |                                     | $V_{CC} = 2.7\text{ V}$                    | -   | -       | 4.5 | ns   |
|             |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$   | 2.0 | 3.2     | 4.3 | ns   |
| $t_{su(H)}$ | set-up time HIGH                    | nAn to nLEAB, nBn to nLEBA; see Fig. 8     |     |         |     |      |
|             |                                     | $V_{CC} = 2.7\text{ V}$                    | 0.5 | -       | -   | ns   |
|             |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$   | 0.8 | 0.4     | -   | ns   |
| $t_{su(L)}$ | set-up time LOW                     | nAn to nLEAB, nBn to nLEBA; see Fig. 8     |     |         |     |      |
|             |                                     | $V_{CC} = 2.7\text{ V}$                    | 1.5 | -       | -   | ns   |
|             |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$   | 1.0 | 0.1     | -   | ns   |
| $t_{h(H)}$  | hold time HIGH                      | nAn to nLEAB, nBn to nLEBA; see Fig. 8     |     |         |     |      |
|             |                                     | $V_{CC} = 2.7\text{ V}$                    | 0.5 | -       | -   | ns   |
|             |                                     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$   | 1.0 | 0.2     | -   | ns   |

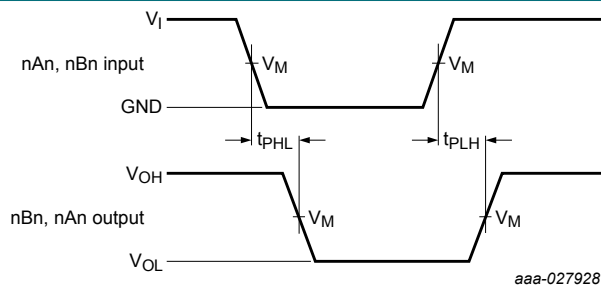


| Symbol      | Parameter        | Conditions                                 | Min | Typ [1] | Max | Unit |
|-------------|------------------|--------------------------------------------|-----|---------|-----|------|
| $t_{h(L)}$  | hold time LOW    | nAn to nLEAB, nBn to nLEBA; see Fig. 8     |     |         |     |      |
|             |                  | $V_{CC} = 2.7 \text{ V}$                   | 1.3 | -       | -   | ns   |
|             |                  | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 1.2 | 0.4     | -   | ns   |
| $t_{su(H)}$ | set-up time HIGH | nAn to nEAB, nBn to nEBA; see Fig. 8       |     |         |     |      |
|             |                  | $V_{CC} = 2.7 \text{ V}$                   | 0.4 | -       | -   | ns   |
|             |                  | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 0.7 | 0.1     | -   | ns   |
| $t_{su(L)}$ | set-up time LOW  | nAn to nEAB, nBn to nEBA; see Fig. 8       |     |         |     |      |
|             |                  | $V_{CC} = 2.7 \text{ V}$                   | 1.5 | -       | -   | ns   |
|             |                  | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 1.3 | 0.1     | -   | ns   |
| $t_{h(H)}$  | hold time HIGH   | nAn to nEAB, nBn to nEBA; see Fig. 8       |     |         |     |      |
|             |                  | $V_{CC} = 2.7 \text{ V}$                   | 0.8 | -       | -   | ns   |
|             |                  | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 1.2 | 0.2     | -   | ns   |
| $t_{h(L)}$  | hold time LOW    | nAn to nEAB, nBn to nEBA; see Fig. 8       |     |         |     |      |
|             |                  | $V_{CC} = 2.7 \text{ V}$                   | 1.4 | -       | -   | ns   |
|             |                  | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 1.3 | 0.4     | -   | ns   |
| $t_{WL}$    | pulse width LOW  | nLEAB and nLEBA; see Fig. 6                |     |         |     |      |
|             |                  | $V_{CC} = 2.7 \text{ V}$                   | 1.8 | -       | -   | ns   |
|             |                  | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 1.8 | 1.0     | -   | ns   |

[1] Typical values are measured at  $T_{amb} = 25^\circ\text{C}$  and  $V_{CC} = 3.3 \text{ V}$

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$

## 10.1. Waveforms and test circuit



See Table 8 for measurement points.

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 5. Input (nAn, nBn) to output (nBn, nAn) propagation delays**

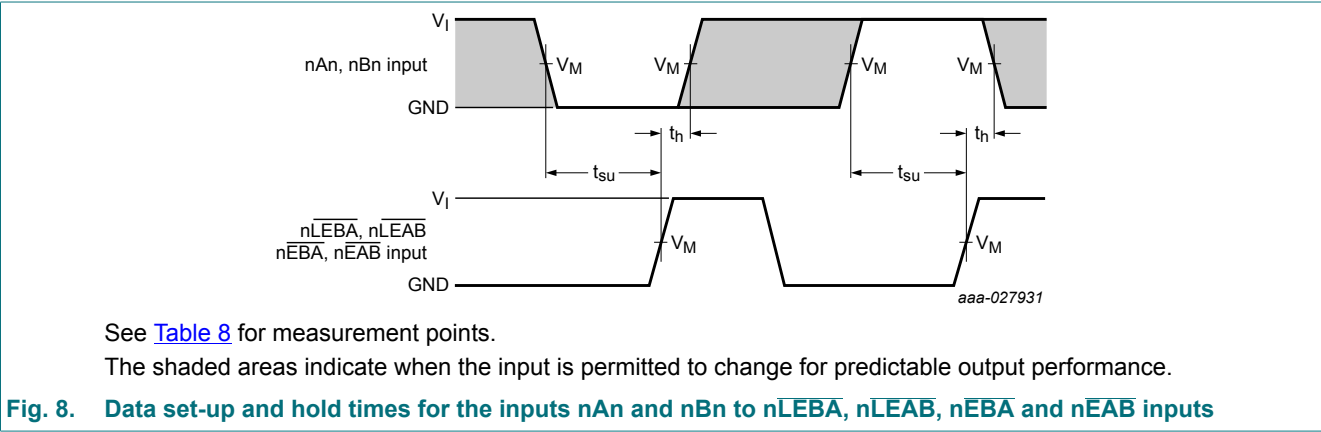
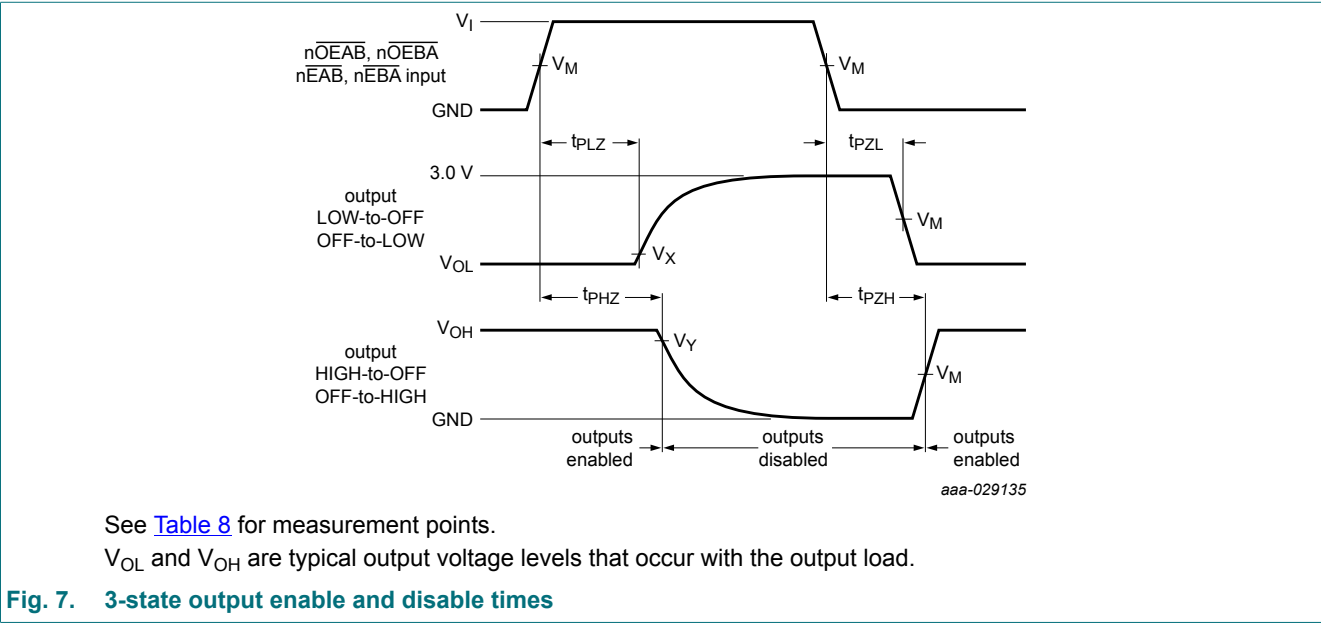
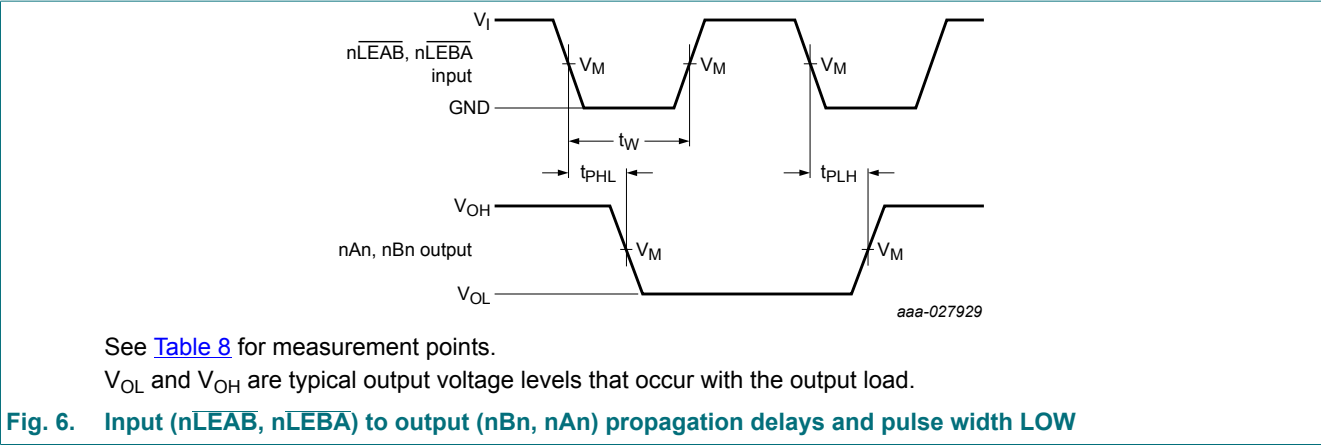
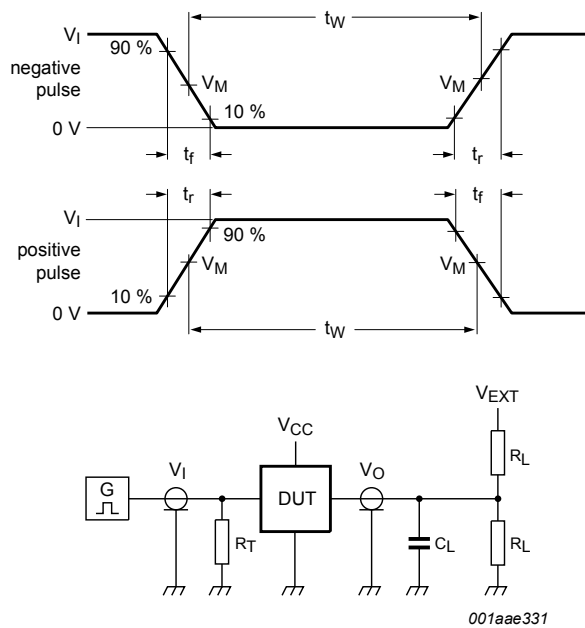


Table 8. Measurement points

| Input |       | Output |                          |                          |
|-------|-------|--------|--------------------------|--------------------------|
| $V_I$ | $V_M$ | $V_M$  | $V_x$                    | $V_y$                    |
| 2.7 V | 1.5 V | 1.5 V  | $V_{OL} + 0.3 \text{ V}$ | $V_{OH} - 0.3 \text{ V}$ |



Test data is given in [Table 9](#).  
Definitions test circuit:  
 $R_L$  = Load resistance;  
 $C_L$  = Load capacitance including jig and probe capacitance;  
 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;  
 $V_{EXT}$  = External voltage for measuring switching times.

Fig. 9. Test circuit for measuring switching times

Table 9. Test data

| Input |               |        |               | Load         |       | $V_{EXT}$          |                    |                    |
|-------|---------------|--------|---------------|--------------|-------|--------------------|--------------------|--------------------|
| $V_I$ | $f_i$         | $t_W$  | $t_r, t_f$    | $R_L$        | $C_L$ | $t_{PHZ}, t_{PZH}$ | $t_{PLZ}, t_{PZL}$ | $t_{PLH}, t_{PHL}$ |
| 2.7 V | $\leq 10$ MHz | 500 ns | $\leq 2.5$ ns | 500 $\Omega$ | 50 pF | GND                | 6 V                | open               |

11. Package outline

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

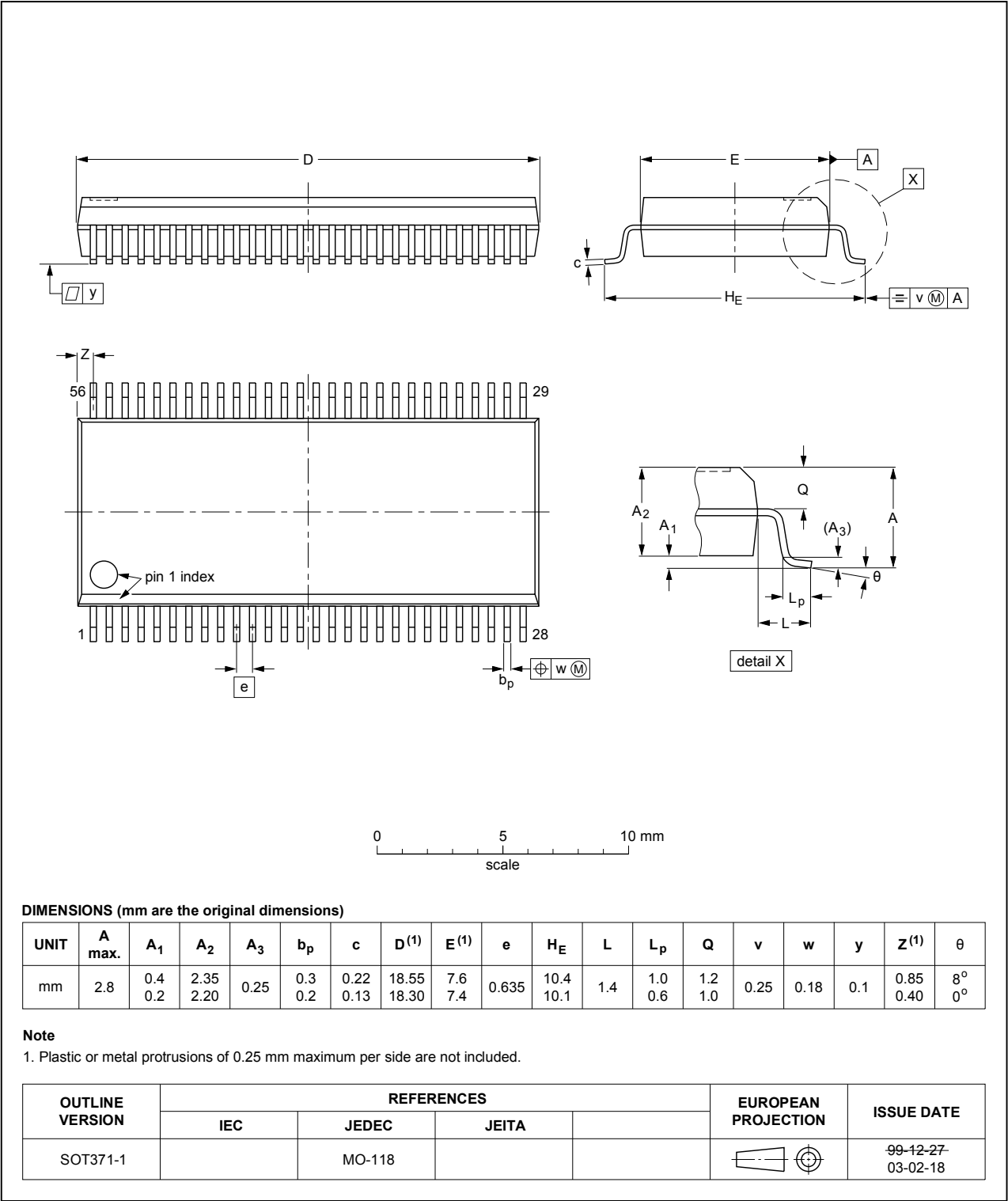


Fig. 10. Package outline SOT371-1 (SSOP56)

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

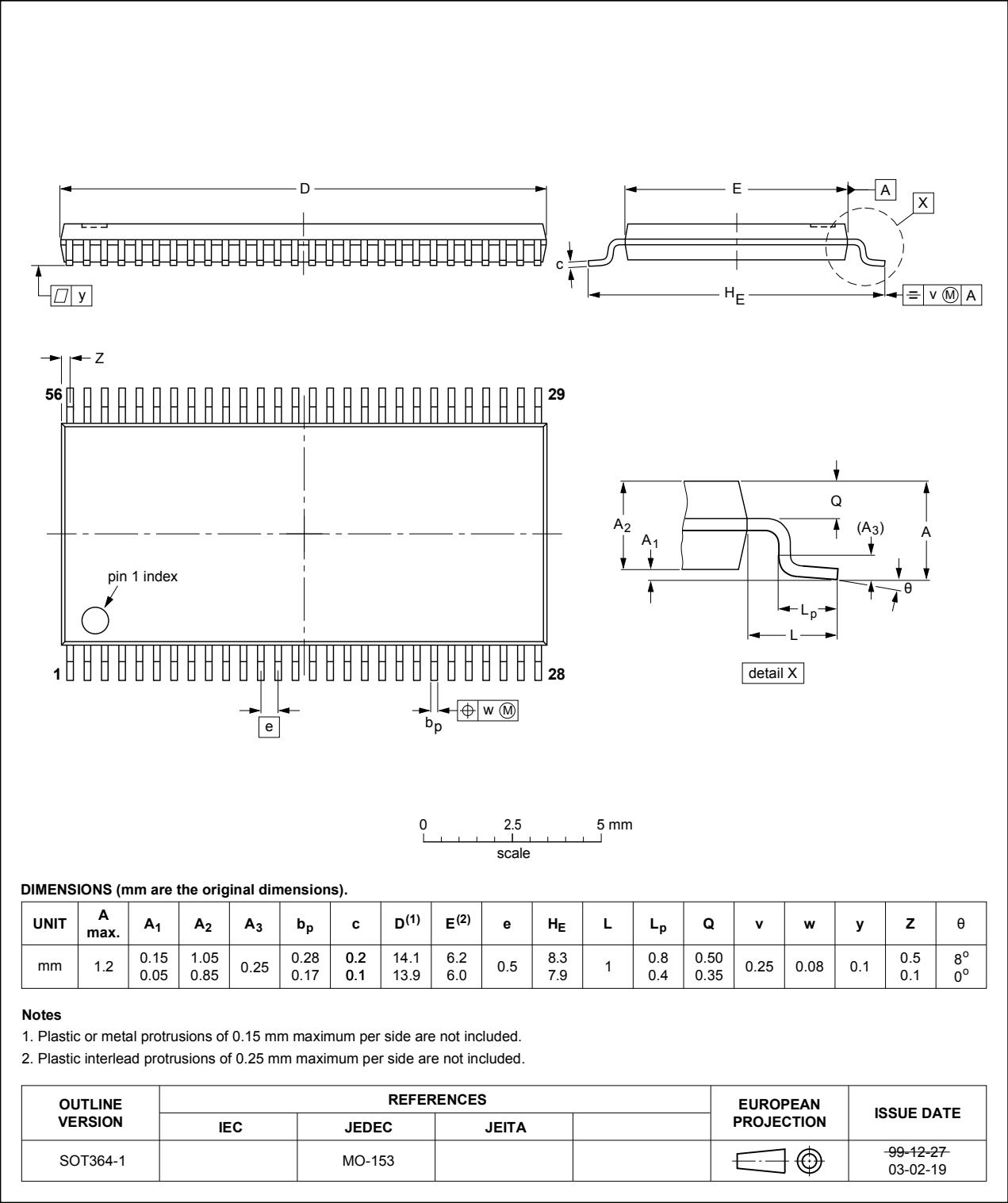


Fig. 11. Package outline SOT364-1 (TSSOP56)

## 12. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description                                     |
|---------|-------------------------------------------------|
| BiCMOS  | Bipolar Complementary Metal Oxide Semiconductor |
| DUT     | Device Under Test                               |
| ESD     | ElectroStatic Discharge                         |
| MIL     | Military                                        |
| MM      | Machine Model                                   |
| TTL     | Transistor-Transistor Logic                     |

## 13. Revision history

**Table 11. Revision history**

| Document ID     | Release date                                                                                                                                                                                                                           | Data sheet status     | Change notice | Supersedes      |
|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|---------------|-----------------|
| 74LVT16543A v.3 | 20181001                                                                                                                                                                                                                               | Product data sheet    | -             | 74LVT16543A v.2 |
| Modifications:  | <ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>Legal texts have been adapted to the new company name where appropriate.</li></ul> |                       |               |                 |
| 74LVT16543A v.2 | 19980219                                                                                                                                                                                                                               | Product specification | -             | 74LVT16543A v.1 |
| 74LVT16543A v.1 | -                                                                                                                                                                                                                                      | Product specification |               | -               |

## 14. Legal information

### Data sheet status

| Document status<br>[1][2]      | Product status [3] | Definition                                                                            |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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