

FEATURES

- 3.3 Volt power supply
- Fast 35ns read/write cycle
- SRAM compatible timing
- Unlimited read & write endurance
- Commercial, Industrial, and Extended Temperatures
- Data non-volatile for >20 years at temperature
- RoHS-compliant TSOP2 and BGA packages available

BENEFITS

- One memory replaces FLASH, SRAM, EEPROM and BBSRAM in system for simpler, more efficient designs
- Improves reliability by replacing battery-backed SRAM
- Automatic data protection on power loss

INTRODUCTION

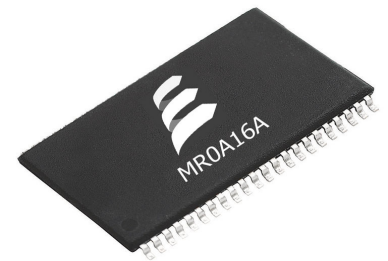
The **MR0A16A** is a 1,048,576-bit magnetoresistive random access memory (MRAM) device organized as 65,536 words of 16 bits. The **MR0A16A** offers SRAM compatible 35 ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20 years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification.

MR0A16A is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

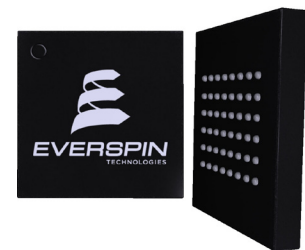
The **MR0A16B** is available in a small footprint 48-pin ball grid array (BGA) package and a 44-pin thin small outline package (TSOP Type 2). These packages are compatible with similar low-power SRAM products and other nonvolatile RAM products.

The **MR0A16A** provides highly reliable data storage over a wide range of temperatures. The product is available with commercial temperature (0 to +70 °C), industrial temperature (-40 to +85 °C), and extended temperature (-40 to +105 °C) range options.

64K x 16 MRAM Memory



44-pin TSOP2



48-ball BGA



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BLOCK DIAGRAM AND PIN ASSIGNMENTS

Figure 1 – Block Diagram

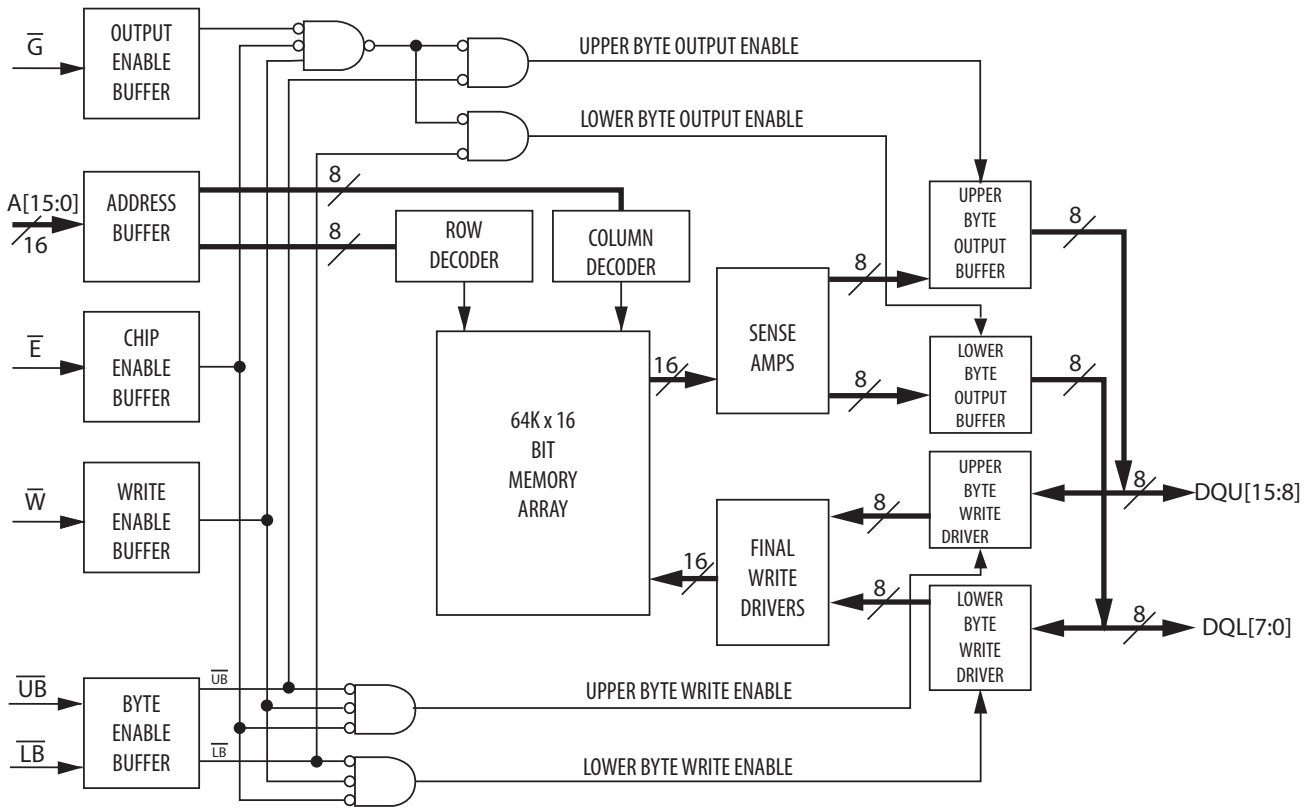


Table 1 – Pin Functions

| Signal Name | Function |
|-------------|-------------------|
| A | Address Input |
| \bar{E} | Chip Enable |
| \bar{W} | Write Enable |
| \bar{G} | Output Enable |
| \bar{UB} | Upper Byte Enable |
| \bar{LB} | Lower Byte Enable |
| DQ | Data I/O |
| V_{DD} | Power Supply |
| V_{SS} | Ground |
| DC | Do Not Connect |
| NC | No Connection |

ABSOLUTE MAXIMUM RATINGS

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, normal precautions should be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

Table 3 – Absolute Maximum Ratings ¹

| Symbol | Parameter | Temp Range | Package | Value | Unit |
|------------------------|---|----------------------|------------|-------------------------------|------|
| V _{DD} | Supply voltage ² | - | - | -0.5 to 4.0 | V |
| V _{IN} | Voltage on any pin ² | - | - | -0.5 to V _{DD} + 0.5 | V |
| I _{OUT} | Output current per pin | - | - | ±20 | mA |
| P _D | Package power dissipation ³ | - | Note 3 | 0.600 | W |
| T _{BIAS} | Temperature under bias | Commercial | - | -10 to 85 | °C |
| | | Industrial | - | -45 to 95 | |
| | | Extended | - | -45 to 110 | |
| T _{stg} | Storage Temperature | - | - | -55 to 150 | °C |
| T _{Lead} | Lead temperature during solder (3 minute max) | - | - | 260 | °C |
| H _{max_write} | Maximum magnetic field during write | Commercial | TSOP2, BGA | 2,000 | A/m |
| | | Industrial, Extended | BGA | 2,000 | |
| | | | TSOP2 | 10,000 | |
| H _{max_read} | Maximum magnetic field during read or standby | Commercial | TSOP2, BGA | 8,000 | A/m |
| | | Industrial, Extended | BGA | 8,000 | |
| | | | TSOP2 | 10,000 | |

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
2. All voltages are referenced to V_{SS}.
3. Power dissipation capability depends on package characteristics and use environment.

OPERATING CONDITIONS

Table 4 – Operating Conditions

| Symbol | Parameter | Temp Range | Min | Typical | Max | Unit |
|----------|-----------------------------------|------------|-------------------|---------|-----------------------------|------|
| V_{DD} | Power supply voltage ¹ | All | 3.0 | 3.3 | 3.6 | V |
| V_{WI} | Write inhibit voltage | All | 2.5 | 2.7 | 3.0 ¹ | V |
| V_{IH} | Input high voltage | All | 2.2 | - | $V_{DD} + 0.3$ ² | V |
| V_{IL} | Input low voltage | All | -0.5 ³ | - | 0.8 | V |
| T_A | Ambient Temperature under bias | Commercial | 0 | | 70 | °C |
| | | Industrial | -40 | | 85 | |
| | | Extended | -40 | | 105 | |

Notes:

1. There is a 2 ms startup time once V_{DD} exceeds $V_{DD, (min)}$. See **Power Up and Power Down Sequencing** below.
2. $V_{IH(max)} = V_{DD} + 0.3 V_{DC}$; $V_{IH(max)} = V_{DD} + 2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.
3. $V_{IL(min)} = -0.5 V_{DC}$; $V_{IL(min)} = -2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.

Power Up and Power Down Sequencing

The MRAM is protected from write operations whenever V_{DD} is less than V_{WI} . As soon as V_{DD} exceeds $V_{DD(min)}$, there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The \bar{E} and \bar{W} control signals should track V_{DD} on power up to $V_{DD} - 0.2\text{ V}$ or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives \bar{E} and \bar{W} should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where V_{DD} goes below V_{WI} , writes are protected and a startup time must be observed when power returns above $V_{DD(min)}$.

Figure 3 – Power Up and Power Down Timing

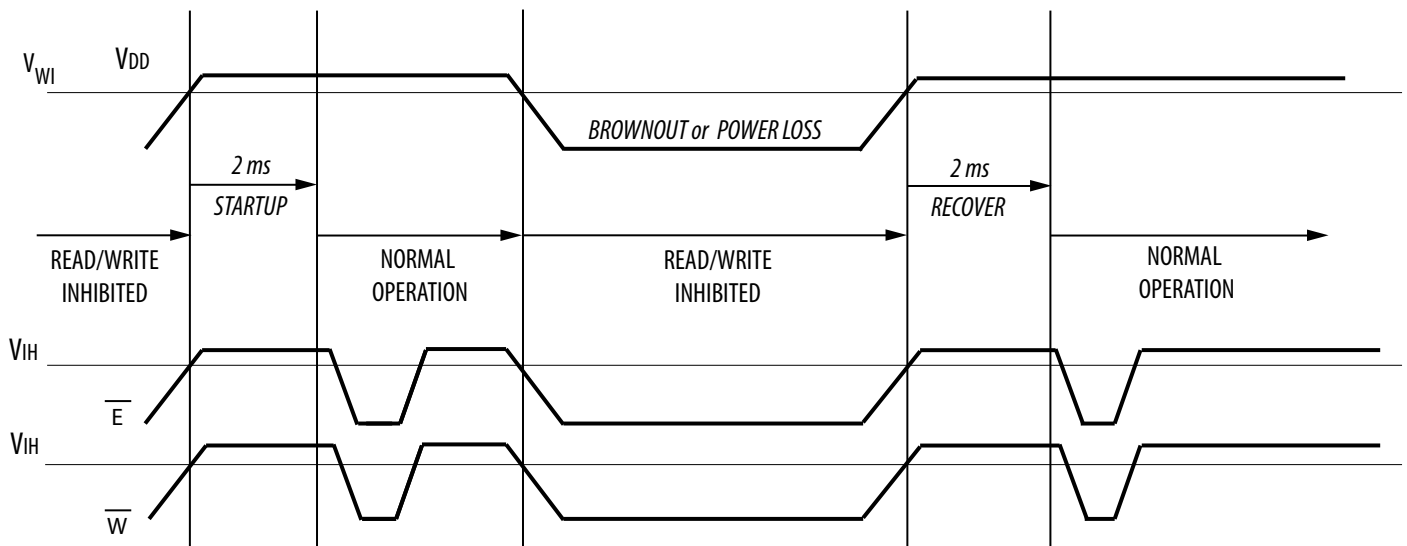


Table 5 – DC Characteristics

| Symbol | Parameter | Condition | Min | Max | Unit |
|--------------|------------------------|--------------------------|----------------|----------------|---------|
| $I_{Ikg(I)}$ | Input leakage current | All | - | ± 1 | μA |
| $I_{Ikg(O)}$ | Output leakage current | All | - | ± 1 | μA |
| V_{OL} | Output low voltage | $I_{OL} = +4 \text{ mA}$ | - | 0.4 | V |
| | | $I_{OL} = +100 \mu A$ | | $V_{SS} + 0.2$ | |
| V_{OH} | Output high voltage | $I_{OH} = -4 \text{ mA}$ | 2.4 | - | V |
| | | $I_{OH} = -100 \mu A$ | $V_{DD} - 0.2$ | | |

Table 6 – Power Supply Characteristics

| Symbol | Parameter | Condition | Temp Range | Typical | Max | Unit |
|-----------|---|---|-----------------|---------|-----|------|
| I_{DDR} | AC active supply current - read modes ¹ | $I_{OUT} = 0 \text{ mA}, V_{DD} = \text{max}$ | All | 55 | 80 | mA |
| I_{DDW} | AC active supply current - write modes ¹ | $V_{DD} = \text{max}$ | Commer- cial | 105 | 155 | mA |
| | | | Industrial | 105 | 165 | |
| | | | Extended | 105 | 165 | |
| I_{SB1} | AC standby current | $V_{DD} = \text{max}, E = V_{IH}$ No other restrictions on other inputs | All | 18 | 28 | mA |
| I_{SB2} | CMOS standby current | $E \geq V_{DD} - 0.2 \text{ V}$ and $V_{In} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{DD} - 0.2 \text{ V}$ $V_{DD} = \text{max}, f = 0 \text{ MHz}$ | | 9 | 12 | mA |

Notes:

1. All active current measurements are measured with one address transition per cycle and at minimum cycle time.

TIMING SPECIFICATIONS

Table 7 – Capacitance¹

| Symbol | Parameter | Typical | Max | Unit |
|-----------|---------------------------|---------|-----|------|
| C_{In} | Address input capacitance | - | 6 | pF |
| C_{In} | Control input capacitance | - | 6 | pF |
| $C_{I/O}$ | Input/Output capacitance | - | 8 | pF |

Notes:

- $f = 1.0 \text{ MHz}$, $dV = 3.0 \text{ V}$, $T_A = 25 \text{ }^\circ\text{C}$, periodically sampled rather than 100% tested.

Table 8 – AC Measurement Conditions

| Parameter | Value | Unit |
|---|--------------|------|
| Logic input timing measurement reference level | 1.5 | V |
| Logic output timing measurement reference level | 1.5 | V |
| Logic input pulse levels | 0 or 3.0 | V |
| Input rise/fall time | 2 | ns |
| Output load for low and high impedance parameters | See Figure 4 | |
| Output load for all other timing parameters | See Figure 5 | |

Figure 4 – Output Load Test Low and High

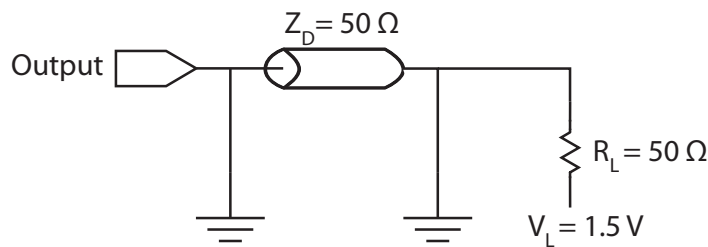


Figure 5 – Output Load Test All Others

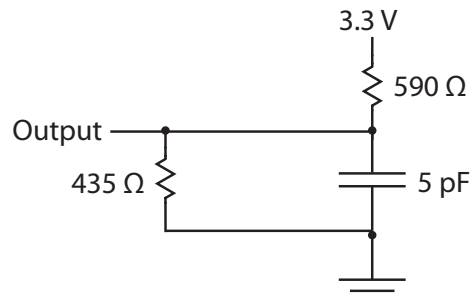


Table 9 – Read Cycle Timing¹

| Symbol | Parameter | Min | Max | Unit |
|-------------------|---|-----|-----|------|
| t _{AVAV} | Read cycle time | 35 | - | ns |
| t _{AVQV} | Address access time | - | 35 | ns |
| t _{ELQV} | Enable access time ² | - | 35 | ns |
| t _{GLQV} | Output enable access time | - | 15 | ns |
| t _{BLQV} | Byte enable access time | - | 15 | ns |
| t _{AXQX} | Output hold from address change | 3 | - | ns |
| t _{ELQX} | Enable low to output active ³ | 3 | - | ns |
| t _{GLQX} | Output enable low to output active ³ | 0 | - | ns |
| t _{BLQX} | Byte enable low to output active ³ | 0 | - | ns |
| t _{EHQZ} | Enable high to output Hi-Z ³ | 0 | 15 | ns |
| t _{GHQZ} | Output enable high to output Hi-Z ³ | 0 | 10 | ns |
| t _{BHQZ} | Byte high to output Hi-Z ³ | 0 | 10 | ns |

Notes:

1. W is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.
2. Addresses valid before or at the same time E goes low.
3. This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage.

Table 10 – Write Cycle Timing 1 (\overline{W} Controlled) ¹

| Symbol | Parameter | Min | Max | Unit |
|--------------------------|--|-----|-----|------|
| t_{AVAV} | Write cycle time ² | 35 | - | ns |
| t_{AVWL} | Address set-up time | 0 | - | ns |
| t_{AVWH} | Address valid to end of write (G high) | 18 | - | ns |
| t_{AVWL} | Address valid to end of write (G low) | 20 | - | ns |
| t_{WLWH} t_{WLEH} | Write pulse width (G high) | 15 | - | ns |
| t_{WLWH} t_{WLEH} | Write pulse width (G low) | 15 | - | ns |
| t_{DVWH} | Data valid to end of write | 10 | - | ns |
| t_{WHDX} | Data hold time | 0 | - | ns |
| t_{WLQZ} | Write low to data Hi-Z ³ | 0 | 12 | ns |
| t_{WHQX} | Write high to output active ³ | 3 | - | ns |
| t_{WHAX} | Write recovery time | 12 | - | ns |

Notes:

1. All write occurs during the overlap of \overline{E} low and \overline{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \overline{G} goes low at the same time or after \overline{W} goes low, the output will remain in a high impedance state. After \overline{W} or \overline{E} has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between \overline{E} being asserted low in one cycle to \overline{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage. At any given voltage or temperature, $t_{WLQZ}(\max) < t_{WHQX}(\min)$

Figure 8 – Write Cycle Timing 1 (\overline{W} Controlled)

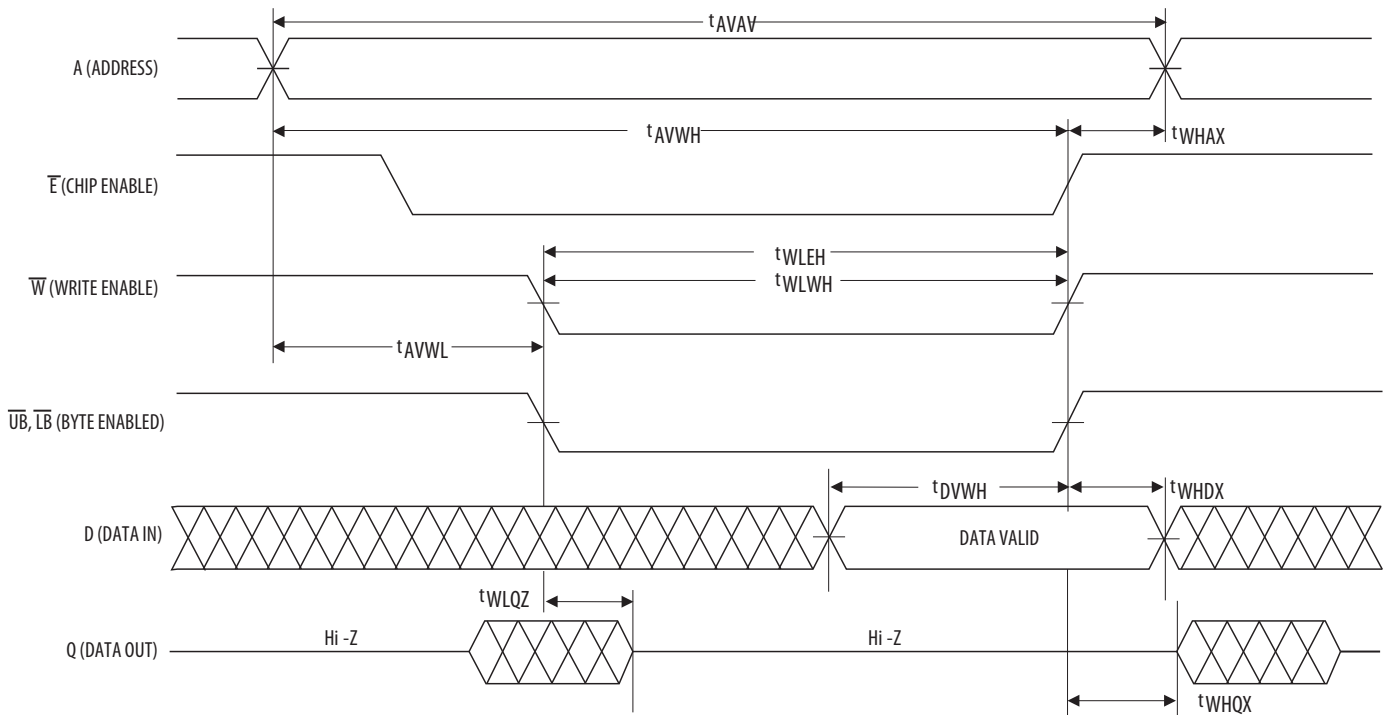


Table 11 – Write Cycle Timing 2 (E Controlled)¹

| Symbol | Parameter | Min | Max | Unit |
|--------------------------|---|-----|-----|------|
| t_{AVAV} | Write cycle time ² | 35 | - | ns |
| t_{AVEL} | Address set-up time | 0 | - | ns |
| t_{AVEH} | Address valid to end of write (G high) | 18 | - | ns |
| t_{AVEH} | Address valid to end of write (G low) | 20 | - | ns |
| t_{ELEH} t_{ELWH} | Enable to end of write (G high) | 15 | - | ns |
| t_{ELEH} t_{ELWH} | Enable to end of write (G low) ³ | 15 | - | ns |
| t_{DVEH} | Data valid to end of write | 10 | - | ns |
| t_{EHDX} | Data hold time | 0 | - | ns |
| t_{EHAX} | Write recovery time | 12 | - | ns |

Notes:

1. All write occurs during the overlap of \bar{E} low and \bar{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \bar{G} goes low at the same time or after \bar{W} goes low, the output will remain in a high impedance state. After \bar{W} or \bar{E} has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between \bar{E} being asserted low in one cycle to \bar{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. If \bar{E} goes low at the same time or after \bar{W} goes low, the output will remain in a high-impedance state. If \bar{E} goes high at the same time or before \bar{W} goes high, the output will remain in a high-impedance state.

Figure 9 – Write Cycle Timing 2 (E Controlled)

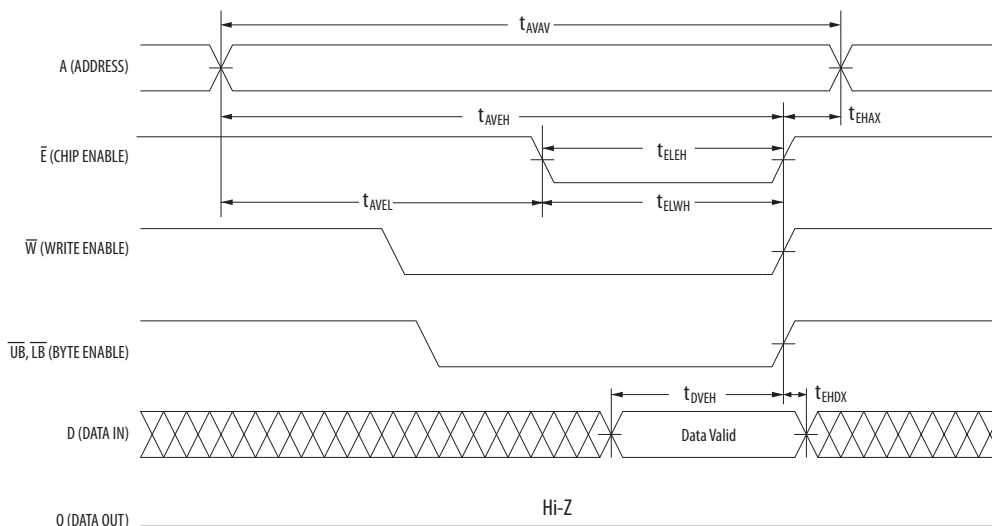


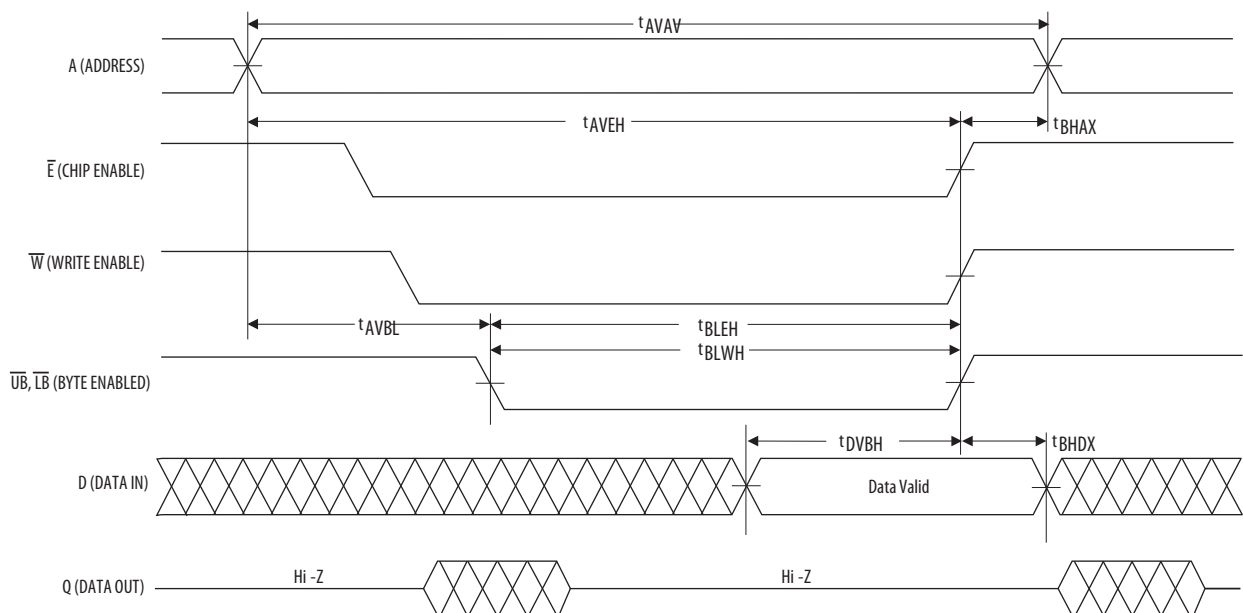
Table 12 – Write Cycle Timing 3 ($\overline{\text{LB}}/\overline{\text{UB}}$ Controlled)¹

| Symbol | Parameter | Min | Max | Unit |
|--|--|-----|-----|------|
| t_{AVAV} | Write cycle time ² | 35 | - | ns |
| t_{AVBL} | Address set-up time | 0 | - | ns |
| t_{AVBH} | Address valid to end of write (G high) | 18 | - | ns |
| | Address valid to end of write (G low) | 20 | - | ns |
| t_{BLEH} t_{BLWH} | Write pulse width (G high) | 15 | - | ns |
| t_{BLEH} t_{BLWH} | Write pulse width (G low) | 15 | - | ns |
| t_{DVBH} | Data valid to end of write | 10 | - | ns |
| t_{BHDX} | Data hold time | 0 | - | ns |
| t_{BHAX} | Write recovery time | 12 | - | ns |

Notes:

1. All write occurs during the overlap of $\overline{\text{E}}$ low and $\overline{\text{W}}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{\text{G}}$ goes low at the same time or after $\overline{\text{W}}$ goes low, the output will remain in a high impedance state. After $\overline{\text{W}}$, $\overline{\text{E}}$ or $\overline{\text{UB}}/\overline{\text{LB}}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them. The minimum time between $\overline{\text{E}}$ being asserted low in one cycle to $\overline{\text{E}}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.

Figure 10 – Write Cycle Timing 3 ($\overline{\text{UB}}/\overline{\text{LB}}$ Controlled)



ORDERING INFORMATION

Table 13 – Part Numbering System

| Product Family Number | | MR | 4 | A | 16 | B | | | | | |
|------------------------------|--------------|--------|---------|------|-----------|------|------|---------|-------|---------|-------|
| Ordering Part Number | | Memory | Density | Type | I/O Width | Rev. | Temp | Package | Speed | Packing | Grade |
| MRAM | MR | MR | 0 | A | 16 | A | C | MA | 35 | R | ES |
| 256 Kb | 256 | | | | | | | | | | |
| 1 Mb | 0 | | | | | | | | | | |
| 4 Mb | 2 | | | | | | | | | | |
| 16 Mb | 4 | | | | | | | | | | |
| Async 3.3v | A | | | | | | | | | | |
| Async 3.3v Vdd and 1.8v Vddq | D | | | | | | | | | | |
| 8-bit | 8 | | | | | | | | | | |
| 16-bit | 16 | | | | | | | | | | |
| Rev A | A | | | | | | | | | | |
| Rev B | B | | | | | | | | | | |
| Commercial | 0 to 70°C | Blank | | | | | | | | | |
| Industrial | -40 to 85°C | C | | | | | | | | | |
| Extended | -40 to 105°C | V | | | | | | | | | |
| AEC Q-100 Grade 1 | -40 to 125°C | M | | | | | | | | | |
| 44-TSOP-2 | YS | | | | | | | | | | |
| 48-FBGA | MA | | | | | | | | | | |
| 32-SOIC | SO | | | | | | | | | | |
| 35 ns | 35 | | | | | | | | | | |
| 45 ns | 45 | | | | | | | | | | |
| Tray | Blank | | | | | | | | | | |
| Tape and Reel | R | | | | | | | | | | |
| Engineering Samples | ES | | | | | | | | | | |
| Customer Samples | Blank | | | | | | | | | | |
| Mass Production | Blank | | | | | | | | | | |

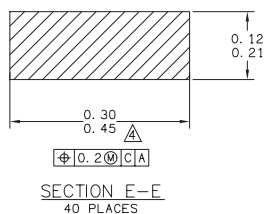
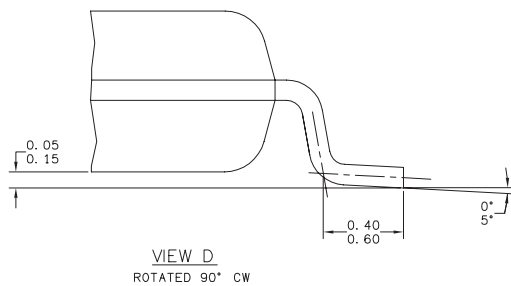
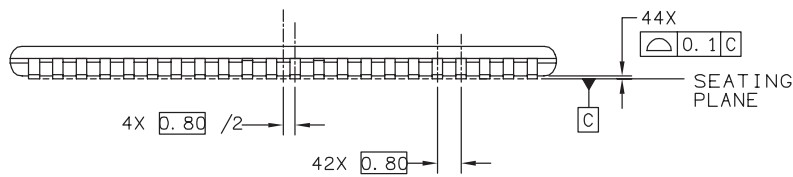
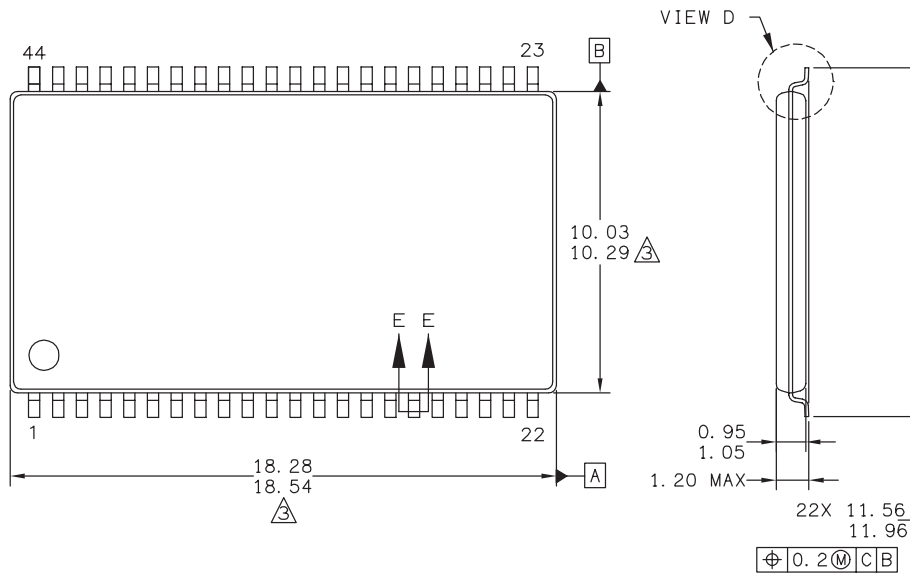
Product Family Number and Ordering Part Number given are for illustration only.

Table 14 – MR0A16A Ordering Part Numbers

| Temp Grade | Temp | Package | Shipping | Ordering Part Number |
|------------|----------------|----------|---------------|----------------------|
| Commercial | 0 to +70 °C | 44-TSOP2 | Tray | MR0A16AYS35 |
| | | | Tape and Reel | MR0A16AYS35R |
| | | 48-BGA | Tray | MR0A16AMA35 |
| | | | Tape and Reel | MR0A16AMA35R |
| Industrial | -40 to +85 °C | 44-TSOP2 | Tray | MR0A16ACYS35 |
| | | | Tape and Reel | MR0A16ACYS35R |
| | | 48-BGA | Tray | MR0A16ACMA35 |
| | | | Tape and Reel | MR0A16ACMA35R |
| Extended | -40 to +105 °C | 44-TSOP2 | Tray | MR0A16AVYS35 |
| | | | Tape and Reel | MR0A16AVYS35R |
| | | 48-BGA | Tray | MR0A16AVMA35 |
| | | | Tape and Reel | MR0A16AVMA35R |

PACKAGE OUTLINE DRAWINGS

Figure 11 – 44-pin TSOP2



Notes:

1. Dimensions and tolerances per ASME Y14.5M - 1994.
2. Dimensions in Millimeters.
3. Dimensions do not include mold protrusion.
4. Dimension does not include DAM bar protrusions.
5. DAM Bar protrusion shall not cause the lead width to exceed 0.58.

REVISION HISTORY

| Revision | Date | Description of Change |
|----------|----------------|--|
| 0 | Jun 18, 2007 | Initial Advanced Information Release |
| 1 | Sept 21, 2007 | Table 6, Applied Values to TBD's in IDD Specifications |
| 2 | Nov 12, 2007 | Table 2, Changed IDDA to IDDR or IDDW |
| 3 | Sep 12, 2008 | Reformat Datasheet for EverSpin, Add BGA Packaging Information, Add Tape & Reel Part Numbers, Add Power Sequencing Info, Correct IOH spec of VOH to -100 uA, Correct ac Test Conditions. |
| 4 | Feb 28, 2011 | Add TSOPII Lead Cross-Section, Add Production Note. Converted to new document format. |
| 5 | Dec 9, 2011 | Figure 2.1 cosmetic update. Figure 5.2 BGA package outline drawing revised for ball size. Updated logo and contact information. |
| 6 | August 6, 2012 | Revised Table 1 and Figure 1 to be correct for x16 device. Revised magnetic immunity ratings for TSOP2 Industrial Grade. Revised figure 3. Complete document reformat and restructure. |

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