

Data Sheet

ADG772

FEATURES

- USB 2.0 (480 Mbps) and USB 1.1 (12 Mbps) signal switching compliant**
- Tiny 10-lead 1.3 mm × 1.6 mm mini LFCSP package and 12-lead 3 mm × 3 mm LFCSP package**
- 2.7 V to 3.6 V single-supply operation**
- Typical power consumption: <0.1 µW**
- RoHS compliant**

APPLICATIONS

- USB 2.0 signal switching circuits**
- Cellular phones**
- PDAs**
- MP3 players**
- Battery-powered systems**
- Headphone switching**
- Audio and video signal routing**
- Communications systems**

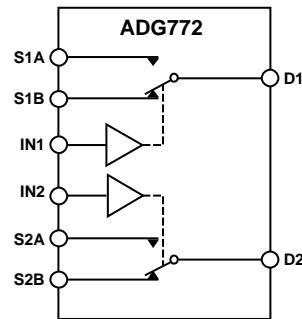
GENERAL DESCRIPTION

The [ADG772](#) is a low voltage CMOS device that contains two independently selectable single-pole, double throw (SPDT) switches. It is designed as a general-purpose switch and can be used for routing both USB 1.1 and USB 2.0 signals.

This device offers a data rate of 1260 Mbps, making the device suitable for high frequency data switching. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. The [ADG772](#) exhibits break-before-make switching action.

The [ADG772](#) is available in a 12-lead LFCSP and a 10-lead mini LFCSP. These packages make the [ADG772](#) the ideal solution for space-constrained applications.

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC 0 INPUT

06832-001

Figure 1.

PRODUCT HIGHLIGHTS

1. 1.6 mm × 1.3 mm mini LFCSP package.
2. USB 1.1 (12 Mbps) and USB 2.0 (480 Mbps) compliant.
3. Single 2.7 V to 3.6 V operation.
4. 1.8 V logic compatible.
5. RoHS compliant.

Rev. C

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TABLE OF CONTENTS

Features	1	ESD Caution.....	4
Applications.....	1	Pin Configuration and Function Descriptions.....	5
Functional Block Diagram	1	Truth Table	5
General Description	1	Typical Performance Characteristics	6
Product Highlights	1	Test Circuits.....	9
Revision History	2	Terminology	11
Specifications.....	3	Outline Dimensions.....	12
Absolute Maximum Ratings.....	4	Ordering Guide	12

REVISION HISTORY

5/16—Rev. B to Rev. C

Changes to Figure 3	5
Updated Outline Dimensions	12
Changes to Ordering Guide	12

4/13—Rev. A to Rev. B

Added EPAD Notation	5
Changes to Figure 10.....	7
Updated Outline Dimensions	12
Changes to Ordering Guide	12

6/08—Rev. 0 to Rev. A

Changes to Product Highlights.....	1
Changes to Input High Voltage, V _{INH} , Parameter.....	3

8/07—Revision 0: Initial Version

Specifications

V_{DD} = 2.7 V to 3.6 V, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	+25°C	-40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range	0 V to V_{DD}		V	
On-Resistance (R_{ON})	6.7	8.8	Ω typ	$V_{DD} = 2.7$ V, $V_S = 0$ V to V_{DD} , $I_{DS} = 10$ mA; see Figure 21
On-Resistance Match Between Channels (ΔR_{ON})	0.04	0.2	Ω typ	$V_{DD} = 2.7$ V, $V_S = 1.5$ V, $I_{DS} = 10$ mA
On Resistance Flatness ($R_{FLAT(ON)}$)	3.3	3.6	Ω max	$V_{DD} = 2.7$ V, $V_S = 0$ V to V_{DD} , $I_{DS} = 10$ mA
LEAKAGE CURRENTS				
Source Off Leakage I_S (Off)	± 0.2		nA typ	$V_{DD} = 3.6$ V
Channel On Leakage I_D , I_S (On)	± 0.2		nA typ	$V_S = 0.6$ V/3.3 V, $V_D = 3.3$ V/0.6 V; see Figure 22
DIGITAL INPUTS				
Input High Voltage, V_{INH}	1.35		V min	
Input Low Voltage, V_{INL}	0.8		V max	
Input Current, I_{INL} or I_{INH}	0.005	± 0.1	μ A typ	$V_{IN} = V_{INL}$ or V_{INH}
Digital Input Capacitance, C_{IN}	2		μ A max	$V_{IN} = V_{INL}$ or V_{INH}
DYNAMIC CHARACTERISTICS ¹			pF typ	
t_{ON}	9		ns typ	$R_L = 50 \Omega$, $C_L = 35$ pF
t_{OFF}	12.5	13.5	ns max	$V_S = 2$ V; see Figure 24
Propagation Delay	6		ns typ	$R_L = 50 \Omega$, $C_L = 35$ pF
Propagation Delay Skew, t_{SKEW}	9.5	10	ns max	$V_S = 2$ V; see Figure 24
Break-Before-Make Time Delay (t_{BBM})	250		ps typ	$R_L = 50 \Omega$, $C_L = 35$ pF
Charge Injection	20		ps typ	$R_L = 50 \Omega$, $C_L = 35$ pF
Off Isolation	5		ns typ	$R_L = 50 \Omega$, $C_L = 35$ pF
Channel-to-Channel Crosstalk	3.4	2.9	ns min	$V_{S1} = V_{S2} = 2$ V; see Figure 25
	0.5		pC typ	$V_D = 1.25$ V, $R_S = 0$ Ω , $C_L = 1$ nF; see Figure 26
	73		dB typ	$R_L = 50 \Omega$, $C_L = 5$ pF, $f = 1$ MHz; see Figure 27
	-90		dB typ	S1A to S2A/S1B to S2B; $R_L = 50 \Omega$, $C_L = 5$ pF, $f = 1$ MHz; see Figure 28
	-80		dB typ	S1A to S1B/S2A to S2B; $R_L = 50 \Omega$, $C_L = 5$ pF, $f = 1$ MHz; see Figure 29
-3 dB Bandwidth	630		MHz typ	$R_L = 50 \Omega$, $C_L = 5$ pF; see Figure 30
Data Rate	1260		Mbps typ	$R_L = 50 \Omega$, $C_L = 5$ pF; see Figure 30
C_S (Off)	2.4		pF typ	
C_D , C_S (On)	6.9		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.006	1	μ A typ	$V_{DD} = 3.6$ V
			μ A max	Digital inputs = 0 V or 3.6 V

¹ Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Rating
V_{DD} to GND	−0.3 V to +4.6 V
Analog Inputs, ¹ Digital Inputs	−0.3 V to $V_{DD} + 0.3$ V or 10 mA, whichever occurs first
Peak Current, Pin S1A, Pin S2A, Pin D1, or Pin D2	100 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, Pin S1A, Pin S2A, Pin D1, or Pin D2	30 mA
Operating Temperature Industrial Range (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (4-Layer Board)	
10-Lead Mini LFCSP	131.6°C/W
12-Lead LFCSP	61°C/W
Pb-Free Temperature, Soldering, IR Reflow	
Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	10 sec to 40 sec

¹ Overvoltages at the IN1, IN2, S1A, S2A, D1, or D2 pin are clamped by internal diodes. Current must be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

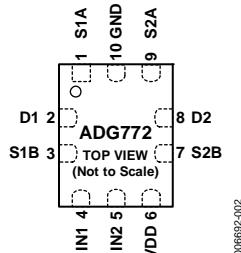


Figure 2. 10-Lead Mini LFCSP Pin Configuration

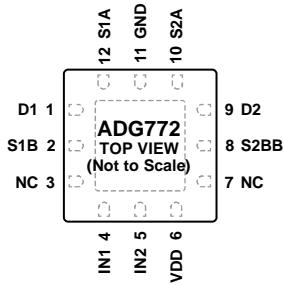


Figure 3. 12-Lead LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.		Mnemonic	Description
10-Lead Mini LFCSP	12-Lead LFCSP		
1	12	S1A	Source Terminal. Can be an input or an output.
2	1	D1	Drain Terminal. Can be an input or an output.
3	2	S1B	Source Terminal. Can be an input or an output.
4	4	IN1	Logic Control Input. This pin controls Switch S1A and Switch S1B to D1.
5	5	IN2	Login Control Input. This pin controls Switch S2A and Switch S2B to D2.
6	6	VDD	Most Positive Power Supply Potential.
7	8	S2B	Source Terminal. Can be an input or an output.
8	9	D2	Drain Terminal. Can be an input or an output.
9	10	S2A	Source Terminal. Can be an input or an output.
10	11	GND	Ground (0 V) Reference.
Not applicable	3, 7	NC	No Connect.
Not applicable	13	EPAD	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to a ground reference.

TRUTH TABLE

Table 4.

Logic (IN1 or IN2)	Switch A (S1A or S2A)	Switch B (S1B or S2B)
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

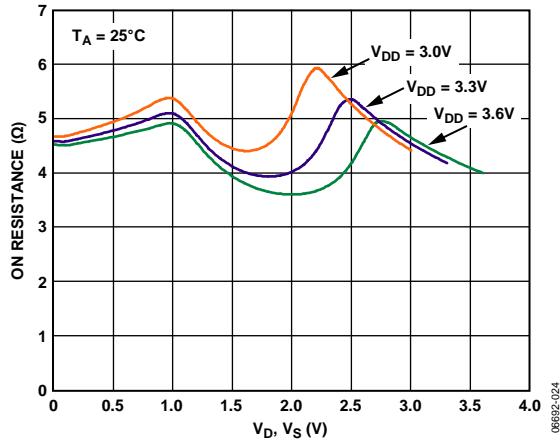


Figure 4. On Resistance vs. V_D, V_S ; $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$

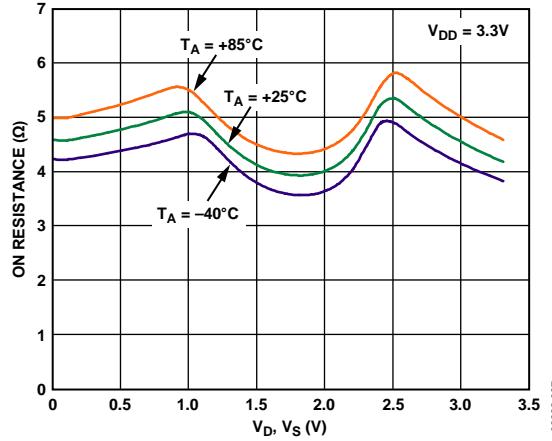


Figure 7. On Resistance vs. V_D, V_S for Different Temperatures; $V_{DD} = 3.3\text{V}$

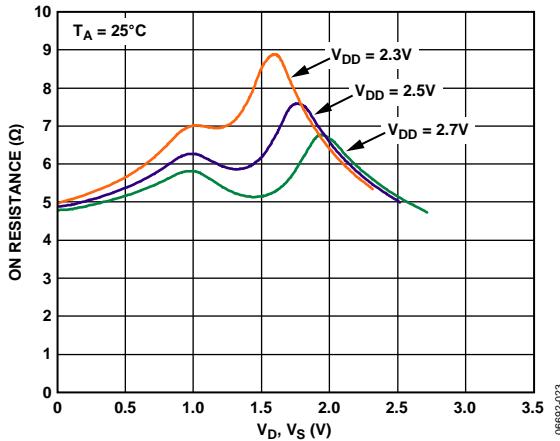


Figure 5. On Resistance vs. V_D, V_S ; $V_{DD} = 2.5\text{V} \pm 0.2\text{V}$

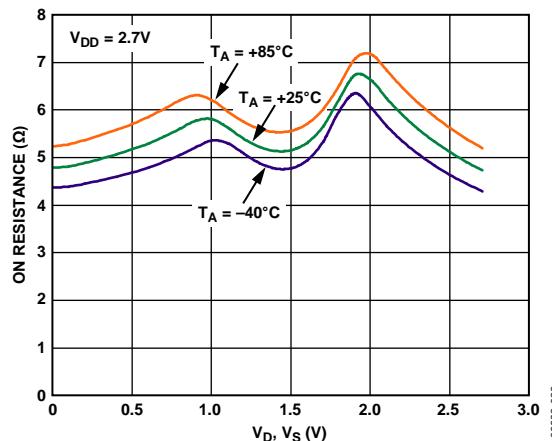


Figure 8. On Resistance vs. V_D, V_S for Different Temperatures; $V_{DD} = 2.7\text{V}$

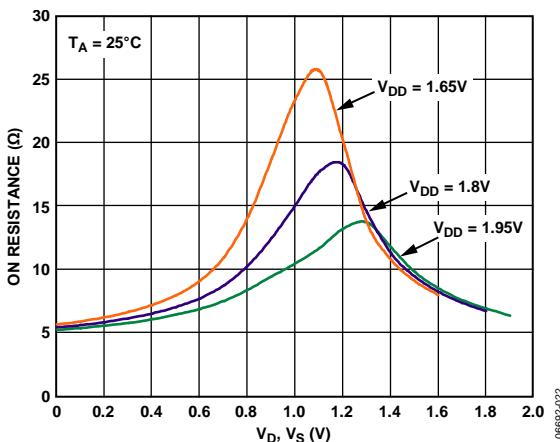


Figure 6. On Resistance vs. V_D, V_S ; $V_{DD} = 1.8\text{V} \pm 0.15\text{V}$

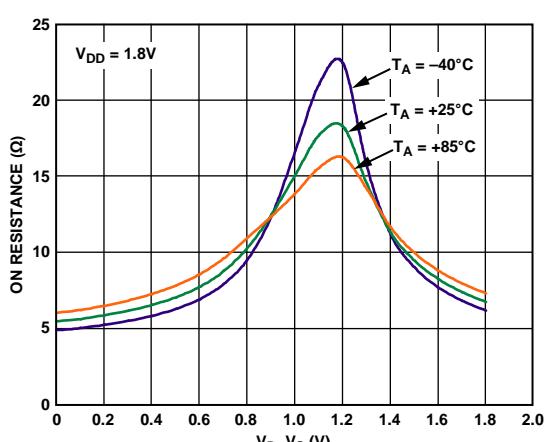
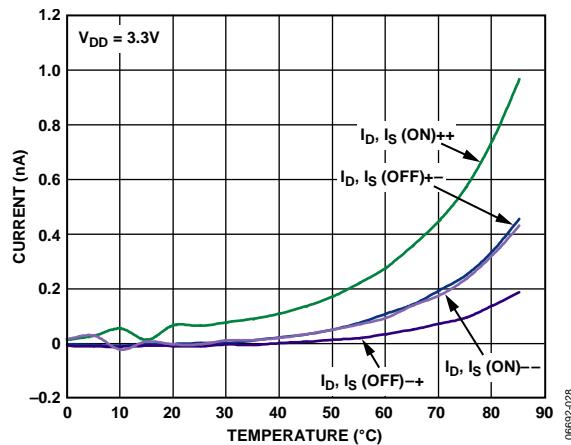
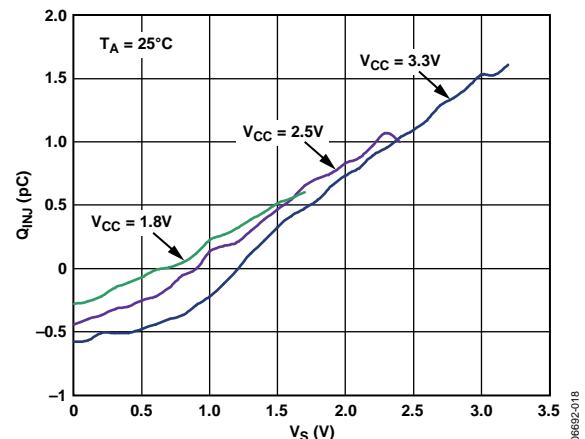
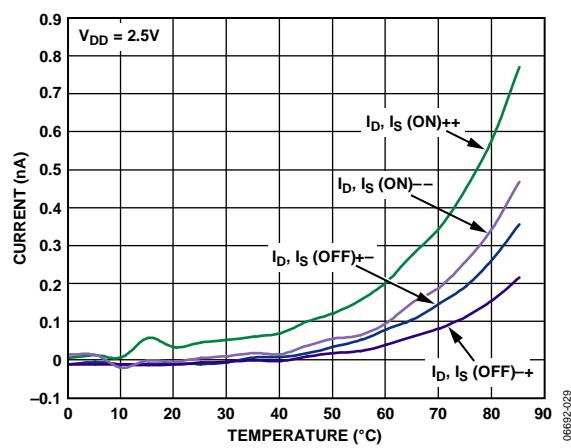
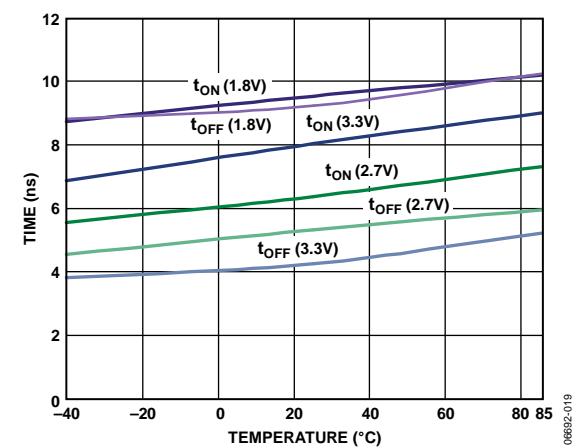


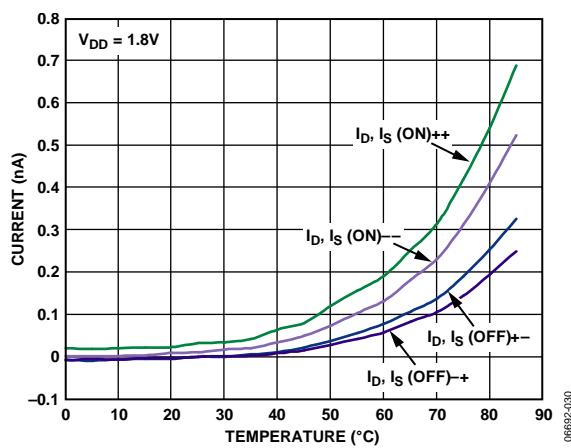
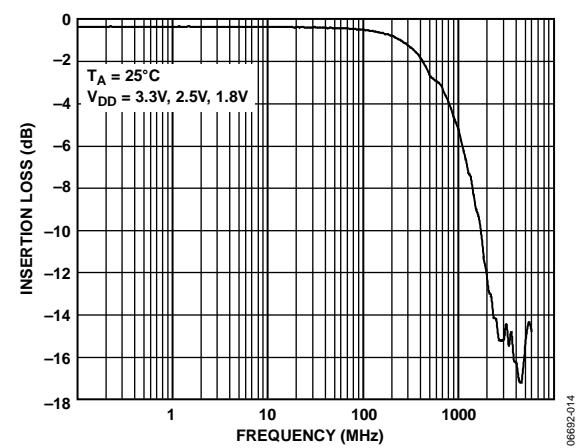
Figure 9. On Resistance vs. V_D, V_S for Different Temperatures; $V_{DD} = 1.8\text{V}$

Figure 10. Leakage Current vs. Temperature; $V_{DD} = 3.3\text{V}$ 

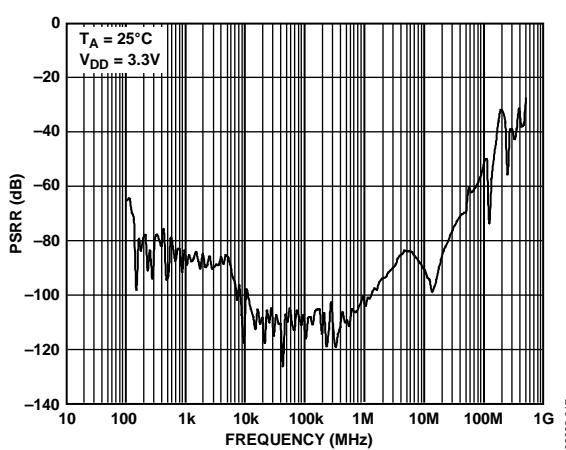
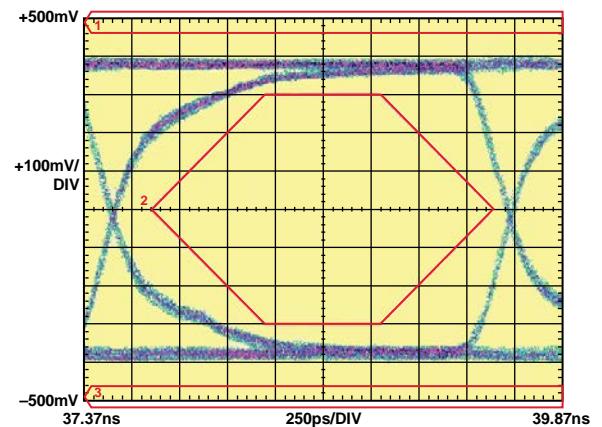
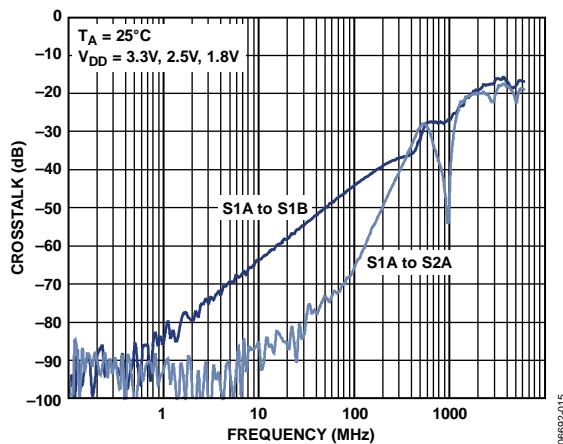
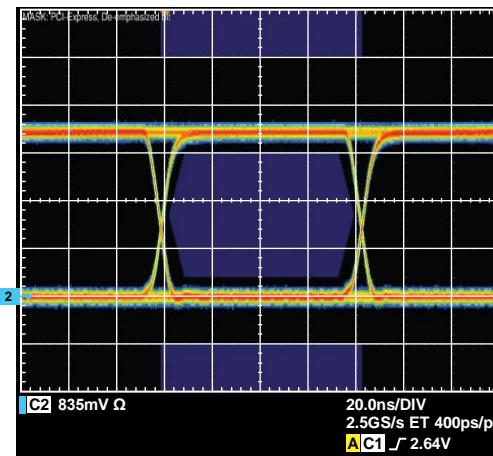
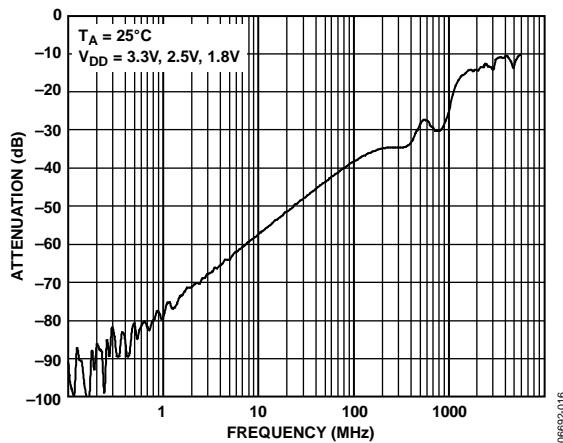
06692-018

Figure 11. Leakage Current vs. Temperature; $V_{DD} = 2.5\text{V}$ 

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Figure 12. Leakage Current vs. Temperature; $V_{DD} = 1.8\text{V}$ 

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TEST CIRCUITS

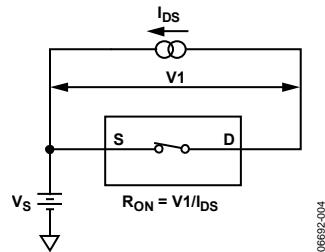


Figure 21. On Resistance

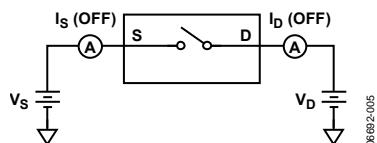


Figure 22. Off Leakage

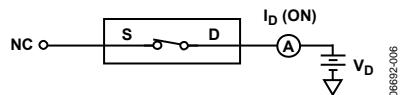


Figure 23. On Leakage

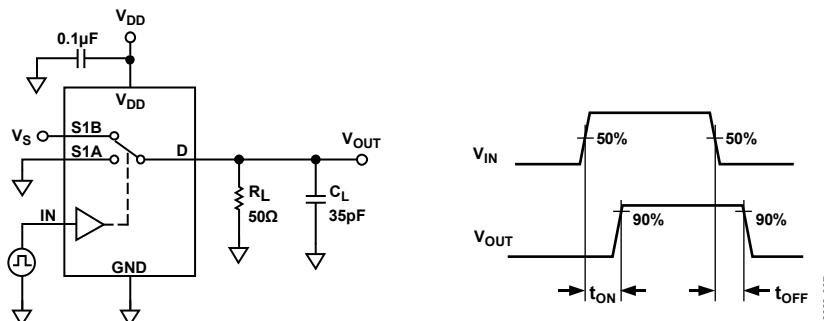
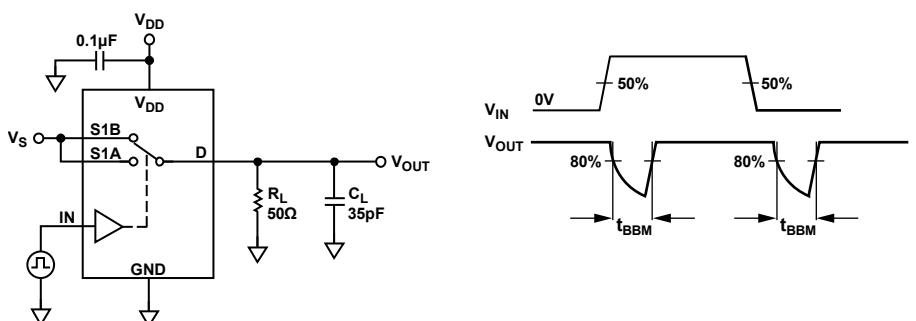
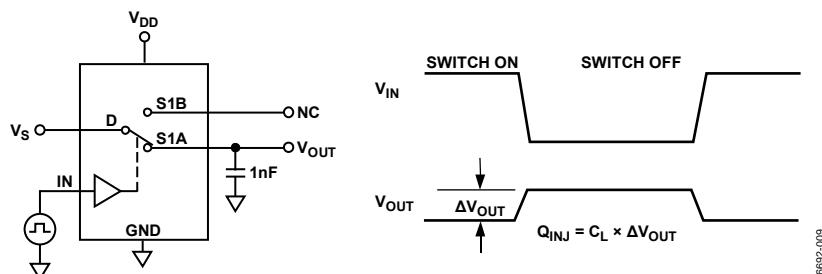
Figure 24. Switching Times, t_{ON} , t_{OFF} Figure 25. Break-Before-Make Time Delay, t_{BBM} 

Figure 26. Charge Injection

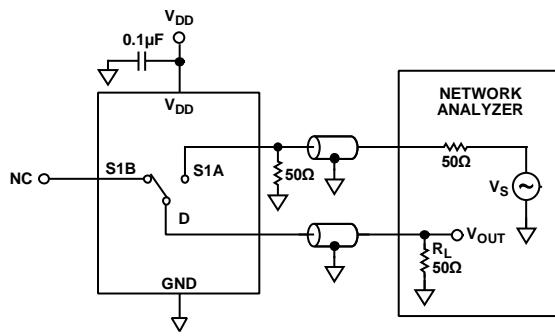


Figure 27. Off Isolation

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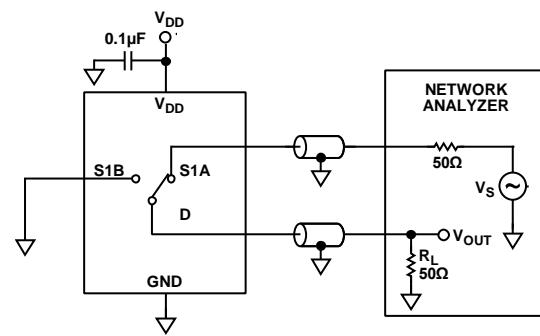


Figure 29. Channel-to-Channel Crosstalk (S1A to S1B)

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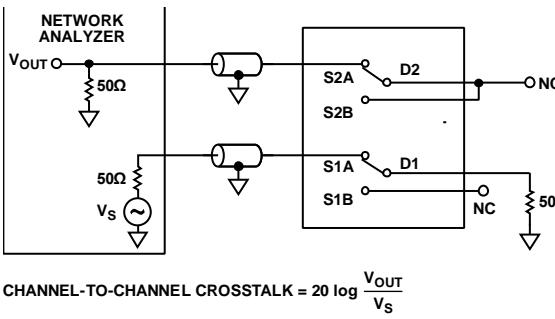


Figure 28. Channel-to-Channel Crosstalk (S1A to S2A)

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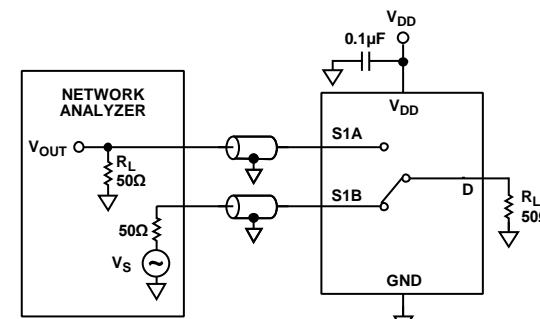


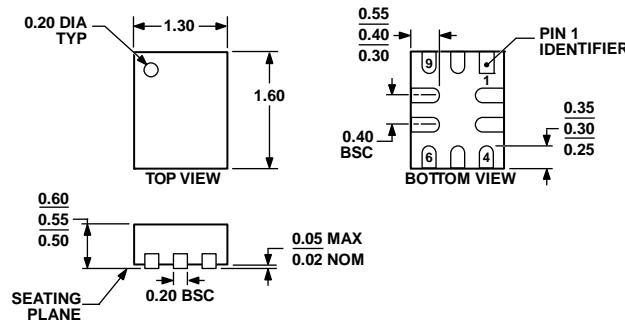
Figure 30. Bandwidth

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TERMINOLOGY

I_{DD}	C _{IN}
Positive supply current.	Digital input capacitance.
V_D, V_S	t_{ON}
Analog voltage on Terminal D and Terminal S.	Delay time between the 50% and 90% points of the digital input and switch on condition.
R_{ON}	t_{OFF}
Ohmic resistance between Terminal D and Terminal S.	Delay time between the 50% and 90% points of the digital input and switch off condition.
R_{FLAT (On)}	t_{BBM}
The difference between the maximum and minimum values of on resistance as measured on the switch.	On or off time measured between the 80% points of both switches when switching from one to another.
ΔR_{ON}	Charge Injection
On resistance match between any two channels.	Measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.
I_{s (Off)}	Off Isolation
Source leakage current with the switch off.	Measure of unwanted signal coupling through an off switch.
I_{D (Off)}	Crosstalk
Drain leakage current with the switch off.	Measure of unwanted signal that is coupled from one channel to another as a result of parasitic capacitance.
I_{D, I_{s (On)}}	-3 dB Bandwidth
Channel leakage current with the switch on.	Frequency at which the output is attenuated by 3 dB.
V_{INL}	On Response
Maximum input voltage for Logic 0.	Frequency response of the on switch.
V_{INH}	Insertion Loss
Minimum input voltage for Logic 1.	The loss due to the on resistance of the switch.
I_{INL, I_{INH}}	THD + N
Input current of the digital input.	Ratio of the harmonics amplitude plus noise of a signal to the fundamental.
C_{s (Off)}	T_{SKEW}
Off switch source capacitance. Measured with reference to ground.	The measure of the variation in propagation delay between each channel.
C_{D (Off)}	
Off switch drain capacitance. Measured with reference to ground.	
C_{D, C_{s (On)}}	
On switch capacitance. Measured with reference to ground.	

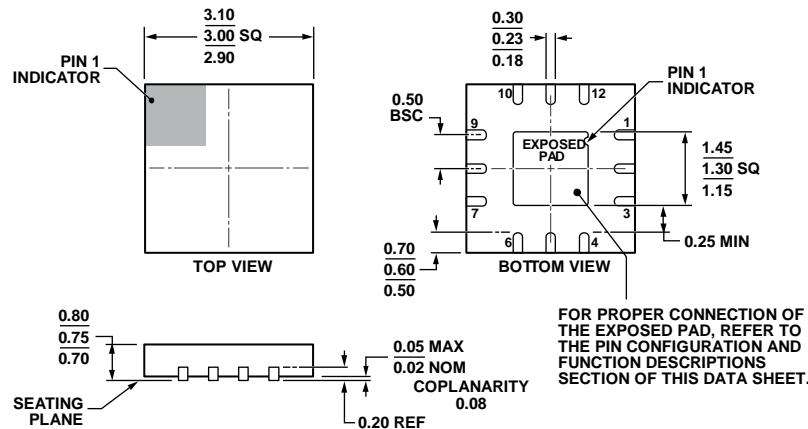
OUTLINE DIMENSIONS



033007-A

Figure 31. 10-Lead Mini Lead Frame Chip Scale Package [LFCSP]
1.30 mm × 1.60 mm Body and 0.55 mm Package Height
(CP-10-10)

Dimensions shown in millimeters



FOR PROPER CONNECTION OF
THE EXPOSED PAD, REFER TO
THE PIN CONFIGURATION AND
FUNCTION DESCRIPTIONS
SECTION OF THIS DATA SHEET.

111808-A

COMPLIANT TO JEDEC STANDARDS MO-220-WEED.
Figure 32. 12-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-12-4)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
ADG772BCPZ-1REEL	-40°C to +85°C	12-Lead Lead Frame Chip Scale Package [LFCSP]	CP-12-4	S2P
ADG772BCPZ-REEL7	-40°C to +85°C	10-Lead Mini Lead Frame Chip Scale Package [LFCSP]	CP-10-10	B
EVAL-ADG772EBZ	-40°C to +85°C	Evaluation Board		

¹ Z = RoHS Compliant Part.



**Стандарт
Электрон
Связь**

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

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