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S34SL01G2, S34SL02G2, S34SL04G2

1 Gbit (128 Mbyte), 2 Gbit (256 Mbyte), 4 Gbit (512 Mbyte) Secure NAND Flash Memory for Embedded

Distinctive Characteristics

- Architecture
  - Input / Output Bus Width: 8-bits / 16-bits
  - Page Size
    - x8
      1 Gbit: (2048 + 64) bytes; 64-byte spare area
      2 Gbit / 4 Gbit: (2048 + 128) bytes; 128-byte spare area
    - x16
      1 Gbit: (1024 + 32) words; 32-word spare area
      2 Gbit / 4 Gbit (1024 + 64) words; 64-word spare area
  - Block Size: 64 Pages
    - x8
      1 Gbit: 128k + 4k bytes
      2 Gbit / 4 Gbit: 128k + 8k bytes
    - x16
      1 Gbit: 64k + 2k words
      2 Gbit / 4 Gbit: 64k + 4k words
  - Plane Size
    - x8
      1 Gbit: 1024 Blocks per Plane or (128M + 4M) bytes
      2 Gbit: 1024 Blocks per Plane or (128M + 8M) bytes
      4 Gbit: 2048 Blocks per Plane or (256M + 16M) bytes
    - x16
      1 Gbit: 1024 Blocks per Plane or (64M + 2M) words
      2 Gbit: 1024 Blocks per Plane or (64M + 4M) words
      4 Gbit: 2048 Blocks per Plane or (128M + 8M) words
  - Device Size
  - 1 Gbit: 1 Plane per Device or 128 Mbyte
  - 2 Gbit: 2 Planes per Device or 256 Mbyte
  - 4 Gbit: 2 Planes per Device or 512 Mbyte

Performance

- Page Read / Program
  - Random access: 25 µs (Max) **(S34SL01G2)**
  - Random access: 30 µs (Max) **(S34SL02G2, S34SL04G2)**
  - Sequential access: 25 ns (Min)
  - Program time / Multiplane Program time: 300 µs (Typ)
- Block Erase (S34SL01G2)
  - Block Erase time: 3 ms (Typ)
- Block Erase / Multiplane Erase (S34SL02G2, S34SL04G2)
  - Block Erase time: 3.5 ms (Typ)
- NAND Flash Interface
  - Open NAND Flash Interface (ONFI) 1.0 compliant
- Supply Voltage
  - 3.3V device: VCC = 2.7V ~ 3.6V
- Security
  - Volatile Protection
    - Industry standard command set
    - One range of block granularity unlock / lock
    - Range lock-down until next power cycle option
  - Non-volatile Protection
    - One fixed permanent block lock range
    - One expandable permanent block lock range
    - Individual block permanent lock option
  - One Time Programmable (OTP) block
  - Serial number (unique ID)
  - Hardware program/erase disabled during power transition
- Additional Features
  - Read Cache
  - Copy Back Program
  - 2 Gb and 4 Gb parts support Multiplane Program, Copy Back Program, and Erase commands
- Operating Temperature
  - Industrial: -40°C to 85°C
  - Industrial Plus: -40°C to 105°C (contact Cypress sales)
- Package Options
  - Lead Free and Low Halogen
  - 63-Ball BGA 9 x 11 x 1 mm
- Reliability
  - 100,000 Program / Erase cycles (Typ) (with 4-bit ECC per 528 bytes (x8) or 264 words (x16))
  - 10 Year Data retention (Typ)
  - Blocks zero and one are valid for at least 1000 program-erase cycles with ECC
  - OTP block is valid for 1M read accesses.

Errata: For information on silicon errata, see See *Errata on page 92*. Details include trigger conditions, devices affected, and proposed workaround.

1. General Description

The Cypress Secure NAND devices are industry standard ONFI 1.0 interface compatible, Single Level Cell (SLC) NAND memories, with added block granularity protection against unintended or malicious program and erase operations.

Protection methods and security features include:

- One, volatile control - software managed - range of blocks, with the option to lock the range until power off
- One, non-volatile control, fixed range of blocks, with the option permanently protect the range
- One, non-volatile control, expandable range of blocks, with the option to permanently protect the range
- Individual non-volatile block protection
- A Write Protect (WP#) input to provide full device hardware protection.
- OTP (one time programmable) area, which is a restricted access area where sensitive data/code can be stored permanently.
- Serial number (unique identifier), which allows the devices to be uniquely identified for pairing with the host system.

Device	Density (bits)		Number of Planes	Number of Blocks per Plane
	Main	Spare		
S34SL01G2	128M x 8 64M x 16	4M x 8 2M x 16	1	1024
S34SL02G2	256M x 8 128M x 16	16M x 8 8M x 16	2	1024
S34SL04G2	512M x 8 256M x 16	32M x 8 16M x 16	2	2048

The Secure NAND (sNAND) S34SL-2 family is offered with 3.3 Volt VCC and VCCQ power supply, and with x8 or x16 I/O interface. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. The page size for x8 I/O is (2048 + spare) bytes; for x16 I/O (1024 + spare) words.

To extend the lifetime of NAND flash devices, the implementation of system level Error Detection and Correction (EDC) via Error Correction Code (ECC) is mandatory. The EDC method must be able to correct up to 4-bits within each partial page (512 bytes) and related spare area (16 or 32 bytes).

The chip supports CE# don't care function. This allows reading the NAND flash memory device by a microcontroller, as the CE# transitions during each access does not stop the read operation.

The devices have a Read Cache feature that improves the read throughput for large files. During cache reading, the devices load the memory array data into a data register while the previous data page is transferred from the cache register through the I/O buffers to the host system.

A program operation typically writes 2 kbytes (x8) or 1 kword (x16) in 300 µs and an erase operation can typically be performed in 3 ms (S34SL01G2) on a 128-kB block (x8) or 64k-word block (x16). In addition, thanks to multiplane architecture, it is possible to program two pages at a time (one per plane) or to erase two blocks at a time (again, one per plane). The multiplane architecture allows program time to be reduced by 40% and erase time to be reduced by 50%.

In multiplane operations, data in the page can be read out at 25 ns cycle time per byte. The I/O pins serve as the ports for command and address input as well as data input/output. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of the footprint.

Commands, Data, and Addresses are asynchronously transfered using the CE#, WE#, ALE, and CLE control signals.

The on-chip Program/Erase Controller automates all read, program, and erase functions including pulse repetition, where required, and internal verification and margining of data.

The Ready/Busy (R/B#) open drain output signal indicates the status of the device during each operation. It identifies if the program/erase/read controller is currently active. The use of an open-drain output allows the R/B# signals from several memories to connect to a single pull-up resistor. In a system with multiple memories the R/B# signals can be connected together to provide a global status signal.

The Reprogram function allows the optimization of defective (bad) block management — when a Page Program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.

Multiplane Copy Back is also supported. Data read out after Copy Back Read (both for single and multiplane cases) is allowed.

In addition, Cache Program and Multiplane Cache Program operations improve the programing throughput by programing data using the cache register.

The devices provide two innovative features: Page Reprogram and Multiplane Page Reprogram. The Page Reprogram re-programs one page. Normally, this operation is performed after a failed Page Program operation. Similarly, the Multiplane Page Reprogram re-programs two pages in parallel, one per plane. The first page must be in the first plane while the second page must be in the second plane. The Multiplane Page Reprogram operation is performed after a failed Multiplane Page Program operation. The Page Reprogram and Multiplane Page Reprogram guarantee improved performance, since data insertion can be omitted during re-program operations.

The Secure NAND devices are available only in BGA packages.

1.1 Input/Output Summary

Signal Descriptions

Signal Name	Type	Description
CE#	Input	**Chip Enable.** CE# low selects the device to perform operations based on the NAND bus signal behavior.When CE# is high all other input signals are ignored and outputs are not actively driven.
CLE	Input	**Command Latch Enable.** This input enables the latching of the I/O inputs into the Command Register on the rising edge of Write Enable (WE#).
ALE	Input	**Address Latch Enable.** This input enables the latching of the I/O inputs into the Address Register on the rising edge of Write Enable (WE#).
RE#	Input	**Read Enable.** The RE# input is the serial data-out control, and when low drives the data onto the I/O bus. Data is valid t_{REA} after the first falling edge of RE#. Each additional RE# falling edge while CE#, CLE, and ALE remain low, increments the internal column address counter by one to deliver the next sequential data output.
WE#	Input	**Write Enable.** This input latches Command, Address and Data. The I/O inputs are latched on the rising edge of WE#.
WP#	Input + IPU	**Write Protect.** The WP# input, when low, provides hardware protection of the entire memory address space against undesired data modification (program / erase). This input has a weak internal Pull-Up (IPU) to disable host system protection if the input is left floating.
VPE	Input + IPD	**Volatile Protection Enable.** The Volatile Protection Enable input, when high during power-on, provides block granularity hardware protection against undesired data modification (program / erase). This input has a weak internal pull-down (IPD) to disable the volatile protection features if the input is left floating.
R/B#	Output, Open Drain	**Ready Busy.** The Ready/Busy input or output is an Open Drain signal that detects the state of attached memory or signals the state of the controller.
I/O[7:0]	Input / Output	**Inputs/Outputs**. The I/O signals are used for command input, address input, data input, and data output. The I/O signals float to High-Z when the device is deselected or the outputs are disabled.

1.2 Block Diagram

Figure 1.1 Functional Block Diagram

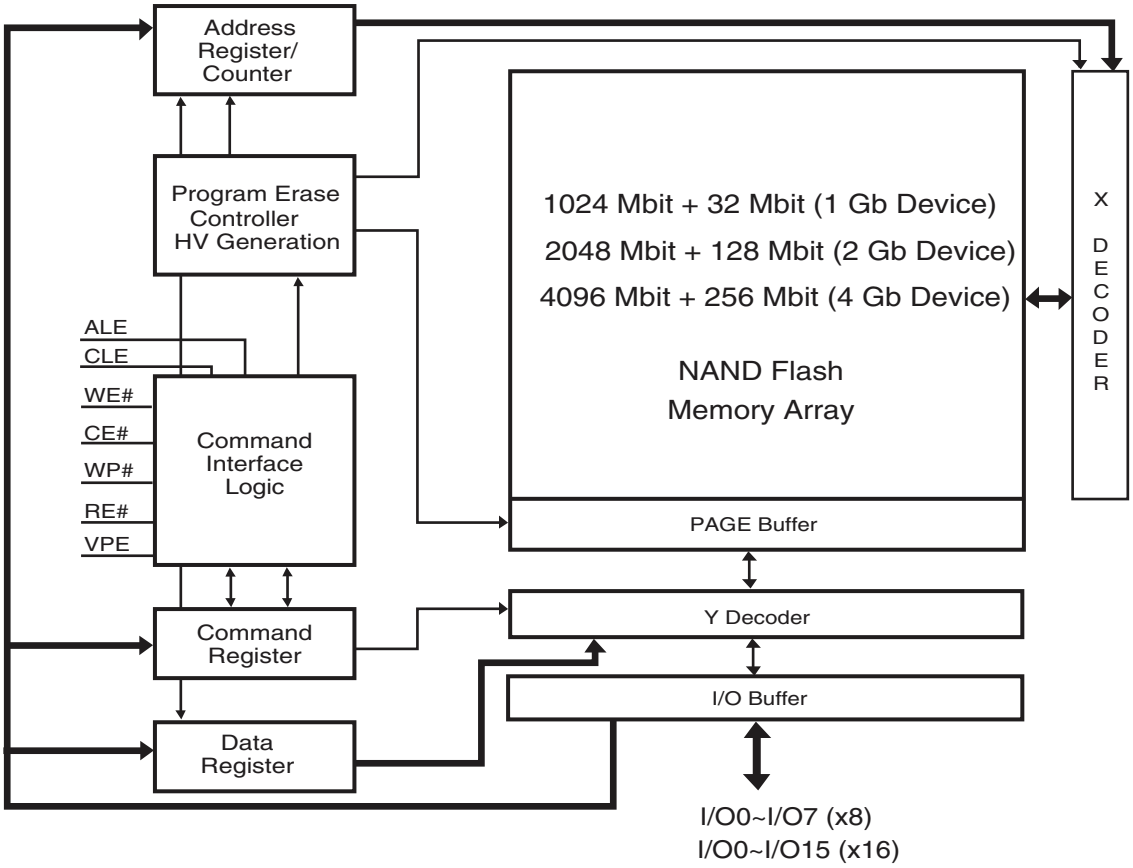


Table of Contents

Software Interface

This section discusses the features and behaviors most relevant to host system software that interacts with sNAND Family memory devices.

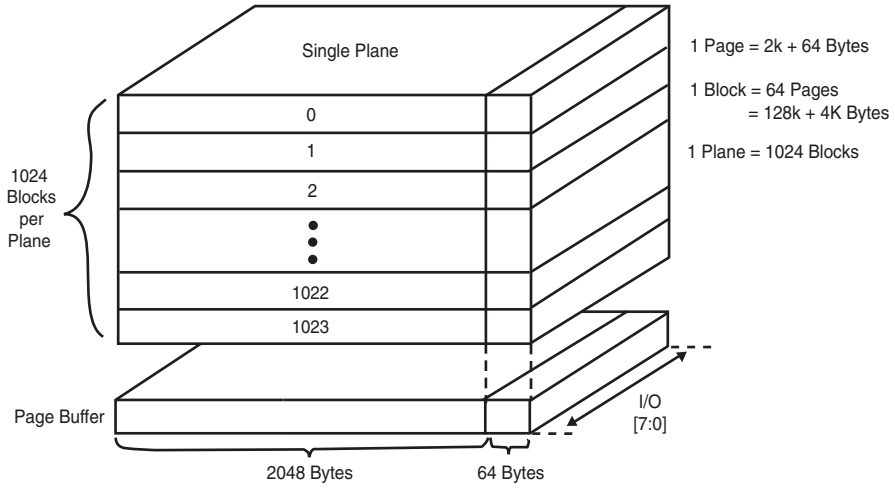
2. Array Organization

The main flash array is divided into erase units called Blocks. All Blocks contain 64 pages. Each page has a data area and a meta-data (spare) area. Each page is subdivided into four partial pages, each with a data and spare area, that may be written individually, one time, before an erase of the block holding the partial page is needed, in order to write new information into that same partial page.

Pages have 64 or 128 bytes of spare area in each page. So, all blocks contain a storage capacity of 128 kbytes of data area and 4 or 8 kbytes of spare area. However, each block uses 256 KB of address space in the address map.

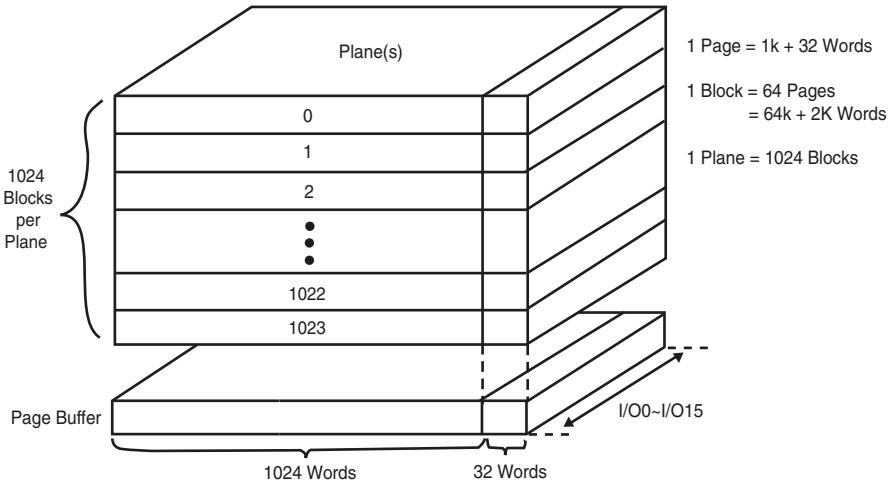
Devices with 2 Gbits or more have a multi-plane architecture in which even and odd address blocks are in separate planes that may be programmed or erased in parallel. With multi-plane architecture it is possible to program two pages at a time (one per plane) or to erase two blocks at a time (again, one per plane).

Figure 2.1 Array Organization — S34Sx01G2 (x8)



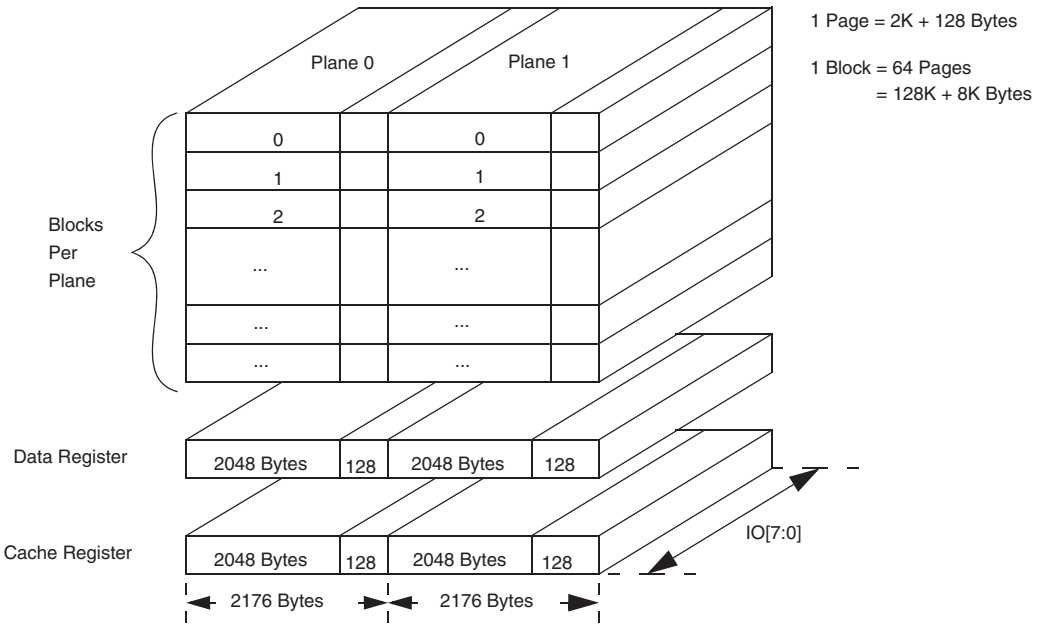
Array Organization (x8)

Figure 2.2 Array Organization — S34Sx01G2 (x16)



Array Organization (x16)

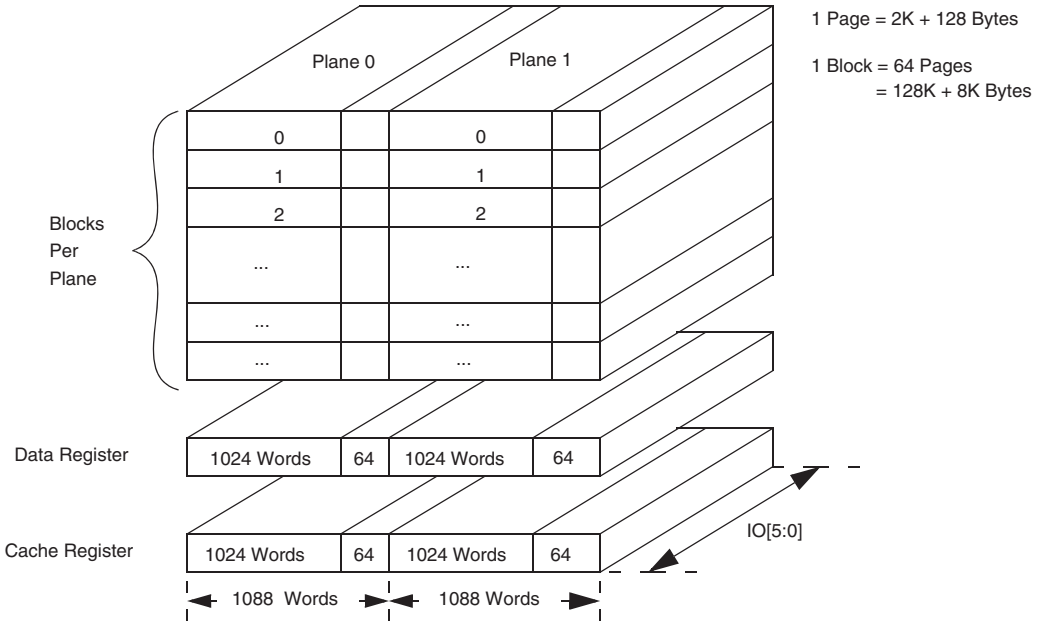
Figure 2.3 Array Organization — S34Sx02G2 to S34Sx16G2 (x8)



Notes:

1. *S34Sx02G2 has 1024 blocks per plane of 128 kbytes data + 8 kbytes meta data per block, for a total of 2048 blocks.*
2. *S34Sx04G2 has 2048 blocks per plane of 128 kbytes data + 8 kbytes meta data per block, for a total of 4096 blocks.*

Figure 2.4 Array Organization — S34Sx02G2 to S34Sx16G2 (x16)



Notes:

1. *S34Sx02G2 has 1024 blocks per plane of 64 kwords data + 4 kwords meta data per block, for a total of 2048 blocks.*
2. *S34Sx04G2 has 2048 blocks per plane of 64 kwords data + 4 kwords meta data per block, for a total of 4096 blocks.*

2.1 Valid Blocks

NAND memories may have individual blocks that do not read, program, or erase properly. These are referred to as bad blocks. These bad blocks may exist in memories when shipped from Cypress. These are referred to as original bad blocks and these blocks are specially marked as bad by Cypress. Additional blocks may fail – become bad blocks – during the lifetime of the device. A limit of 2% of all blocks is set on the number of blocks that are allowed to be or become bad during the lifetime of the device so that there will always be a minimum number of good (valid) blocks in the device.

Blocks zero and one are guaranteed to remain good for up to 1000 program and erase cycles. The OTP area block is also guaranteed good.

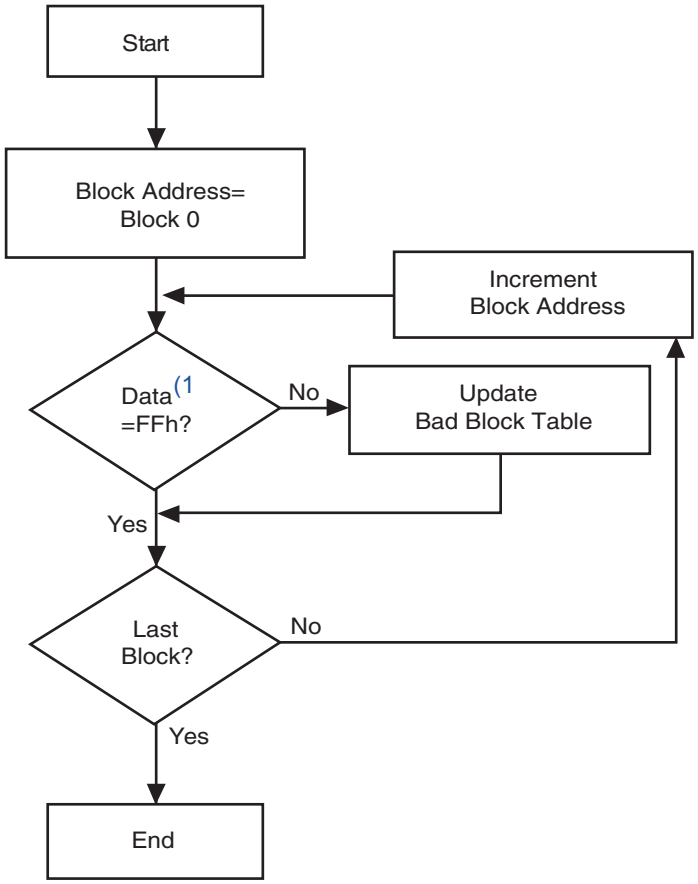
Table 2.1 Valid Blocks

Device	Symbol	Min	Typ	Max	Unit
01G2	N_{VB}	1004	—	1024	Blocks
02G2	N_{VB}	2008	—	2048	Blocks
04G2	N_{VB}	4016	—	4096	Blocks

2.2 Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written prior to shipping. Any block where the 1st byte in the spare area of the 1st or 2nd or last page does not contain FFh is a Bad Block. That is, the first byte of the spare area in the first, second and the last page must be read and if any of these bytes has a non-FFh value, it indicates a bad block.The Bad Block Information must be read before any erase is attempted, as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information, it is recommended to create a Bad Block table following the flowchart shown in Figure 2.5. The host is responsible to detect and track bad blocks, both factory bad blocks and blocks that may go bad during operation. Once a block is found to be bad, data should not be written to that block.

Figure 2.5 Bad Block Management Flowchart



Note:
1. Check for FFh at the 1st byte in the spare area of the 1st, 2nd, and last pages.

2.3 Bad Block Replacement

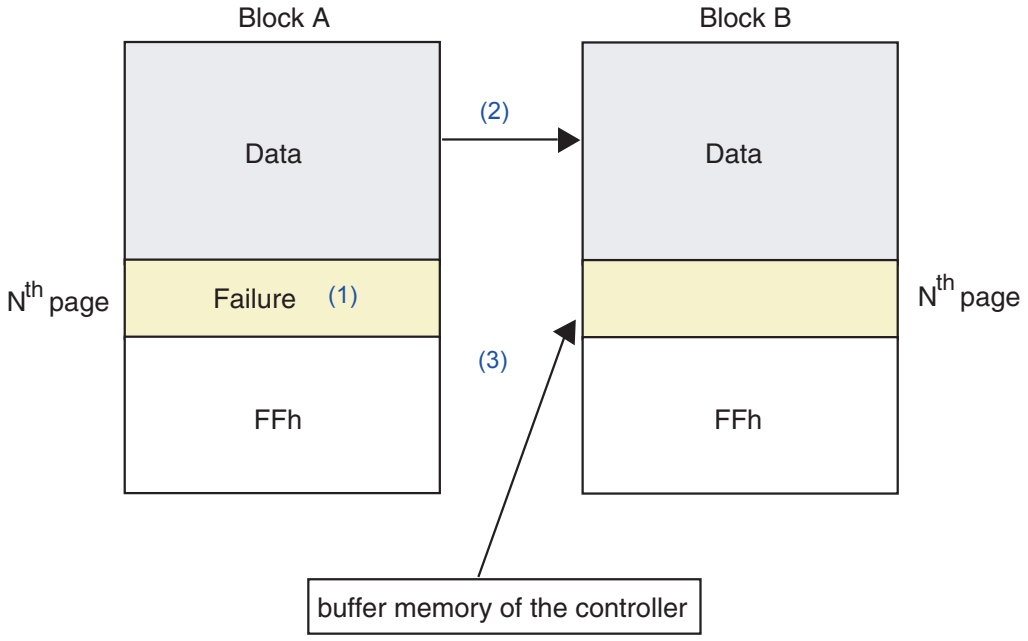
Over the lifetime of the device, additional Bad Blocks may develop. In this case, each bad block has to be replaced by copying any valid data to a new block. These additional Bad Blocks can be identified whenever a program or erase operation reports “Fail” in the Status Register.

The failure of a page program operation does not affect the data in other pages in the same block, thus the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. Refer to Table 2.2 and Figure 2.6 for the recommended procedure to follow if an error occurs during an operation.

Table 2.2 Block Failure

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC (4 bit / 512+16 byte)

Figure 2.6 Bad Block Replacement



Notes:

1. *An error occurs on the Nth page of Block A during a program operation.*
2. *Data in Block A is copied to the same location in Block B, which is a valid block.*
3. *The Nth page of block A, which is in controller buffer memory, is copied into the Nth page of Block B.*
4. *Bad block table should be updated to prevent from erasing or programming Block A.*

2.4 Addressing

The sNAND Family uses the standard ONFI 1.0 NAND command protocol that provides up to a 5-byte address that is split into a Row Address (RA) portion and a Column Address (CA) portion. The Row Address portion selects a Page. Each Page contains a 2 KByte data area along with a related 64-, or 128-byte meta data (spare) area. The spare area size depends on the device density. The 1 Gbit density provides 64 bytes and 2 Gbit or larger densities provide 128 bytes.

While each page contains 2 KB of user data space the spare area uses only a portion of the adjacent 2 KB of address space. The unused portion is reserved and not implemented in the device but does consume space in the overall address map. Effectively, each Page consumes 4 KB of address space which in turn causes each block of 64 pages to consume 256 KB of address space.

The sNAND Family device density is stated in terms of the available user data space in the device, not including the spare or reserved areas.

For example, a 1 Gbit sNAND Family device actually contains:

- 1024 blocks, of 64 pages, of 2 KB data + 64 B meta-data = 135 MBytes of storage

but, consumes 2 Gbits (256 MBytes) of address space as selected by the combined RA and CA portions of the total byte address.

Table 2.3 Flash Memory Array Address Space Allocation

Device OPN	Each Device				Each Block			Each Page		
	Density (Data Space)	Address Space	Blocks	Pages	Data	Meta-Data	Address Space	Data	Meta-Data	Address Space
S34SL01G-G2	1Gb Mbit (128 MB)	256 MB	1024	65536	128 KB	4 KB	256 KB	2 KB	64 B	4 KB
S34SL02G-G2	2Gb Mbit (256 MB)	512 MB	2048	131072	128 KB	8 KB	256 KB	2 KB	128 B	4 KB
S34SL04G-G2	4Gb Mbit (512 MB)	1 GB	4096	262144	128 KB	8 KB	256 KB	2 KB	128 B	4 KB

The Row Address is provided within Page Read commands. These commands select and transfer a page from the NAND Flash memory array into a RAM page cache. Transferring a page requires t_{RD} time. The Row Address is also provided by Program Execute and Block Erase commands to select the page location to be programmed from the data register, or the block to be erased.

The column address portion selects the starting byte location within the page cache for a transfer to or from the host system. The Column Address is provided within Read-From-Cache or Program-Load commands that read from or write to the cache. The CA is an address that is capable of addressing from 0 to 4095 Bytes; however, only Bytes 0 through 2112 to 2176 (depending on device density) are valid. Bytes 2113 or 2177 through 4095 of each page are reserved, do not physically exist in the device, and cannot be accessed.

The RA is always provided as a three byte address field in commands, and the CA is always provided as a two byte address field in commands. The RA & CA together form an overall byte or word address that can logically address up to 64 GBytes of memory space. However, the physical address space is limited to the available space of the device in use.

The highest order Row Address bit in use (RAmax) will vary with the memory density of the sNAND Family device. Higher order address bits in a command RA field, above RAmax, are reserved and must be filled with zeros. The highest order Column Address bit in use (CAmax), matches the page address space of the sNAND Family device. Higher order bits above CAmax, in a command CA field, are reserved and must be filled with zeros.

2.4.1 Address Cycle Maps

Addresses are 4 or 5 bytes in length and transfered in least to most significant byte order. A 4- or 5-byte address may be used for a 1Gbit device where a fifth byte is ignored. All higher densities require a 5-byte address. Higher order address bits not used by a given density must be zero. An address selects a byte of memory in a device with 8 bit IO. An address selects a 16-bit word of memory in a device with 16 bit IO. The least significant 2 bytes are called the column or intra-page address. The following more significant 2 or 3 bytes are referred to as the row address. The row address may be sub-divided into Page Address (PA) bits that select a page within a block, a Plane Address bit (PLA), and Block Address (BA) bits that select a block.

2.4.1.1 S34SL01G2

Table 2.4 Address Cycle Map — 1 Gb Device

Bus Cycle	I/O [15:8] (5)	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
x8									
1st / Col. Add. 1	—	A0 (CA0)	A1 (CA1)	A2 (CA2)	A3 (CA3)	A4 (CA4)	A5 (CA5)	A6 (CA6)	A7 (CA7)
2nd / Col. Add. 2	—	A8 (CA8)	A9 (CA9)	A10 (CA10)	A11 (CA11)	Low	Low	Low	Low
3rd / Row Add. 1	—	A12 (PA0)	A13 (PA1)	A14 (PA2)	A15 (PA3)	A16 (PA4)	A17 (PA5)	A18 (BA0)	A19 (BA1)
4th / Row Add. 2	—	A20 (BA2)	A21 (BA3)	A22 (BA4)	A23 (BA5)	A24 (BA6)	A25 (BA7)	A26 (BA8)	A27 (BA9)
x16									
1st / Col. Add. 1	Low	A0 (CA0)	A1 (CA1)	A2 (CA2)	A3 (CA3)	A4 (CA4)	A5 (CA5)	A6 (CA6)	A7 (CA7)
2nd / Col. Add. 2	Low	A8 (CA8)	A9 (CA9)	A10 (CA10)	Low	Low	Low	Low	Low
3rd / Row Add. 1	Low	A11 (PA0)	A12 (PA1)	A13 (PA2)	A14 (PA3)	A15 (PA4)	A16 (PA5)	A17 (BA0)	A18 (BA1)
4th / Row Add. 2	Low	A19 (BA2)	A20 (BA3)	A21 (BA4)	A22 (BA5)	A23 (BA6)	A24 (BA7)	A25 (BA8)	A26 (BA9)

Notes:

1. *CAx = Column Address bit.*
2. *PAx = Page Address bit.*
3. *BAx = Block Address bit.*
4. *Block address concatenated with page address = actual page address, also known as the row address.*
5. *I/O[15:8] are not used during the addressing sequence and should be driven Low.*

For the x8 address bits, the following rules apply:

- A0 - A11: column address in the page
- A12 - A17: page address in the block
- A18 - A27: block address

For the x16 address bits, the following rules apply:

- A0 - A10: column address in the page
- A11 - A16: page address in the block
- A17 - A26: block address

2.4.1.2 S34SL02G2

Table 2.5 Address Cycle Map — 2 Gb Device

Bus Cycle	I/O [15:8] (6)	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
x8									
1st / Col. Add. 1	—	A0 (CA0)	A1 (CA1)	A2 (CA2)	A3 (CA3)	A4 (CA4)	A5 (CA5)	A6 (CA6)	A7 (CA7)
2nd / Col. Add. 2	—	A8 (CA8)	A9 (CA9)	A10 (CA10)	A11 (CA11)	Low	Low	Low	Low
3rd / Row Add. 1	—	A12 (PA0)	A13 (PA1)	A14 (PA2)	A15 (PA3)	A16 (PA4)	A17 (PA5)	A18 (PLA0)	A19 (BA0)
4th / Row Add. 2	—	A20 (BA1)	A21 (BA2)	A22 (BA3)	A23 (BA4)	A24 (BA5)	A25 (BA6)	A26 (BA7)	A27 (BA8)
5th / Row Add. 3	—	A28 (BA9)	Low	Low	Low	Low	Low	Low	Low
x16									
1st / Col. Add. 1	Low	A0 (CA0)	A1 (CA1)	A2 (CA2)	A3 (CA3)	A4 (CA4)	A5 (CA5)	A6 (CA6)	A7 (CA7)
2nd / Col. Add. 2	Low	A8 (CA8)	A9 (CA9)	A10 (CA10)	Low	Low	Low	Low	Low
3rd / Row Add. 1	Low	A11 (PA0)	A12 (PA1)	A13 (PA2)	A14 (PA3)	A15 (PA4)	A16 (PA5)	A17 (PLA0)	A18 (BA0)
4th / Row Add. 2	Low	A19 (BA1)	A20 (BA2)	A21 (BA3)	A22 (BA4)	A23 (BA5)	A24 (BA6)	A25 (BA7)	A26 (BA8)
5th / Row Add. 3	Low	A27 (BA9)	Low	Low	Low	Low	Low	Low	Low

Notes:

1. *CAx = Column Address bit.*
2. *PAx = Page Address bit.*
3. *PLA0 = Plane Address bit zero.*
4. *BAx = Block Address bit.*
5. *Block address concatenated with page address and plane address = actual page address, also known as the row address.*
6. *I/O[15:8] are not used during the addressing sequence and should be driven Low.*

For the x8 address bits, the following rules apply:

- A0 - A11: column address in the page
- A12 - A17: page address in the block
- A18: plane address (for multiplane operations) / block address (for normal operations)
- A19 - A28: block address

For the x16 address bits, the following rules apply:

- A0 - A10: column address in the page
- A11 - A16: page address in the block
- A17: plane address (for multiplane operations) / block address (for normal operations)
- A18 - A27: block address

2.4.1.3 S34SL04G2

Table 2.6 Address Cycle Map — 4 Gb Device

Bus Cycle	I/O [15:8] (6)	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
x8									
1st / Col. Add. 1	—	A0 (CA0)	A1 (CA1)	A2 (CA2)	A3 (CA3)	A4 (CA4)	A5 (CA5)	A6 (CA6)	A7 (CA7)
2nd / Col. Add. 2	—	A8 (CA8)	A9 (CA9)	A10 (CA10)	A11 (CA11)	Low	Low	Low	Low
3rd / Row Add. 1	—	A12 (PA0)	A13 (PA1)	A14 (PA2)	A15 (PA3)	A16 (PA4)	A17 (PA5)	A18 (PLA0)	A19 (BA0)
4th / Row Add. 2	—	A20 (BA1)	A21 (BA2)	A22 (BA3)	A23 (BA4)	A24 (BA5)	A25 (BA6)	A26 (BA7)	A27 (BA8)
5th / Row Add. 3	—	A28 (BA9)	A29 (BA10)	Low	Low	Low	Low	Low	Low
x16									
1st / Col. Add. 1	Low	A0 (CA0)	A1 (CA1)	A2 (CA2)	A3 (CA3)	A4 (CA4)	A5 (CA5)	A6 (CA6)	A7 (CA7)
2nd / Col. Add. 2	Low	A8 (CA8)	A9 (CA9)	A10 (CA10)	Low	Low	Low	Low	Low
3rd / Row Add. 1	Low	A11 (PA0)	A12 (PA1)	A13 (PA2)	A14 (PA3)	A15 (PA4)	A16 (PA5)	A17 (PLA0)	A18 (BA0)
4th / Row Add. 2	Low	A19 (BA1)	A20 (BA2)	A21 (BA3)	A22 (BA4)	A23 (BA5)	A24 (BA6)	A25 (BA7)	A26 (BA8)
5th / Row Add. 3	Low	A27 (BA9)	A28 (BA10)	Low	Low	Low	Low	Low	Low

Notes:

1. *CAx = Column Address bit.*
2. *PAx = Page Address bit.*
3. *PLA0 = Plane Address bit zero.*
4. *BAx = Block Address bit.*
5. *Block address concatenated with page address and plane address = actual page address, also known as the row address.*
6. *I/O[15:8] are not used during the addressing sequence and should be driven Low.*

For the x8 address bits, the following rules apply:

- A0 - A11: column address in the page
- A12 - A17: page address in the block
- A18: plane address (for multiplane operations) / block address (for normal operations)
- A19 - A29: block address

For the x16 address bits, the following rules apply:

- A0 - A10: column address in the page
- A11 - A16: page address in the block
- A17: plane address (for multiplane operations) / block address (for normal operations)

A18 - A28: block address

3. System Interaction

There are several bus states and cycles that control the host system interaction with an sNAND Family device. See Section 10.1, *Interface States and Cycles* on page 60 for details of the signal levels and transitions that define all bus states and cycles. The following cycles and states are relevant to the software interface with the device: Command Input, Address Input, Data Input, Data Output, Busy, and Write Protect.

3.1 Command Input Cycle

The Command Input cycle is used to give a command to the memory device. Commands are accepted when Chip Enable low, Command Latch Enable high, Address Latch Enable low, and Read Enable high and I/O7:0 are all latched on the rising edge of Write Enable. Command codes are always applied only on I/O7:0 regardless of the bus configuration (x8 or x16). Moreover, for commands that start a modify operation (program/erase) the Write Protect pin must be high.

3.2 Address Input Cycle

The Address Input cycle allows the insertion of the memory address bytes. For the S34SL02G2 and S34SL04G2 devices, five write cycles are needed to input the address bytes. For the S34SL01G2, four write cycles are needed to input the address bytes. If necessary, a 5th dummy address cycle can be issued to S34SL01G2, which will be ignored by the NAND device without causing problems. Addresses are accepted with Chip Enable low, Address Latch Enable high, Command Latch Enable low, and Read Enable high with
I/ O7:0 all latched on the rising edge of Write Enable. Addresses are always applied on I/O7:0 regardless of the bus configuration (x8 or x16). Moreover, for commands that start a modify operation (program/erase) the Write Protect pin must be high.

3.3 Data Input Cycle

The Data Input cycle allows the data to be programmed to be sent to the device. The data insertion is serial and timed by the Write Enable signal. Data is accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable high, and Write Protect high and data all latched on the rising edge of Write Enable. Data is applied on I/O7:0 for x8 or, on I/O15:0 for x16, bus configuration.

3.4 Data Output Cycle

The Data Output cycle allows data to be read from the memory array and to check the Status Register content, and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable high, Address Latch Enable low, and Command Latch Enable low. Data is applied on
I/O7:0 for x8 or, on I/O15:0 for x16, bus configuration.

3.5 Busy State

During the initial read latency period of a page read command the memory will indicate busy status with the R/B# signal pulled low and status register bit 6 at zero. The RE# input must be high if data is not to be driven on the data I/O signals.

During the program or erase operations the memory will indicate busy status with the R/B# signal pulled low and status register bit 6 at zero. The WP# input from the host system must remain High throughout the operations to prevent abort of the operations. If the WP# input from the host does go low during a program or erase operation, the operation will be aborted, leaving the page being programmed or the block being erased in an intermediate state, potentially with unstable and invalid data values.

4. Operations

The host system sends sequences of command, address, and data bytes to an sNAND Family memory to control device behavior. Each completed sequence is called an operation. The operation command, address, and data sequences for each supported operation is described in this section.

4.1 Operation Command Cycles Summary

The commands cycles used in each operation are summarized in the Operation Set table. The address and data cycles are not shown in this summary table. The full sequence for each operation is shown in the individual command descriptions.

Multiplane operations affect two, even and odd address, blocks. If any protection method is protecting one of the blocks in the operation, both blocks will be treated as locked.

Table 4.1 Operation Set (Sheet 1 of 2)

Command	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	Acceptable Command during Busy	Supported on S34Sx01G2
Page Read	00h	30h			No	Yes
Page Program	80h	10h			No	Yes
Random Data Input	85h				No	Yes
Random Data Output	05h	E0h			No	Yes
ONFI Multiplane Program	80h	11h	80h	10h	No	No
Page Reprogram	8Bh	10h			No	Yes
Multiplane Page Reprogram	8Bh	11h	8Bh	10h	No	No
Block Erase	60h	D0h			No	Yes
ONFI Multiplane Block Erase	60h	D1h	60h	D0h	No	No
Copy Back Read	00h	35h			No	Yes
Copy Back Program	85h	10h			No	Yes
ONFI Multiplane Copy Back Program	85h	11h	85h	10h	No	No
Special Read For Copy Back	00h	36h			No	No
Read Status Register	70h				Yes	Yes
Read Status Enhanced	78h				Yes	No
Reset	FFh				Yes	Yes
Read Cache	31h				No	Yes
Read Cache Enhanced	00h	31h			No	Yes
Read Cache End	3Fh				No	Yes
Cache Program (End)	80h	10h			No	Yes
Cache Program (Start) / (Continue)	80h	15h			No	Yes
ONFI Multiplane Cache Program (Start/Continue)	80h	11h	80h	15h	No	No
ONFI Multiplane Cache Program (End)	80h	11h	80h	10h	No	No
Read ID	90h				No	Yes
Read ID2	30h-65h-00h	30h			No	Yes
Read ONFI Signature	90h				No	Yes
Read Parameter Page	ECh				No	Yes
Read Unique ID (Contact Factory)	EDh				No	Yes
One-time Programmable (OTP) Area Entry	29h-17h-04h-19h				No	Yes
Volatile Unlock Lower	23h				No	Yes
Volatile Unlock Upper	24h				No	Yes
Volatile Lock All	2Ah				No	Yes
Volatile Lock-down	2Ch				No	Yes

Table 4.1 Operation Set (Sheet 2 of 2) (Continued)

Command	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	Acceptable Command during Busy	Supported on S34Sx01G2
Block Lock Status (S34SL01G2/S34SL02G2/ S34SL04G2)	72h				No	Yes
Block Lock Status Alternate (S34SL02G2/ S34SL04G2)	7Ah				No	No

4.2 Page Read

Page Read is initiated by writing 00h and 30h to the command register along with five address cycles (four or five cycles for S34SL01G2). Two types of operations are available: random read and serial page read. Random read mode is enabled when the page address is changed. All data within the selected page are transferred to the data registers.

The system controller may detect the completion of this data transfer (t_R) by analyzing the output of the R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 25 ns cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE# signal makes the device output the data, starting from the selected column address up to the last column address.

The device may output random data in a page instead of the sequential data by writing Random Data Output command. The column address of next data, which is going to be out, may be changed to the address that follows Random Data Output command. Random Data Output can be performed as many times as needed.

After power up, the device is in read mode, so 00h command cycle is not necessary to start a read operation. Any operation other than read or Random Data Output causes the device to exit read mode.

See Figure 12.7 on page 73 and Figure 12.13 on page 77 as references.

4.3 Page Program

A page program cycle consists of a serial data loading period in which up to 2 KB (x8) or 1 kword (x16) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

A page program command must start from read mode. A 00h command cycle must be used to return to read mode before writing the page program command sequence. The rising edge of WE# in the 00h command must occur t_{WW} time before the rising edge of WE# in the Serial Data Input command (80h) that sets up the page programming operation.

The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs (four cycles for S34SL01G2) and then serial data. The words other than those to be programmed do not need to be loaded. The device supports Random Data Input within a page. The column address of next data, which will be entered, may be changed to the address that follows the Random Data Input command (85h). Random Data Input may be performed as many times as needed.

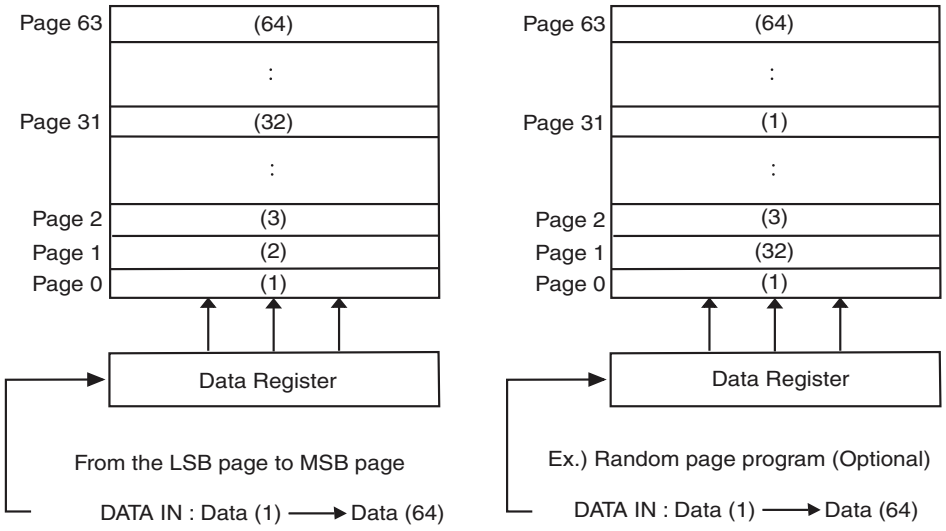
The Page Program confirm command (10h) initiates the programming process. The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks.

Once the program process starts, the Read Status Register commands (70h or 78h) may be issued to read the Status Register. The system controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. Only the Read Status commands (70h or 78h) or Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O0) may be checked. The internal write verify detects only errors for 1's that are not successfully programmed to 0's. The command register remains in Read Status command mode until another valid command is written to the command register. Figure 12.10 on page 75 and Figure 12.12 on page 76 detail the sequence.

The device is programmable by page, but it also allows multiple partial page programming of a word or consecutive bytes up 2 kbytes (x8) or 1 kword (x16) in a single page program cycle.

The number of consecutive partial page programming operations (NOP) within the same page must not exceed the number indicated Table 4.11 on page 36. Pages may be programmed in any order within a block.

Figure 4.1 Page Programming within a Block



If a Page Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted page is not used for further reading or programming operations until the next uninterrupted block erase is complete.

4.4 Multiplane Program

The 2 Gbit or higher density devices support Multiplane Program, making it possible to program two pages in parallel, one page per plane.

A multiplane program command must start from read mode. A 00h command cycle must be used to return to read mode before writing the multiplane program command sequence. The rising edge of WE# in the 00h command must occur t_{WW} time before the rising edge of WE# in the Serial Data Input command (80h) that sets up the first multiplane programming command.

A Multiplane Program cycle consists of a double serial data loading period in which up to 4352 bytes (x8) or 2176 words (x16) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins with inputting the Serial Data Input command (80h), followed by the five cycle address inputs and serial data for the 1st page. The address for this page must be in the 1st plane (PLA0 = 0). The device supports Random Data Input exactly the same as in the case of page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (t_{DBSY}). Once it has become ready again, the '80h' command must be issued, followed by 2nd page address (5 cycles) and its serial data input. The address for this page must be in the 2nd plane (PLA0 = 1). The Program Confirm command (10h) starts parallel programming of both pages. This is the ONFI protocol version of the Multiplane Program command. The legacy version of the Multiplane Program command, in which the first 80h command is followed by a zero address, is not supported.

Figure 12.14 on page 77 describes the sequences using the ONFI protocol. For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane.

The user can check operation status by monitoring R/B# pin or reading the Status Register (command 70h or 78h). The Read Status Register command is also available during Dummy Busy time (t_{DBSY}). In case of failure in either page program, the fail bit of the Status Register will be set. Refer to Section 4.9, *Read Status Register* on page 25 for further info.

The number of consecutive partial page programming operations (NOP) within the same page must not exceed the number indicated in Table 4.11 on page 36. Pages may be programmed in any order within a block.

If a Multiplane Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted pages are not used for further reading or programming operations until the next uninterrupted block erases are complete for the applicable blocks.

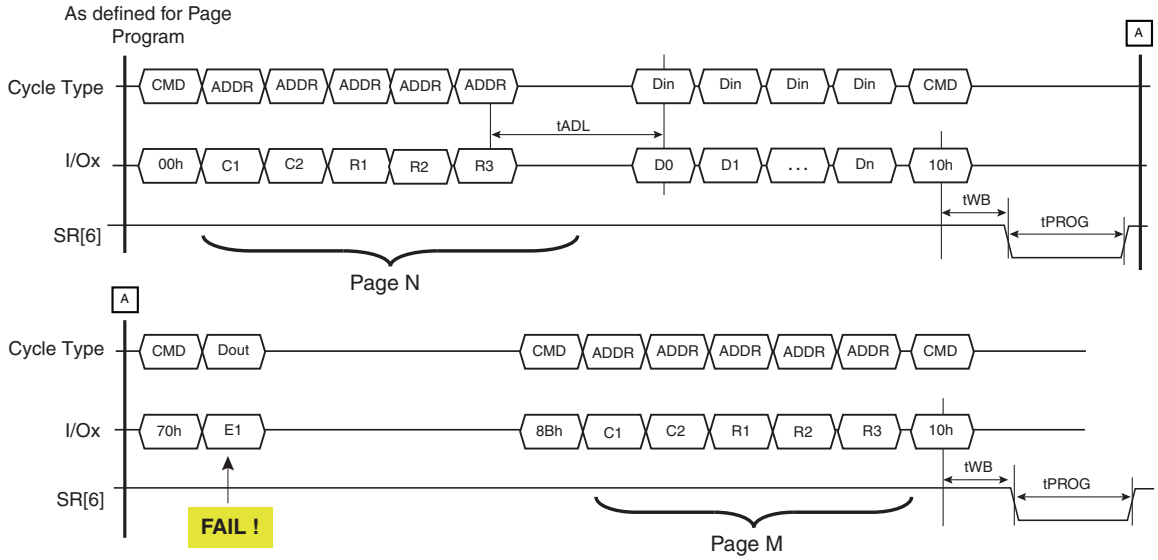
4.5 Page Reprogram

Page Program may result in a fail, which can be detected by Read Status Register. In this event, the host may call Page Reprogram. This command allows the reprogramming of the same pattern of the last (failed) page into another memory location.

A page reprogram command must start from read mode. A 00h command cycle must be used to return to read mode before writing the page reprogram command sequence. The rising edge of WE# in the 00h command must occur t_{WW} time before the rising edge of WE# in the page reprogram setup command (8Bh) that sets up the page reprogramming operation.

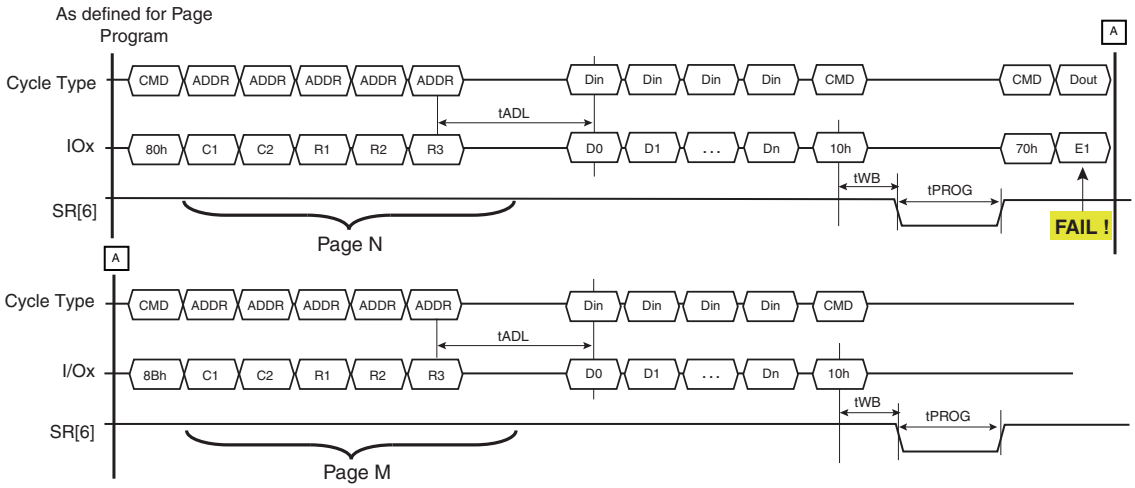
The command sequence initiates with reprogram setup (8Bh), followed by the five cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the last page, the program confirm can be issued (10h) without any data input cycle, as described in Figure 4.2.

Figure 4.2 Page Reprogram



On the other hand, if the pattern bound for the target page is different from that of the previous page, data in cycles can be issued before program confirm ‘10h’, as described in Figure 4.3.

Figure 4.3 Page Reprogram with Data Manipulation



The device supports Random Data Input within a page. The column address of next data, which will be entered, may be changed to the address which follows the Random Data Input command (85h). Random Data Input may be operated multiple times regardless of how many times it is done in a page.

The Program Confirm command (10h) initiates the re-programming process. The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be issued to read the Status Register. The system controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. Only the Read Status command and Reset command are valid when programming is in progress. When the Page Program is complete, the Write Status Bit (I/O0) may be checked. The internal write verify detects only errors for 1's that are not successfully programmed to 0's. The command register remains in Read Status command mode until another valid command is written to the command register.

The Page Reprogram must be issued in the same plane as the Page Program that failed. In order to program the data to a different plane, use the Page Program operation instead. The Multiplane Page Reprogram can re-program two pages in parallel, one per plane. The Multiplane Page Reprogram operation is performed after a failed Multiplane Page Program operation. The command sequence is very similar to Figure 12.14, *Multiplane Page Program (ONFI 1.0 Protocol)* on page 77, except that it requires the Page Reprogram Command (8Bh) instead of 80h.

If a Page Reprogram operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted page is not used for further reading or programming operations until the next uninterrupted block erase is complete.

4.6 Block Erase

The block erase command must start from read mode. A 00h command cycle must be used to return to read mode before writing the block erase command sequence. The rising edge of WE# in the 00h command must occur t_{WW} time before the rising edge of WE# in the block erase setup command (60hh) that sets up the block erase operation.

The Block Erase operation is done on a block basis. Block address loading is accomplished in three cycles (two cycles for S34SL01G2) initiated by an Erase Setup command (60h). Only the block address bits are valid while the page address bits are ignored.

The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by the execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase verify. Once the erase process starts, the Read Status Register commands (70h or 78h) may be issued to read the Status Register.

The system controller can detect the completion of an erase by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. Only the Read Status commands (70h or 78h) and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O0) may be checked. Figure 12.15 on page 78 details the sequence.

If a Block Erase operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted block is erased under continuous power conditions before that block can be trusted for further programming and reading operations.

4.7 Multiplane Block Erase

The 2 Gbit or higher density devices support Multiplane Erase. Multiplane Block Erase allows the erase of two blocks in parallel, one block per memory plane.

The multiplane block erase command must start from read mode. A 00h command cycle must be used to return to read mode before writing the multiplane block erase command sequence. The rising edge of WE# in the 00h command must occur t_{WW} time before the rising edge of WE# in the first multiplane block erase setup command (60hh) that sets up the block erase operation.

The Erase setup command (60h) is followed by the three cycle block address inputs for the 1st block. The address for this block must be in the 1st plane (PLA0 = 0). The Dummy Erase Confirm command (D1h) indicates this is a Multiplane Erase. Multiplane erase does not need any Dummy Busy Time between the1st and 2nd block Erase command. Then the second Erase setup (60h) command must be issued, followed by the 2nd Block address (3 cycles). The address for this block must be in the 2nd plane (PLA0 = 1). The Erase Confirm command (D0h) starts parallel erasing of both blocks. This is the ONFI protocol version of the Multiplane Erase command. The legacy version of the Multiplane Erase command, in which the block erase setup command (60h) is repeated two times without a D1h command, is not supported.

Figure 12.16, *Multiplane Block Erase (ONFI 1.0 Protocol)* on page 78 describes the sequences using the ONFI protocol. For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane.

The user can check operation status by monitoring R/B# pin or reading the Status Register (command 70h or 78h). The Read Status Register command is also available during Dummy Busy time (t_{DBSY}). In case of failure in either erase, the fail bit of the Status Register will be set.

If a Multiplane Block Erase operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted blocks are erased under continuous power conditions before those blocks can be trusted for further programming and reading operations.

4.8 Copy Back Program

The copy back feature is intended to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is greatly improved. The benefit is especially obvious when a portion of a block needs to be updated and the rest of the block also needs to be copied to the newly assigned free block. The operation for performing a copy back is a sequential execution of page-read (without mandatory serial access) and Copy Back Program with the address of destination page. A read operation with the ‘35h’ command and the address of the source page moves the whole page of data into the internal data register. As soon as the device returns to the Ready state, optional data read-out is allowed by toggling RE# (see Figure 12.17 on page 79), or the Copy Back Program command (85h) with the address cycles of the destination page may be written. The Program Confirm command (10h) is required to actually begin programming.

The source and destination pages in the Copy Back Program sequence must belong to the same device plane (same PLA0 for S34SL02G2 and S34SL04G2). Copy Back Read and Copy Back Program for a given plane must be between odd address pages or between even address pages for the device to meet the program time (t_{PROG}) specification. Copy Back Program may not meet this specification when copying from an odd address page (source page) to an even address page (target page) or from an even address page (source page) to an odd address page (target page).

The data input cycle for modifying a portion or multiple distinct portions of the source page is allowed as shown in Figure 12.18 on page 79.

If a Copy Back Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted page is not used for further reading or programming operations until the next uninterrupted block erase is complete.

4.8.1 Multiplane Copy Back Program

The 2 Gbit or higher density devices support Multiplane Copy Back Program with exactly the same sequence and limitations as the Page Program. Multiplane Copy Back Program must be preceded by two single page Copy Back Read command sequences (1st page must be read from the 1st plane and 2nd page from the 2nd plane).

Multiplane Copy Back cannot cross plane boundaries — the contents of the source page of one device plane can be copied only to a destination page of the same plane.

Figure 12.19 on page 79 describes the sequence using the ONFI protocol. For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane. The legacy Multiplane Copy Back protocol is not supported.

If a Multiplane Copy Back Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted pages are not used for further reading or programming operations until the next uninterrupted block erases are complete for the applicable blocks.

4.8.2 Special Read for Copy Back

The 2 Gbit or higher density devices support Special Read for Copy Back. If Copy Back Read (described in Section 4.8 and Section 4.8.1) is triggered with confirm command ‘36h’ instead ‘35h’, Copy Back Read from target page(s) will be executed with an increased internal (V_{PASS}) voltage.

This special feature is used in order to minimize the number of read errors due to over-program or read disturb — it shall be used only if ECC read errors have occurred in the source page using Page Read or Copy Back Read sequences.

Excluding the Copy Back Read confirm command, all other features described in Section 4.8 and Section 4.8.1 for standard copy back remain valid (including the figures referred to in those sections).

4.9 Read Status Register

The Status Register is used to retrieve the status value for the last operation issued. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two-line control allows the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. Refer to Section 4.2 on page 26 for specific Status Register definition, and to Figure 12.20 on page 80 for timings.

If the Read Status Register command is issued during multiplane operations then Status Register polling will return the combined status value related to the outcome of the operation in the two planes according to the following table:

Status Register Bit	Composite Status Value
Bit 0, Pass/Fail	OR
Bit 1, Cache Pass/Fail	OR

In other words, the Status Register is dynamic; the user is not required to toggle RE# / CE# to update it.

The command register remains in Status Read mode until further commands are issued. Therefore, if the Status Register is read during a random read cycle, the read command (00h) must be issued before starting read cycles.

Note: The Read Status Register command shall not be used for concurrent operations in multi-die stack configurations (single CE#). “Read Status Enhanced” shall be used instead.

Note that read status 70h is not supported during a Block Lock Status command read of block protection status.

4.10 Read Status Enhanced

The 2 Gbit or higher density devices support Read Status Enhanced. Read Status Enhanced is used to retrieve the status value for a previous operation in the specified plane.

Figure 12.21 on page 80 defines the Read Status Enhanced behavior and timings. The plane and die address must be specified in the command sequence in order to retrieve the status of the die and the plane of interest.

Refer to Table 4.2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued.

The Status Register is dynamic; the user is not required to toggle RE# / CE# to update it.

Note that read status 78h is not supported during a Block Lock Status command read of block protection status.

4.11 Read Status Register Field Definition

Table 4.2 below lists the meaning of each bit of the Read Status Register and Read Status Enhanced (S34SL02G2 and S34SL04G2).

Table 4.2 Status Register Coding

ID	Page Program / Page Reprogram	Block Erase	Read	Read Cache	Cache Program / Cache Reprogram	Coding
0	Pass / Fail	Pass / Fail	NA	NA	Pass / Fail	N Page Pass: 0 Fail: 1
1	NA	NA	NA	NA	Pass / Fail	N - 1 Page Pass: 0 Fail: 1
2	NA	NA	NA	NA	NA	—
3	NA	NA	NA	NA	NA	—
4	NA	NA	NA	NA	NA	—
5	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Internal Data Operation Active: 0 Idle: 1
6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy Busy: 0 Ready: 1
7	Write Protect	Write Protect	NA	NA	Write Protect	Protected: 0 Not Protected: 1

4.12 Reset

The Reset feature is executed by writing FFh to the command register. If the device is in the Busy state during random read, program, or erase mode, the Reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data may be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high or value 60h when WP# is low. If the device is already in reset state a new Reset command will not be accepted by the command register. The R/B# pin transitions to low for t_{RST} after the Reset command is written. Refer to Figure 12.22 on page 81 for further details. The Status Register can also be read to determine the status of a Reset operation.

When the OTP area is entered, the Reset operation only causes exit from the OTP area. When the OTP area is not entered, the Reset has no effect on non-volatile protection configuration.

4.13 Read Cache

Read Cache can be used to increase the read operation speed, as defined in Section 4.2 on page 19, and it cannot cross a block boundary. As soon as the user starts to read one page, the device automatically loads the next page into the cache register. Serial data output may be executed while data in the memory is read into the cache register. Read Cache is initiated by the Page Read sequence (00-30h) on a page M.

After random access to the first page is complete (R/B# returned to high, or Read Status Register I/O6 switches to high), two command sequences can be used to continue read cache:

- Read Cache (command ‘31h’ only): once the command is latched into the command register (see Figure 12.24 on page 82), device goes busy for a short time (t_{CBSYR}), during which data of the first page is transferred from the data register to the cache register. At the end of this phase, the cache register data can be output by toggling RE# while the next page (page address M+1) is read from the memory array into the data register.
- Read Cache Enhanced (sequence ‘00h’ <page N address> ‘31’): once the command is latched into the command register (see Figure 12.25 on page 82), device goes busy for a short time (t_{CBSYR}), during which data of the first page is transferred from the data register to the cache register. At the end of this phase, cache register data can be output by toggling RE# while page N is read from the memory array into the data register.

Subsequent pages are read by issuing additional Read Cache or Read Cache Enhanced command sequences. If serial data output time of one page exceeds random access time (t_R), the random access time of the next page is hidden by data downloading of the previous page.

On the other hand, if 31h is issued prior to completing the random access to the next page, the device will stay busy as long as needed to complete random access to this page, transfer its contents into the cache register, and trigger the random access to the following page.

To terminate the Read Cache operation, 3Fh command should be issued (see Figure 12.26 on page 82). This command transfers data from the data register to the cache register without issuing next page read.

During the Read Cache operation, the device doesn't allow any other command except for 00h, 31h, 3Fh, Read SR, or Reset (FFh). To carry out other operations, Read Cache must be terminated by the Read Cache End command (3Fh) or the device must be reset by issuing FFh.

Read Status command (70h) may be issued to check the status of the different registers and the busy/ready status of the cached read operations.

- The Cache-Busy status bit I/O6 indicates when the cache register is ready to output new data.
- The status bit I/O5 can be used to determine when the cell reading of the current data register contents is complete.

Note: The Read Cache and Read Cache End commands reset the column counter, thus, when RE# is toggled to output the data of a given page, the first output data is related to the first byte of the page (column address 00h). Random Data Output command can be used to switch column address.

4.14 Cache Program

Cache Program can improve the program throughput by using the cache register. The Cache Program operation cannot cross a block boundary. The cache register allows new data to be input while the previous data that was transferred to the data register is programmed into the memory array.

After the serial data input command (80h) is loaded to the command register, followed by five cycles of address, a full or partial page of data is latched into the cache register.

Once the cache write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in the Busy state for a short time (t_{CBSYW}). After all data of the cache register is transferred into the data register, the device returns to the Ready state and allows loading the next data into the cache register through another Cache Program command sequence (80h-15h).

The Busy time following the first sequence 80h - 15h equals the time needed to transfer the data from the cache register to the data register. Cell programming the data of the data register and loading of the next data into the cache register is consequently processed through a pipeline model.

In case of any subsequent sequence 80h - 15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete; till this moment the device will stay in a busy state (t_{CBSYW}).

Read Status commands (70h or 78h) may be issued to check the status of the different registers, and the pass/fail status of the cached program operations.

- The Cache-Busy status bit I/O6 indicates when the cache register is ready to accept new data.
- The status bit I/O5 can be used to determine when the cell programming of the current data register contents is complete.
- The Cache Program error bit I/O1 can be used to identify if the previous page (page N-1) has been successfully programmed or not in a Cache Program operation. The status bit is valid upon I/O6 status bit changing to 1.
- The error bit I/O0 is used to identify if any error has been detected by the program/erase controller while programming page N. The status bit is valid upon I/O5 status bit changing to 1.

I/O1 may be read together with I/O0.

If the system monitors the progress of the operation only with R/B#, the last page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O5 must be polled to find out if the last programming is finished before starting any other operation. See Table 4.2 on page 26 and Figure 12.27 on page 83 for more details.

If a Cache Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted pages are not used for further reading or programming operations until the next uninterrupted block erases are complete for the applicable blocks.

4.15 Multiplane Cache Program

The 2 Gbit or higher density devices support Multiplane Cache Program. The Multiplane Cache Program enables high program throughput by programming two pages in parallel, while exploiting the data and cache registers of both planes to implement cache.

The command sequence can be summarized as follows:

- Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (PLA0 = 0). The data of 1st page other than those to be programmed do not need to be loaded. The device supports Random Data Input exactly like Page Program operation.
- The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (t_{DBSY}).
- Once device returns to ready again, 80h command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be within 2nd plane (PLA0 = 1). The data of 2nd page other than those to be programmed do not need to be loaded.
- Cache Program confirm command (15h). Once the cache write command (15h) is loaded to the command register, the data in the cache registers is transferred into the data registers for cell programming. At this time the device remains in the Busy state for a short time (t_{CBSYW}). After all data from the cache registers are transferred into the data registers, the device returns to the Ready state, and allows loading the next data into the cache register through another Cache Program command sequence.

The sequence 80h-...- 11h...-...80h...-...15h can be iterated, and each time the device will be busy for the t_{CBSYW} time needed to complete programming the current data register contents, and transferring the new data from the cache registers. The sequence to end Multiplane Cache Program is 80h-...- 11h...-...80h...-...10h.

The Multiplane Cache Program is available only within two paired blocks in separate planes. Figure 12.28 on page 84 shows the ONFI protocol for the Multiplane Cache Program operation. For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane. Multiplane Cache programming cannot cross block boundaries.

The user can check operation status by R/B# pin or Read Status Register commands (70h or 78h). If the user opts for 70h, Read Status Register will provide “global” information about the operation in the two planes.

- I/O6 indicates when both cache registers are ready to accept new data.
- I/O5 indicates when the cell programming of the current data registers is complete.
- I/O1 identifies if the previous pages in both planes (pages N-1) have been successfully programmed or not. This status bit is valid upon I/O6 status bit changing to 1.
- I/O0 identifies if any error has been detected by the program/erase controller while programming the two pages N. This status bit is valid upon I/O5 status bit changing to 1.

See Table 4.2 on page 26 for more details.

If the system monitors the progress of the operation only with R/B#, the last pages of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O5 must be polled to find out if the last programming is finished before starting any other operation. Refer to Section 4.9 on page 25 for further information.

If a Multiplane Cache Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted pages are not used for further reading or programming operations until the next uninterrupted block erases are complete for the applicable blocks.

4.16 Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h.

Note: If you want to execute Read Status command (0x70) after Read ID sequence, you should input dummy command (0x00) before Read Status command (0x70).

For the S34SL02G2 and S34SL04G2 devices, five read cycles sequentially output the manufacturer code (01h), and the device code and 3rd, 4th, and 5th cycle ID, respectively. For the S34SL01G2 device, four read cycles sequentially output the manufacturer

code (01h), and the device code and 80h, 4th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 12.29 on page 85 shows the operation sequence, while Table 4.3 to Table 4.8 explain the byte meaning.

Table 4.3 Read ID for Supported Configurations

Density	Org	V_{CC}	1st	2nd	3rd	4th	5th
1 Gb	x8	3.3V	01h	F1h	80h	1Dh	—
2 Gb			01h	DAh	90h	95h	46h
4 Gb			01h	DCh	90h	95h	56h
1 Gb	x16		01h	C1h	80h	5Dh	—
2 Gb			01h	CAh	90h	D5h	46h
4 Gb			01h	CCh	90h	D5h	56h

Table 4.4 Read ID Bytes

Device Identifier Byte	Description
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell type, etc.
4th	Page Size, Block Size, Spare Size, Serial Access Time, Organization
5th **(S34SL02G2, S34SL04G2)**	ECC, Multiplane information

3rd ID Data

Table 4.5 Read ID Byte 3 Description

	Description	I/O7	I/O6	I/O5 I/O4	I/O3 I/O2	I/O1 I/O0
Internal Chip Number	1					00
	2					01
	4					10
	8					11
Cell type	2-level cell				00	
	4-level cell				01	
	8-level cell				10	
	16-level cell				11	
Number of simultaneously programmed pages	1			00		
	2			01		
	4			10		
	8			11		
Interleave program Between multiple chips	Not supported		0			
	Supported		1			
Cache Program	Not supported	0				
	Supported	1				

4th ID Data

Table 4.6 Read ID Byte 4 Description — S34SL01G2

	Description	I/O7	I/O6	I/O5 I/O4	I/O3	I/O2	I/O1 I/O0
Page Size (without spare area)	1 kB						0 0
	2 kB						0 1
	4 kB						1 0
	8 kB						1 1
Block Size (without spare area)	64 kB			0 0			
	128 kB			0 1			
	256 kB			1 0			
	512 kB			1 1			
Spare Area Size (byte / 512 byte)	8					0	
	16					1	
Serial Access Time	45 ns	0			0		
	25 ns	0			1		
	Reserved	1			0		
	Reserved	1			1		
Organization	x8		0				
	x16		1				

Table 4.7 Read ID Byte 4 Description — S34SL02G2 and S34SL04G2

	Description	I/O7	I/O6	I/O5 I/O4	I/O3	I/O2	I/O1 I/O0
Page Size (without spare area)	1 kB						0 0
	2 kB						0 1
	4 kB						1 0
	8 kB						1 1
Block Size (without spare area)	64 kB			0 0			
	128 kB			0 1			
	256 kB			1 0			
	512 kB			1 1			
Spare Area Size (byte / 512 byte)	16					0	
	32					1	
Serial Access Time	50 ns / 30 ns	0			0		
	25 ns	1			0		
	Reserved	0			1		
	Reserved	1			1		
Organization	x8		0				
	x16		1				

5th ID Data

Table 4.8 Read ID Byte 5 Description — S34SL02G2 and S34SL04G2

	Description	I/O7	I/O6 I/O5 I/O4	I/O3 I/O2	I/O1 I/O0
ECC Level	1 bit / 512 bytes 2 bit / 512 bytes 4 bit / 512 bytes 8 bit / 512 bytes				0 0 0 1 1 0 1 1
Plane Number	1 2 4 8			0 0 0 1 1 0 1 1	
Plane Size (without spare area)	64 Mb 128 Mb 256 Mb 512 Mb 1 Gb 2 Gb 4 Gb		0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0		
Reserved		0			

4.17 Read ID2

The device contains an alternate identification mode, initiated by writing 30h-65h-00h to the command register, followed by address inputs, followed by command 30h. The address for S34SL01G2 will be 00h-02h-02h-00h. The address for S34SL02G2 and S34SL04G2 will be 00h-02h-02h-00h-00h. The ID2 data can then be read from the device by pulsing RE#. The command register remains in Read ID2 mode until further commands are issued to it. Figure 12.30 on page 85 shows the Read ID2 command sequence. Read ID2 values are all 0xFs, unless specific values are requested when ordering from Cypress.

4.18 Read ONFI Signature

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values. Figure 12.31 on page 86 shows the operation sequence.

4.19 Read Parameter Page

The device supports the ONFI Read Parameter Page operation, initiated by writing ECh to the command register, followed by an address input of 00h. The host may monitor the R/B# pin or wait for the maximum data transfer time (t_R) before reading the Parameter Page data. The command register remains in Parameter Page mode until further commands are issued to it. If the Status Register is read to determine when the data is ready, the Read Command (00h) must be issued before starting read cycles. Figure 12.32 on page 86 shows the operation sequence, while Table 4.9 explains the parameter fields.

For x16 devices, the upper eight I/Os are not used and are 0xFF.

Note: For 32 nm Cypress NAND, for a particular condition, the Read Parameter Page command does not give the correct values. To overcome this issue, the host must issue a Reset command before the Read Parameter Page command. Issuance of Reset before the Read Parameter Page command will provide the correct values and will not output 00h values.

Table 4.9 Parameter Page Description (Sheet 1 of 3)

Byte	O/M	Description	Values
Revision Information and Features Block			
0-3	M	Parameter page signature Byte 0: 4Fh, “O” Byte 1: 4Eh, “N” Byte 2: 46h, “F” Byte 3: 49h, “I”	4Fh, 4Eh, 46h, 49h
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)	02h, 00h
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width	S34SL01G200 **(x8)**: 14h, 00h S34SL02G200 **(x8)**: 1Ch, 00h S34SL04G200 **(x8)**: 1Ch, 00h S34SL01G204 **(x16)**: 15h, 00h S34SL02G204 **(x16)**: 1Dh, 00h S34SL04G204 **(x16)**: 1Dh, 00h
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache commands 0 1 = supports Page Cache Program command	S34SL01G2: 33h, 00h S34SL02G2: 3Bh, 00h S34SL04G2: 3Bh, 00h
10-31		Reserved (0)	00h
Manufacturer Information Block			
32-43	M	Device manufacturer (12 ASCII characters)	53h, 50h, 41h, 4Eh, 53h, 49h, 4Fh, 4Eh, 20h, 20h, 20h, 20h
44-63	M	Device model (20 ASCII characters)	S34SL01G2: 53h, 33h, 34h, 53h, 4Ch, 30h, 31h, 47h, 32h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h S34SL02G2: 53h, 33h, 34h, 53h, 4Ch, 30h, 32h, 47h, 32h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h S34SL04G2: 53h, 33h, 34h, 53h, 4Ch, 30h, 34h, 47h, 32h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	M	JEDEC manufacturer ID	01h
65-66	O	Date code	00h
67-79		Reserved (0)	00h
Memory Organization Block			

Table 4.9 Parameter Page Description (Sheet 2 of 3) (Continued)

Byte	O/M	Description	Values
80-83	M	Number of data bytes per page	00h, 08h, 00h, 00h
84-85	M	Number of spare bytes per page	S34SL01G2: 40h, 00h S34SL02G2: 80h, 00h S34SL04G2: 80h, 00h
86-89	M	Number of data bytes per partial page	00h, 00h, 00h, 00h
90-91	M	Number of spare bytes per partial page	00h, 00h
92-95	M	Number of pages per block	40h, 00h, 00h, 00h
96-99	M	Number of blocks per logical unit (LUN)	S34SL01G2: 00h, 04h, 00h, 00h S34SL02G2: 00h, 08h, 00h, 00h S34SL04G2: 00h, 10h, 00h, 00h
100	M	Number of logical units (LUNs)	01h
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles	S34SL01G2: 22h S34SL02G2: 23h S34SL04G2: 23h
102	M	Number of bits per cell	01h
103-104	M	Bad blocks maximum per LUN	S34SL01G2: 14h, 00h S34SL02G2: 28h, 00h S34SL04G2: 50h, 00h
105-106	M	Block endurance	01h, 05h
107	M	Guaranteed valid blocks at beginning of target	01h
108-109	M	Block endurance for guaranteed valid blocks	01h, 03h
110	M	Number of programs per page	04h
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00h
112	M	Number of bits ECC correctability	04h
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	S34SL01G2: 00h S34SL02G2: 01h S34SL04G2: 01h
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	S34SL01G2: 00h S34SL02G2: 04h S34SL04G2: 04h
115-127		Reserved (0)	00h
Electrical Parameters Block			
128	M	I/O pin capacitance	0Ah
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1	S34SL: 1Fh, 00h

Table 4.9 Parameter Page Description (Sheet 3 of 3) (Continued)

Byte	O/M	Description	Values
131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0	S34SL: 1Fh, 00h
133-134	M	t_{PROG} Maximum page program time (µs)	BCh, 02h
135-136	M	t_{BERS} Maximum block erase time (µs)	10h, 27h
137-138	M	t_R Maximum page read time (µs)	S34SL01G2: 19h, 00h S34SL02G2: 1Eh, 00h S34SL04G2: 1Eh, 00h
139-140	M	t_{CCS} Minimum Change Column setup time (ns)	C8h, 00h
141-163		Reserved (0)	00h
Vendor Block			
164-165	M	Vendor specific Revision number	00h
166-253		Vendor specific	00h
254-255	M	Integrity CRC	S34SL01G200 **(x8)**: DAh, 14h S34SL02G200 **(x8)**: E4h, B0h S34SL04G200 **(x8)**: 9Ah, FBh
Redundant Parameter Pages			
256-511	M	Value of bytes 0-255	Repeat Value of bytes 0-255
512-767	M	Value of bytes 0-255	Repeat Value of bytes 0-255
768+	O	Additional redundant parameter pages	FFh

Note:
1. O" Stands for Optional, "M" for Mandatory.

4.20 Read Unique ID

The device supports the ONFI Read Unique ID function, initiated by writing EDh to the command register, followed by an address input of 00h. The host must monitor the R/B# pin or wait for the maximum data transfer time (t_R) before reading the Unique ID data. The first sixteen bytes returned by the flash is a unique value. The next sixteen bytes returned are the bit-wise complement of the unique value. The host can verify the Unique ID was read correctly by performing an XOR of the two values. The result should be all ones. The command register remains in Unique ID mode until further commands are issued to it. Figure 12.33 on page 87 shows the operation sequence, while Table 4.10 shows the Unique ID data contents.

Table 4.10 Unique ID Data Description (Contact Factory) (Sheet 1 of 2)

Byte	Description
0-15	Unique ID
16-31	ID Complement
32-47	Unique ID
48-63	ID Complement
64-79	Unique ID
80-95	ID Complement
96-111	Unique ID
112-127	ID Complement
128-143	Unique ID
144-159	ID Complement

Table 4.10 Unique ID Data Description (Contact Factory) (Sheet 2 of 2) (Continued)

Byte	Description
160-175	Unique ID
176-191	ID Complement
192-207	Unique ID
208-223	ID Complement
224-239	Unique ID
240-255	ID Complement
256-271	Unique ID
272-287	ID Complement
288-303	Unique ID
304-319	ID Complement
320-335	Unique ID
336-351	ID Complement
352-367	Unique ID
368-383	ID Complement
384-399	Unique ID
400-415	ID Complement
416-431	Unique ID
432-447	ID Complement
448-463	Unique ID
464-479	ID Complement
480-495	Unique ID
496-511	ID Complement

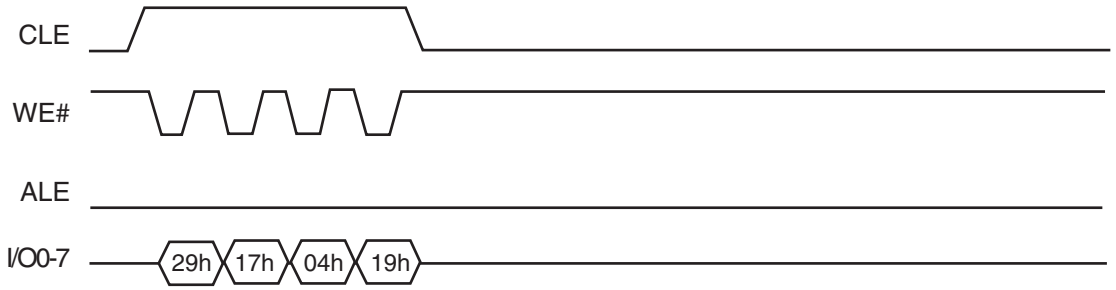
Note:

1. *For 32 nm Cypress NAND, for a particular condition, if read unique id does not give the correct values, the host must issue a Reset command before the read unique id command. Issuance of Reset before the read unique id command will provide the correct values and will not output false values.*

4.21 One-Time Programmable (OTP) Entry

The device contains a one-time programmable (OTP) area, which is accessed by writing 29h-17h-04h-19h to the command register. The device is then ready to accept Page Read and Page Program commands (refer to *Page Read* and *Page Program* on page 19). The OTP area is of a single erase block size (64 pages), and hence only row addresses between 00h and 3Fh are allowed. The host must issue the Reset command (refer to *Reset* on page 26) to exit the OTP area and access the normal flash array. The Block Erase command is not allowed in the OTP area. Refer to Figure 4.4 for more detail on the OTP Entry command sequence.

Figure 4.4 OTP Entry Sequence



4.22 One-Time Programmable (OTP) Lock

The OTP area is permanently protected from further programming when the OTP Lock command is sent by writing a command byte sequence to the command register. The device goes busy while locking the OTP area.

The command details are provided under a Non-disclosure Agreement, contact a local sales office for further information on implementing the OTP lock command.

4.23 Program / Erase Characteristics

Table 4.11 Program / Erase Characteristics

Parameter		Description	Min	Typ	Max	Unit
Program Time / Multiplane Program Time (2)		t_{PROG}	—	300	700	µs
Dummy Busy Time for Multiplane Program (**S34SL02G2, S34SL04G2)**		t_{DBSY}	—	0.5	1	µs
Cache Program short busy time		t_{CBSYW}	—	5	t_{PROG}	µs
Number of partial Program Cycles in the same page	Main + Spare	NOP	—	—	4	Cycle
Block Erase Time / Multiplane Erase Time (**S34SL02G2, S34SL04G2)**		t_{BERS}	—	3.5	10	ms
Block Erase Time (**S34SL01G2)**		t_{BERS}	—	3	10	ms
Read Cache busy time (**S34SL01G2)**		t_{CBSYR}	—	3	t_R	µs
Read Cache busy time (**S34SL02G2, S34SL04G2)**		t_{CBSYR}	—	5	t_R	µs

Notes:

1. *Typical program time is defined as the time within which more than 50% of the whole pages are programmed (V_{CC} = 3.3V, 25°C).*
2. *Copy Back Read and Copy Back Program for a given plane must be between odd address pages or between even address pages for the device to meet the program time (t_{PROG}) specification. Copy Back Program may not meet this specification when copying from an odd address page (source page) to an even address page (target page) or from an even address page (source page) to an odd address page (target page).*

5. Protection Overview

The sNAND Family provides three categories of block granularity protection: volatile, non-volatile, and permanent. The volatile protection settings can be altered by software as needed during system operation or trusted boot code can configure the desired protection and then lock-down the protection until the device is powered down. Non-volatile protection settings are preserved across power cycles but can be erased and redefined. Permanent protection settings are irreversible.

Volatile protection provides a single range of blocks that can be defined to start and end on any block boundary so that the size of the range is unlimited. The range can be set to unlock blocks within the range or to lock the blocks within the range and unlock all other blocks. After the range is defined a command can be issued to lock-down the defined volatile protection so that the range cannot be modified until power is turned off and back on again.

Non-volatile protection is controlled by parameters, programmed by the host system, to a specific location in the NAND memory. After POR, the host system reads these parameters from the NAND memory to transfer the parameters values to the security controller logic during the read access. Until the protection parameters are read, all blocks are protected by default. The parameters define the overall non-volatile protection range of blocks, the protection methods that can be applied within the non-volatile range, and whether each method is enabled:

- Single fixed block range protection
- Single expandable block range protection
- Non-volatile individual block protection

Any particular block may be protected by more than one method i.e. protection ranges may overlap on the same block. The protection method precedence order, from highest to lowest is:

- Non-volatile protection - a block locked by any of the non-volatile methods cannot be unlocked by any other method.
- Volatile protection in lock-down state - a block not locked by a non-volatile method can be locked or unlocked by the volatile method. The WP# input is ignored in the volatile lock-down state.
- Volatile protection WP# override - when volatile protection is enabled but not in the lock-down state, driving the WP# input low will invalidate the volatile unlock range, and protect all blocks.
- Volatile protection - when volatile protection is enabled and WP# remains high, the volatile protection method may unlock blocks that are not protected by the non-volatile methods.

Permanent protection can be provided by permanently protecting the area of memory where the protection parameters are stored, so that no further changes can be made to the non-volatile protection settings.

It is required that the non-volatile protection parameter loading be completed by trusted boot code before releasing control of the system to any other code. After the non-volatile protection parameters are loaded and valid the configured protection cannot be changed while power remains within the operating range. A power down and power up cycle is required to clear the non-volatile protection parameters to the default all blocks protected state and enable protection parameters to again be loaded by trusted boot code.

Additionally, the NAND legacy protection methods remain available:

- When the volatile protection is disabled or not locked down, the Write Protect (WP#) input low level is used to protect all blocks. It is recommended, but not required, to drive the WP# input low during power on, POR, and power off, as an extra level of protection.
- Secure NAND continues support of the legacy separate OTP block, this block can be protected independent of the other sNAND Family protection methods.

6. Data Protection Methods

All main Flash memory array blocks are protected against program or erase operations (locked) by default during and after POR. Individual blocks or ranges of blocks can be unprotected (unlocked) to allow program or erase operations on those blocks. Blocks may be unlocked by signal, volatile, and non-volatile methods. If any enabled method is protecting a block, that block remains locked even though another method may not be locking the block. The address loaded in to the stacked NAND memory as part of a program or erase operation is captured by the controller and compared with the addresses of blocks unlocked by each protection method. If the selected block is unlocked, a program or erase confirm command is allowed to initiate the operation. If the selected block is locked, the program or erase confirm operations are ignored, preventing program or erase operations from starting and the R/B# from going low.

Volatile configuration registers are used to control each method of protection during power-on time. The registers are loaded by the host system either by commands or by reading protection configuration parameters from non-volatile memory. These volatile protection control registers are referred to as Protection Management Registers (PMR).

6.1 Volatile Range Protection

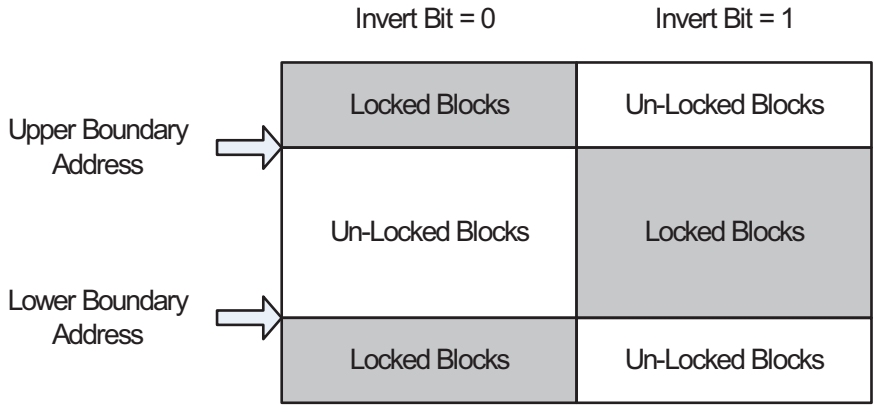
The Volatile Protection Enable (VPE) and WP# input levels are examined when a volatile protection command is received, to determine whether the sNAND Family volatile protection command can be accepted. If the VPE input is Low or WP# is Low when a volatile protection command is received, the volatile protection command is ignored or the volatile range is made invalid. If VPE is High and WP# is High when a volatile protection command is received, the command is accepted if the volatile protection method is not yet locked down. If the volatile protection method is locked down the volatile protection command is ignored.

The POR default state has the Volatile Protection method disabled, not locking any block. However, all blocks are locked by the POR default state of the Non-volatile Protection method. The Volatile Unlock Lower and Upper commands must be received with VPE High and WP# High to enable the Volatile Protection Method. The Non-Volatile Protection parameters must also be read from NAND memory to define which blocks are not locked by the Non-Volatile method, so that the Volatile Protection method may control the blocks not locked by the Non-Volatile method.

The Unlock Lower operation defines the lower address boundary for a range of blocks that are unlocked and may be programmed or erased. The Unlock Upper operation defines the upper address boundary for the range of unlocked blocks.

The least significant bit (LSB) of the Unlock Upper address indicates whether the range of unlocked blocks is *inclusive* – including the lower and upper addressed blocks and all blocks between the lower and upper boundary blocks or, *exclusive* – unlocking all blocks above the upper boundary block and below the lower boundary block. When the Unlock Upper address LSB (invert bit) = 0, the unlocked range is inclusive of the boundary blocks. When the LSB = 1, the unlocked range is exclusive (inverted) and begins with the block above the upper boundary address block, extends to the highest address block, then wraps around to the lowest address block, and continues through the block below the lower boundary address block.

Figure 6.1 Unlock Range Options



Blocks can be selectively locked again by writing the Unlock Lower and Unlock Upper commands to change the lower and upper boundary addresses. All blocks can be locked by writing the Lock All blocks command, writing the reset command, or by driving the

WP# input low. When these events occur, the unlock boundary addresses are made invalid, requiring new Unlock Lower and Unlock Upper operations to unlock blocks again.

The volatile protection commands can be disabled by the Lock-down operation to preserve the current unlocked range settings until the next Power On Reset (POR). When locked-down no changes can be made to volatile protection. The reset command will not change locked-down volatile protection configuration. The WP# input does not override or change locked-down volatile protection configuration.

Writing a reset command when the NAND OTP area is entered, will only exit the OTP area and will not affect any of the protection methods current state. A reset command does not change any of the volatile protection configuration when volatile protection is locked-down. Only a V_{CC} drop below V_{RST} for t_{PD} will initiate a POR to release volatile protection from the lock-down state and return the volatile protection configuration to its default state. A Reset command received when volatile protection is not locked-down, invalidates the volatile range and locks all blocks. Following such a Reset, volatile protection must be reloaded with a valid address range value.

If volatile range protection will not be used, the volatile lock down command should be used to lock down the volatile protection in the default disabled state to prevent Reset commands or malicious code from later enabling volatile range protection.

6.1.1 Volatile Unlock Lower and Unlock Upper

The Unlock Lower operation (command 23h) and Unlock Upper operation (command 24h) together define the range of blocks to be unlocked. The Unlock Lower operation must always precede the Unlock Upper operation. Each Unlock command is followed by a three byte address to select the block at the boundary of unlocked blocks. The LSB (invert-bit) in the address following the Unlock Upper command selects the inclusive or exclusive nature of the unlocked block range. If the invert-bit is set to 0 the address selected blocks are within the unlocked range; in contrast, if the invert-bit is set to 1, the selected blocks are outside the unlocked range. If the Unlock operations are issued again, the new address values replace the previous values to modify the unlock range. The unlock operations must both be issued in the order of lower then upper. The lower boundary address must be less than or equal to the upper boundary address. Only when both operations have been issued at least once is the unlock range valid. The Lock All operation or WP# input going low will invalidate both upper and lower addresses.

Table 6.1 Address Cycle Definition of Unlock Operations (x8 IO)

Address Cycle	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
Row Address 1	Invert Bit (1)	0	0	0	0	0	A18	A19
Row Address 2	A20	A21	A22	A23	A24	A25	A26	A27
Row Address 3	A28	A29	A30	A31	0	0	0	0

Note:
1. The Invert bit is set only by the 24h command, the bit can be 0 or 1 in the 23h command address.

Table 6.2 Address Cycle Definition of Unlock Operations (x16 IO)

Address Cycle	IO[15:8]	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
Row Address 1	X	Invert Bit (1)	0	0	0	0	0	A17	A18
Row Address 2	X	A19	A20	A21	A22	A23	A24	A25	A26
Row Address 3	X	A27	A28	A29	A30	0	0	0	0

Notes:
1. The Invert bit is set only by the 24h command, the bit can be 0 or 1 in the 23h command address.
2. IO[15:8] is relevant only for 16 bit wide IO devices.

6.1.2 Volatile Lock All Blocks

The Volatile Lock All operation (command 2AH) locks all Blocks in the memory array by invalidating the lower and upper unlock addresses, protecting all blocks from programming or erasure.

Figure 6.2 Volatile Unlock Block Operation Sequence

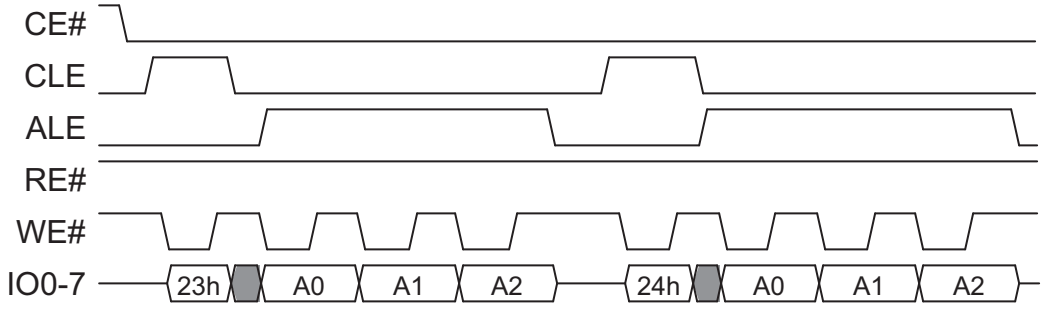
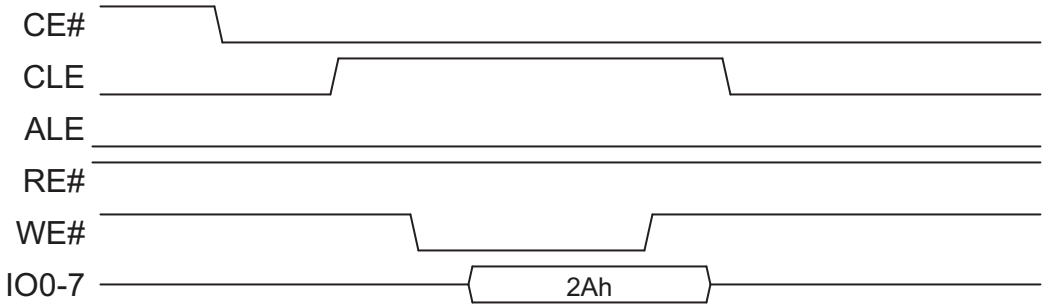


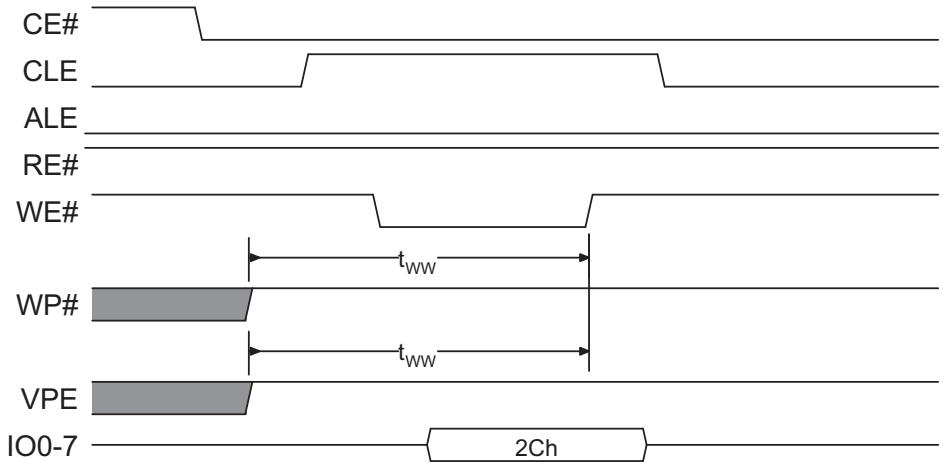
Figure 6.3 Volatile Lock All Blocks Operation Sequence



6.1.3 Volatile Lock-down

The volatile Lock-down (command 2Ch) disables all volatile protection operations thereby maintaining the existing volatile block unlock settings; which means the locked blocks cannot be unlocked and the unlocked blocks cannot be locked. The volatile protection operations remain disabled until the next POR. The WP# and VPE inputs must be high t_{WW} time before the rising edge of WE# when writing the Lock-down command.

Figure 6.4 Volatile Lock-Down Operation Sequence



6.2 Non-Volatile Protection

Non-volatile parameters that control block protection are stored in specific locations in the NAND memory. The block location used depends on a configuration register bit.

The sNAND Family device protection controller logic recognizes the address of a read command selecting the location for the protection parameters so that when these parameters are read by the host, they will also be captured by the sNAND Family protection controller to configure the non-volatile protection methods.

The protection parameters are accepted only from the configuration bit selected block. Programming of pages in this block, or erase of the block, is allowed only when other configuration register bits indicate that the block is enabled for program or erase. After the parameter block program and erase are disabled by the configuration register bit parameter values stored in NAND memory, the parameters are permanent.

Until the protection parameters are read, all blocks are protected by default. Non-volatile protection is always enabled and has precedence over the volatile method and the WP# input. If a block is protected by the non-volatile method, the block is locked even though the volatile method or WP# may indicate the block is not locked.

The protection parameters must not be read while the NAND indicates it is busy with an operation. Read accesses are ignored by the NAND during busy status and read data is not driven on the IO signals. The IO signals in this situation are left floating. Attempting to read the protection parameters during busy status would result in loading undefined data (noise) as the protection parameters. This would cause the non-volatile protection parameters to be invalid and leave all blocks protected.

Writing a reset command when the NAND OTP area is not entered, has no effect on the non-volatile protection methods current state. The protection state remains the same. Only a power off to power on cycle will clear the Protection Management Registers that hold the protection state during power on. Writing a reset command when the NAND OTP area is entered, will only exit the OTP area and will not affect any of the protection methods current state.

The non-volatile protection parameters define:

- **Non-volatile Configuration:** Setting of the non-volatile sNAND Family protection controller configuration register. The configuration includes enable bits for the non-volatile individual block, fixed range, and expandable range parameter protection methods.
- **Non-volatile Protection Range Base:** A boundary below which blocks may never be protected by the non-volatile protection method.
- **Non-volatile Protection Range Limit:** A boundary above which blocks may never be protected by the non-volatile protection method. The protection range ensures that malicious code cannot permanently lock blocks outside the range that must remain available for program and erase during normal system operation.
- **Non-volatile Fixed Range:** A single range of blocks defined to start and end on any block boundary within the protection range so that the size of the fixed range is unlimited within the non-volatile protection range.
- **Non-volatile Expandable Range:** A single contiguous range of blocks defined to start and end on any block boundary so that the size of the range is unlimited within the non-volatile protection range. The range is initially set by a base block address and a limit block address. The range can be incrementally expanded by programming additional limit addresses that are greater than previous limit address. Each additional larger address incrementally extends the range. Programming an address of 000000h ends the ability to read additional extension addresses. This prevents the Expandable range from further extension by malicious code.

6.2.1 Non-Volatile Protection Configuration (NVPC)

The protection configuration parameter is used to disable or enable the desired non-volatile protection methods.

Table 6.3 Non-volatile Protection Configuration Parameter

Bits	Field Name	Function	Default State	Description
15	NVPCRV	Non-Volatile Protection Configuration Register Valid	FF37h	1 = This protection configuration register is not valid. (default) 0 = This protection configuration register is valid.
14	NVPV	Non-volatile Parameters Valid		1 = The enabled protection parameters are not valid. All blocks are protected. (default) 0 = All enabled protection parameters are valid. This value is set by integrity checking logic after all protection parameter values are loaded. All enabled protection methods must have valid register values.
13 to 8	RFU	Reserved		Reserved for Future Use
7	MPCE	Multi-Plane Command Enable		1 = Multi-plane commands are enabled 0 = Multi-plane commands are disabled (default)
6	NVPBPE	Non-volatile Parameter Block Program-Erase Enable		1 = Parameter Block may be programmed or erased 0 = Parameter Block cannot be programmed or erased (default)
5	IOW	IO Width		1 = IO is 8 bits wide (default) 0 = IO is 16 bits wide
4	RFU	Reserved		Must be set to one.
3	PPL	Protection Parameter Location		1 = Protection Parameters are located in block 1, page 63, location 0) 0 = Protection Parameters are located in the OTP area, page 63, location 0 (default) If the OTP area page 63 is not programmed yet, all bytes are = FFh and reading the OTP area for parameters will change this bit to 1 to enable block 1 to then be checked for protection parameters.
2	NVERD	Non-volatile Expandable Range Disable		1 = The expandable range protection feature is disabled (default) 0 = The expandable range protection feature is enabled
1	NVFRD	Non-volatile Fixed Range Disable		1 = The fixed range protection feature is disabled (default) 0 = The fixed range protection feature is enabled
0	RFU	Reserved		Must be set to one.

Bit 15 is used to indicate whether the NVPC configuration register has valid configuration information. After POR, this bit is set to 1 to indicate that the configuration register is not valid and all blocks are protected.

Bit 14 is used to indicate whether all enabled non-volatile protection methods have valid register values. If any register needed for an enabled non-volatile protection method is not valid, this bit is =1 and all blocks are protected. If either the Non-Volatile Range Base (NVRB) or Limit (NVRL) registers is not valid, all blocks in the memory remain protected by default. If bits 2:0 are 1, no non-volatile protection method is enabled, bit 14 is then =0 to indicate no other non-volatile parameter registers need to be valid and, no blocks are locked by the non-volatile methods.

Bits 13 to 8 of the configuration parameter are reserved for future use.

Bits 7 (MPCE) controls whether multi-plane program or erase commands are enabled. When bit 7 is set to 1, multi-plane commands are enabled, requiring that even and odd address block pairs must be protected i.e. the minimum protection granularity is two adjacent blocks. The value of an individual block lock location will apply to both blocks in an even & odd address block pair when a multi-plane command is executed. When bit 7 is cleared to 0, multi-plane commands are prevented from executing and the minimum protection granularity is a single block. Note that the 1 Gbit density device does not support multi-plane command and it is required that bit 7 be cleared to 0 when using the 1 Gbit device.

Bit 6 controls protection for the block where all the protection parameters are stored. This protection control is independent of the other protection methods, except that WP# Low will protect the protection parameter block, unless volatile protection is enabled and locked down. Bit 6 is used to permanently disable program or erase of the current parameter block, when cleared to 0.

When set to 1, bit 6 allows for multiple program-erase cycles of the protection parameters, when the protection parameters are stored in block 1, during system development. Or, incremental programming of range extension addresses in block1. The

independent protection of the parameter block allows the parameter block to be in an area what would otherwise be permanently unlocked.

Bit 5 indicates the IO width as 8 or 16 bits.

Bit 3 selects the location from which the protection parameters will be accepted. After POR, this bit is cleared to 0 to select the NAND OTP area, page 63, location 0, as the starting point for the protection parameters. If this bit is set to 1, the protection parameters are accepted from block 1, page 63, location 0, instead.

Using the OTP area page 63, allows the protection parameters to be outside the main Flash array so that there is no conflict with legacy software use of the Flash array. The OTP area is guaranteed good and is programmable but not erasable.

When the NAND OTP area is used for protection parameters, the legacy NAND OTP protection command may also be used to permanently lock the NAND OTP area, after all updates to the protection parameters and all other portions of the OTP area are completed.

Using block 1 page 63, allows the protection parameters to be programmed and erased during system development and testing. Block 1 is guaranteed good for up to 1K program and erase cycles.

When the NVPC register is valid (NVPC[15]=1) and bit 3 is set to 1, the OTP area is protected from programming. This prevents alteration of the OTP area while block 1 is in use as the protection parameter block.

Bits 1 to 2 individually enable the fixed range, or expandable range protection methods. When Bit 1 is cleared to 0, the fixed range protection feature is enabled. When Bit 2 is cleared to 0, the expandable range protection feature is enabled. The PMR related to methods that are not enabled, are considered invalid i.e. they need not be read and, if read, will not be loaded, since those registers are not in use.

6.2.2 Density Mask

The size of the NAND memory array must be known so that all block addresses above the physical memory array are locked to prevent aliasing of any lower address unlocked block addresses. The density mask is a single byte of address that is used to mask the third row address (R3) to the array size. Bits in this address byte are 0 for row address bits that are not valid for the array size and 1 for the valid array address bits. For 1 Gbit density devices, the addresses used with commands, that use row addresses, require only the R1 and R2 addresses to be provided; the R3 address is optional, if R3 is provided, it is masked (ignored).

Table 6.4 Density Mask Values

Density (Gbit)	Mask Bits 7:0 (Binary)
1	00000000
2	00000001
4	00000011
8	00000111
16	00001111

6.2.3 Non-Volatile Range Boundaries

The space available for non-volatile protection is defined by the non-volatile range base (NVRB) and limit (NVRL) block address parameters. The limit address follows the base address. Each address is three bytes of NAND row address in low to high order byte order.

If one or more of the non-volatile protection methods are enabled and the base address is greater than the limit address, the non-volatile range is invalid, NVPC[14] will be set to one and all blocks in the memory array remain protected by default. When all non-volatile protection methods are disabled (NVPC[2:0]=111b), NVPC[14] is cleared to 0 and no blocks are locked by the non-volatile protection methods - the non-volatile range boundaries are don't care in this case.

6.2.4 Non-Volatile Individual Block Protection

An option exists for blocks within the non-volatile range boundary to be individually locked. For additional information on how to enable and use this feature, contact a sales representative. Obtain the latest list of company locations and contact information at:

http://www.spansion.com/About/Pages/Locations.aspx or
http://www.cypress.com/?id=7&source=footer

6.2.5 Non-Volatile Fixed Range Protection

The fixed range protection feature must be enabled by the non-volatile configuration NVFRD bit.

Blocks within the non-volatile range boundary can be locked as a separate group by fixed range protection. The fixed range is defined by base (NVFRB) and limit (NVFRL) block address parameters. Each address is three bytes of NAND row address in low to high byte order. The base address must be less than or equal to the limit address to be valid. The addresses must define a range within the overall non-volatile range boundaries.

6.2.6 Non-Volatile Expandable Range Protection

The expandable range protection feature must be enabled by the non-volatile configuration NVERD bit.

Blocks within the non-volatile range boundary can be locked as an additional separate group by expandable range protection. The initial expandable range is defined by base (NVERB) and limit (NVERL) block address parameters. Each address is three bytes of NAND row address in low to high byte order. The base address must be less than or equal to the limit address to be valid.

The range can be expanded by writing a new limit address in the NVERL parameter of the next lower page in the parameter block (current parameter page address minus 1). After the expandable range limit is loaded, only the next lower page will be recognized when reading protection parameter page. The NVERL value in the new page is read as a new limit address to replace the current limit address. This allows incremental expansion of the range as more data is added that needs permanent protection. After a new limit address is loaded, the parameter page address is decremented, then only the next lower page will be recognized as the parameter page address.

Each additional new limit address must be equal or greater than the previous limit address. If a new limit address is less than the prior limit, the value is not accepted and the parameter page address is decremented. Programming an additional NVERL address that lies outside the protection range protects only blocks within the protection range that are between the expandable range base (NVERB) and the protection range limit (NVRL) but, does not protect any blocks beyond the protection range limit.

When the Expandable Range Limit (NVERL) address is read as zero (000000h), the ability to extend the expandable range by reading any lower address page is ended and the end of the expandable range is fixed at the previous valid NVERL value.

The addresses must define a range within the overall non-volatile range boundaries.

6.2.7 Non-Volatile Protection Parameter Integrity

The protection parameters are captured directly from the NAND dice during a host system read access. The sNAND Family protection controller logic uses a combination of single-bit Error Correction Code (ECC), with double-bit error detection, per parameter byte, and data redundancy, to protect the integrity of each byte in the parameter data.

Each parameter byte is combined with it's related ECC and stored as a 16-bit unit.

Table 6.5 Format of Each Non-volatile Parameter Unit

Bits	Field Name	Function	Default State	Description
15 to 13	RFU	Reserved	FFFFh	Reserved for Future Use - must be set to ones.
12 to 8	ECC P[4:0]	Error Correction Code		ECC parity bits P[4:0]. Single bit error correction code for data bits 7 to 0. A two bit error detection invalidates the data in this parameter byte copy.
7 to 0	Data	Byte of Parameter		Parameter data bits

Users must calculate the ECC parity bits (P[4:0]) for each parameter byte unit according to the below equations, where an exclusive OR operation is indicated by the carrot symbol (^):

P4=P3^P2^P1^P0^D7^D6^D5^D4^D3^D2^D1^D0
P3=D7^D6^D5^D4
P2=D7^D3^D2^D1
P1=D6^D5^D3^D2^D0
P0=D6^D4^D3^D1^D0

Three copies of each parameter byte unit are stored sequentially. As the parameter byte units are read, the copies are error detected and corrected, then compared. Two or more of the copies must be valid (with no double-bit error detected) and match, for the data byte to be loaded into a Protection Management Register (PMR) in the controller as valid information. All bytes belonging to a PMR must be valid for that register to be considered valid.

If any of the enabled protection method related PMRs does not get valid data, all blocks within the non-volatile protection range set by NVRB and NVRL, remain protected by NVPC[14] remaining set to 1. If either the NVRB or NVRL registers is not valid, all blocks in the memory remain protected by default. Only when NVRB, NVRL, and all enabled non-volatile PMRs have been loaded with valid information is NVPC[14] cleared to 0.

Following POR, the protection parameters may be read only from the highest address page of the OTP area. A Reset command received when the OTP area is entered, only exits the OTP area.

If any of the enabled PMRs are not valid after reading all enabled PMRs from the protection parameter page, the protection parameter page pointer may be decremented to allow reading of the next lower address page. This allows for multiple back-up copies of the protection parameter page in successively lower address pages of the protection parameter block. The parameter page pointer is decremented when the NVERL parameter is read and its value is not 000000h.

When a PMR is valid it will no longer accept data from the current protection parameter page. Only a PMR that still is not valid will accept valid data from the current protection parameter page. This prevents any lower address parameter page back-up copy from changing a parameter value that has already been read as valid in a previously read higher address page. However, there is one exception:

- The NVERL parameter may be loaded with valid data from multiple copies of the protection parameter page in order to extend the expandable range, until NVERL is read and its value is 000000h.

6.2.8 Non-Volatile Parameter Block Format

Each incrementally lower address page in the protection parameter block is required to contain a copy of all the protection parameters. In each lower address page only the NVERL value may change, to extend the expandable range. Incrementally lower pages may be read until the Expandable Range Limit (NVERL) address is loaded as zero (000000h). When the Expandable Range Limit (NVERL) address is zero (000000h), the ability to extend the expandable range by reading any lower address page is ended and the end of the expandable range is fixed at the previous valid NVERL value.

It may be useful to mark the parameter block as bad to prevent file system software from attempting to use the block.

The non-volatile protection parameters are stored in memory so that the bytes always appear on IO[7:0] for both 8 and 16 bit wide IO devices. This means only even byte locations are used for the parameter bytes. All odd byte locations are unused (don't care) and may be left unprogrammed as FFh.

When reading from a x8 (byte wide data bus) sNAND, each parameter byte requires two pulses of RE# to read the even byte of parameter then skip the odd byte. When reading from a x16 (word wide data bus) sNAND each even and odd byte pair is delivered with a single RE# pulse. The information about whether a x8 or x16 device is in use is provided in the first parameter byte read (NVPC[5]). Until all three copies of the NVPC parameter byte are read, the correct value of NVPC[5] is not known. The sNAND must read NVPC assuming that the configuration is x8 and pulse RE# twice for each byte of the parameter format. This requires that the NVPC parameter format be different for x8 versus x16 devices. All remaining parameters have a common format and the number of RE# pulses per parameter byte read is reduced to a single RE# pulse for a x16 configuration.

The parameters are placed in the parameter page with the formats shown below:

Table 6.6 Non-volatile Parameter Page Map - NVPC (x16 device)

Byte Address (Hex)	Parameter Abbreviation	Byte	Copy	Bits
0	NVPC	0	1	7:0
4				15:8
8		0	2	7:0
C				15:8
10		0	3	7:0
14				15:8

Table 6.7 Non-volatile Parameter Page Map - NVPC (x8 device)

Byte Address (Hex)	Parameter Abbreviation	Byte	Copy	Bits
0	NVPC	0	1	7:0
2				15:8
4		0	2	7:0
6				15:8
8		0	3	7:0
A				15:8
C	Reserved	0	1	7:0
E				15:8
10		0	2	7:0
12				15:8
14		0	3	7:0
16				15:8

Table 6.8 Non-volatile Parameter Page Map - Parameters Following NVPC (Sheet 1 of 4)

Byte Address (Hex)	Parameter Abbreviation	Byte	Copy	Bits
18	Density R3 Mask	R3	1	7:0
1A				15:8
1C			2	7:0
1E				15:8
20			3	7:0
22				15:8
24	NVRB	R1	0	7:0
26				15:8
28			1	7:0
2A				15:8
2C			2	7:0
2E				15:8
30		R2	0	7:0
32				15:8
34			1	7:0
36				15:8
38			2	7:0
3A				15:8
3C		R3	0	7:0
3E				15:8
40			1	7:0
42				15:8
44			2	7:0
46				15:8

Table 6.8 Non-volatile Parameter Page Map - Parameters Following NVPC (Sheet 2 of 4) (Continued)

Byte Address (Hex)	Parameter Abbreviation	Byte	Copy	Bits
48	NVRL	R1	0	7:0
4A				15:8
4C			1	7:0
4E				15:8
50			2	7:0
52				15:8
54		R2	0	7:0
56				15:8
58			1	7:0
5A				15:8
5C			2	7:0
5E				15:8
60		R3	0	7:0
62				15:8
64			1	7:0
66				15:8
68			2	7:0
6A				15:8
6C	Reserved for Future Use (RFU) These bytes must be FFh value.	RFU	0	7:0
6E				15:8
70			1	7:0
72				15:8
74			2	7:0
76				15:8
78		RFU	0	7:0
7A				15:8
7C			1	7:0
7E				15:8
80			2	7:0
82				15:8
84		RFU	0	7:0
86				15:8
88			1	7:0
8A				15:8
8C			2	7:0
8E				15:8

Table 6.8 Non-volatile Parameter Page Map - Parameters Following NVPC (Sheet 3 of 4) (Continued)

Byte Address (Hex)	Parameter Abbreviation	Byte	Copy	Bits
90	NVFRB	R1	0	7:0
92				15:8
94			1	7:0
96				15:8
98			2	7:0
9A				15:8
9C		R2	0	7:0
9E				15:8
A0			1	7:0
A2				15:8
A4			2	7:0
A6				15:8
A8		R3	0	7:0
AA				15:8
AC			1	7:0
AE				15:8
B0			2	7:0
B2				15:8
B4	NVFRL	R1	0	7:0
B6				15:8
B8			1	7:0
BA				15:8
BC			2	7:0
BE				15:8
C0		R2	0	7:0
C2				15:8
C4			1	7:0
C6				15:8
C8			2	7:0
CA				15:8
CC		R3	0	7:0
CE				15:8
D0			1	7:0
D2				15:8
D4			2	7:0
D6				15:8

Table 6.8 Non-volatile Parameter Page Map - Parameters Following NVPC (Sheet 4 of 4) (Continued)

Byte Address (Hex)	Parameter Abbreviation	Byte	Copy	Bits
D8	NVERB	R1	0	7:0
DA				15:8
DC			1	7:0
DE				15:8
E0			2	7:0
E2				15:8
E4		R2	0	7:0
E6				15:8
E8			1	7:0
EA				15:8
EC			2	7:0
EE				15:8
F0		R3	0	7:0
F2				15:8
F4			1	7:0
F6				15:8
F8			2	7:0
FA				15:8
FC	NVERL	R1	0	7:0
FE				15:8
100			1	7:0
102				15:8
104			2	7:0
106				15:8
108		R2	0	7:0
10A				15:8
10C			1	7:0
10E				15:8
110			2	7:0
112				15:8
114		R3	0	7:0
116				15:8
118			1	7:0
11A				15:8
11C			2	7:0
11E				15:8

6.2.9 Non-Volatile Protection Parameter Loading

Following POR, the NVPC register and protection page counter default values select the OTP area page 63 base address as the location from which protection parameters will be accepted.

The OTP entry command must be used to enter the OTP area. Then the protection parameters must be read starting at block address zero, location zero within page 63 of the OTP area.

The protection parameters must be read using the related timing parameters t_{RPPP}, t_{REA}, and t_{RCPP} to ensure the parameters are loaded without errors.

When reading the protection parameters the RE# pulse width t_{RPPP} must be greater than or equal to the RE# read access time t_{REA} + 5ns to ensure proper transfer of the protection parameters from non-volatile memory to the protection control logic. This in turn means that the read cycle time for protection parameters t_{RCPP} is t_{RPPP} + t_{REH}.

The non-volatile parameters may be read in one sequential page read operation. However, if the host system NAND memory controller is limited to reading smaller contiguous byte groups, the Random Data Output commands (05h & E0h) may be used to select the starting address of each individual parameter, so that each parameter may be read individually to limit the length of the parameter read operations. Each parameter, with all three copies, must be read as a single read operation. Parameter reading must not start or stop within a parameter. Only addresses at the starting boundary of a parameter are accepted for loading the protection parameters.

The NVERL parameter must be the last one read from the page. If NVERL is invalid or valid and not block address zero (000000h), the parameter page pointer will decrement to select the next lower page as the current protection parameter page. This allows reading additional back-up copies of the protection parameters in the event one of the enabled methods was not yet loaded with valid register values. This also allows reading the next Expandable Range Limit address. The NVERL parameter may be read even when the Expandable Range method is not enabled so that the read of NVERL can be used to access the next lower address protection parameter page. When NVERL is read as a valid value of 000000h, the parameter page pointer does not decrement to the next lower parameter page thus preventing any further additions to the Expandable Range.

If the NVPC parameter is read and is not valid, no other parameter values are accepted from the current protection parameter page. The NVERL parameter location must be read, to decrement the protection page pointer, to enable reading from a back-up copy of the protection parameters, in the next lower page.

If the NVPC parameter read, has all bytes = FFh, the protection parameter location is immediately changed to Block 1, by setting NVPC[3]=1, and no other parameter values are accepted from the OTP area.

To then read protection parameters from Block 1 a reset command is sent to exit the OTP area. Then the protection parameters must be read starting at location zero in page 63 of Block 1.

6.2.9.1 Unprogrammed Protection Parameters (Factory Default Condition)

If the NAND OTP area has not yet been programmed, as is the case for a new unprogrammed device in factory default condition, the OTP area data bytes are all FFh. The POR default state of NVPC is invalid, and protects all blocks by default. Due to NVPC[3] being cleared to 0 by default, selecting the OTP area, the protection parameters are first read from the OTP area. Reading the OTP default FFh value for NVPC causes NVPC[3] to be set to 1 to select block 1 as the location for protection parameters.

When the NAND OTP area is enabled for access (entered), a reset command (FFh) is used to exit the OTP area and enable reading of the main Flash array. A reset command sent while the NAND OTP area is entered does not clear the NVPC[3] to 0, so when NVPC[3] =1 because the NVPC value was read as all bytes FFh, the protection parameters can be read from block 1.

If block 1 protection parameters have not been programmed the data bytes are all FFh. When the protection parameters area is read, the FFh state of the NVPC parameter bytes is used to set NVPC[6, 2:0] to 1 to remove all non-volatile block protection. This enables programming of protection parameters in a new device still in factory default condition. The parameters may be programmed either into the OTP area or block 1. Because block 1 is erasable, placing the protection parameters in block 1 allows for modifying protection parameters during system development and testing.

6.3 Block Lock Status

The Block Lock Status (BLS) operation is used to read the protection status of an individual block or to read the Protection Management Registers (PMR) in order to verify the state of the protection configuration.

The Block Lock Status operation must be used when the NAND array is not busy, and not performing a program or erase operation. The Block Lock Status command must be preceded by entry to OTP area command, followed by a Reset (FFh) command, in order to end all prior commands and, prepare for the reading of protection status. There is a required wait time of up to t_{RST} for the Reset command operation to complete. The host system can monitor the R/B# signal to know when the device is no longer busy with the reset operation, rather than waiting for the maximum t_{RST} time. A status register read command is not allowed for monitoring the busy status, as the Reset command must precede the Block Lock Status command with no commands between the Reset and the BLS command sequence.

The Block Lock Status command is followed by a similar address format as used with the volatile unlock lower and upper operations. The Register Byte Address (RBA) field, selects the register byte that is read. Address bits A17 (x16 IO) or A18 (x8 IO) and higher select the block when reading the block protection status. When reading the protection configuration register bytes, the address bits A17 or A18 and higher are don't care.

Following the load of address bytes, the status is immediately readable. There is no read latency for status registers or need to check for a busy status. On the falling edge of RE# the selected register byte is output on the IO[7:0] signals.

On 16 bit wide IO devices, the upper IO[15:8] signals are not driven during the status read. The host system must mask the IO[15:8] bits as these are floating and undefined. Toggling RE# more than once will repeatedly read out the same register byte.

When the Block Lock Status command is received, all blocks are protected. The Block Lock Status that is reported is based on the current state of the Protection Management Registers. The Block Lock Status command may be repeated with different register addresses to read out all of the available status information. The Block Lock Status mode must be ended by writing the read set-up command (00h).

Table 6.9 Address Cycle Definition of Block Lock Status Command for Protection Status (x8 IO)

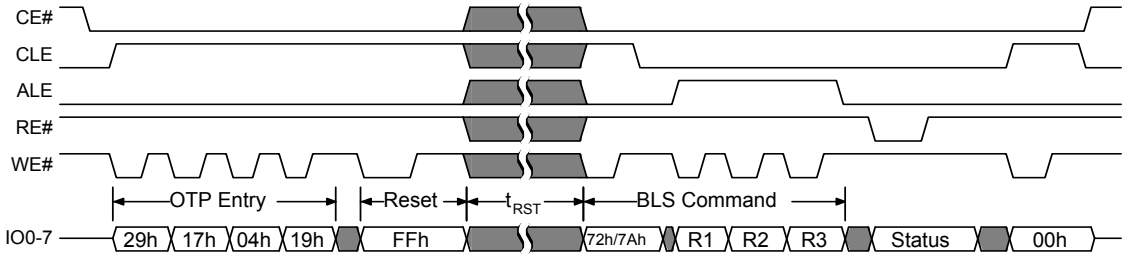
Address Cycle	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
Row Address 1	RBA0	RBA1	RBA2	RBA3	RBA4	0	A18	A19
Row Address 2	A20	A21	A22	A23	A24	A25	A26	A27
Row Address 3	A28	A29	A30	A31	0	0	0	0

Table 6.10 Address Cycle Definition of Block Lock Status Command for Protection Status (x16 IO)

Address Cycle	IO[15:8]	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
Row Address 1	X	RBA0	RBA1	RBA2	RBA3	RBA4	0	A17	A18
Row Address 2	X	A19	A20	A21	A22	A23	A24	A25	A26
Row Address 3	X	A27	A28	A29	A30	0	0	0	0

Note:
1. IO[15:8] is relevant only for 16 bit wide IO devices.

Figure 6.5 Block Lock Status Operation Sequence



Note:
1. 72h for S34SL01G2, 72h or 7Ah for S34SL02G2/S34SL04G2.

Table 6.11 Block Lock Status Registers Address Map

Register Byte Address RBA[4:0]	Register Name	Register Byte
0h	Block Lock Status (BLS)	0
1h	Protection Status (PS)	0
2h	NVPC	0
3h		1
4h	NVRB	0
5h		1
6h	NVRL	0
7h		1
8h	Reserved for Future Use	0
9h		1
Ah		2
Bh	NVFRB	0
Ch		1
Dh	NVFRL	0
Eh		1
Fh	NVERB	0
10h		1
11h	NVERL	0
12h		1
13h	Protection Parameter Page Pointer	0
14h	Density Mask (DM)	0
15h		1
16h	Volatile Unlock Lower (VUL)	0
17h		1
18h	Volatile Unlock Upper (VUU)	0
19h		1

The Block Lock Status register indicates whether the address selected block is locked-down, locked or unlocked, and whether the volatile, non-volatile, or WP# signal protection methods are the source of the lock or unlocked condition.

Table 6.12 Block Lock Status (BLS) Register

Bits	Field Name	Function	Default State	Description
7	RFU	Reserved for Future Use	0	
6	RFU	Reserved for Future Use	0	
5	WP#-unlocked	Not WP# Locked	1	1 = WP# is high or volatile lock down is active and WP# is don't care 0 = Locked by WP# Low and volatile protection is not locked down
4	NV-unlocked	Not Non-volatile Locked	0	1 = The address selected block is not locked by a non-volatile protection parameter 0 = The address selected block is locked by a non-volatile protection parameter
3	V-unlocked	Not Volatile Locked	1	1 = The address selected block is not locked by a volatile protection parameter 0 = The address selected block is locked by a volatile protection parameter
2	Block-unlocked	Block-unlocked	0	1 = The address selected block is unlocked. 0 = The address selected block is locked.

Table 6.12 Block Lock Status (BLS) Register (Continued)

Bits	Field Name	Function	Default State	Description
1	Not_Lock-down	Not Locked-down	0	1 = Volatile protection is not locked-down. 0 = Volatile protection is locked-down.
0	Lock-down	Locked-down	1	1 = Volatile protection is locked-down. 0 = Volatile protection is not locked-down.

The Protection Status register shows the state of the volatile protection method.

Table 6.13 Protection Status (PS) Register

Bits	Field Name	Function	Default State	Description
7	RFU	Reserved for Future Use	0	
6	RFU	Reserved for Future Use	0	
5	RFU	Reserved for Future Use	0	
4	RFU	Reserved for Future Use	0	
3	RFU	Reserved for Future Use	0	
2	RFU	Reserved for Future Use	0	
1	VPME	Volatile Protection Method Enabled	0	1 = The volatile protection method is enabled. One or more volatile protection commands have been received with VPE and WP# =1. 0 = The volatile protection method is not enabled (default after POR)
0	VPV	Volatile Parameter Valid	1	1 = Volatile protection lower and upper boundary registers are not valid. All blocks are protected if volatile protection is enabled. 0 = Volatile protection lower and upper boundary registers are valid. VUL and VUU are valid and VUU ≥ VUL

The NVPC parameter has the following bit position format with bit definitions as shown in Table 6.3, *Non-volatile Protection Configuration Parameter* on page 42:

Table 6.14 Block Lock Status NVPC Format (x8 IO or x16 IO)

Register Byte	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
0	7	6	5	4	3	2	1	0
1	15	14	13	12	11	10	9	8

The pointer to the current protection parameter page has the following format.

Table 6.15 Block Lock Status Protection Parameter Page Pointer Format

Register Byte	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
0	OTP=1 Block1=0	0	Page Address					
			PA5	PA4	PA3	PA2	PA1	PA0

The remaining Protection Management Registers displayed by the Block Lock Status command have the following formats for either x8 IO or x16 IO.

Table 6.16 Block Lock Status Address Register Format (x8 IO)

Register Byte	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
0	A25	A24	A23	A22	A21	A20	A19	A18
1	Valid=0	0	A31	A30	A29	A28	A27	A26

The valid bit for each non-volatile configuration register is displayed as the MSB of the register. The register contents are valid if the MSB is 0. The default POR value of all these registers is FFFFh.

Table 6.17 Block Lock Status Address Register Format (x16 IO)

Register Byte	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
0	A24	A23	A22	A21	A20	A19	A18	A17
1	Valid=0	0	A30	A29	A28	A27	A26	A25

6.4 Write Protect Operation

Erase and program operations are enabled or disabled by the protection control logic prior to the host system issuing the confirm commands (10h, 15h, or D0h).

The state of protection is updated by the program address load commands (8xh) or erase address load commands (60h or D1h) and their following address cycles. If the address loaded for the target block matches a protected (locked) block address, the block is locked, if not, the block is unlocked. A confirm command may immediately follow the last address byte of a program or erase address load command.

The state of the WP# input is considered when volatile protection is not enabled or not locked-down. When volatile protection is enabled and locked-down the WP# input is ignored. The level of WP# must be set t_{WW} time prior to raising the WE# signal for the confirm command, as shown in Figure 12.34, *Program Enabling / Disabling Through WP# Handling* on page 87 and Figure 12.35, *Erase Enabling / Disabling Through WP# Handling* on page 87.

Erase and program operations are aborted if WP# is driven low during busy time, and kept low for at least 100 ns. Switching WP# low during this time is equivalent to issuing a Reset command (FFh) to the NAND memory. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The R/B# input will stay low for t_{RST} (similarly to Figure 12.22, *Reset Operation Timing* on page 81). At the end of this time, the command register is ready to process the next command, and the Status Register bit I/O6 will be cleared to 1, while I/O7 value will be related to the WP# value.

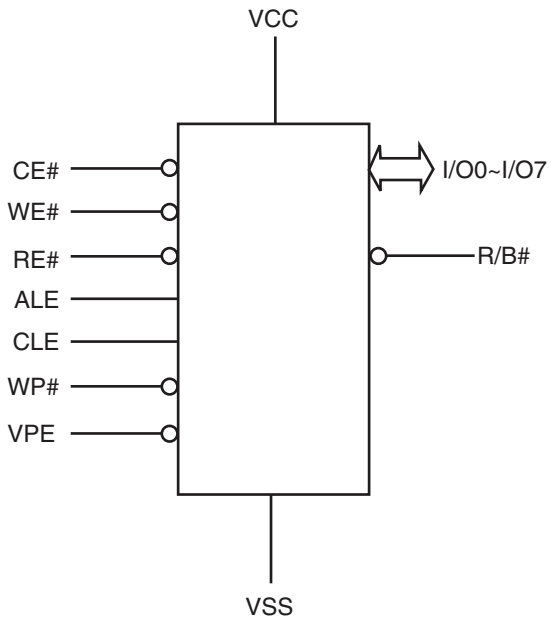
Switching WP# low during busy does not reset the secure NAND controller PMR. The protection methods state is not lost in this situation even though the NAND memory program or erase operation has been aborted.

The volatile protection method configuration should not be modified during erase or program operation busy time. Any modification of the volatile protection during busy time may abort the operation in progress.

Hardware Interface

7. Logic Diagram

Figure 7.1 Logic Diagram



8. Signal Descriptions

Table 8.1 Signal Descriptions

Signal Name	Type	Description
CE#	Input	**Chip Enable.** CE# low selects the device to perform operations based on the NAND bus signal behavior.When CE# is high all other input signals are ignored and outputs are not actively driven.
CLE	Input	**Command Latch Enable.** This input enables the latching of the I/O inputs into the Command Register on the rising edge of Write Enable (WE#).
ALE	Input	**Address Latch Enable.** This input enables the latching of the I/O inputs into the Address Register on the rising edge of Write Enable (WE#).
RE#	Input	**Read Enable.** The RE# input is the serial data-out control, and when low drives the data onto the I/O bus. Data is valid t_{REA} after the first falling edge of RE#. Each additional RE# falling edge while CE#, CLE, and ALE remain low, increments the internal column address counter by one to deliver the next sequential data output.
WE#	Input	**Write Enable.** This input latches Command, Address and Data. The I/O inputs are latched on the rising edge of WE#.
WP#	Input + IPU	**Write Protect.** The WP# input, when low, provides hardware protection of the entire memory address space against undesired data modification (program / erase). This input has a weak internal Pull-Up (IPU) to disable host system protection if the input is left floating.
VPE	Input + IPD	**Volatile Protection Enable.** The Volatile Protection Enable input, when high during power-on, provides block granularity hardware protection against undesired data modification (program / erase). This input has a weak internal pull-down (IPD) to disable the volatile protection features if the input is left floating.
R/B#	Output, Open Drain	**Ready Busy**. The Ready/Busy input or output is an Open Drain signal that detects the state of attached memory or signals the state of the controller.
I/O[7:0]	Input / Output	**Inputs/Outputs**. The I/O signals are used for command input, address input, data input, and data output. The I/O signals float to High-Z when the device is deselected or the outputs are disabled.
VCC	Supply	**Supply Voltage**. The V_{CC} supplies the power for all the device operations. An internal circuit prevents the execution of commands when V_{CC} is less than V_{RST}.
VSS	Ground	**Ground.** VSS is the common voltage drain and ground reference for the device core, input signal receivers, and output drivers.
NC	Unused	**Not Connected.** No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB).
RFU	Reserved	**Reserved for Future Use.** No device internal signal is currently connected to the package connector but there is potential future use of the connector. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.
DNU	Do Not Use	**Do Not Use.** A device internal signal may be connected to the package connector. The connection may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at VIL. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to VSS. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections.

Notes:

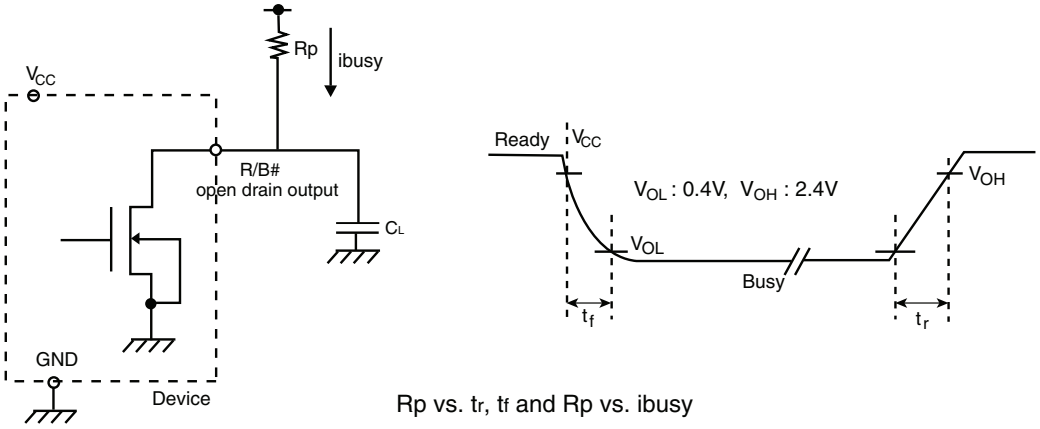
1. *A 0.1 µF capacitor should be connected between the V_{CC} Supply Voltage and the V_{SS} Ground to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.*
2. *An internal voltage detector disables all functions whenever V_{CC} is below 1.8V to protect the device from any involuntary program/erase during power transitions.*

8.1 Ready/Busy

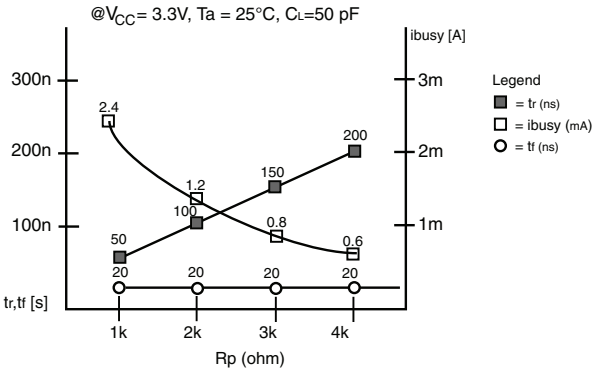
The Ready/Busy output provides a method of indicating the completion of a page program, erase, copyback, or read completion. The R/B# pin is normally high and goes to low when the device is busy (after a reset, read, program, or erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because the pull-up resistor value is related to t_r (R/B#) and the current drain during busy (ibusy), and output load capacitance is related to t_f, an appropriate value can be obtained with the reference chart shown in Figure 8.1.

For example, for a particular system with 20 pF of output load, t_f from V_{CC} to V_{OL} at 10% to 90% will be 10 ns, whereas for a particular load of 50 pF, Cypress measured it to be 20 ns as shown in Figure 8.1.

Figure 8.1 Ready/Busy Pin Electrical Application



Rp vs. tr, tf and Rp vs. ibusy



Rp value guidence

$$Rp\ (min.) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/B# pin.
Rp(max) is determined by maximum permissible limit of tr.

9. Hardware Data Protection

Some basic protections against unintended changes to stored data are provided and controlled purely by the hardware design. These are described below. Other software managed protection methods are discussed in the software section of this document.

9.1 Data Protection During Power On / Off

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever V_{CC} is below V_{RST}.

The power-up and power-down sequence is shown in Figure 11.5, *Power On or Off and Data Protection Timing* on page 66.

A recovery time of t_{POR} is required after V_{CC} reaches V_{CCM} before the device is ready for any command sequences.

9.2 Write Protect (WP#)

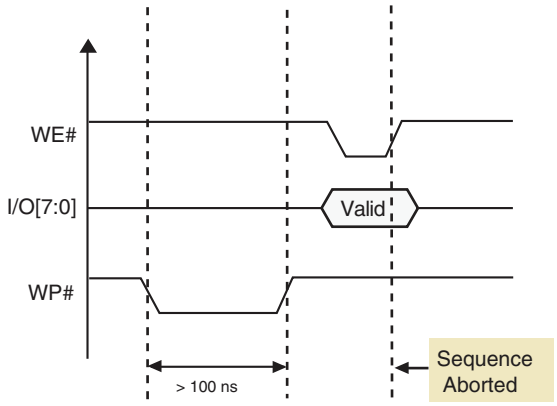
The WP# pin provides hardware protection when low and is recommended to be kept at or below V_{IL} during power-up. A recovery time of t_{WW} is required after WP# returns high, before any program or erase command sequences are accepted as shown in Figure 11.5, *Power On or Off and Data Protection Timing* on page 66. The two-step command sequence for program/erase operation provides additional software protection.

After power on, the WP# signal also provides hardware protection when volatile protection is not enabled or not in lock-down. When volatile protection is enabled and locked-down the WP# input is ignored.

Erase and program operations are aborted if WP# is driven low during busy time, and kept low for about 100 ns. Switching WP# low during this time is equivalent to issuing a Reset command (FFh). The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The R/B# pin will stay low for t_{RST} (similarly to Figure 12.22 on page 81). At the end of this time, the command register is ready to process the next command, and the Status Register bit I/O6 will be cleared to 1, while I/O7 value will be related to the WP# value. Refer to Table 4.2 on page 26 for more information on device status.

Erase and program operations are enabled or disabled by setting WP# to high or low respectively, prior to issuing the setup commands (80h or 60h). The level of WP# shall be set t_{WW} ns prior to raising the WE# pin for the set up command, as explained in Figure 12.34 and Figure 12.35 on page 87.

Figure 9.1 WP# Low Timing Requirements during Program/Erase Command Sequence



10. Bus Operation

10.1 Interface States and Cycles

There are several bus states and cycles that define the host system interaction with the sNAND Family device: Standby, Command Input, Address Input, Data Input, Busy, Data Output, and Write Protect. States are in effect while input signals are at a stable level. Cycles involve signal rising or falling edges that trigger information transfer on the bus.

Typically glitches less than 5 ns on Chip Enable, Write Enable, and Read Enable are ignored by the device and do not affect bus operations.

Table 10.1 Interface States and Cycles

State or Event	CE#	CLE	ALE	WE#	RE#	WP#	R/B#	V_{CC}
Power Off State	X	X	X	X	X	X	X	V_{CC} >= V_{RST}
Stand By State	High	X	X	X	X	0V / V_{CC} (2)	X	V_{CC} >= V_{CC} Minimum
Command Input Latch Cycle	Low	High	Low	Rising	High	X / High (2)	High	V_{CC} >= V_{CC} Minimum
Address Input Latch Cycle	Low	Low	High	Rising	High	X	High	V_{CC} >= V_{CC} Minimum
Busy State During Read	X	X	X	High	High (3)	X	Low	V_{CC} >= V_{CC} Minimum
Busy State During Program or Erase	X	X	X	X	X	High	Low	V_{CC} >= V_{CC} Minimum
Data Output Cycle	Low	Low	Low	High	Falling	X	X / High	V_{CC} >= V_{CC} Minimum
Data Output Suspended State	X	X	X	High	High	X	X	V_{CC} >= V_{CC} Minimum
Write Protect State	X	X	X	X	X	Low	X	V_{CC} >= V_{CC} Minimum

Notes:

1. *X can be V_{IL} or V_{IH}. High = Logic level high, Low = Logic level low.*
2. *WP# should be biased to CMOS high or CMOS low for stand-by state to ensure lowest power consumption. WP# must be high during the input of commands that initiate (confirm) commands that modify non-volatile data e.g. program confirm (10h). WP# must remain high through out the duration of the data modifying operation. If WP# is low at the time these initiating commands are input, the commands are ignored and do not initiate the command operation.*
3. *During Busy State Read, RE# must be held high to prevent unintended data out.*
4. *During Data Output Cycle the R/B# signal may be high or low during a status register read but must be high during the reading of data.*

10.2 Power-Off State

When the core supply voltage is at or below the V_{RST} voltage, the device is considered to be powered off. The device does not react to external signals, and all blocks are locked to prevent any program or erase operation.

10.3 Standby State

In Standby, the device is deselected: inputs other than CE# are ignored and the device draws only standby current (I_{SB}).

10.4 Command Input Latch Cycle

The Command Input Latch Cycle is used to give a command to the memory device. Commands are accepted with Chip Enable low, Command Latch Enable high, Address Latch Enable low, and Read Enable high and latched on the rising edge of Write Enable. Moreover, for commands that start a modify operation (program/erase) the Write Protect pin must be high. See Figure 12.2, *Command Latch Cycle* on page 70 for details of the timing requirements.

10.5 Address Input Latch Cycle

The Address Input Latch Cycle allows the insertion of the memory address. For 2 Gbit or higher density memories, five write cycles are needed to input the addresses. For 1 Gbit or lower density memories, four write cycles are needed to input the addresses. If necessary, a 5th dummy address cycle can be issued to 1 Gbit memories, which will be ignored by the NAND device. Addresses are accepted with Chip Enable low, Address Latch Enable high, Command Latch Enable low, and Read Enable high and latched on the rising edge of Write Enable. See Figure 12.3, *Address Latch Cycle* on page 71 for details of the timing requirements. Addresses are always applied on I/O7:0. Refer to Section 2.4.1, *Address Cycle Maps* on page 14 for more detailed information.

10.6 Data Input Cycle

The Data Input Cycle allows the data to be programmed to be sent to the device. The data insertion is serial and timed by the Write Enable cycles. Data is accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable high, and Write Protect high and latched on the rising edge of Write Enable. See Figure 12.4, *Input Data Latch Cycle* on page 72 for details of the timing requirements.

10.7 Busy State During Read

During the initial read latency period of a page read command the memory will indicate busy status with the R/B# signal pulled low. The RE# input must be high if data is not to be driven on the data I/O signals.

10.8 Busy State During Program or Erase

During the program or erase operations the memory will indicate busy status with the R/B# signal pulled low. The WP# input from the host system must remain High throughout the operations to prevent abort of the operations. If the WP# input from the host does go low during a program or erase operation, the operation will be aborted, leaving the page being programmed or the block being erased in an intermediate state, potentially with unstable and invalid data values.

10.9 Data Output Cycle

The Data Output events allows data to be read from the memory array and to check the Status Register content. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable high, Address Latch Enable low, and Command Latch Enable low. Each falling edge of the RE# signal drives the next sequential data on to the data I/O signals. During Data Output the R/B# signal may be high or low during a status register read but must be high during the reading of data. See Figure 12.5, *Data Output Cycle Timing (CLE=L, WE#=H, ALE=L)* on page 72 for details of the timings requirements.

10.10 Data Output Suspended State

During the reading of sequential data or register values, the reading may be suspended by taking and holding RE# high.

10.11 Write Protect State

Hardware Write Protection is activated when the Write Protect (WP#) signal from the host system is low. In this condition, modify operations do not start and the content of the memory is not altered. The Write Protect signal is not latched by Write Enable (WE#) to ensure the protection even during power up.

10.12 CE# Don’t Care

CE# may be inactive during data loading or sequential data reading as shown in Figure 10.1. By operating in this way, it is possible to connect NAND flash directly to a microprocessor.

Figure 10.1 Program Operation with CE# Don't Care

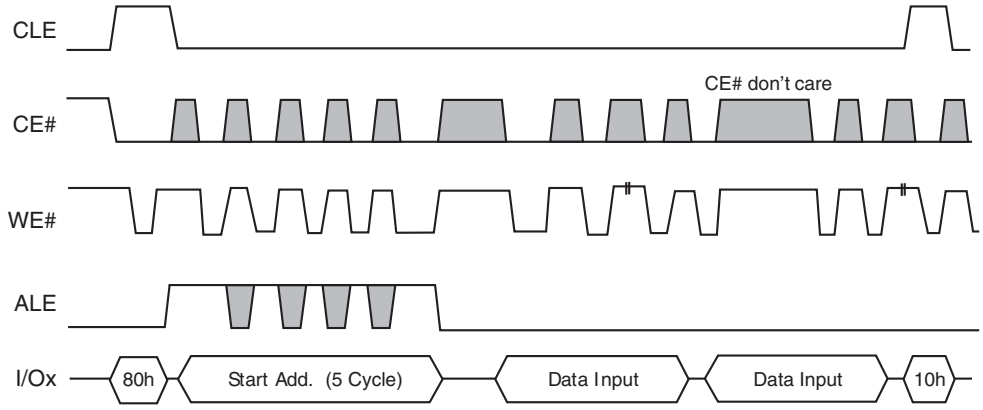
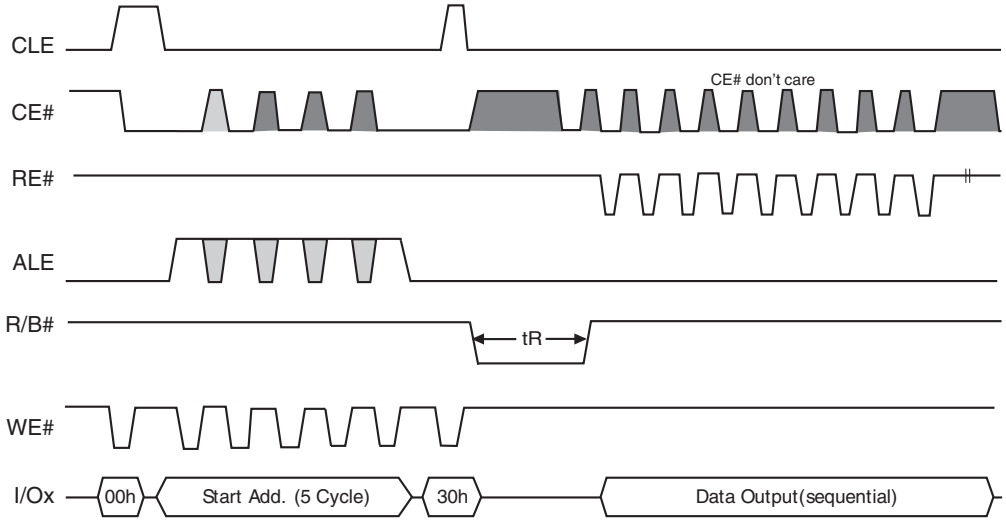


Figure 10.2 Read Operation with CE# Don't Care



11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Table 11.1 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Storage Temperature	T_{STG}	-65 to +150	°C
Temperature under Bias	T_{BIAS}	-50 to +125	°C
Supply Voltage	V_{CC}	-0.6 to +4.6	V
Input or Output Voltage	V_{IO}	-0.6 to +4.6	V
Output Short Circuit Current	I_{SC}	100	mA

Notes:

1. *Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating Ranges section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.*

No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

11.1.1 Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{CC}. During voltage transitions, inputs or I/Os may overshoot V_{SS} to -2.0V or overshoot to V_{CC} +2.0V, for periods up to 20 ns.

Figure 11.1 Maximum Negative Overshoot Waveform

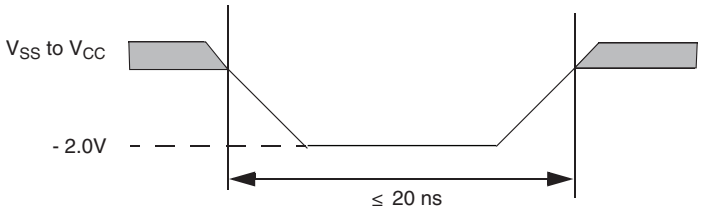
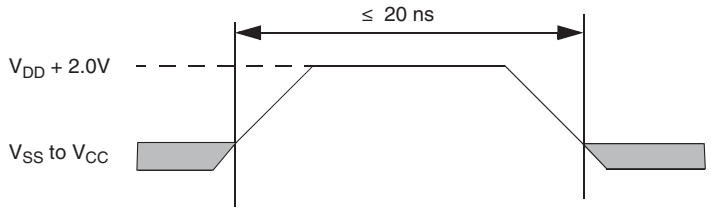


Figure 11.2 Maximum Positive Overshoot Waveform



11.2 Latchup Characteristics

Table 11.2 Latchup Specification

Description	Min	Max	Unit
Input voltage with respect to V_{SS} on all input only connections	-1.0	V_{CC} + 1.0	V
Input voltage with respect to V_{SS} on all I/O connections	-1.0	V_{CC} + 1.0	V
V_{CC} Current	-100	+100	mA

Notes:

1. *Excludes power supply V_{CC}.*
2. *Test conditions: V_{CC} = 1.8V, 3.3 V, one connection at a time tested, connections not being tested are at V_{SS}.*

11.3 Operating Ranges

Table 11.3 Operating Ranges

Parameter	Symbol	Value	Unit
Ambient Industrial Temperature Range	T_A	-40 to +85	°C
3V Range Supply Voltage	V_{CC}	2.7 to 3.6	V
3V Range Input or Output Voltage	V_{IO}	2.7 to 3.6	V

11.4 Power On / Off Sequence

The device ignores CE# until a time delay of t_{POR} has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold. See Figure 11.3. However, correct operation of the device is not guaranteed if V_{CC} returns below V_{CC} (min) during t_{POR}. No command should be sent to the device until the end of t_{POR}.

The device draws I_{POR} during t_{POR}. After power on (t_{POR}), with CE# High, the device is in Standby state and draws CMOS standby current (I_{SB}).

During power off or voltage drops below V_{CCM}, the voltage must drop below V_{RST} for a period of t_{PD} for the part to initialize correctly after power on. See Figure 11.4. If during a voltage drop the V_{CC} stays above V_{RST} the part will stay initialized and will work correctly when V_{CC} is again above V_{CCM}. In the event Power On Reset (POR) did not complete correctly after power on, receiving a software reset command (RESET) will restart the POR process.

Normal precautions must be taken for supply rail decoupling to stabilize the V_{CC} supply at the device. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package supply connection (this capacitor is generally of the order of 0.1 µf).

Table 11.4 Power On / Off Voltage and Timing

Symbol	Parameter	Min	Typ	Max	Unit
V_{CCM}	V_{CC} (minimum 3V operation voltage)	2.7			V
V_{TH}	V_{CC} threshold below which it is recommended to drive WP# low. (3V supply)		1.8		V
V_{LKO}	V_{CC} threshold below which data is protected (3V supply)		1.8		V
V_{RST}	V_{CC} threshold below which POR is triggered at the next power-on reaching V_{CCM}.		0.7		V
t_{POR}	V_{CCM} to Read operation			5	ms
t_{PD}	V_{CC} below V_{RST} time	10.0			µs

Figure 11.3 Power On Timing

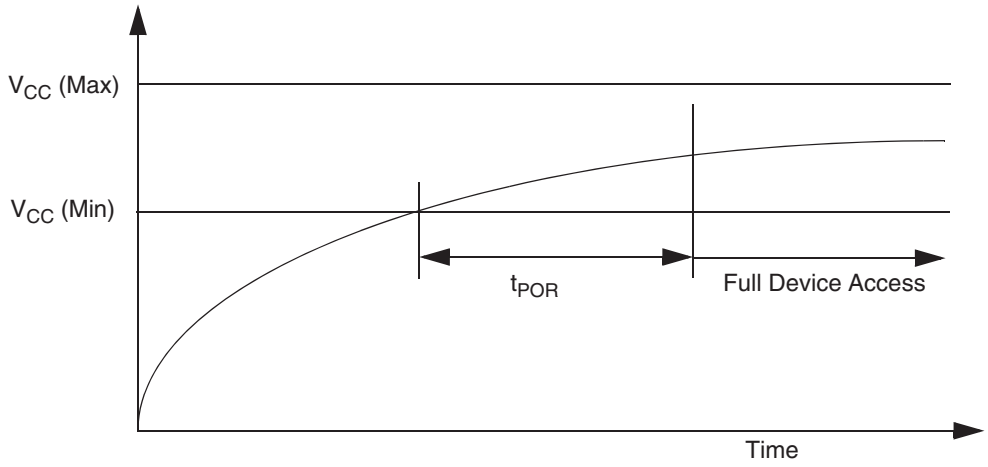
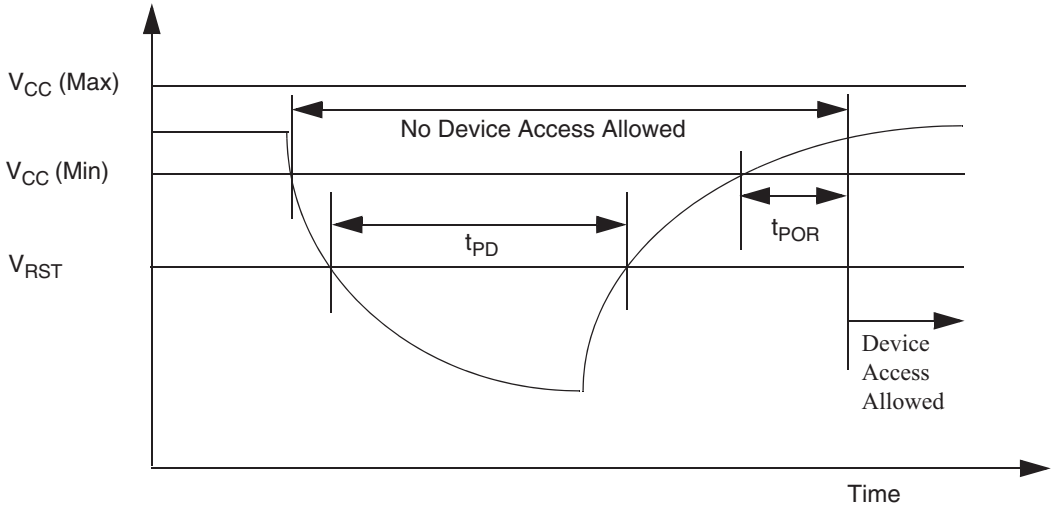


Figure 11.4 Power Off and Voltage Drop



11.5 Hardware Data Protection and Power On / Off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below V_{TH}.

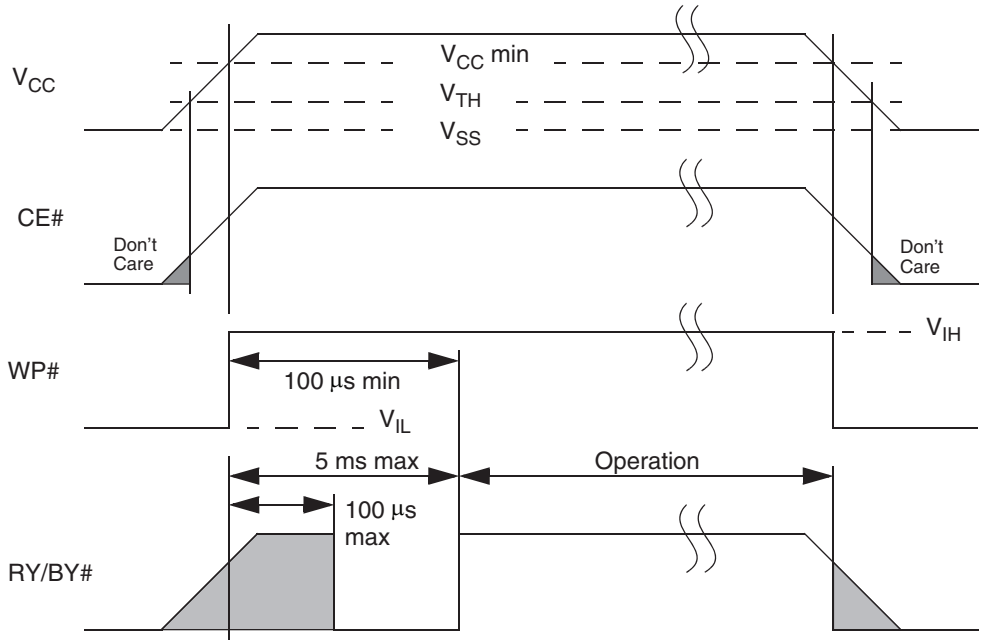
The power-up and power-down sequence is shown in Figure 11.5, *Power On or Off and Data Protection Timing* on page 66, in this case V_{CC} and V_{CCQ} on the one hand (and V_{SS} and V_{SSQ} on the other hand) are shorted together at all times.

The Ready/Busy signal shall be valid within 100 µs after the power supplies have reached the minimum values (as specified on), and shall return to one within 5 ms (max).

During this busy time, the device executes the initialization process, and dissipates a current I_{CC0} (30 mA max), in addition, it disregards all commands excluding Read Status Register (70h).

At the end of this busy time, the device defaults into “read setup”, thus if the user decides to issue a page read command, the 00h command may be skipped.

Figure 11.5 Power On or Off and Data Protection Timing



The WP# pin provides hardware protection when low and is recommended to be kept at or below V_{IL} during power-up. A recovery time of t_{WW} is required after WP# returns high, before any program or erase command sequences are accepted

11.5.1 Power-On Reset

When the core voltage supply remains at or below the V_{CCM} voltage for ≥ t_{PD} time, then rises to ≥ V_{CCM} the device will begin its Power On Reset (POR) process. POR continues until the end of t_{POR}. During t_{POR} the device does not react to external input signals nor drive any outputs. Following the end of t_{POR} the device transitions to the Interface Standby state and can accept commands.

11.6 DC Characteristics

Table 11.5 DC Characteristics and Operating Conditions

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Power On Current		I_{CC0}	FFh command input after power on	—	—	55	mA
Operating Current (3V supply)	Sequential Read	I_{CC1}	$t_{RC} = t_{RC}$ (min) CE# = V_{IL}, Iout = 0 mA	—	16.5	32	mA
	Program	I_{CC2}	Normal	—	16.5	32	mA
			Cache	—	16.5	32	mA
	Erase	I_{CC3}	—	—	16.5	32	mA
Standby Current (3V supply), (TTL)		I_{CC4}	CE#= WP# = V_{CC}-0.2	—	—	2	mA
Standby Current (3V supply), (CMOS)		I_{CC5}	CE#= WP# = V_{CC}-0.2	—	25	70	µA
Input Leakage Current		I_{LI}	V_{IN} = 0 to V_{CC}(max)	—	—	±12	µA
Output Leakage Current		I_{LO}	V_{OUT} = 0 to V_{CC}(max)	—	—	±12	µA
Input High Voltage		V_{IH}	—	V_{CC} x 0.8	—	V_{CC} + 0.3	V
Input Low Voltage		V_{IL}	—	-0.3	—	V_{CC} x 0.2	V
Output High Voltage		V_{OH}	I_{OH} = -400 µA	2.4	—	—	V
Output Low Voltage (3V supply)		V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V
Output Low Current (R/B#) (3V supply)		$I_{OL(R/B\#)}$	V_{OL} = 0.4V	8	10	—	mA

Notes:

1. *All $V_{CC}Q$ and V_{CC} pins, and V_{SS} and $V_{SS}Q$ pins respectively are shorted together.*
2. *Values listed in this table refer to the complete voltage range for V_{CC} and $V_{CC}Q$ and to a single device in case of device stacking.*
3. *All current measurements are performed with a 0.1 µF capacitor connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin.*
4. *Standby current measurement can be performed after the device has completed the initialization process at power up. Refer to Section 11.5.1, Power-On Reset on page 66 for more details.*
5. *Standby current increases by 2 µA if WP# ≤ V_{IH}.*

11.7 AC Test Conditions

Figure 11.6 Test Setup

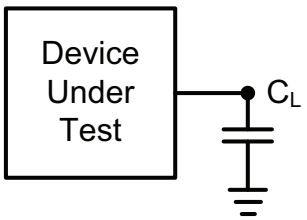


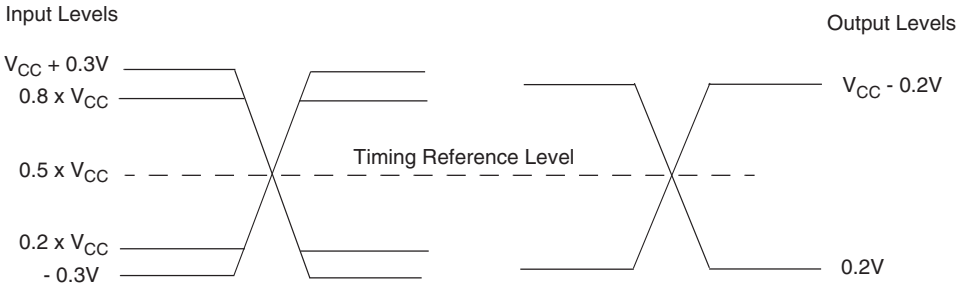
Table 11.6 AC Measurement Conditions

Parameter	Min	Max	Unit
Load Capacitance		50	pF
Input Pulse Voltage	0.2 x V_{CC}	0.8 V_{CC}	V
Input slew rate	0.43	2	V/ns
Input Rise and Fall Times (3V supply)	1.1	5	ns
Input Timing Ref Voltage	0.5 V_{CC}		V
Output Timing Ref Voltage	0.5 V_{CC}		V

Notes:

1. *Input slew rate measured from input pulse min to max at V_{CC} max. Example: (3.6V x 0.8) - (3.6V x 0.2) = 2.16V; 2.16V/ 2V/ns = 1.1 ns rise or fall time.*
2. *AC characteristics tables assume clock and data signals have the same slew rate (slope).*

Figure 11.7 Input, Output, and Timing Reference Levels



11.7.1 Pin Capacitance

Table 11.7 Pin Capacitance (TA = 25°C, f = 1.0 MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input	C_{IN}	V_{IN} = 0V	—	15	pF
Input / Output	C_{IO}	V_{IL} = 0V	—	15	pF

Note:

1. *For the stacked devices version the Input is 10 pF x [number of stacked chips] and the Input/Output is 10 pF x [number of stacked chips].*

11.8 AC Characteristics 3V Industrial Operating Range

Table 11.8 AC Characteristics (Industrial)

Parameter	Symbol	Min	Max	Unit
ALE to RE# delay	t_{AR}	10	—	ns
ALE hold time	t_{ALH}	5	—	ns
ALE setup time	t_{ALS}	10	—	ns
Address to data loading time	t_{ADL}	70	—	ns
CE# access time	t_{CEA} (4)	—	25	ns
CE# low to RE# low	t_{CR}	10	—	ns
CE# hold time	t_{CH}	5	—	ns
CE# high to output High-Z	t_{CHZ}	—	30	ns
CLE hold time	t_{CLH}	5	—	ns
CLE to RE# delay	t_{CLR}	10	—	ns
CLE setup time	t_{CLS}	10	—	ns
CE# high to output hold	t_{COH} (3)	1	—	ns
CE# high to ALE or CLE don't care	t_{CSD}	10	—	ns
CE# setup time	t_{CS}	20	—	ns
Data hold time	t_{DH}	5	—	ns
Data setup time	t_{DS}	10	—	ns
Data transfer from cell to register **(1 Gbit)**	t_{R}	—	25	µs
Data transfer from cell to register **(≥ 2 Gbit)**	t_{R}	—	30	µs
Output High-Z to RE# low	t_{IR}	0	—	ns
Read cycle time	t_{RC}	25	—	ns
RE# access time	t_{REA}	—	20	ns
Read cycle time (protection parameters)	t_{RCPP}(5)	35	—	ns
RE# high hold time	t_{REH}	10	—	ns
RE# high to output hold	t_{RHOH} (3)	15	—	ns
RE# high to WE# low	t_{RHW}	100	—	ns
RE# high to output High-Z	t_{RHZ}	—	100	ns
RE# low to output hold	t_{RLOH}	5	—	ns
RE# pulse width	t_{RP}	12	—	ns
RE# pulse width (protection parameters)	t_{RPPP}(5)	25	—	ns
Ready to RE# low	t_{RR}	20	—	ns
Device resetting time (Read/Program/Erase)	t_{RST}	—	5/10/500	µs
WE# high to busy	t_{WB}	—	100	ns
Write cycle time	t_{WC}	25	—	ns
WE# high hold time	t_{WH}	10	—	ns
WE# high to RE# low	t_{WHR}	60	—	ns
WE# high to RE# low for Random Data Output	t_{WHR2}	200	—	ns
WE# pulse width	t_{WP}	12	—	ns
Write protect time	t_{WW}	100	—	ns

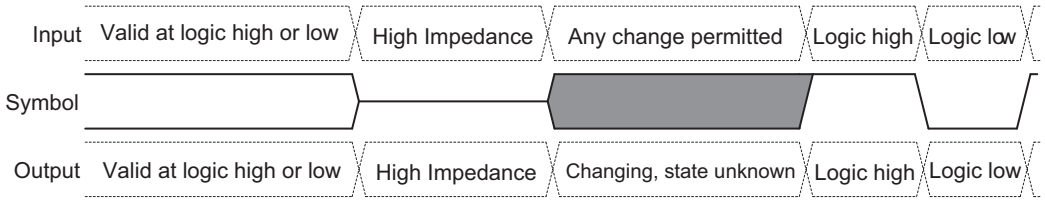
Notes:

1. *The time to Ready depends on the value of the pull-up resistor tied to R/B# pin.*
2. *If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5 µs.*
3. *CE# low to high or RE# low to high can be at different times and produce three cases. Depending on which signal comes high first, either t_{COH} or t_{RHOH} will be met.*
4. *During data output, t_{CEA} depends partly on t_{CR} (CE# low to RE# low). If t_{CR} exceeds the minimum value specified, then the maximum time for t_{CEA} may also be exceeded ($t_{CEA} = t_{CR} + t_{REA}$).*
5. *When reading the protection parameters the RE# pulse width t_{RPPP} must be greater than or equal to the RE# read access time t_{REA} + 5ns to ensure proper transfer of the protection parameters from non-volatile memory to the protection control logic. This in turn means that the read cycle time for protection parameters t_{RCPP} is t_{RPPP} + t_{REH}. Reading of data from the NAND memory array to the host may use the legacy t_{RP} and t_{RC} read parameter values.*

12. Timing Diagrams

12.1 Key to Switching Waveforms

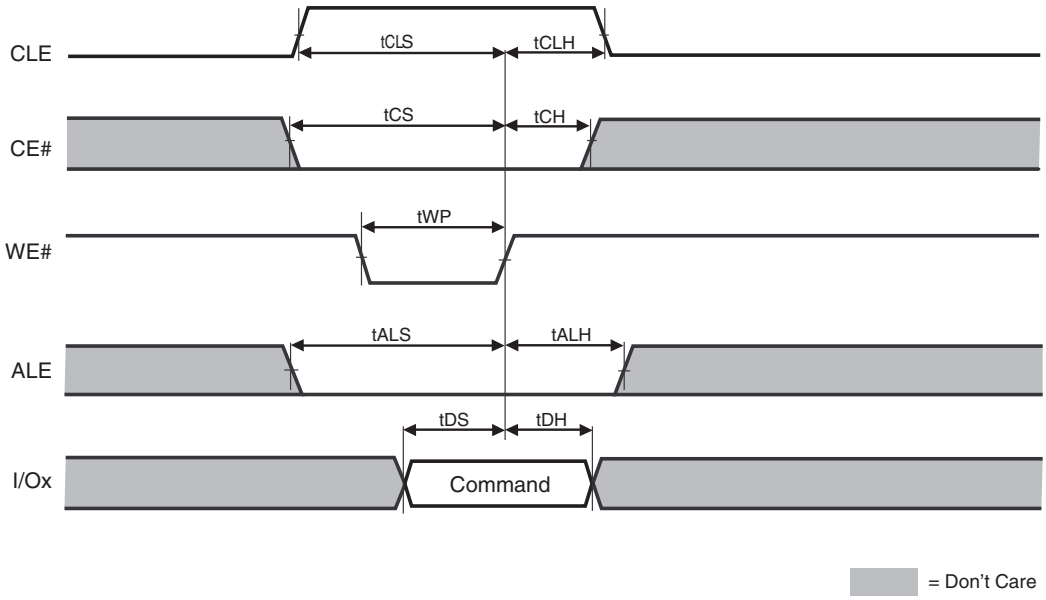
Figure 12.1 Waveform Element Meanings



12.2 Command Latch Cycle

Command Input bus operation is used to give a command to the memory device. Commands are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low, and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation
(write/ erase) the Write Protect pin must be high.

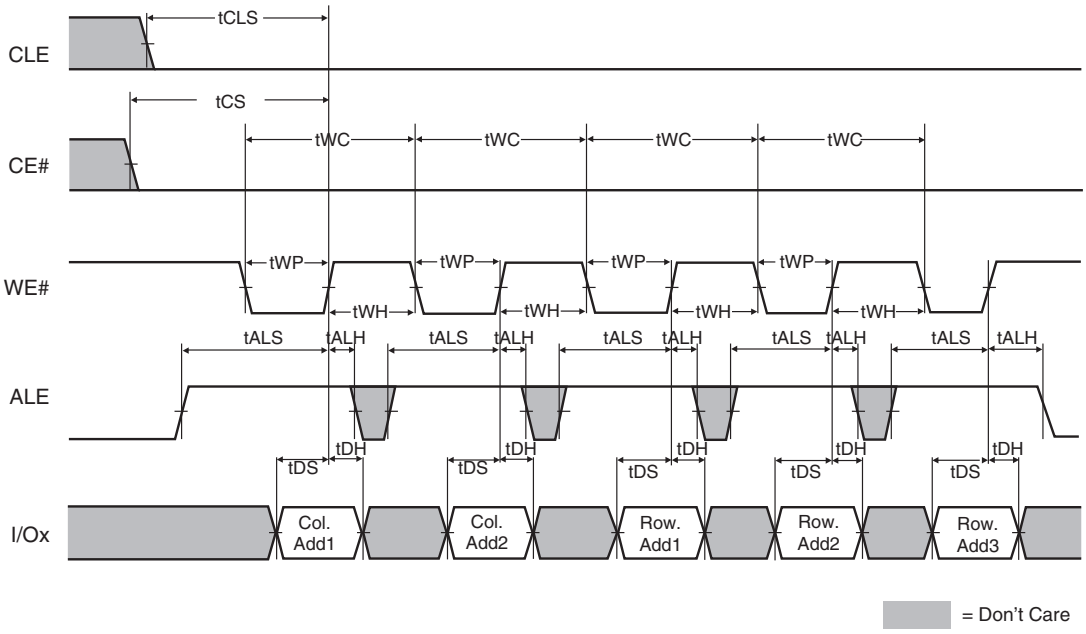
Figure 12.2 Command Latch Cycle



12.3 Address Latch Cycle

Address Input bus operation allows the insertion of the memory address. To insert the 27 (x8 Device) addresses needed to access the 1 Gb, four write cycles are needed. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low, and Read Enable High and latched on the rising edge of Write Enable. Moreover, for commands that start a modify operation (write/ erase) the Write Protect pin must be high.

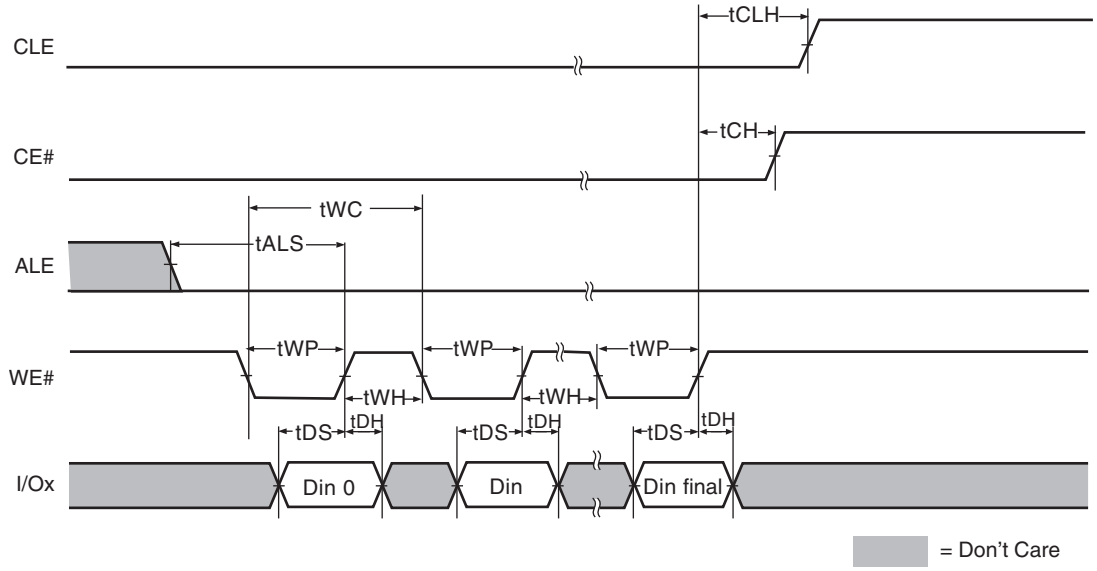
Figure 12.3 Address Latch Cycle



12.4 Data Input Cycle Timing

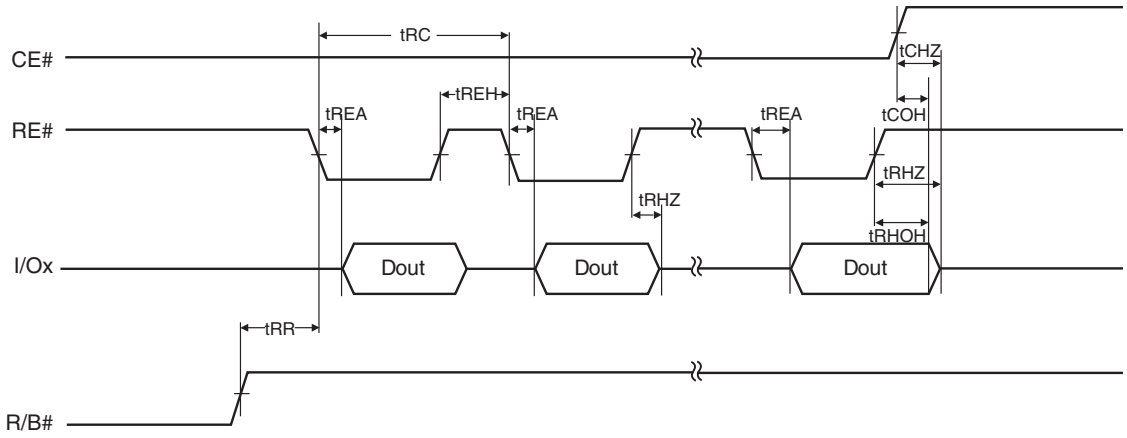
Data Input bus operation allows the data to be programmed to be sent to the device. The data insertion is serially, and timed by the Write Enable cycles. Data is accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable.

Figure 12.4 Input Data Latch Cycle



12.5 Data Output Cycle Timing (CLE=L, WE#=H, ALE=L, WP#=H)

Figure 12.5 Data Output Cycle Timing (CLE=L, WE#=H, ALE=L)

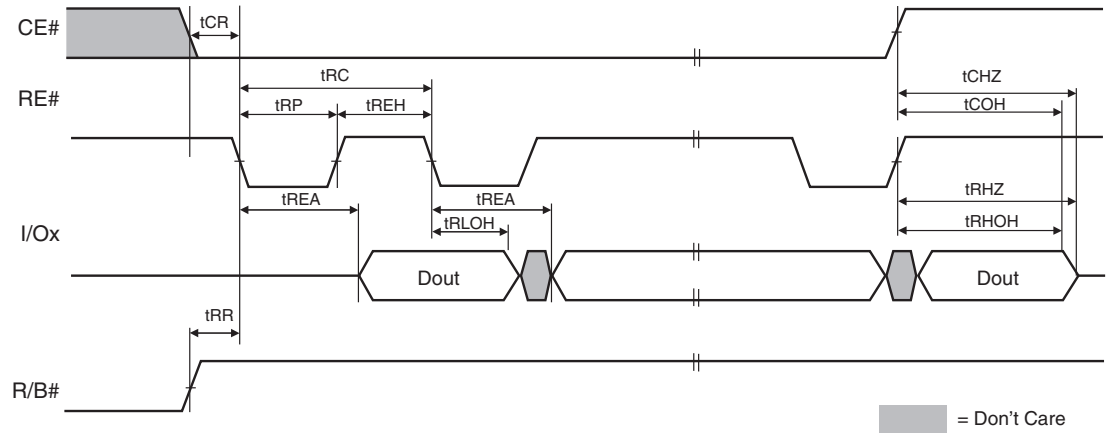


Notes:

1. *Transition is measured at ± 200 mV from steady state voltage with load.*
2. *This parameter is sampled and not 100% tested.*
3. *t_{RHOH} starts to be valid when frequency is lower than 33 MHz.*

12.6 Data Output Cycle Timing (EDO Type, CLE=L, WE#=H, ALE=L)

Figure 12.6 Data Output Cycle Timing (EDO)

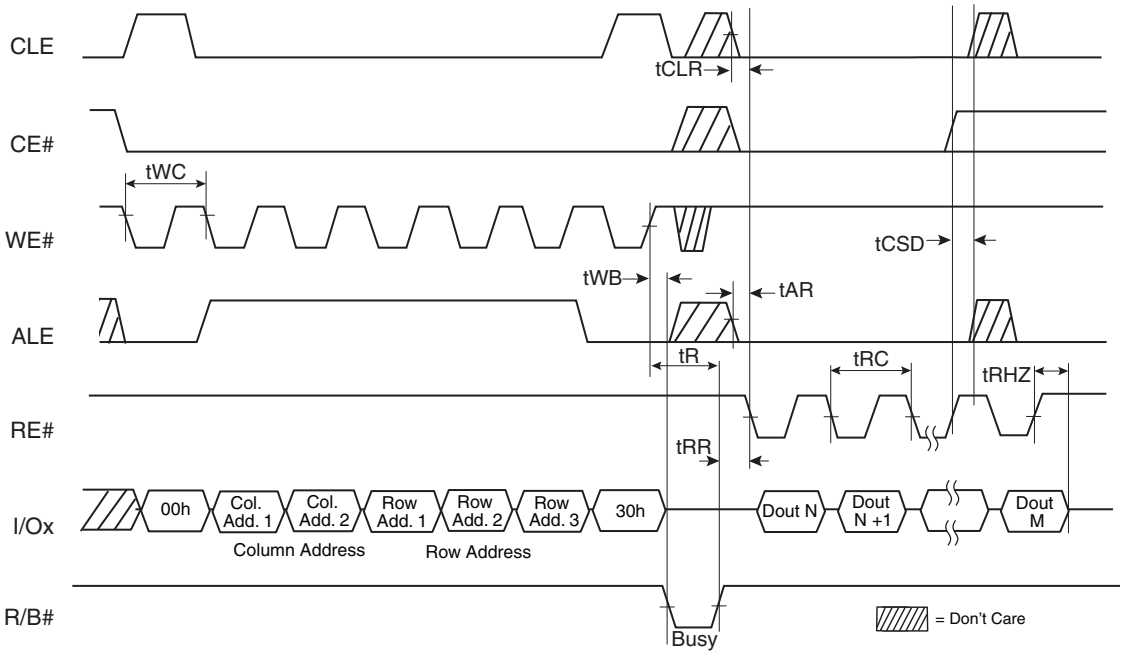


Notes:

1. *Transition is measured at ± 200 mV from steady state voltage with load.*
2. *This parameter is sampled and not 100% tested.*
3. *t_{RLOH} is valid when frequency is higher than 33 MHz.*
4. *t_{RHOH} starts to be valid when frequency is lower than 33 MHz.*

12.7 Page Read Operation

Figure 12.7 Page Read Operation (Read One Page)

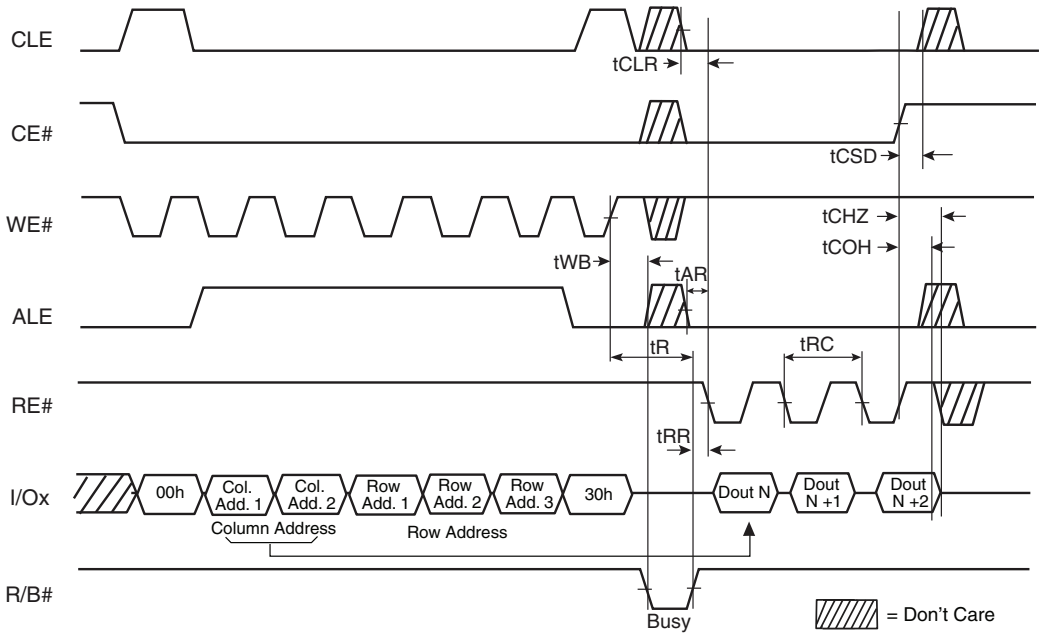


Note:

1. *If Status Register polling is used to determine completion of the read operation, the Read Command (00h) must be issued before data can be read from the page buffer.*

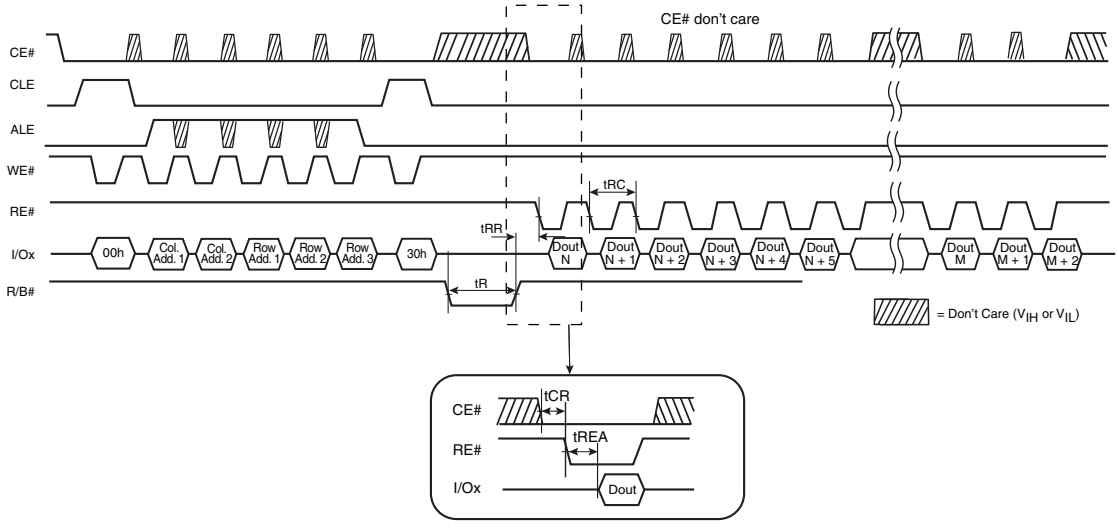
12.8 Page Read Operation (Interrupted by CE#)

Figure 12.8 Page Read Operation Interrupted by CE#



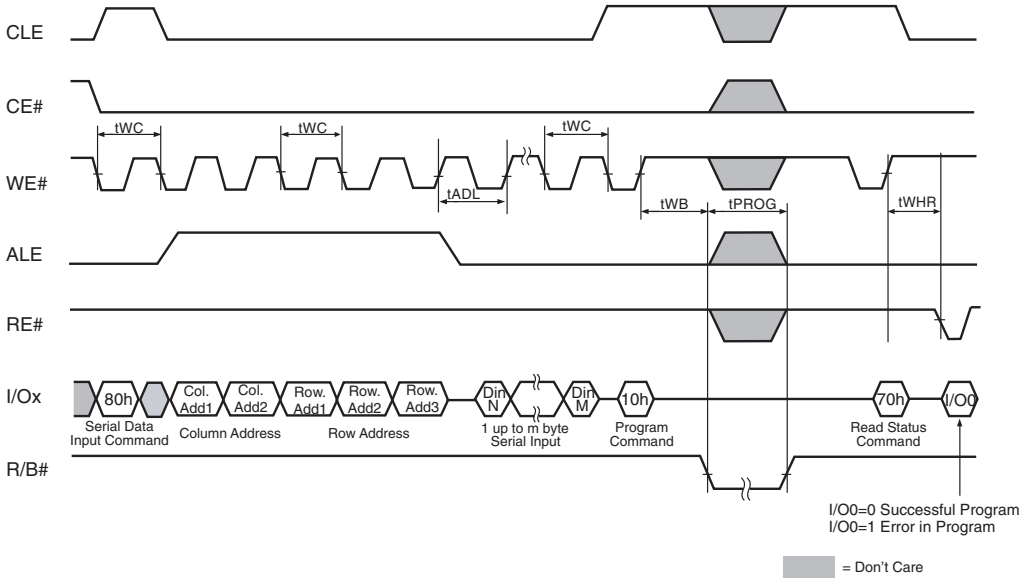
12.9 Page Read Operation Timing with CE# Don't Care

Figure 12.9 Page Read Operation Timing with CE# Don't Care



12.10 Page Program Operation

Figure 12.10 Page Program Operation

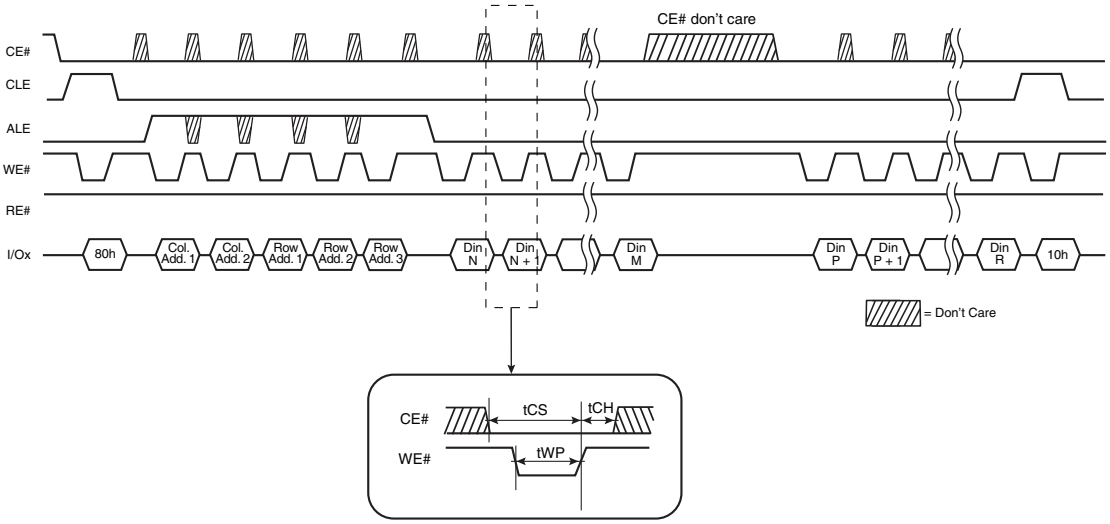


Note:

1. *t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.*

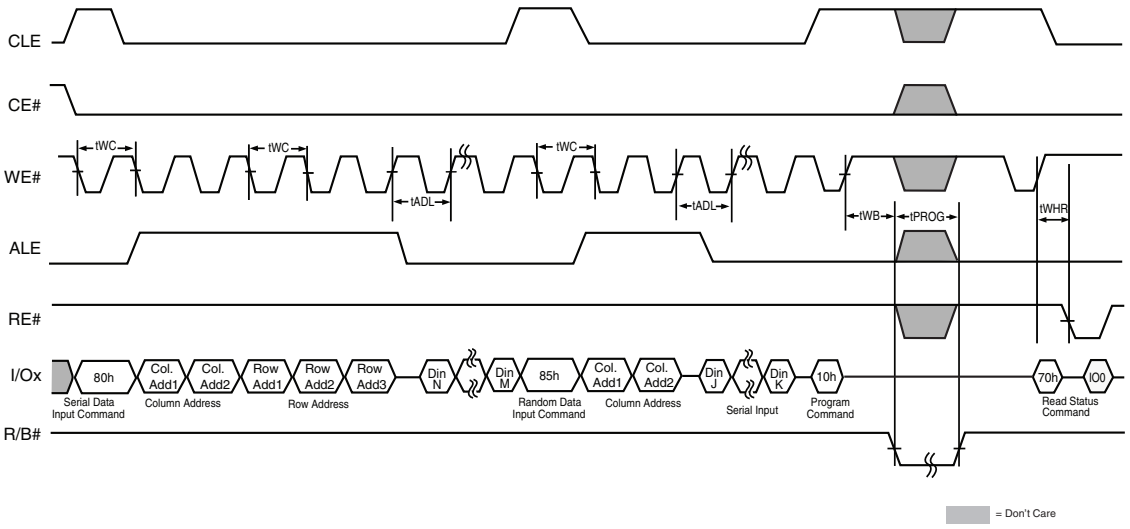
12.11 Page Program Operation Timing with CE# Don't Care

Figure 12.11 Page Program Operation Timing with CE# Don't Care



12.12 Page Program Operation with Random Data Input

Figure 12.12 Random Data Input

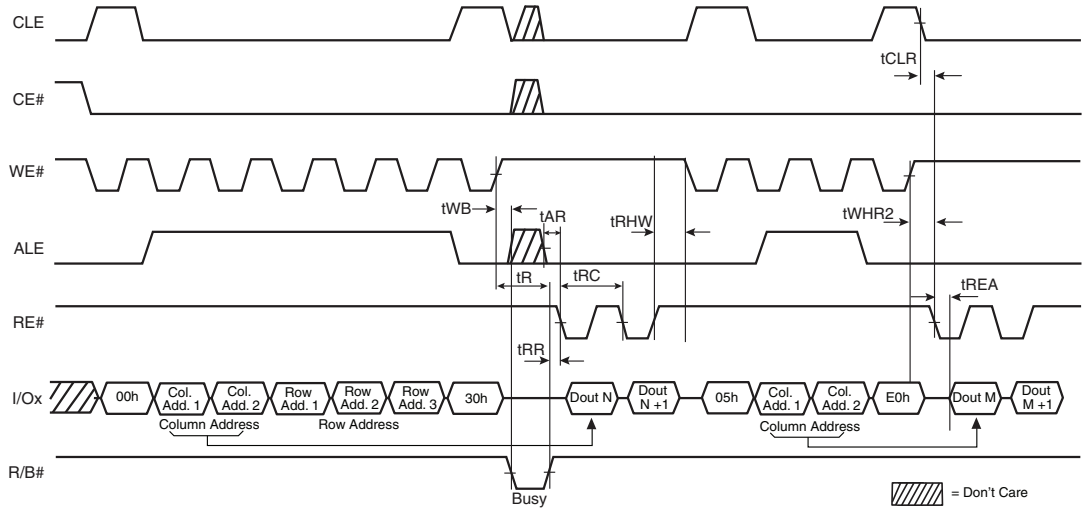


Note:

1. *t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.*

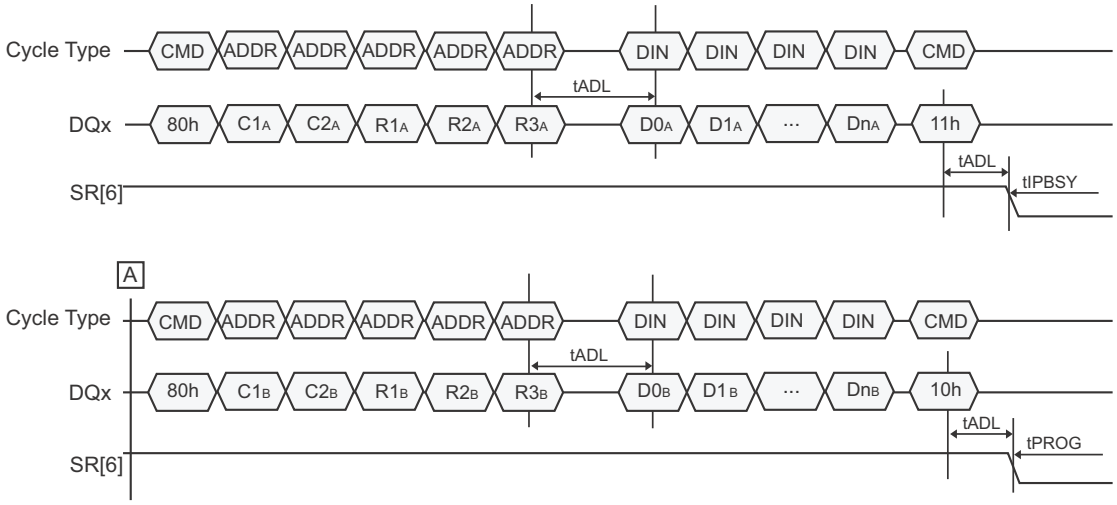
12.13 Random Data Output In a Page

Figure 12.13 Random Data Output



12.14 Multiplane Page Program Operation — S34SL02G2 and S34SL04G2

Figure 12.14 Multiplane Page Program (ONFI 1.0 Protocol)

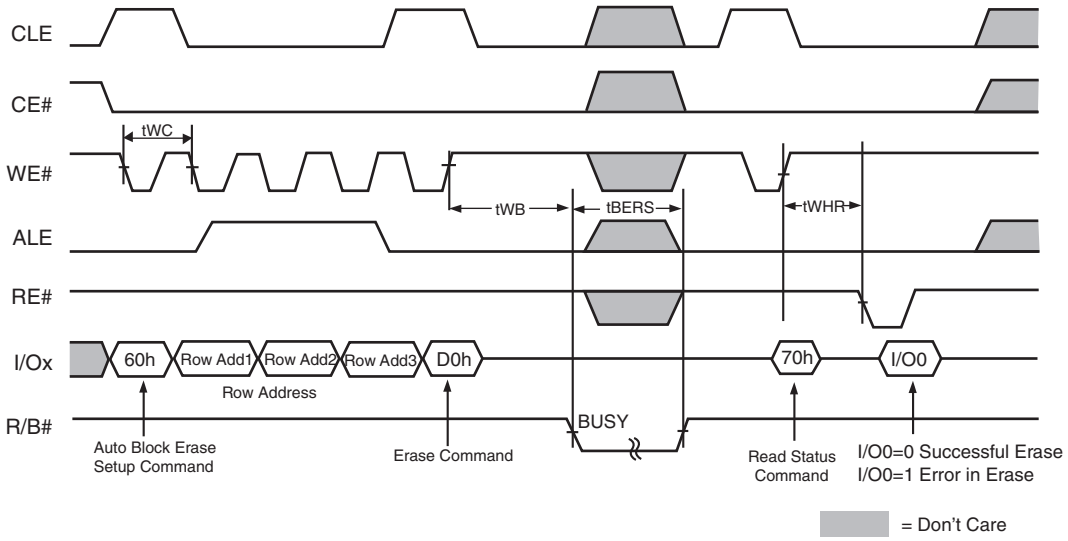


Notes:

1. *C1A-C2A Column address for page A. C1A is the least significant byte.*
2. *R1A-R3A Row address for page A. R1A is the least significant byte.*
3. *D0A-DnA Data to program for page A.*
4. *C1B-C2B Column address for page B. C1B is the least significant byte.*
5. *R1B-R3B Row address for page B. R1B is the least significant byte.*
6. *D0B-DnB Data to program for page B.*
7. *The block address bits must be the same except for the bit(s) that select the plane.*

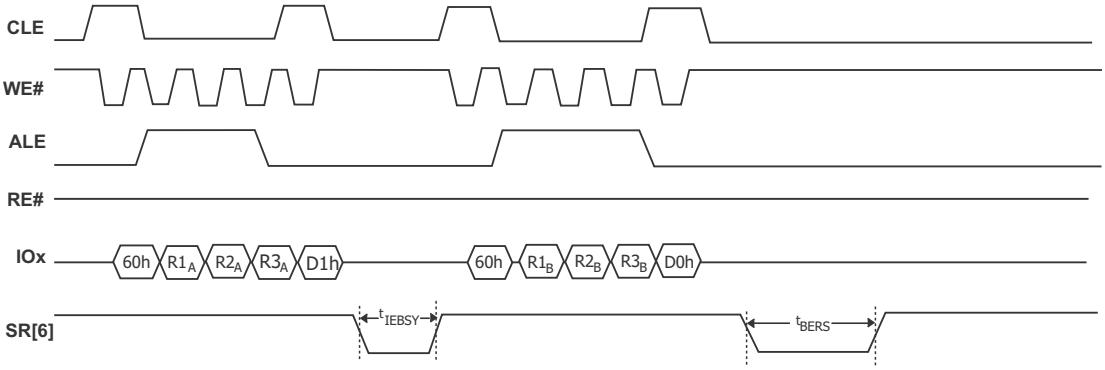
12.15 Block Erase Operation

Figure 12.15 Block Erase Operation (Erase One Block)



12.16 Multiplane Block Erase — S34SL02G2 and S34SL04G2

Figure 12.16 Multiplane Block Erase (ONFI 1.0 Protocol)

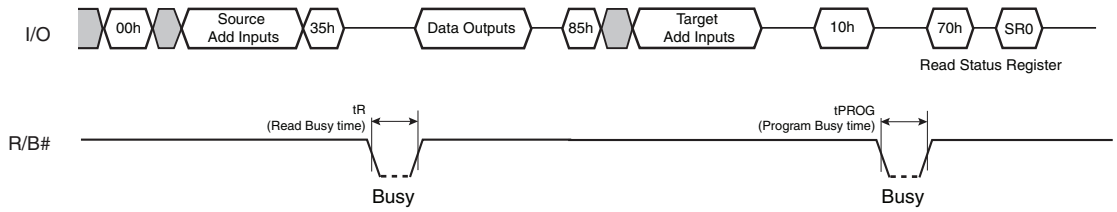


Notes:

1. *R1A-R3A Row address for block on plane 0. R1A is the least significant byte.*
2. *R1B-R3B Row address for block on plane 1. R1B is the least significant byte.*
3. *The block address bits must be the same except for the bit(s) that select the plane.*

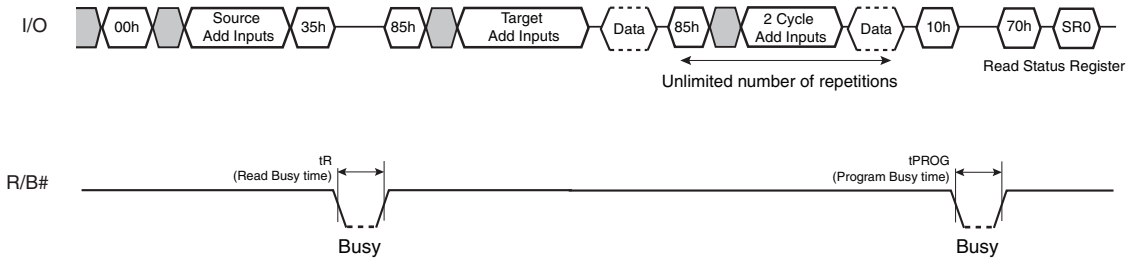
12.17 Copy Back Read with Optional Data Readout

Figure 12.17 Copy Back Read with Optional Data Readout



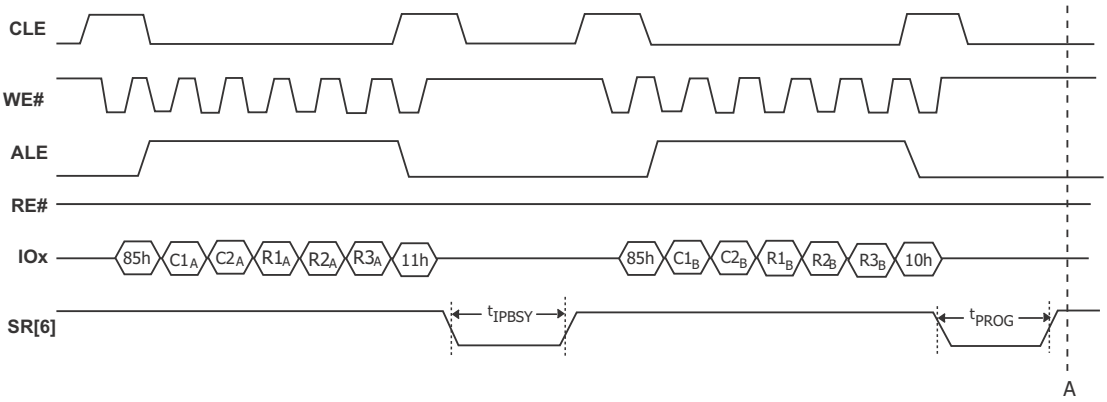
12.18 Copy Back Program Operation with Random Data Input

Figure 12.18 Copy Back Program with Random Data Input



12.19 Multiplane Copy Back Program — S34SL02G2 and S34SL04G2

Figure 12.19 Multiplane Copy Back Program (ONFI 1.0 Protocol)

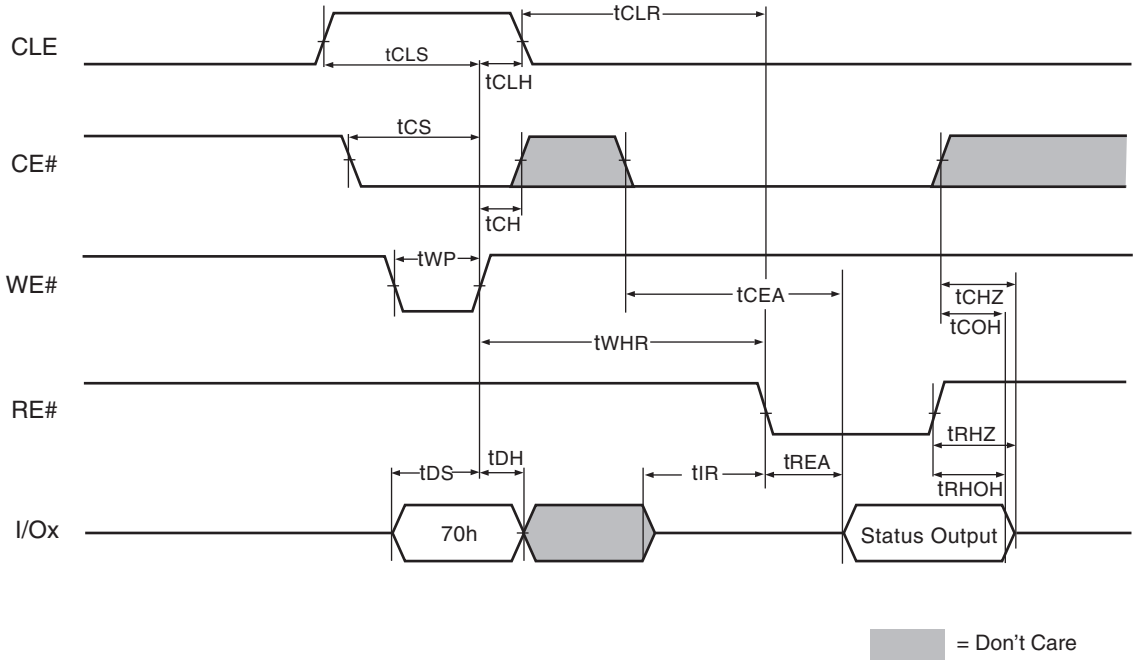


Notes:

1. *C1A-C2A Column address for page A. C1A is the least significant byte.*
2. *R1A-R3A Row address for page A. R1A is the least significant byte.*
3. *C1B-C2B Column address for page B. C1B is the least significant byte.*
4. *R1B-R3B Row address for page B. R1B is the least significant byte.*
5. *The block address bits must be the same except for the bit(s) that select the plane.*

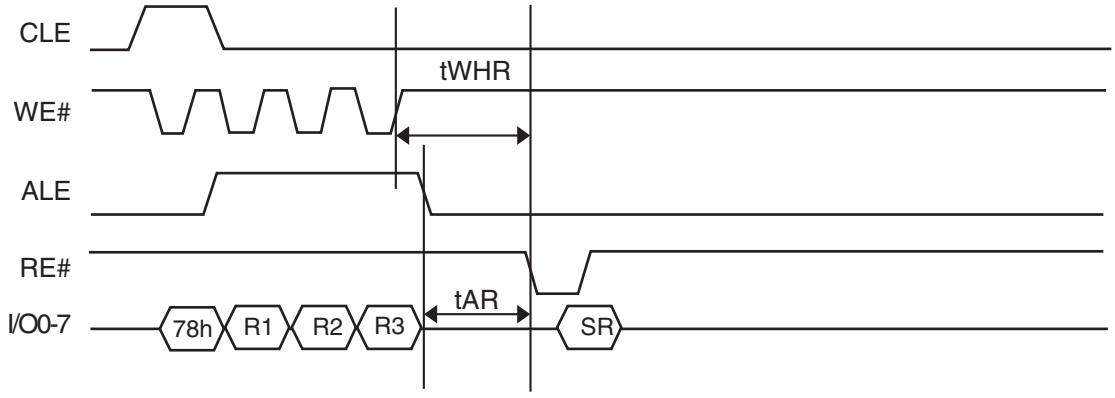
12.20 Read Status Register Timing

Figure 12.20 Read Status Cycle



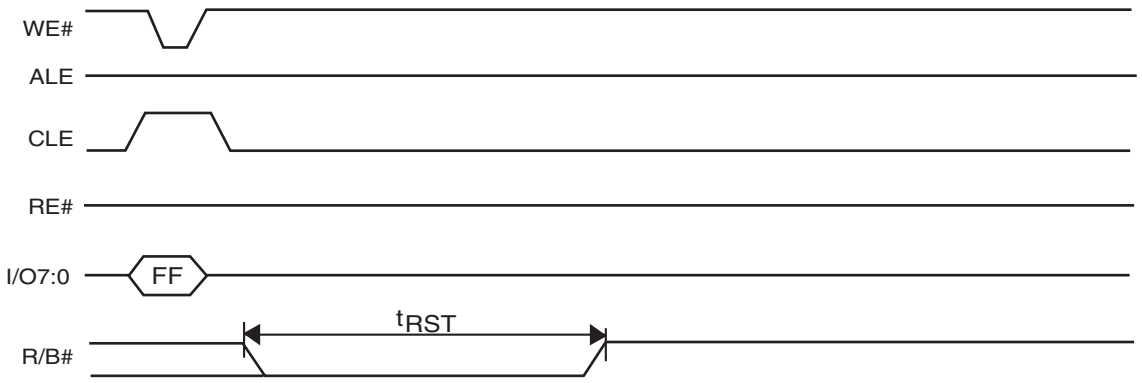
12.21 Read Status Enhanced Timing

Figure 12.21 Read Status Enhanced Timing



12.22 Reset Operation Timing

Figure 12.22 Reset Operation Timing



12.23 Read Cache

Figure 12.23 Read Cache Operation Timing

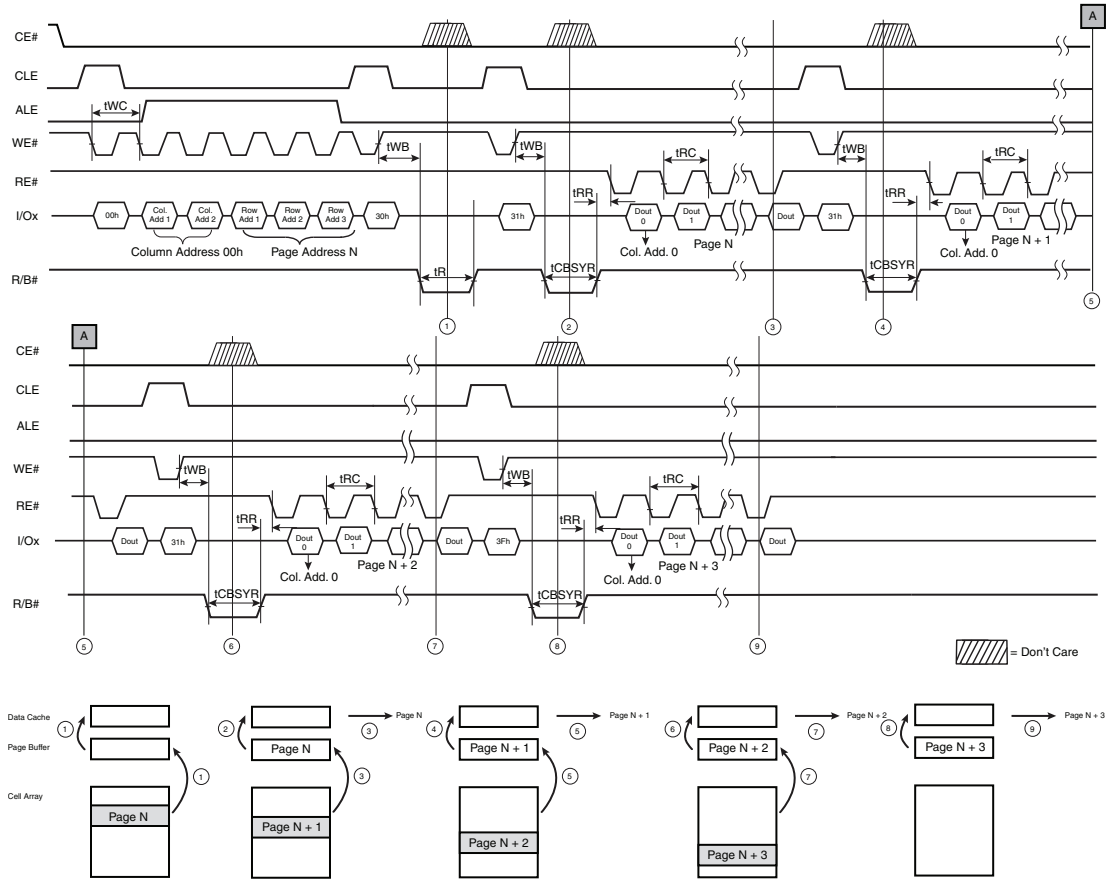


Figure 12.24 "Sequential" Read Cache Timing, Start (and Continuation) of Cache Operation

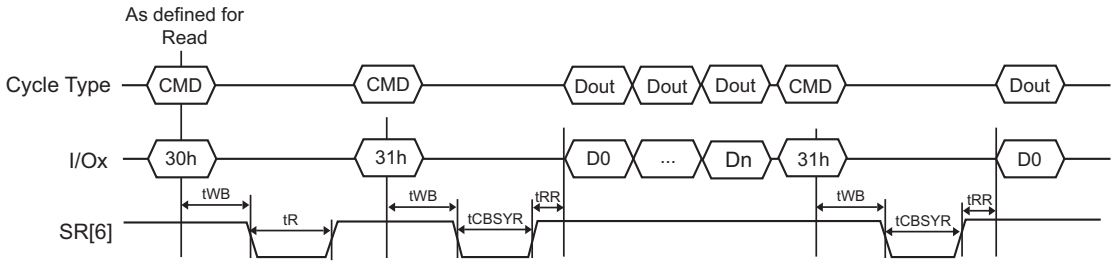


Figure 12.25 "Random" Read Cache Timing, Start (and Continuation) of Cache Operation

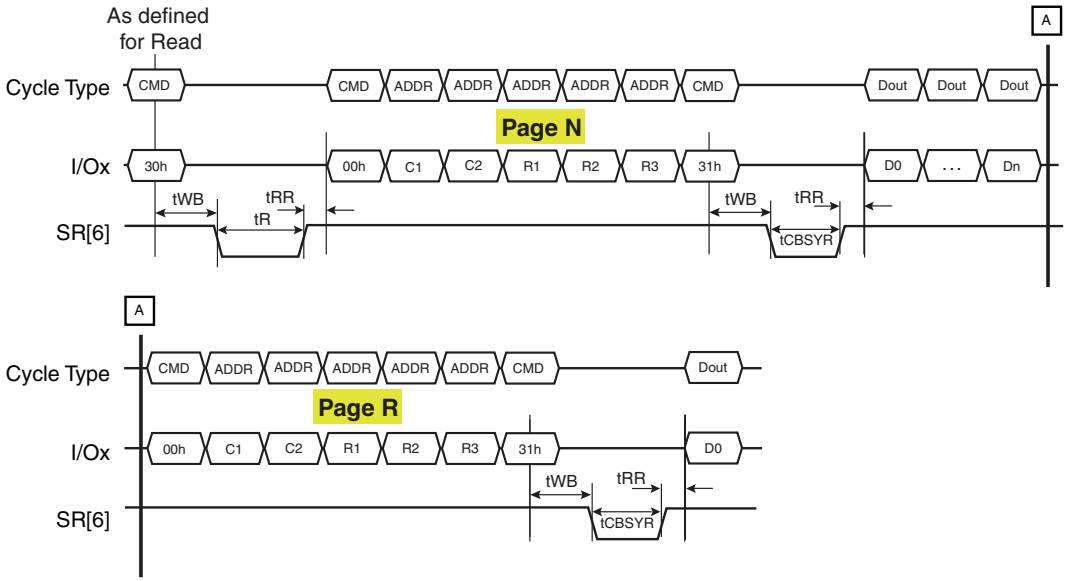
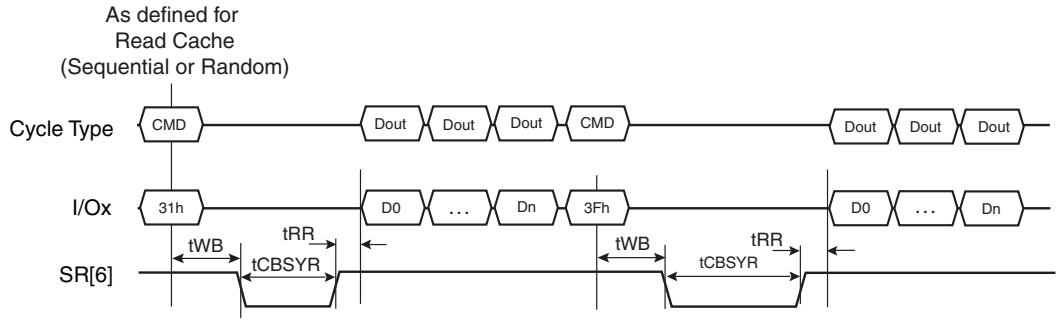
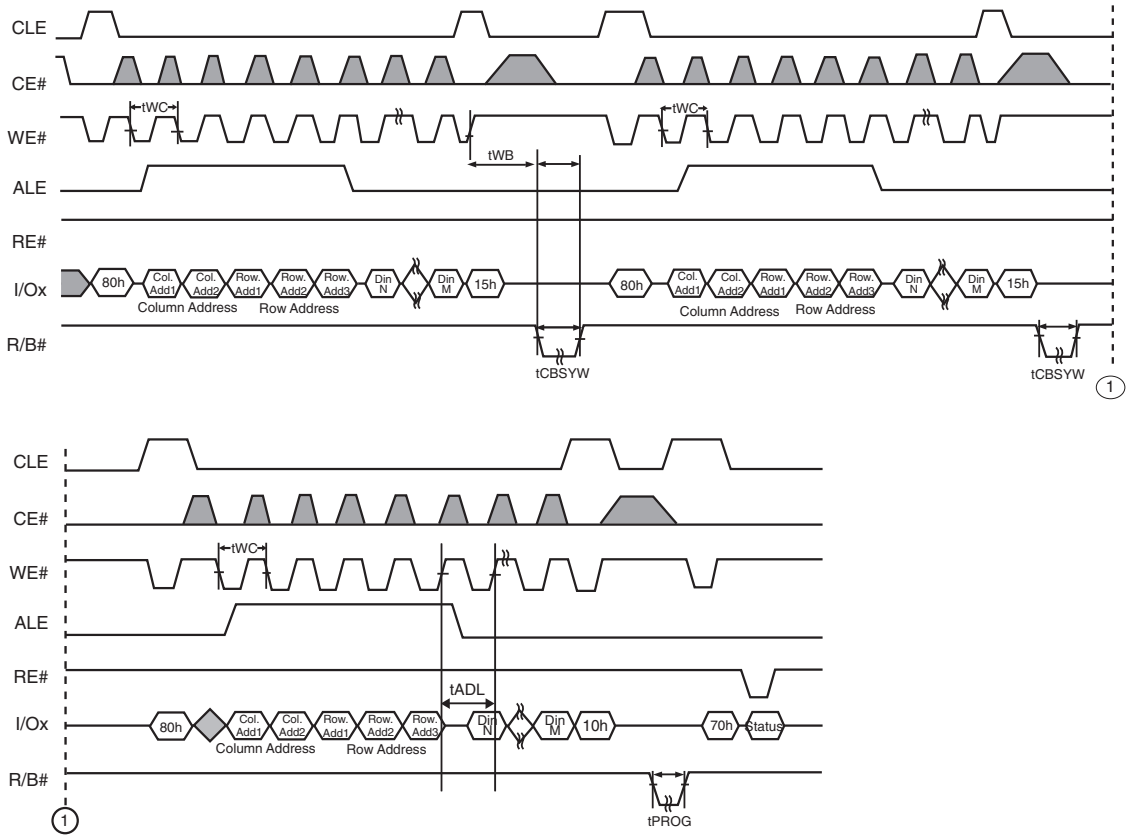


Figure 12.26 Read Cache Timing, End Of Cache Operation



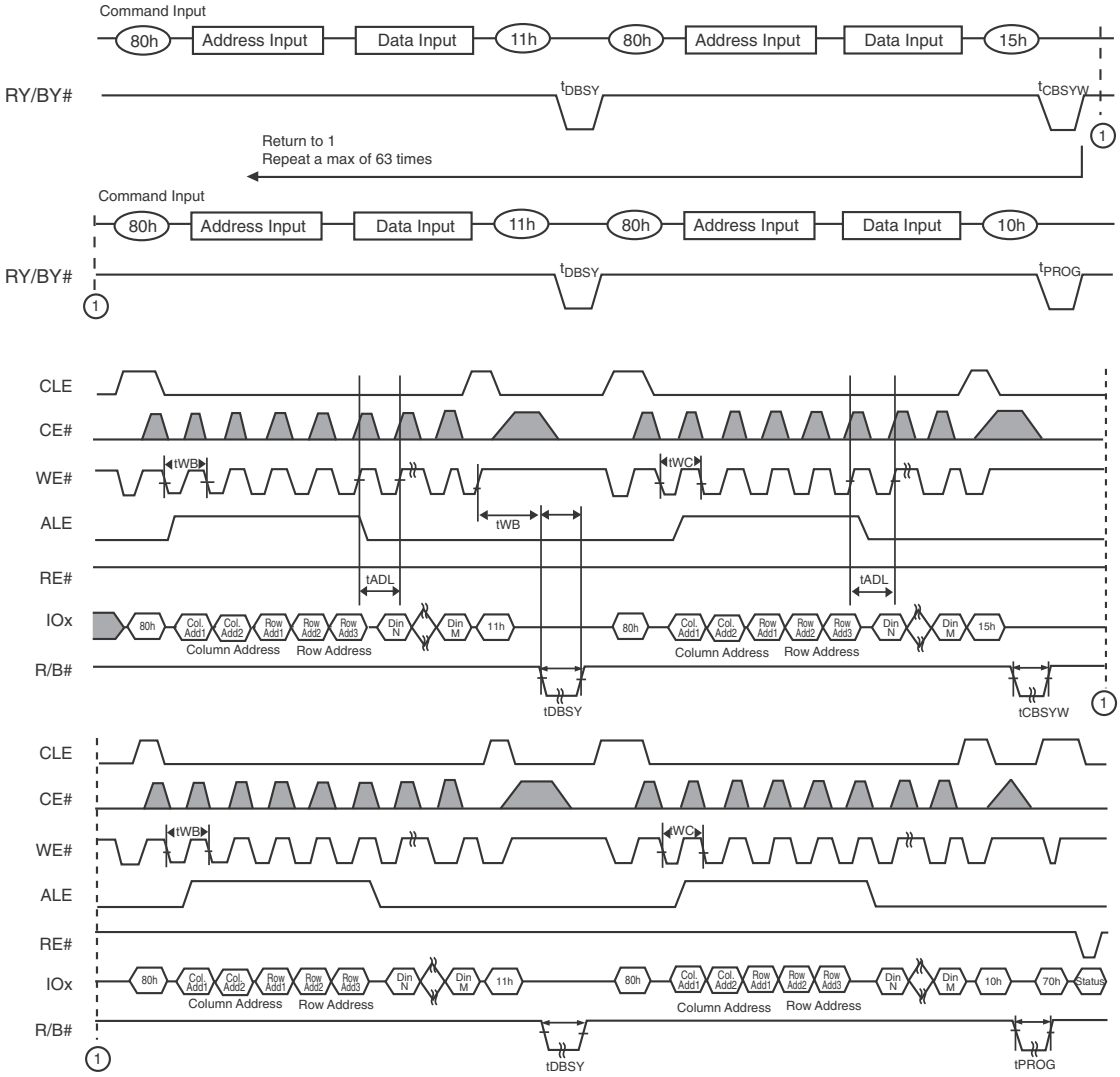
12.24 Cache Program

Figure 12.27 Cache Program



12.25 Multiplane Cache Program — S34SL02G2 and S34SL04G2

Figure 12.28 Multiplane Cache Program (ONFI 1.0 Protocol)

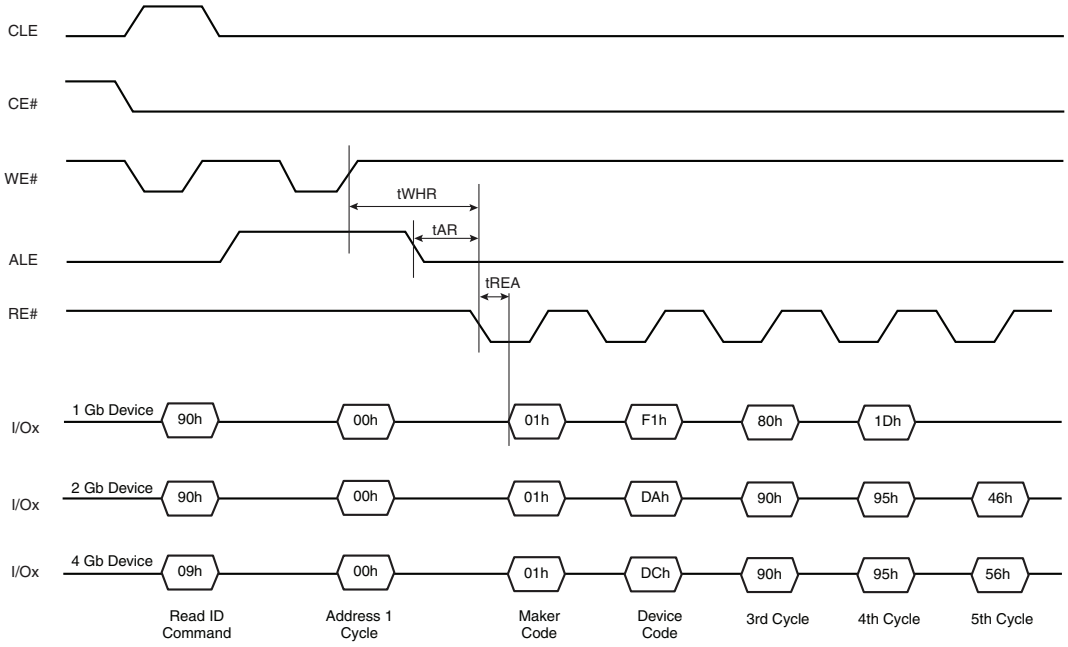


Notes:

1. *The block address bits must be the same except for the bit(s) that select the plane.*
2. *Read Status register (70h) is used in the figure. Read Status Enhanced (78h) can be also used.*

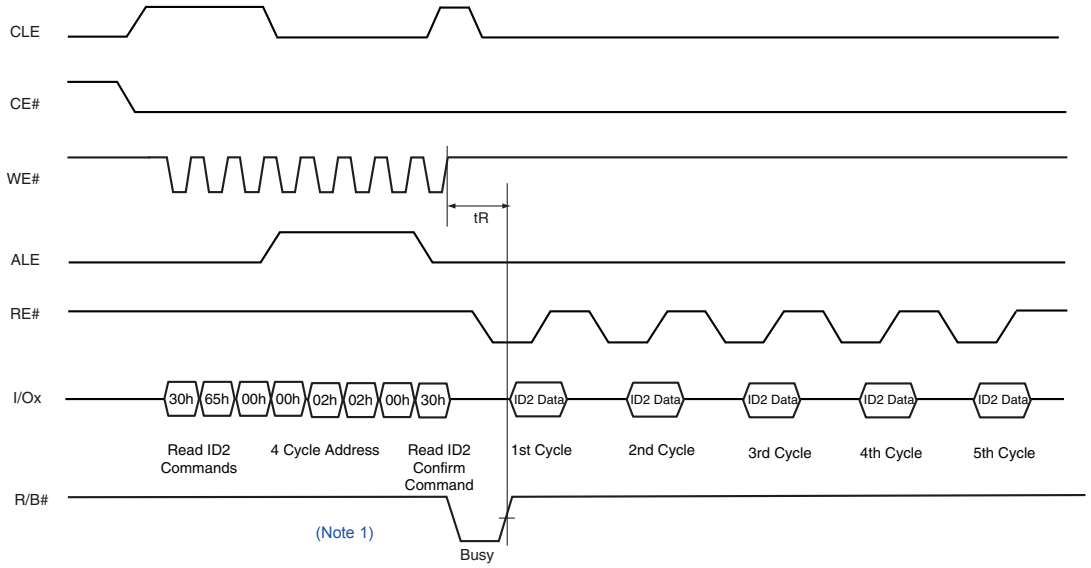
12.26 Read ID Operation Timing

Figure 12.29 Read ID Operation Timing



12.27 Read ID2 Operation Timing

Figure 12.30 Read ID2 Operation Timing

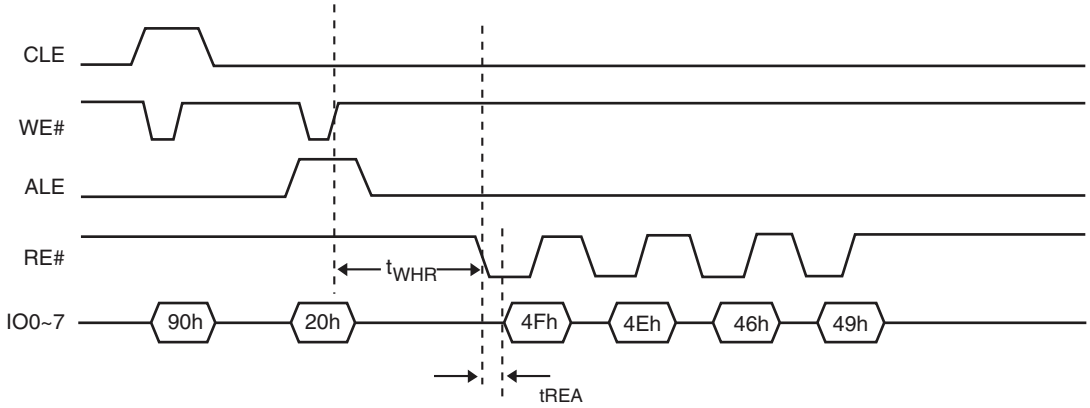


Notes:

1. *4-cycle address is shown for the S34SL01G2. For S34SL02G2 and S34SL04G2, insert an additional address cycle of 00h.*
2. *If Status Register polling is used to determine completion of the Read ID2 operation, the Read Command (00h) must be issued before ID2 data can be read from the flash.*

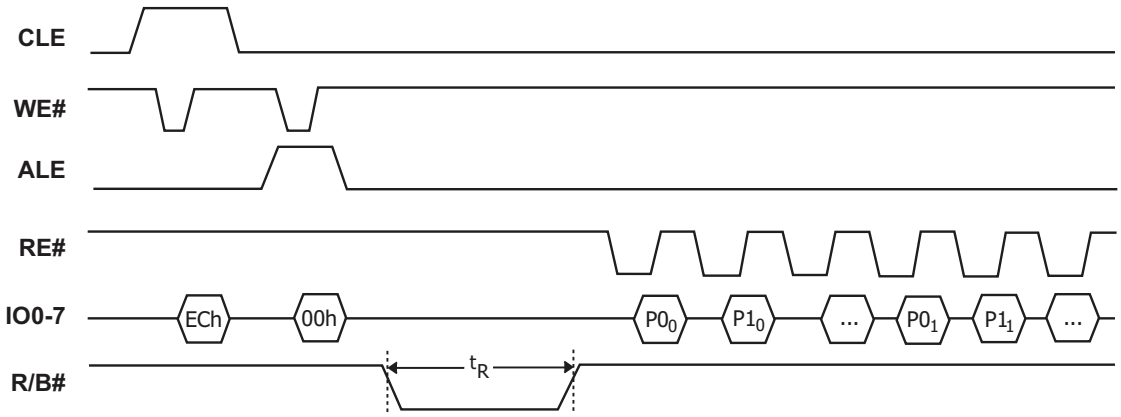
12.28 Read ONFI Signature Timing

Figure 12.31 ONFI Signature Timing



12.29 Read Parameter Page Timing

Figure 12.32 Read Parameter Page Timing

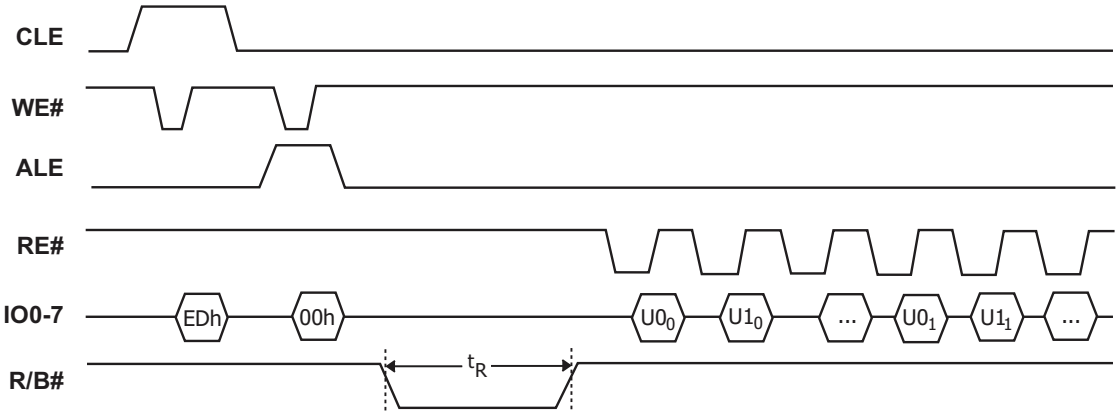


Note:

1. *If Status Register polling is used to determine completion of the read operation, the Read Command (00h) must be issued before data can be read from the page buffer.*

12.30 Read Unique ID Timing

Figure 12.33 Read Unique ID Timing



12.31 WP# Handling

Figure 12.34 Program Enabling / Disabling Through WP# Handling

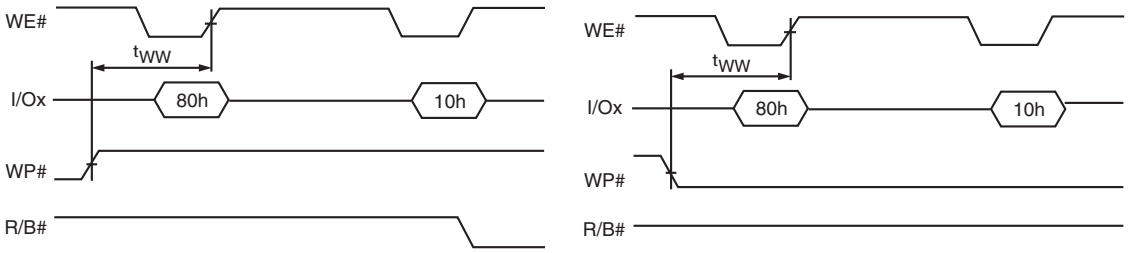
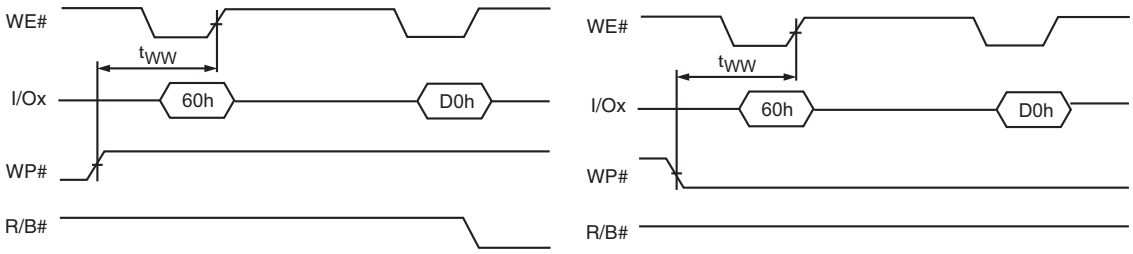


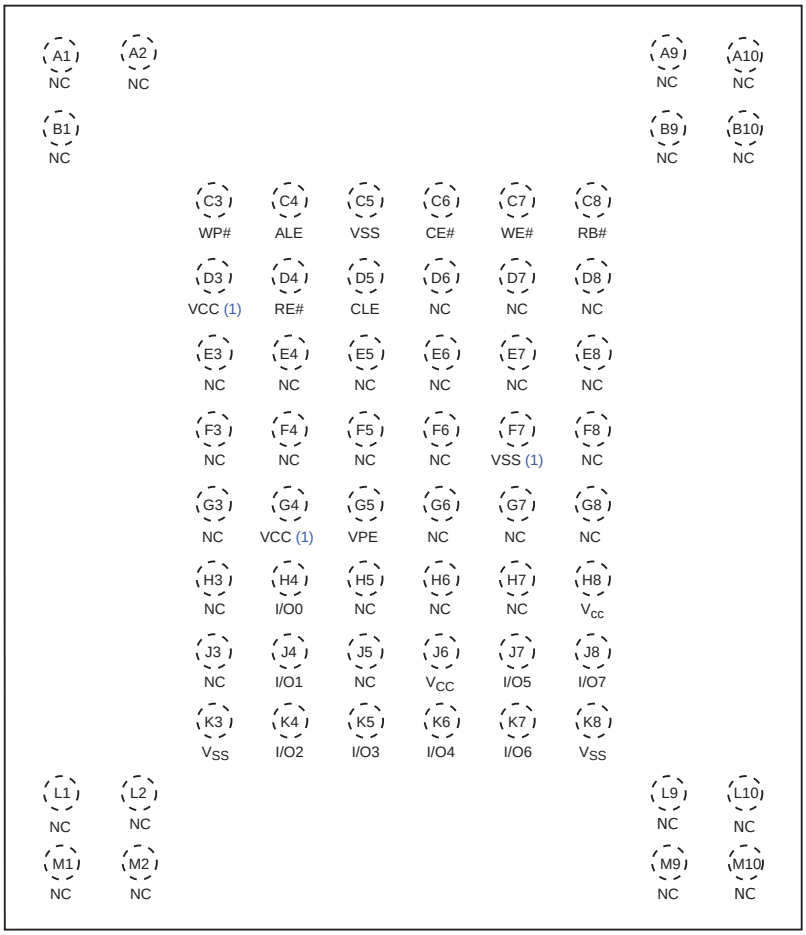
Figure 12.35 Erase Enabling / Disabling Through WP# Handling



13. Physical Interface

13.1 Connection Diagrams

Figure 13.1 63-BGA Contact, x8 Device (Balls Down, Top View)



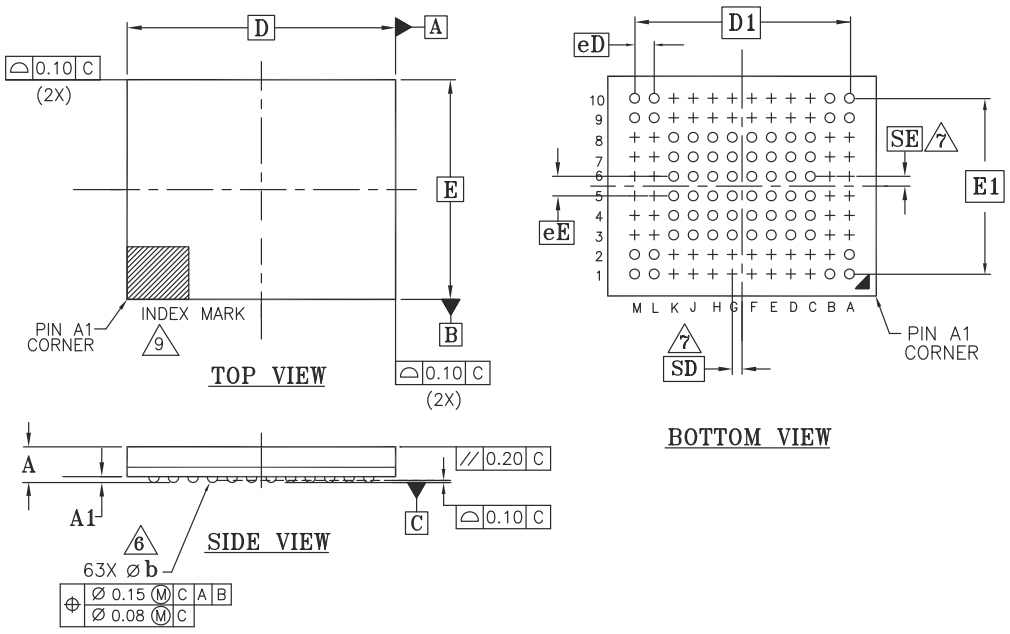
Note:

1. *These pins must be connected to power supply or ground (as designated) following the ONFI specification.*

13.2 Physical Diagrams

13.2.1 63-Ball, Ball Grid Array (BGA)

Figure 13.2 VBM063 — 63-Pin BGA, 11 mm x 9 mm Package



PACKAGE	VBM 063			
JEDEC	M0-207(M)			
	11.00 mm x 9.00 mm NOM PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.00	PROFILE
A1	0.25	---	---	BALL HEIGHT
D	11.00 BSC.			BODY SIZE
E	9.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	63			BALL COUNT
ø b	0.40	0.45	0.50	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC.			BALL PITCH
SD	0.40 BSC.			SOLDER BALL PLACEMENT
SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A3-A8,B2-B8,C1,C2,C9,C10 D1,D2,D9,D10,E1,E2,E9,E10 F1,F2,F9,F10,G1,G2,G9,G10 H1,H2,H9,H10,J1,J2,J9,J10 K1,K2,K9,K10 L3-L8,M3-M8			DEPOPULATED SOLDER BALLS

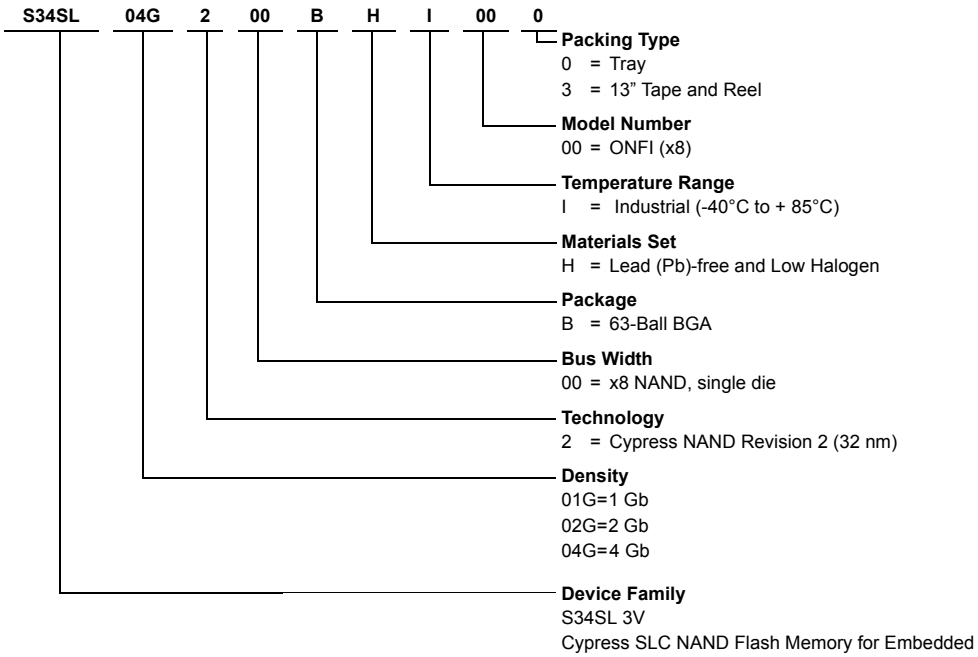
NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE TOTAL NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

g5011\ 16-038.25 \ 6.5.13

14. Ordering Information

The ordering part number is formed by a valid combination of the following:



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations								
Device Family	**Density**	**Technology**	**Bus Width**	**Package Type**	**Temperature Range**	**Additional Ordering Options**	**Packing Type**	**Package Description**
S34SL	01G	2	00	BH	I	00	0, 3	BGA (1)
	02G							
	04G							

Note:

1. BGA package marking omits the leading “S34” and the Packing Type designator from the ordering part number.

15. Errata

This section describes the errata for the Cypress Secure NAND S34SL-2 Product Family. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions. For a list of sales offices, go to http://www.cypress.com/sales.

Part Numbers Affected

Part Number	Device Characteristics
S34SL01G200BHI000	All variants
S34SL02G200BHI000	All variants
S34SL04G200BHI000	All variants

S34SL-2 Qualification Status

Product Status: Sampling

S34SL-2 Errata Summary

The following table defines the errata applicability to available S34SL-2 devices. An "X" indicates that the errata pertains to the selected device.

Note Errata items, in the table below, are hyperlinked. Click on any item entry to jump to its description.

Items	Part Number	Silicon Revision	Fix Status
[1]. Block Lock Status (BLS) register command (72h) does not output the block lock status	S34SL01G200BHI000 S34SL02G200BHI000 S34SL04G200BHI000	*A	Silicon fix planned. Samples of the fixed device will available by November 2015.

1. Block Lock Status (BLS) register command (72h) does not output the block lock status

- **Problem Definition**

  The Block Lock Status (BLS) register command of 72h does not output the block lock status. The alternative Block Lock Status (BLS) register command of 7Ah (supported on the S34SL02G2 and S34SL04G2) is not affected.

- **Parameters Affected**

  NA

- **Trigger Conditions**

  Issuing the BLS command of 72h

- **Scope of Impact**

  It will impact the functionality of the system.

- **Workaround**

  S34SL02G2/S34SL04G2 will accept the alternative BLS register command of 7Ah. There is no workaround for S34SL01G2.

- **Fix Status**

  Silicon fix planned. S34SL01G2 will support the Block Lock Status (BLS) register command of 72h. S34SL02G2/S34SL04G2 will support the Block Lock Status (BLS) register command of 72h or 7Ah. Samples of the fixed device will be available by November 2015.

16. Revision History

Spansion Publication Number: S34SL01G2_04G2

Section	Description
Revision 01 (July 9, 2015)	
	Initial release

Document History Page

Document Title: S34SL01G2, S34SL02G2, S34SL04G2 1 Gbit (128 Mbyte), 2 Gbit (256 Mbyte), 4 Gbit (512 Mbyte) Secure NAND Flash Memory for Embedded Document Number: 001-99252				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	MAMC	07/09/2015	Initial release
*A	4854305	MAMC	08/06/2015	Updated to Cypress template. Updated Table 4.1. Updated Figure 6.5. Added 72h command as an alternative Block Lock Status (BLS) command code in Block Lock Status. Removed Figure 13.2 63-BGA Contact, x16 Device (Balls Down, Top View). Updated Ordering Information. Added Errata.

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