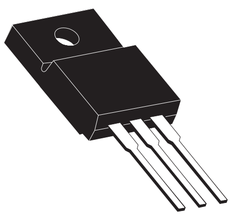
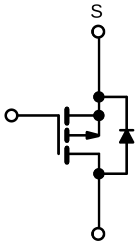
Power MOSFET

[illegible]		
V_{DS} (V)	- 200	
$R_{DS(on)}$ (W)	V_{GS} = - 10 V	1.5
Q_g (Max.) (nC)	15	
Q_{gs} (nC)	3.2	
Q_{gd} (nC)	8.4	
Configuration	Single	

TO-220 FULLPAK





P-Channel MOSFET

[illegible]

- Isolated Package
- High Voltage Isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz)
- Sink to Lead Creepage Dist. = 4.8 mm
- P-Channel
- Dynamic dV/dt
- Low Thermal Resistance
- Lead (Pb)-free Available

Pb Available
RoHS*
COMPLIANT

[illegible]

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.
The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

[illegible]	
Package	TO-220 FULLPAK
Lead (Pb)-free	IRFI9620GPbF
	SiHFI9620G-E3
SnPb	IRFI9620G
	SiHFI9620G

[illegible] T_C = 25 °C, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	- 200	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	T_C = 25 °C	I_D	- 3.0	A
		T_C = 100 °C		- 1.9	
Pulsed Drain Current[a]			I_{DM}	- 12	
Linear Derating Factor				0.24	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	80	mJ
Repetitive Avalanche Current[a]			I_{AR}	- 3.0	A
Repetitive Avalanche Energy[a]			E_{AR}	3.0	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	30	W
Peak Diode Recovery dV/dt[c]			dV/dt	- 5.0	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = - 50 V, starting T_J = 25 °C, L = 13 mH, R_G = 25 W, I_{AS} = - 3.0 A (see fig. 12).
c. I_{SD} ¢- 3.9 A, dI/dt ¢95 A/µs, V_{DD} ¢V_{DS}, T_J ¢150 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

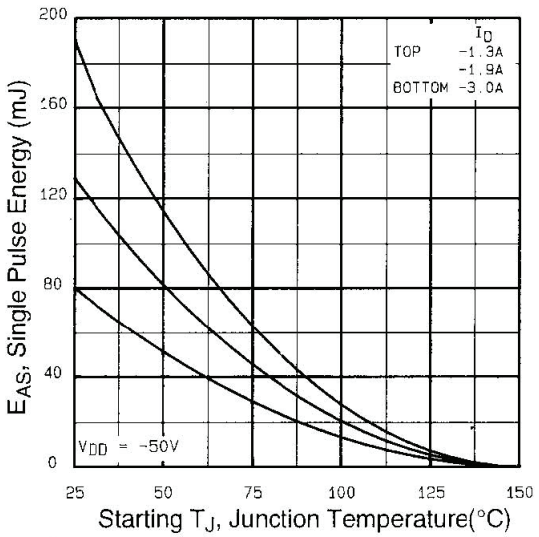


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

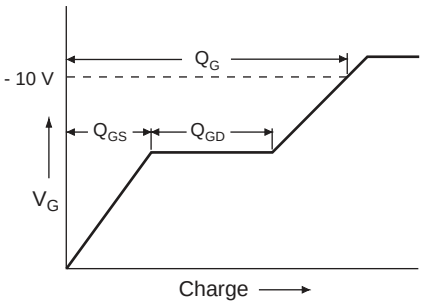


Fig. 13a - Basic Gate Charge Waveform

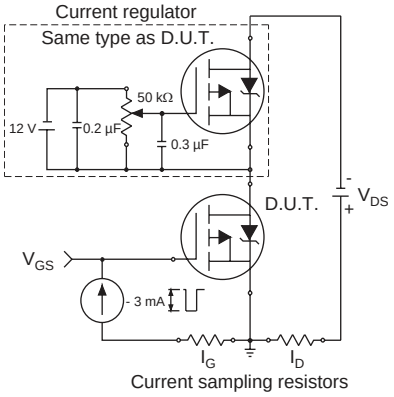
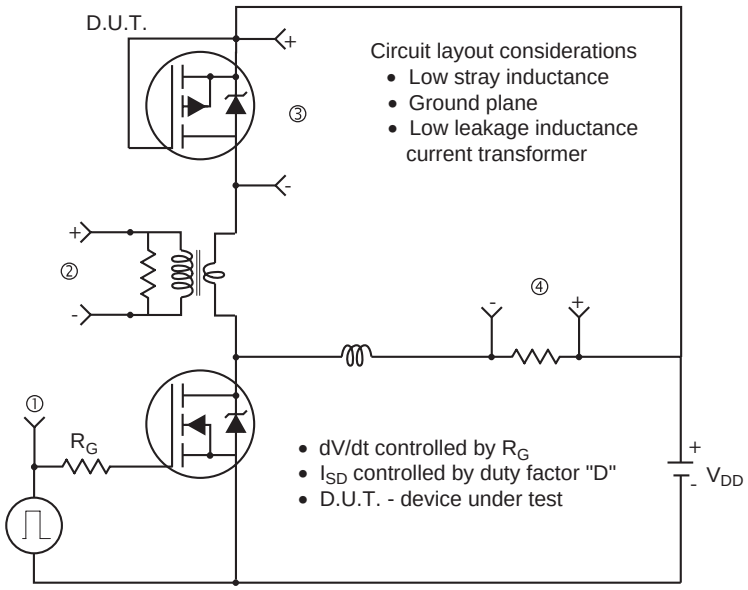
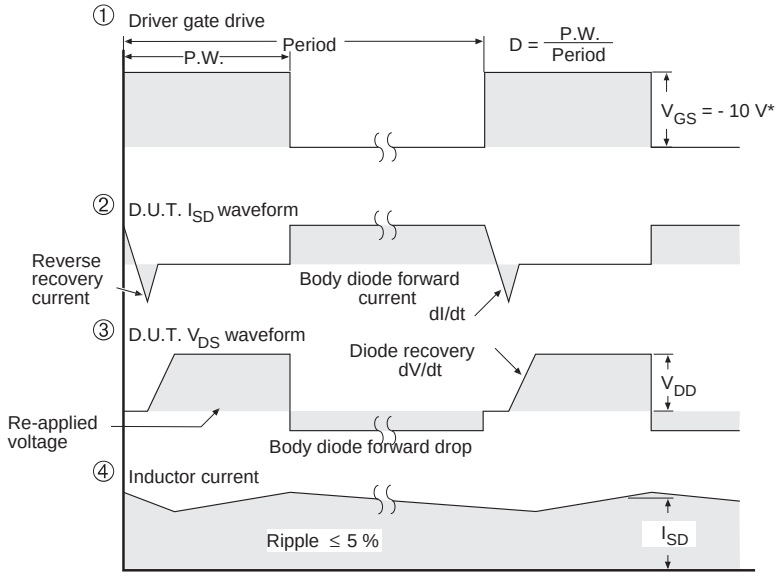


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



• Compliment N-Channel of D.U.T. for driver



* V_{GS} = - 5 V for logic level and - 3 V drive devices

Fig. 14 - For P-Channel

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