swissbit®

Product Data Sheet

Industrial SDHC Memory Card

S-40 Series

SD/SDHC compliant

made in germany

S-40 Series

Industrial SDHC Memory Card – 4/8/16/32GByte

Main Features

- Fully compliant with SD Memory Card specification 3.0
  - SDHC high speed mode, non UHS
  - Speed class 6 according SD3.0 specification
  - SD2.0 backward compliant
  - FAT32 preformatted

- High performance 3.0 specification
  - SD burst up to 25MB/s
  - SD Normal speed 0…25MHz clock rate
  - SD High speed 25…50MHz clock rate
  - Flash burst up to 90MB/s
  - Up to 24MByte/sec sequential data rate

- Power Supply: (Low-power CMOS technology)
  - 2.7…3.6V normal operating voltage

- Standard SD Memory card form factor
  - 32.0mm x 24.0mm x 2.1mm and Write Protect slider

- Optimized FW algorithms especially for high read access and long data retention applications
  - Patented power-off reliability technology
  - Wear Leveling technology
    Equal wear leveling of static and dynamic data. The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is guaranteed
  - Write Endurance technology
    Due to intelligent wear leveling an even use of the entire flash is guaranteed, regardless how much "static" (OS) data is stored.
  - Read Disturb Management
    The read commands are monitored and the content is refreshed when critical levels have occurred
  - Data Care Management
    The interruptible background process maintain the user data for Read Disturb effects or Retention degradation due to high temperature effects
  - Near miss ECC technology
    Minimize the risk of uncorrectable bit failure over the product life time. Each read command analyzes the ECC margin level and refresh data if necessary
  - Diagnostic features with Life Time Monitoring tool support

- High reliability
  - Designed for industrial market especially read intensive application like navigation, infotainment, POS/POI, Medical and general boot medium use case
  - The product is optimized for long life cycle that requires a good data retention because of high temperature mission profile.
  - Intensive write application should use the S-450 Series SLC cards
  - Number of card insertions/removals up to 20,000
  - Extended and Industrial Temperature range -25° up to 85°C and -40° up to 85°C, respectively
  - SIP (System In Package) process for extreme dust, water and ESD proof
  - Selected AEC-Q100 qualification

- Controlled BOM & PCN process
- Manufactured in a TS 16949 certified factory
- Customized options like CID registers, CPRM keys, firmware incl. settings and marking by projects

1 Order Information

1.1 Standard product list

Table 1: Standard Product List

Density	Part Number	Temp. Range	Flash Technology
4GB	SFSD4096LgBM1TO-t-GE-1x1-STD	-25°C to 85°C or -40°C to 85°C	MLC NAND Flash
8GB	SFSD8192LgBM1TO-t-GE-1x1-STD		
16GB	SFSD016GLgBM1TO-t-GE-1x1-STD		
32GB	SFSD032GLgBM1TO-t-LF-1x1-STD		

g defines the product generation
x defines the FW
t defines the temperature range (E=-25°C to +85°C, I=-40°C to +85°C)

1.2 Current product generation

Table 2: Standard Product List

Density	Part Number	Temp. Range	Flash Technology
4GB	SFSD4096L2BM1TO-E-GE-121-STD	-25°C to 85°C	MLC NAND Flash
8GB	SFSD8192L2BM1TO-E-GE-121-STD		
16GB	SFSD016GL2BM1TO-E-GE-121-STD		
32GB	SFSD032GL2BM1TO-E-LF-121-STD		
4GB	SFSD4096L2BM1TO-I-GE-121-STD	-40°C to 85°C	
8GB	SFSD8192L2BM1TO-I-GE-121-STD		
16GB	SFSD016GL2BM1TO-I-GE-121-STD		
32GB	SFSD032GL2BM1TO-I-LF-121-STD		

Contents

2 Product Specification

The SD Memory Card is a small form factor non-volatile memory card which provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.
The card operates in two basic modes:

- **SD/SDHC card mode**
- **SPI mode**

The SD Memory Card also supports SD **High Speed mode** with up to 50MHz clock frequency.
The cards are compliant with

- SD Memory card Specification Part 1, Physical layer Specification V3.01
- SD Memory card Specification Part 2, File System Specification V3.00
- SD Memory card Specification Part 3, Security Specification V3.00
- SD Memory Card Addendum V4.00

Simplified specifications are available at https://www.sdcard.org/downloads/pls/simplified_specs/

The Card has an internal **intelligent controller** which manages interface protocols, data storage and retrieval as well as hardware **BCH Error Correction Code (ECC)**, **defect handling, diagnostics and clock control**.
The **advanced wear leveling** mechanism assures an equal usage of the Flash memory cells to extend the life time.
The hardware BCH-code ECC allows to **detect and correct up to 40 defect bits per 1kByte.**
The controller performs control read operations and checks the consistence of the data. If an error of some bits is detected, the card refreshes all data in the flash cells to prevent data retention problems.

The card has a **power-loss management feature** to prevent data corruption after power-down.

The cards are RoHS compliant and lead-free.

2.1 System Performance

Table 3: Performance

System Performance		typ	max	Unit
Burst Data transfer Rate (max SD clock 50MHz)			25	MB/s
Sustained Sequential Read	4...8GB	23 (1)(2)	24(1)(3)	
	16GB/32GB	23(1)(2)	24(1)(3)	
Sustained Sequential Write	4...8GB	11 / 12 (1)(2)	14(1)(3)	
	16GB/32GB	11 / 12(1)(2)	14(1)(3)	

1. All values refer to Toshiba Flash 32/64Gb
2. Sustained Speed measured with USB-SD Memory Card reader. It depends on burst speed, flash number, and file size.
3. Maximum values were measured with Testmetrix tester.

2.2 Environmental Specifications

2.2.1 Recommended Operating Conditions

Table 4: SD Memory Card Recommended Operating Conditions

Parameter	min	typ	max	unit
Extended Operating Temperature	-25	25	85*)	°C
Industrial Operating Temperature	-40	25	85*)	°C

2.2.2 Recommended Storage Conditions

Table 5: SD Memory Card Recommended Storage Conditions

Parameter	min	typ	max	unit
Extended Storage Temperature	-25	25	100*)	°C
Industrial Operating Temperature	-40	25	100*)	°C

*) high temperature storage without operation reduces the data retention, in operation the data will be refreshed, if data error issues were detected

2.2.3 Humidity & EMC

Table 6: Humidity & EMC

Parameter	Condition
Humidity (non-condensing)	85% RH @85°C 1000h
ESD	up to ±4 kV (contact discharge), according to IEC61000-4-2 and SDA, Human Body Model 150pF/ 330Ohm, on each contact pad, non-operating up to ±15 kV, (air discharge), according to IEC61000-4-2 and SDA, Human Body Model 150pF/ 330Ohm, isolated contact pad area, non-operating

2.2.4 Environmental Conditions

Table 7: Environmental Conditions

Parameter	Condition
UV light exposure	UV: 254nm, 15Ws/cm² according to ISO7816-1
X-Ray	0.1 Gy 70keV to 140KeV (ISO7816-1) according SDA
Durability	20,000 mating cycles
Drop Test	1.5m free fall
Bending / Torque	10N / 0.15Nm ±2.5° max
Mechanical Shock	1500G, 0.5ms, half sine wave ±xyz-axis, 4 pulses each non-operating, JESD22B110/B104 Condition B
Vibration	50G, p-p, 20..2000Hz, sweep xyz-axis, 4 pulses each, non-operating, MIL-STD-883 M2007.3 Condition B

2.3 Physical Dimensions

Table 8: Physical Dimensions

Outer Physical Dimensions	Value	Unit
Length	32.00±0.1	mm
Width	24.00±0.1	
Thickness	2.10±0.15	
Weight (typ.)	2	g

2.4 Reliability

Table 9: Reliability

Parameter	Value
Data Retention at beginning @ 40°C	10 years *)
Data Retention at life end (2k PE cycles) @ 40°C	1 year *)

*) After every power on the card reads the whole flash and performs a data refresh if necessary. So the data retention can be much longer in most use cases.

3 Capacity specification

Table 10: SD Memory Card capacity specification

Capacity	Sectors	Total addressable capacity (Byte)
4GB	7'774'208	3'980'394'496
8GB	15'802'368	8'090'812'416
16GB	31'834'112	16'299'065'344
32GB	63'930'368	32'732'348'416

4 Card physical

4.1 Physical description

The SD Memory Card contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s). Figure 1 and Figure 2 show card dimensions.

Figure 1: Mechanical Dimensions SD Memory Card

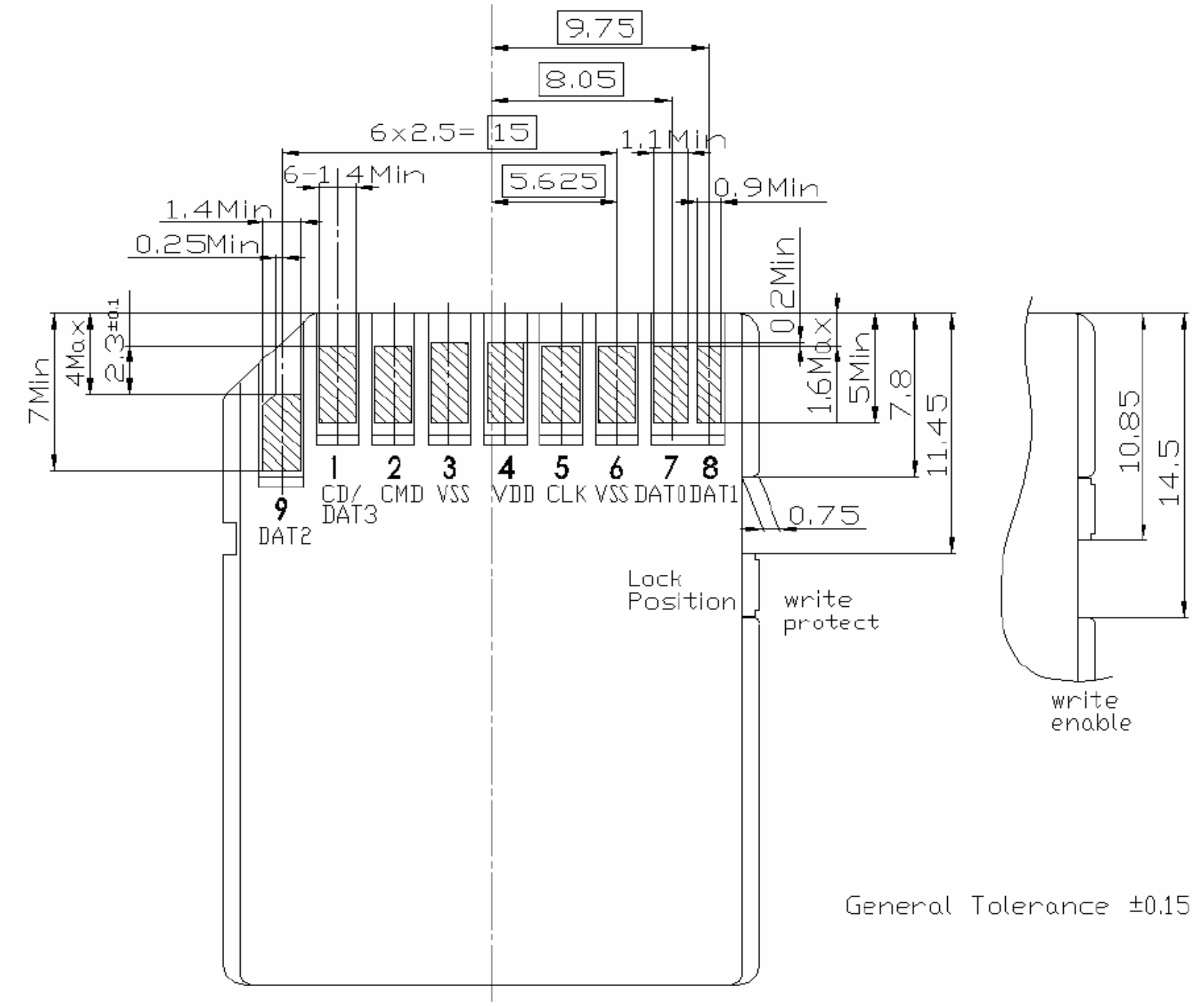
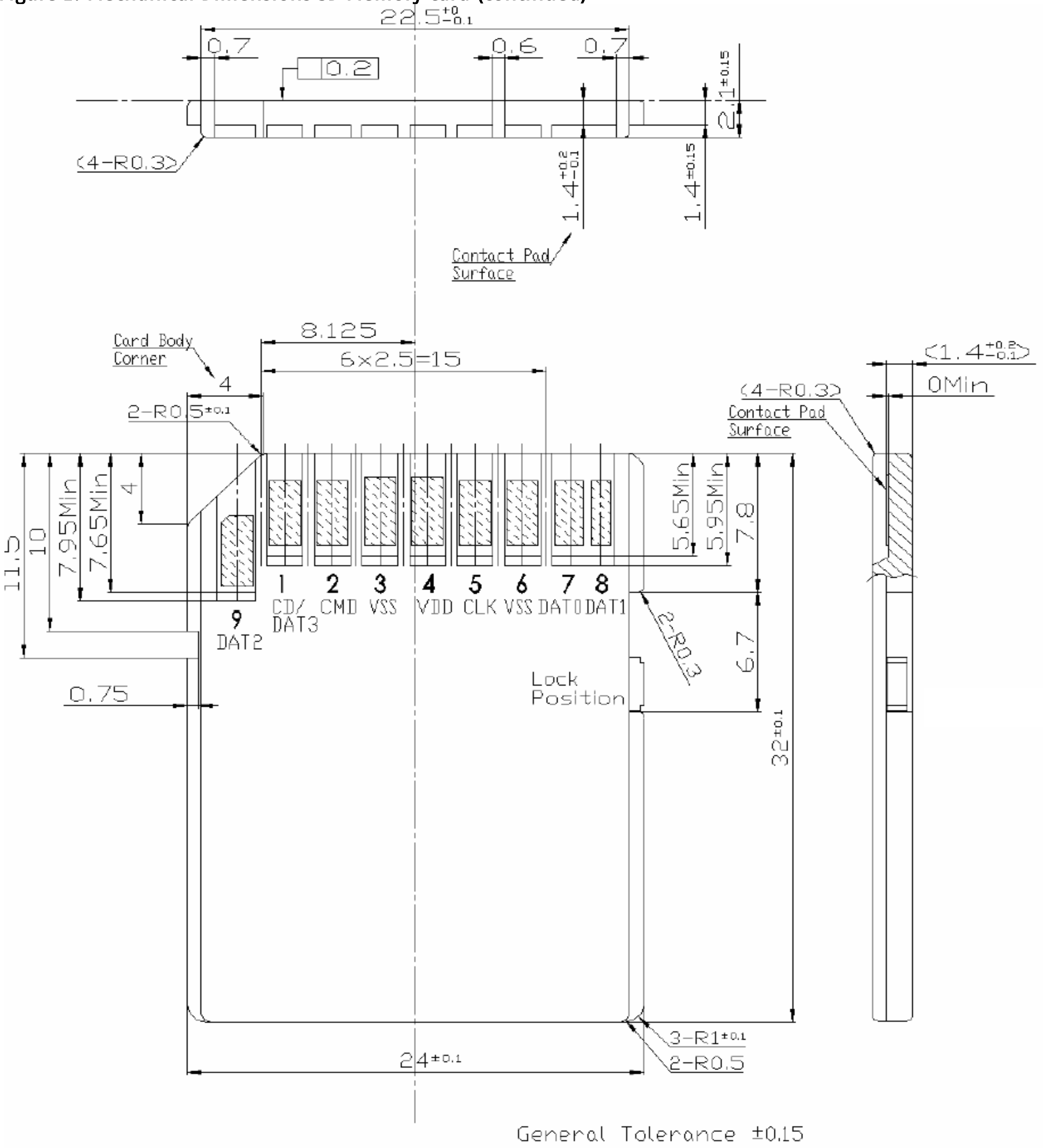


Figure 2: Mechanical Dimensions SD Memory Card (continued)



5 Electrical interface

5.1 Electrical description

Figure 3: SD Memory Card Block Diagram

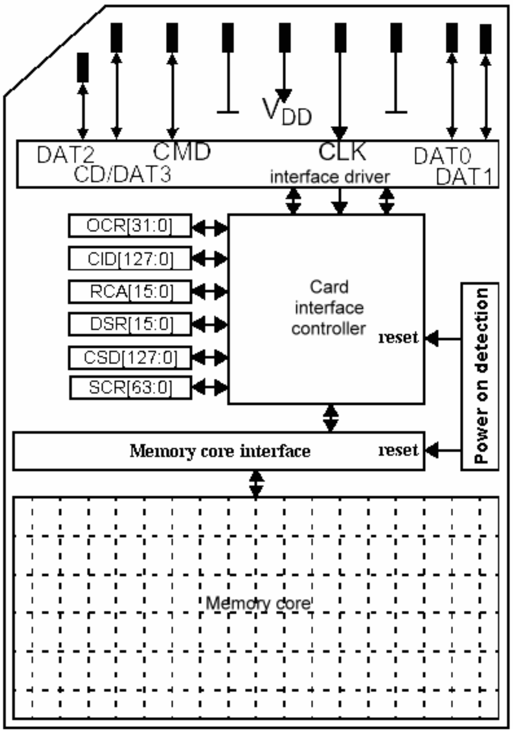


Figure 4: SD Memory Card Shape and Interface (Bottom View)

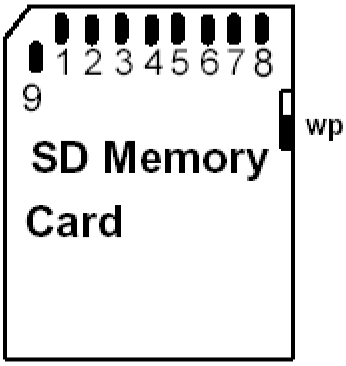


Table 11: SD Memory Card Pad Assignment

Pin #	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type[1]	Description
1	CD/DAT3[2]	I/O/PP[3]	Card Detect/ Data Line [Bit 3]	CS	I[3]	Chip Select (neg true)
2	CMD	PP	Command/Response	DI	I	Data In
3	VSS1	S	Supply voltage ground	VSS	S	Supply voltage ground
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS2	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1[4]	I/O/PP	Data Line [Bit 1]	RSV		
9	DAT2[5]	I/O/PP	Data Line [Bit 2]	RSV		

Notes:

1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;
2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
3) At power up this line has a 50kOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command
4) DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).
5) DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).

5.2 Power up / Power down beaviour and reset

5.2.1 Power up

When the voltage is ramped up the controller is ready (internal reset pin released) if the voltage reaches 1.65V. The host can start with communication 1ms after 2.7V is reached according the SDA soecification. That should perform 74 clock cycles and start with the sequence CMD0, CMD8, ACMD41 until card is ready as described in the SD specification 3.01.

5.2.2 Power down

When the power falls below 2.6V the controller stopps the communication to the flash, but enables the flash to finish a started flash program operation (if voltage drop is not fast).

After next initialization the controller checks the last written data for consistency and refreshs the data. Either the new or the old data (if the write operation could not be finished) are available.

5.2.3 Power drop

If the voltage drops below 2.6V and rises again, the card performes a reset. The card must be initialized like after a power on.

5.2.4 Operation below minimum voltage

If the card initialization is perfomed below the specified voltage of 2.7V, the card may be detected as 1MB card with no usefull data. In this case the host should power off and on the card and start initialization above 2.7V.

5.3 DC characteristics

Measurements are at Recommended Operating Conditions unless otherwise specified.

Table 12: DC Characteristics

Symbol	Parameter	min	typ	max	unit	notes
V_{OH}	Output HIGH Voltage	$0.75*V_{DD}$			V	V_{OH}=-2mA
V_{OL}	Output LOW Voltage			$0.125*V_{DD}$	V	V_{OL}=2mA
V_{IH}	Input HIGH Voltage	$0.625*V_{DD}$		VDD+0.3	V	
V_{IL}	Input LOW Voltage	-0.3		$0.25*V_{DD}$	V	
I_{DD}	Operating Current Read		40	60	mA	@ 25°C
	Operating Current Write		60	80	mA	@ 25°C
	Background read and refresh [1]		70	95	mA	@ 25°C
	Pre-initialization Standby Current		4800	8000	µA	@ 25°C
	Post-initialization Standby Current [2]		1100	3000	µA	@ 25°C
			5000	8000	µA	@ 85°C
I_{LI}	Input Leakage Current [3]	-10		10	µA	without pull up R
I_{LO}	Output Leakage Current [3]	-10		10	µA	

Notes:

1) The card performs auto data read of the whole card to check for ECC errors and performs data refresh. Typical this operation starts 5-10 minutes after power on or if some large multiple bit errors were detected
2) Before auto read the idle current is larger than the typical idle current after auto read
3) Before initialization DAT1 and DAT2 have a pull-up resistor with a leakage current of 60µA

Figure 5: Bus Signal levels

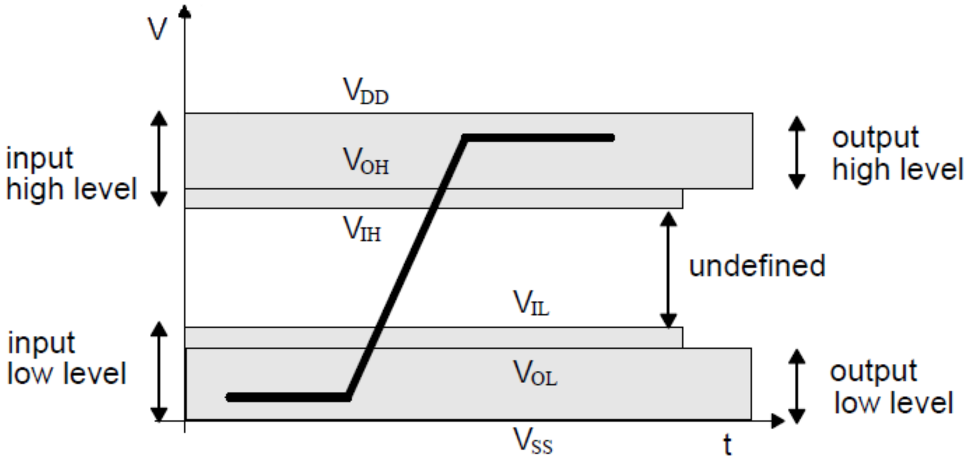


Table 13: SD Memory Card Recommended Operating Conditions

Symbol	Parameter		min	typ	max	unit
V_{DD}	Supply Voltage	Normal Operating Status	2.7	3.3	3.6	V
-	Power Up Time (from 0V to VDD min)				250	ms

5.4 Signal Loading

The total capacitance C_L is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS}, and the capacitance C_{CARD} of the card connected to the line:

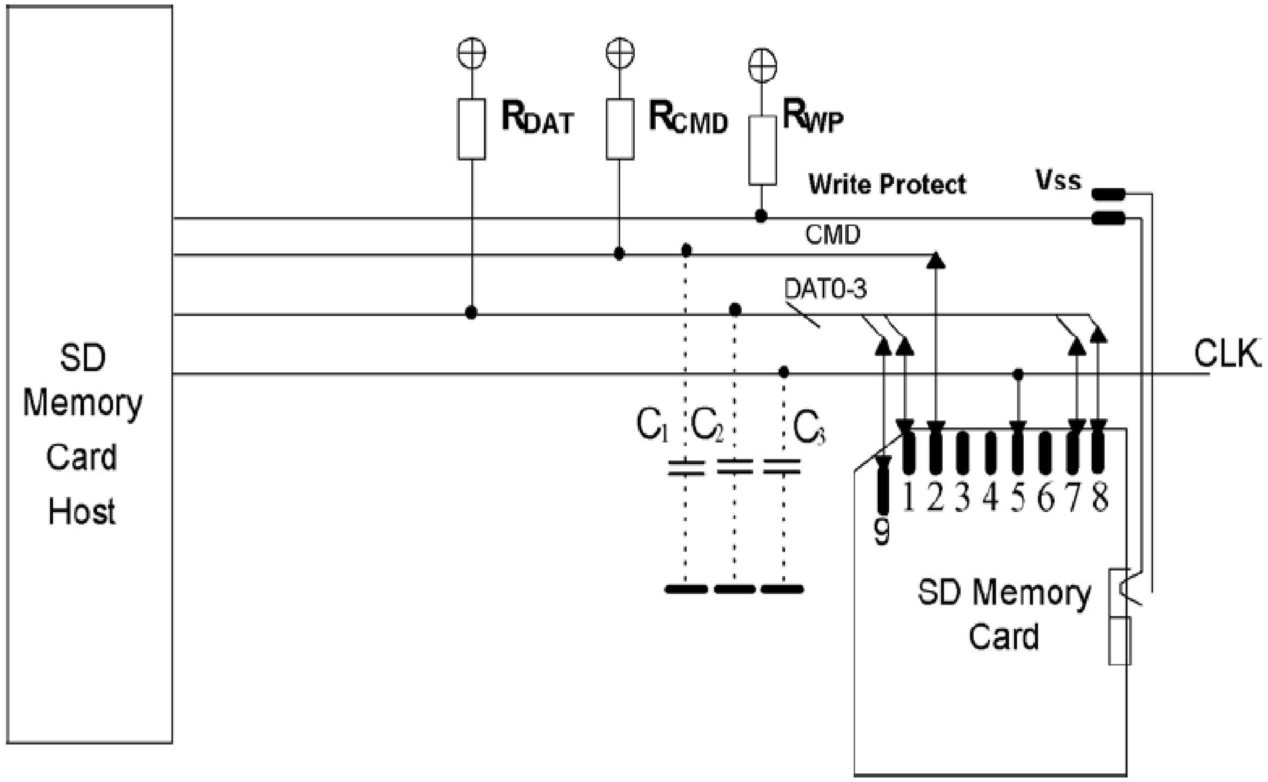
$C_L = C_{HOST} + C_{BUS} + C_{CARD}$

To allow the sum of the host and bus capacitances to be up to 20pF for the card, the following conditions in the table below are met by the card.

Table 14: Signal loading

Parameter	Symbol	Min	Max	Unit	Notes
Pull up resistance	R_{CMD}	10	100	kOhm	To prevent bus floating
Pull up resistance	R_{DAT}	10	100	kOhm	To prevent bus floating
Bus signal line capacitance	C_L		40	pF	Single card
Signal card capacitance	C_{CARD}		10	pF	Single card
Signal line inductance			16	nH	$f \leq 20MHz$

Figure 6: Signal Loading



5.5 AC characteristics

5.5.1 Default Speed mode (0 – 25MHz)

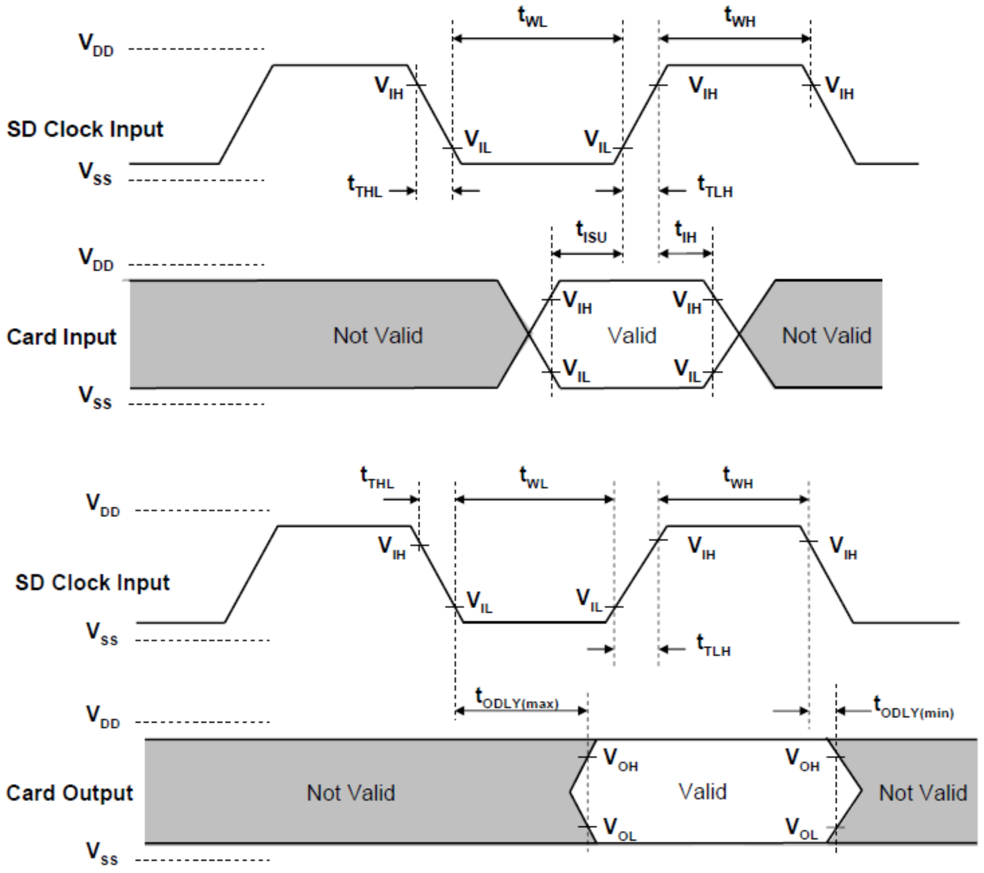
Table 15: AC Characteristics Default Speed Mode

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency in data transfer mode	fPP	0	25	MHz	CL≤100pF
Clock frequency in card id mode	fOD	0	400	KHz	CL≤100pF
Clock low time	tWL	10		ns	CL≤100pF
Clock high time	tWH	10		ns	
Clock rise time	tTLH		10	ns	
Clock fall time	tTHL		10	ns	
CMD, DAT input setup time	tISU	5		ns	CL≤25pF
CMD, DAT input hold time	tIH	5		ns	
CMD, DAT output delay time	tODLY	0	14	ns	CL≤40pF, data transfer
CMD, DAT output delay time	tODLY	0	50	ns	CL≤40pF, identification

Notes

1. Rise and fall times are measured from 10% to 90% of voltage level.
2. CLK referenced to VIH min and VIL max.
3. CMD and DAT inputs and outputs referenced to CLK.

Figure 7: AC Characteristics Default Speed Mode



High Speed mode (0 – 50MHz)

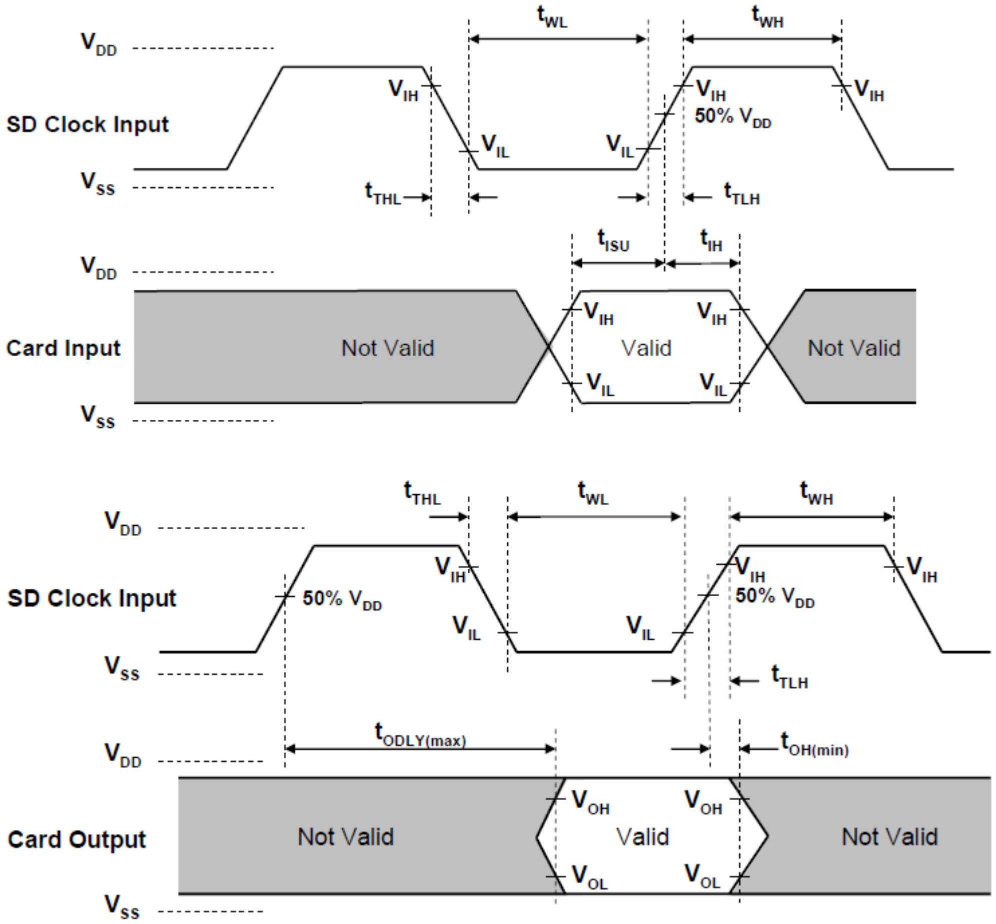
Table 16: AC Characteristics High Speed Mode

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency in data transfer mode	fPP	0	50	MHz	CL≤10pF
Clock low time	tWL	7.0		ns	
Clock high time	tWH	7.0		ns	
Clock rise time	tTLH		3	ns	
Clock fall time	tTHL		3	ns	
CMD, DAT input setup time	tISU	6		ns	
CMD, DAT input hold time	tIH	2		ns	
CMD, DAT output delay time during data transfer mode	tODLY		14	ns	
CMD, DAT output hold time	tOH	2.5		ns	

Notes

1. Rise and fall times are measured from 10% to 90% of voltage level.
2. CLK referenced to VIH min and VIL max.
3. CMD and DAT inputs and outputs referenced to CLK.
4. In order to satisfy severe timing, the host shall drive only one card with max 40pF total at each line.

Figure 8: AC Characteristics High Speed Mode



6 Host access Specification

The following chapters summarize how the host accesses the card:

- Chapter 6.1 summarizes the SD and SPI buses.
- Chapter 6.2 summarizes the registers.

6.1 SD and SPI Bus Modes

The card supports SD and the SPI Bus modes. Application can chose either one of the modes. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. The SD mode uses a 4-bit high performance data transfer, and the SPI mode provides compatible interface to MMC host systems with little redesign, but with a lower performance.

6.1.1 SD Bus Mode Protocol

The SD Bus mode has a single master (host) and multiple slaves (cards) synchronous topology. Clock, power, and ground signals are common to all cards. After power up, the SD Bus mode uses DAT0 only; after initialization, the host can change the cards' bus width from 1 bit (DAT0) to 4 bits (DAT0-DAT3). In high speed mode, only one card can be connected to the bus.
Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

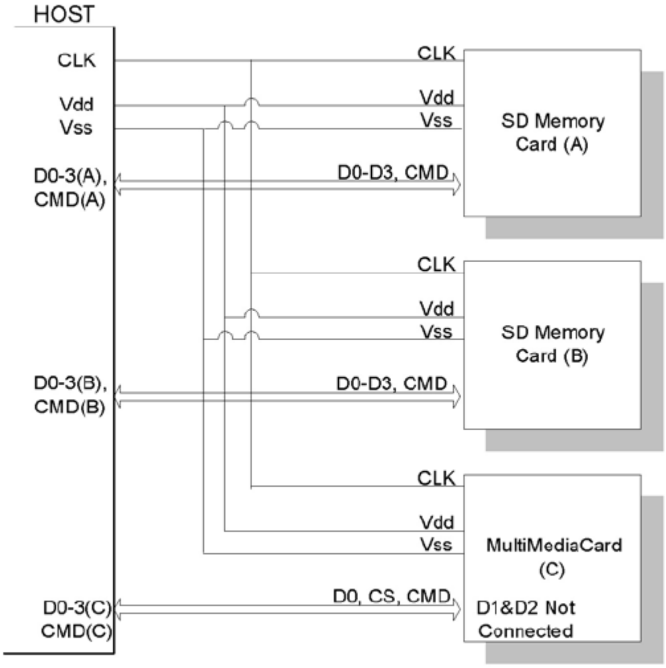
- Command: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- Response: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

The SD bus signals are listed in Table 17, and the SD bus topology is illustrated in Figure 9: SD Bus Topology.

Table 17: SD Bus Signals

Signal	Description
CLK	Host to card clock signal
CMD	Bidirectional Command/Response signal
DAT0-DAT3	4 Bidirectional data signals
Vdd, Vss	Power and Ground

Figure 9: SD Bus Topology



6.1.2 SPI Bus Mode Protocol

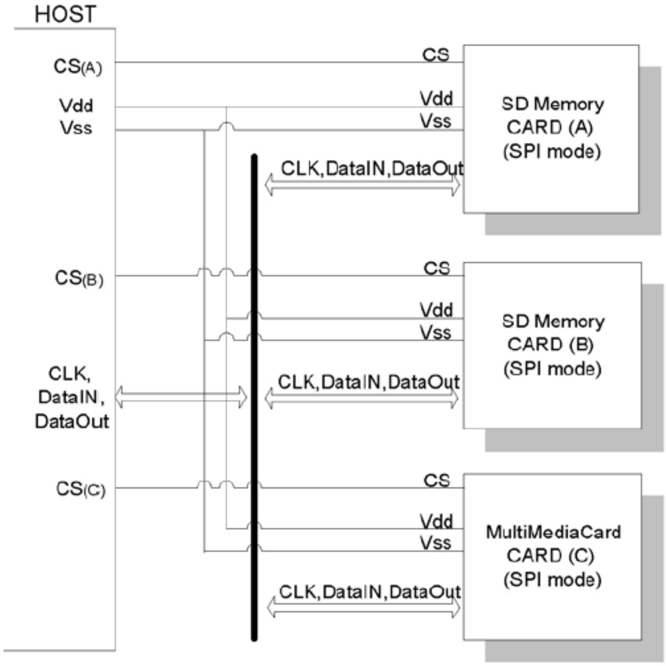
The Serial Parallel Interface (SPI) Bus is a general purpose synchronous serial interface. The SPI mode consists of a secondary communication protocol. The interface is selected during the first reset command after power up (CMD0) and it cannot be changed once the card is powered on.
While the SD channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal.
The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal.
The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.
The bidirectional CMD and DAT lines are replaced by unidirectional *dataIn* and *dataOut* signals.

The SPI bus signals are listed Table 18 and the SPI bus topology is illustrated in Figure 10.

Table 18: SPI Bus Signals

Signal	Description
/CS	Host to card chip select
CLK	Host to card clock signal
Data In	Host to card data signal
Data Out	Card to host data signal
Vdd, Vss	Power and ground

Figure 10: SPI bus topology



6.1.3 Mode Selection

The SD Memory Card wakes up in the SD mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0) and the card is in *idle_state*. If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode.
If SPI mode is required the card will switch to SPI and respond with the SPI mode R1 response.
The only way to return to the SD mode is by entering the power cycle. In SPI mode the SD Memory Card protocol state machine is not observed. All the SD Memory Card commands supported in SPI mode are always available.
During the initialization sequence, if the host gets Illegal Command indication for ACMD41 sent to the card, it may assume that the card is Multimedia Card. In that case it should re-start the card as Multimedia Card using CMD0 and CMD1.

6.2 Card Registers

The SD Memory Card has registers. Refer to Table 19 to Table 25 for detail.

Table 19: SD Memory Card registers

Register Name	Bit Width	Description	Function
CID	128	Card Identification information	This register contains the card identification information used during the Card Identification phase.
OCR	32	Operation Conditions Registers	This register describes the operating voltage range and contains the status bit in the power supply.
CSD	128	Card specific information	This register provides information on how to access the card content. Some fields of this register are writeable by PROGRAM_CSD (CMD27).
SCR	64	SD Memory Card's Special features	This register provides information on special features.
RCA	16	Relative Card Address	This register carries the card address is SD Card mode.
SSR	512	SD Status	information about the card proprietary features and vendor specific life time information

Table 20: CID register

Register Name	Bit Width	Description	typ. value
MID	8	Manufacture ID	0x5d
OID	16	OEM/Application ID	0x5342
PNM	40	Product Name	("LgBM1") g=generation
PRV	8	Product Revision	0xgg
PSN	32	Product Serial Number	xxxxxxxx
–	4	Reserved	0x0
MDT	12	Manufacture Date	0xyym
CRC	7	Check sum of CID contents	chksum
–	1	Not used; always=1	1

Table 21: OCR register

OCR bit position	VDD voltage window	typ. value	OCR bit position	VDD voltage window	typ. value
0-3	Reserved	0	15	2.7-2.8	1
4	1.6-1.7	0	16	2.8-2.9	1
5	1.7-1.8	0	17	2.9-3.0	1
6	1.8-1.9	0	18	3.0-3.1	1
7	1.9-2.0	0	19	3.1-3.2	1
8	2.0-2.1	0	20	3.2-3.3	1
9	2.1-2.2	0	21	3.3-3.4	1
10	2.2-2.3	0	22	3.4-3.5	1
11	2.3-2.4	0	23	3.5-3.6	1
12	2.4-2.5	0	24	Switching to 1.8V accepted	0
13	2.5-2.6	0	25-30	Reserved	
14	2.6-2.7	0	30	Card Capacity Status (CCS)	*1)
			31	0=busy; 1=ready	*2)

Notes

1. This bit is valid only when the card power up status bit is set.
2. This bit is set to LOW if the card has not finished the power up routine.

Table 22: CSD register

Register Name	Bits	Bit Width	Description	typ. Value
CSD_STRUCTURE	127:126	2	CSD structure	01
–	125:120	6	Reserved	00000
TAAC	119:112	8	Data read access time 1	00001110
NSAC	111:104	8	Data read access time 2 (CLK cycle)	00000000
TRAN_SPEED	103:96	8	Data transfer rate	00110010
CCC	95:84	12	Card command classes	010110110101
READ_BL_LEN	83:80	4	Read data block length	1001
READ_BL_PARTIAL	79	1	Partial blocks for read allowed	0
WRITE_BLK_MISALIGN	78	1	Write block misalignment	0
READ_BLK_MISALIGN	77	1	Read block misalignment	0
DSR_IMP	76	1	DSR implemented	0
–	75:70	6	Reserved	000000
C_SIZE	69:48	22	Device size	xxx*)
–	47	1	Reserved	0
ERASE_BLK_EN	46	1	Erase single block enable	1
SECTOR_SIZE	45:39	7	Erase sector size	1111111
WP_GRP_SIZE	38:32	7	Write protect group size	0000000
WP_GRP_ENABLE	31	1	Write protect group enable	0
–	30:29	2	Reserved	00
R2W_FACTOR	28:26	3	Write speed factor	010
WRITE_BL_LEN	25:22	4	Write data block length	1001*)
WRITE_BL_PARTIAL	21	1	Partial blocks for write allowed	0
–	20:16	5	Reserved	00000
FILE_FORMAT_GRP	15	1	File format group	0 W(1)
COPY	14	1	Copy flag	0 W(1)
PERM_WRITE_PROTECT	13	1	Permanent write protection	0 W(1)
TMP_WRITE_PROTECT	12	1	Temporary write protection	0 W
FILE_FORMAT	11:10	2	File format	00 W(1)
–	9:8	2	Reserved	00 W
CRC	7:1	7	Checksum of CSD contents	xxxxxxx W
–	0	1	Always=1	1

***) Drive Size and block sizes vary with card capacity**
memory capacity = (C_SIZE+1) * 512kByte
W value can be changed with CMD27 (PROGRAM_CSD)
W(1) value can be changed ONCE with CMD27 (PROGRAM_CSD)

Table 23: SCR register

Field	Bits	Bit Width	typ Value	remark
SCR_STRUCTURE	63:60	4	0000	SCR 1.01...2.00
SD_SPEC	59:56	4	0010	SD 2.0 or 3.0
DATA_STAT_AFTER_ERASE	55	1	1	data are 0xFF after erase
SD_SECURITY	54:52	3	011	2.00 (SDHC)
SD_BUS_WIDTHS	51:48	4	0101	1 or 4 bit
SD_SPEC3	47	1	1	yes→ SD3.0
EX_SECURITY	46:43	4	0000	no extended security
Reserved	42:34	9	0	0
CMD_SUPPORT	33:32	2	11	CMD23 and CMD20 supported
Reserved	31:0	32	0	0

Table 24: RCA register

Field	Bit Width	typ Value
RCA	16	0x0000*)

*) After Initialization the card can change the RCA register.

Table 25: SSR register

Field	Bits	Bit Width	typ Value	remark
Data bus width	511:510	2	0x2*)	4 bit width
Secured mode	509:509	1	0x0	not secured
Reserved for security	508:502	7	0x00	-
Reserved	501:496	6	0x00	-
SD card type	495:480	16	0x0000	Regular SD
Size protected area	479:448	32	*0x03000000* *0x04000000*	*48MB* *64MB*
Speed class	447:440	8	0x03	Class 6
Move performance	439:432	8	0x05	5 MB/s
Allocation unit size	431:428	4	0x9	4 MiB
Reserved	427:424	4	0x0	
Erase unit size	423:408	16	*0x0001*	1 AU
Erase unit timeout	407:402	6	0x10	16 seconds
Erase unit offset	401:400	2	0x1	1 seconds
UHS mode Speed Grade	399:396	4	0x0	(no UHS)
Allocation unit size in UHS mode	395:392	4	*0x0*	no UHS
Reserved	391:312	80		
Data structure version identifier, currently 1	311:304	8	*0x01*	version 1
Number of manufacturer marked defect blocks	303:288	16	*0x0008*	8 initial BB
Number of initial spare blocks (worst chip)	287:272	16	*0x0074*	116 spare blocks
Number of initial spare blocks (sum over all chips)	271:256	16	*0x0074*	116 spare blocks
Percentage of remaining spare blocks (worst chip)	255:248	8	*0x64*)*	100%
Percentage of remaining spare blocks (all chips)	247:240	8	*0x64*)*	100%
Number of uncorrectable ECC errors (not including ECC errors during startup)	239:224	16	*0x0000*)*	0 uncorrectable errors
Number of correctable ECC errors (not including ECC errors during startup)	223:192	32	*0x0045074b*)*	4523851 correctable ECC errors
Lowest wear level class	191:176	16	*0x0000*)*	0
Highest wear level class	175:160	16	*0x0000*)*	0
Wear level threshold	159:144	16	*0x007f*	127 block erases per WL class
Total number of block erases	143:96	48	*0x00...1ff0*)*	8176 block erase commands
Number of flash blocks, in units of 256 blocks	95:80	16	*0x0008*	2048 flash blocks
Maximum flash block erase count target, in wear level class units	79:64	16	*0x00xx*	Flash endurance xx WL classes
Power on count	63:32	32	*0x00000003*)*	3x power on
Firmware version	31:0	32	*0xYYMMDDXX*	Firmware Version

Bit 311:0 are vendor specific, example values in the table *) value change in operation

6.3 Busy Times / Time Out

The host should tolerate this max. busy times.

Table 26: SD Busy times of the cards

Transfer	min	typ	max
single sector random write	1.4ms	380ms	1400ms possible
single sector sequential write	1.4ms	1.5ms	500ms possible
read access	<0.5ms	1.5ms	500ms possible

7 RoHS and WEEE update from Swissbit

Dear Valued Customer,

We at Swissbit place great value on the environment and thus pay close attention to the diverse aspects of manufacturing environmentally and health friendly products. The European Parliament and the Council of the European Union have published two Directives defining a European standard for environmental protection. This states that Products must comply with both Directives in order for them to be sold on the European market:

- RoHS – Restriction of Hazardous Substances
- WEEE – Waste Electrical and Electronic Equipment

Swissbit would like to take this opportunity to inform our customers about the measures we have implemented to adapt all our products to the European norms.

What is the WEEE Directive (2012/19/EU)?

The Directive covers the following points:

- Prevention of WEEE
- Recovery, recycling and other measures leading to a minimization of wastage of electronic and electrical equipment
- Improvement in the quality of environmental performance of all operators involved in the EEE life cycle, as well as measures to incorporate those involved at the EEE waste disposal points

What are the key elements?

The WEEE Directive covers the following responsibilities on the part of producers:

Producers must draft a disposal or recovery scheme to dispose of EEE correctly.
Producers must be registered as producers in the country in which they distribute the goods.
They must also supply and publish information about the EEE categories.
Producers are obliged to finance the collection, treatment and disposal of WEEE.

Inclusion of WEEE logos on devices

In reference to the Directive, the WEEE logo must be printed directly on all devices that have sufficient space. «In exceptional cases where this is necessary because of the size of the product, the symbol of the WEEE Directive shall be printed on the packaging, on the instructions of use and on the warranty» (WEEE Directive 2012/19/EU)

When does the WEEE Directive take effect?

The Directive came into effect internationally on July 04, 2012.

What is RoHS (2011/65/EU)?

The goals of the Directive are to:

- Place less of a burden on human health and to protect the environment by restricting the use of hazardous substances in new electrical and electronic devices
- To support the WEEE Directive (see above)

RoHS enforces the restriction of the following 6 hazardous substances in electronic and electrical devices:

- Lead (Pb) – no more than 0.1% by weight in homogeneous materials
- Mercury (Hg) – no more than 0.1% by weight in homogeneous materials
- Cadmium (Cd) – no more than 0.01% by weight in homogeneous materials
- Chromium (Cr6+) – no more than 0.1% by weight in homogeneous materials
- PBB, PBDE – no more than 0.1% by weight in homogeneous materials

Swissbit is obliged to minimize the hazardous substances in the products.

According to part of the Directive, manufacturers are obliged to make a self-declaration for all devices with RoHS. Swissbit carried out intensive tests to comply with the self-declaration. We have also already taken steps to have the analyses of the individual components guaranteed by third-party companies.

Swissbit carried out the following steps during the year with the goal of offering our customers products that are fully compliant with the RoHS Directive.

- **Preparing all far-reaching directives, logistical enhancements and alternatives regarding the full understanding and introduction of the RoHS Directive's standards**
- **Checking the components and raw materials:**
  - Replacing non-RoHS-compliant components and raw materials in the supply chain
  - Cooperating closely with suppliers regarding the certification of all components and raw materials used by Swissbit
- **Modifying the manufacturing processes and procedures**
  - Successfully adapting and optimizing the new management-free integration process in the supply chain
  - Updating existing production procedures and introducing the new procedures to support the integration process and the sorting of materials
- **Carrying out the quality process**
  - Performing detailed function and safety tests to ensure the continuous high quality of the Swissbit product line

When does the RoHS Directive take effect?

As of June 08, 2011 only new electrical and electronic devices with approved quantities of RoHS will be put on the market.

When will Swissbit be offering RoHS-approved products?

Swissbit's RoHS-approved products are available now. Please contact your Swissbit contact person to find out more about exchanging your existing products for RoHS-compliant devices.

For your attention

We understand that packaging and accessories are not EEE material and are therefore not subject to the WEEE or RoHS Directives.

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8 Part Number Decoder

S	F	SD	016G	L	2	B	M	1	TO	-	I	-	L	F	-	121	-	STD
1	2	3	4	5	6	7	8	9	10		11		12	13		14		15

Manuf.
Memory Type.
Product Type
Capacity
Platform
Generation
Memory Organization
Technology
Number of flash chips/channels
Flash vendor Code
Temp. Option
Manuf. Code: Flash Package
Manuf. Code: Flash Mode
Configuration
Option

1. **Manufacturer**

Swissbit code	S

2. **Memory Type**

Flash	F

3. **Product Type**

SD Memory Card	SD

4. **Capacity**

4 GByte	4096
8 GByte	8192
16 GByte	016G
32 GByte	032G
64 Gbyte	064G

5. **Platform**

SD Memory Card	L

6. **Generation**

Generation	1
	2

7. **Memory Organization**

x8	B

8. **Technology**

SD Memory Card controller	S-4xx Platform	M

9. **Channels**

1 Flash Channel	1

10. **Flash Code**

Toshiba	TO

11. Temp. Option

Extended Temp. Range -25°C to 85°C	E
Industrial Temp. Range -40°C to 85°C	I

12. DIE Classification

	S-40 MLC
MONO (single die package)	G
DDP (dual die package)	L
QDP (dual die package)	H

13. PIN Mode

Single nCE & R/nB	E
Dual nCE & Dual R/nB	F
Quad nCE & Quad R/nB	G

14. Configuration XYZ

X→ Configuration

Configuration	X
default	1

Y → FW Revision

FW Revision	Y
Version 1	1
Version 2	2

Z → optional

Optional	Z
optional	1

15. Option

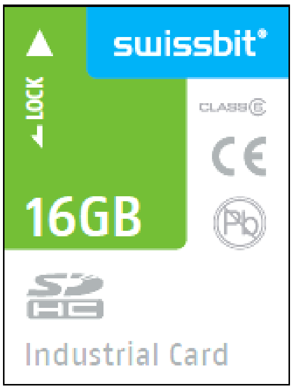
Swissbit / Standard	STD

9 Swissbit Label specification

9.1 Front side label

4GB SDHC Memory Card

8GB SDHC Memory Card



16GB SDHC Memory Card

32GB SDHC Memory Card

9.2 Back side marking

SWISSBIT
SFSD8192L2BM1 Part-
TO-E-GE-121-STD number
5013-6131210X Date-Lot/Serial
Made in Germany
CE WEEE

Example of the back side laser marking

10 Revision History

Table 27: Document Revision History

Date	Revision	Description	Revision details
October 10, 2013	0.80	Initial preliminary release	
December 16, 2013	0.90	updated card LBA values	
December 20, 2013	0.95	Add SD 3.0 compliant, SCR register	
March 05, 2014	0.96	Standby currents corrected DC and AC characteristics updated to SDA 3.0 specification SSR-Register erase count target, CE Declaration removed (extra document)	
October 31, 2014	1.00	Detailed power on/off behaviour description, add busy times values Second generation part number, changed performance values and back side picture	Change req. no. 0226
May 07, 2015	1.01	Added new preferred parts	Doc. req. no. 0510

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

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Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

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С нами вы становитесь еще успешнее!

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