

Vishay Siliconix

Low-Voltage Dual SPST Analog Switch

DESCRIPTION

The DG9232, 9233 is a single-pole/single-throw monolithic CMOS analog device designed for high performance switching of analog signals. Combining low power, high speed (t_{ON}: 35 ns, t_{OFF}: 20 ns), low on-resistance (R_{DS(on}): 20 Ω) and small physical size, the DG9232, 9233 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG9232, 9233 is built on Vishay Siliconix's low voltage BCD-15 process. Minimum ESD protection, per method 3015.7 is 2000 V. An epitaxial layer prevents latchup. Break-before -make is guaranteed for DG9232. 9233.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

BENEFITS

- Reduced power consumption
- Simple logic interface
- High accuracy
- Reduce board space

FEATURES

- Low voltage operation (+2.7 V to + 5 V)
- Low on-resistance $R_{DS}(on)$: 20 Ω
- Fast switching t_{ON}: 35 ns, t_{OFF}: 20 ns
- Low leakage I_{COM(on)}: 200 pA max.
- Low charge injection QINJ: 1 pC
- Low power consumption
- TTL/CMOS compatible
- ESD protection > 2000 V (method 3015.7)
- Available in MSOP-8 and SOIC-8
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Battery operated systems
- Portable test equipment
- Sample and hold circuits
- Cellular phones
- Communication systems
- Military radio
- PBX, PABX guidance and control systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View

TRUTH TABLE - DG9232				
Logic	Switch			
0	On			
1	Off			
Logic "0" ≤ 0.8 V				

Logic "1" ≥ 2.4 V

TRUTH TABLE - DG9233				
Logic	Switch			
0	Off			
1	On			
Logic "0" ≤ 0.8 V				

Logic "1" ≥ 2.4 V

ORDERING INFORMATION Temp Range Part Number Package DG9232DY DG9232DY-E3 DG9232DY-T1 DG9232DY-T1-E3 SOIC-8 DG9233DY - 40 °C to 85 °C DG9233DY-E3 DG9233DY-T1 DG9233DY-T1-E3 DG9232DQ-T1-E3 MSOP-8 DG9233DQ-T1-E3

* Pb containing terminations are not RoHS compliant, exemptions may apply

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COMPLIANT

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ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit		
Reference V+ to GND	- 0.3 to + 13	Ň			
IN, COM, NC, NO ^a	- 0.3 to (V+ + 0.3)	v			
Continuous Current (Any terminal)	± 20	mA			
Peak Current (Pulsed at 1 ms, 10 % duty cycle)				± 40	
ESD (Method 3015.7)		> 2000	V		
Storage Temperature	D suffix	- 65 to 125	°C		
Power Dissipation (Packages) ^b	8-pin narrow body SOIC ^c	400	mW		

Notes:

a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings. b. All leads welded or soldered to PC board.

c. Derate 6.5 mW/°C above 70 °C.

SPECIFICATIONS $(V + = 3 V)$							
		Test Conditions		D Suffix			
		Otherwise Unless Specified	- 40 °C to 85 °C		5 °C		
Parameter	Symbol	V+ = 3 V, \pm 10 %, V $_{\rm IN}$ = 0.8 V or 2.4 V $^{\rm e}$	Temp. ^a	Min. ^c	Typ. ^b	Max. ^c	Unit
Analog Switch							
Analog Signal Range ^d	V _{ANALOG}		Full	0		3	V
Drain-Source On-Resistance	R _{DS(on)}	$V_{NO} \text{ or } V_{NC} = 1.5 \text{ V}, \text{ V} + = 2.7 \text{ V}$ $I_{COM} = 5 \text{ mA}$	Room Full		30	50 80	
R _{DS(on)} Match ^d	$\Delta R_{DS(on)}$	$V_{\rm NO}$ or $V_{\rm NC}$ = 1.5 V	Room		0.4	2	Ω
R _{DS(on)} Flatness ^d	R _{DS(on)} Flatness	V_{NO} or V_{NC} = 1 and 2 V	Room		4	8	
NO or NC Off Leakage Current ^g	I _{NO/NC(off)}	$V_{\rm NO}$ or $V_{\rm NC}$ = 1 V/2 V, $V_{\rm COM}$ = 2 V/1 V	Room Full	- 100 - 5000	5	100 5000	
COM Off Leakage Current ^g	I _{COM(off)}	V_{COM} = 1 V/2 V, V_{NO} or V_{NC} = 2 V/1 V	Room Full	- 100 - 5000	5	100 5000	pА
Channel-On Leakage Current ^g	I _{COM(on)}	$V_{COM} = V_{NO} \text{ or } V_{NC} = 1 \text{ V/2 V}$	Room Full	- 200 - 10000	10	200 10000	1
Digital Control							
Input Current	I _{INL} or I _{INH}		Full		1		μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	$V_{\rm res}$ or $V_{\rm res} = 1.5 V_{\rm res}$	Room Full		50	120 200	2
Turn-Off Time	t _{OFF}	$v_{\rm NO}$ or $v_{\rm NC} = 1.5$ v	Room Full		20	50 120	ns
Charge Injection ^d	Q _{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		1	5	рС
Off-Isolation	OIRR	$B_{1} = 50.0$ C ₂ = 5 pE f = 1 MHz	Room		- 74		AB
Crosstalk	X _{TALK}	112 - 30 sz, $02 - 3$ pr, $1 - 1$ withz	Room		- 90		uВ
NC and NO Capacitance	C _{S(off)}		Room		7		
Channel-On Capacitance	C _{COM(on)}	f = 1 MHz	Room		20		pF
COM-Off Capacitance	C _{COM(off)}	Roc			13		
Power Supply							
Positive Supply Range	V+			2.7		12	V
Power Supply Current	l+	V+ = 3.3 V, V _{IN} = 0 or 3.3 V				1	μA

Notes:

a. Room = 25 $^{\circ}$ C, Full = as determined by the operating suffix.

b. Typical values are for design aid only, not guaranteed nor subject to production testing.

c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.

d. Guarantee by design, nor subjected to production test.

e. V_{IN} = input voltage to perform proper function.

f. Difference of min and max values.

g. Guaranteed by 5 V leakage tests, not production tested.

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SPECIFICATIONS (V+ =	: 5 V)						
		Test Conditions			D Suffix		
		Otherwise Unless Specified		- 40	0 °C to 8	5°C	
Parameter	Symbol	V+ = 5 V, \pm 10 %, V _{IN} = 0.8 V or 2.4 V ^e	Temp. ^a	Min. ^c	Тур. ^ь	Max. ^c	Unit
Analog Switch							
Analog Signal Range ^d	V _{ANALOG}		Full	0		5	V
Drain-Source On-Resistance	R _{DS(on)}	$V_{\rm NO} \text{ or } V_{\rm NC} = 3.5 \text{ V}, \text{ V} + = 4.5 \text{ V}$	Room		20	30 50	
Bookers Match ^d	$\Delta R_{DS(op)}$	$V_{NO} \text{ or } V_{NC} = 3.5 \text{ V}$	Boom		0.4	2	Ω
R _{DS(on)} Flatness ^d	R _{DS(on)} Flatness	V_{NO} or V_{NC} = 1, 2 and 3 V	Room		2	6	
NO or NC Off Leakage Current ^g	I _{NO/NC(off)}	$V_{\rm NO}~{\rm or}~V_{\rm NC}$ = 1 V/4 V, $V_{\rm COM}$ = 4 V/1 V	Room Full	- 100 - 5000	10	100 5000	
COM Off Leakage Current	I _{COM(off)}	V_{COM} = 1 V/4 V, V_{NO} or V_{NC} = 4 V/1 V	Room Full	- 100 - 5000	10	100 5000	pА
Channel-On Leakage Current	I _{COM(on)}	$V_{COM} = V_{NO} \text{ or } V_{NC} = 1 \text{ V/4 V}$	Room Full	- 200 - 10000		200 10000	
Digital Control	• •		4				!
Input Current	$I_{\rm INL}$ or $I_{\rm INH}$		Full		1		μΑ
Dynamic Characteristics			•				
Turn-On Time	t _{ON}		Room Full		35	75 150	
Turn-Off Time	t _{OFF}	$v_{\rm NO}$ or $v_{\rm NC} = 3.0$ v	Room Full		20	50 100	ns
Charge Injection ^d	Q _{INJ}	${\sf C}_{\sf L}$ = 1 nF, ${\sf V}_{\sf GEN}$ = 0 V, ${\sf R}_{\sf GEN}$ = 0 Ω	Room		2	5	рС
Off-Isolation	OIRR	$P_{-}=50.0$ $C_{-}=5$ $p_{-}=1$ MHz	Room		- 74		dD
Crosstalk	X _{TALK}	$H_{L} = 50.52, G_{L} = 5.007, T = 1.0012$	Room		- 90		uв
NC and NO Capacitance	C _(off)		Room		7		
Channel-On Capacitance	C _{D(on)}	f = 1 MHz	Room		20		pF
COM-Off Capacitance	C _{D(off)}		Room		13		
Power Supply							
Positive Supply Range	V+			2.7		12	V
Power Supply Current	l+	V+ = 5.5 V, V _{IN} = 0 or 5.5 V				1	μA

Notes:

a. Room = 25 °C, Full = as determined by the operating suffix.

b. Typical values are for design aid only, not guaranteed nor subject to production testing.

c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.

d. Guarantee by design, nor subjected to production test.

e. V_{IN} = input voltage to perform proper function.

f. Difference of min and max values.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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TYPICAL CHARACTERISTICS $T_A = 25$ °C, unless otherwise noted



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TYPICAL CHARACTERISTICS $T_A = 25$ °C, unless otherwise noted



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TEST CIRCUITS



 $t_r < 5 \text{ ns}$

t_f < 5 ns

t_D



V+



$$V_{\text{OUT}} = V_{\text{COM}} \left(\frac{R_{\text{L}}}{R_{\text{L}} + R_{\text{ON}}} \right)$$



Logic "1" = Switch On Logic input waveforms inverted for switches that have the opposite logic sense.





CL (includes fixture and stray capacitance)

Figure 2. Break-Before-Make Interval

Figure 1. Switching Time

Logic

Input

 $V_{NC} = V_{NO}$

Switch

Output

3 V

0 V

Vo

0 V

90 %

 t_{D}





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DG9232, DG9233 Vishay Siliconix

TEST CIRCUITS



Figure 4. Off-Isolation



Figure 5. Channel Off/On Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?70837.



Package Information

Vishay Siliconix

SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





	MILLIMETERS		INC	HES	
DIM	Min	Мах	Min	Мах	
А	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
Е	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					



Package Information Vishay Siliconix

MSOP: 8-LEADS

JEDEC Part Number: MO-187, (Variation AA and BA)







NOTES:

<u>/4.</u> /5.

- 1. Die thickness allowable is 0.203 ± 0.0127 .
- 2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
- /3. Dimensions "D" and "E₁" do not include mold flash or protrusions, and are measured at Datum plane _-H- , mold flash or protrusions shall not exceed 0.15 mm per side.
 - Dimension is the length of terminal for soldering to a substrate.
 - Terminal positions are shown for reference only.
- 6 Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
- The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
- /8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
- 9. Controlling dimension: millimeters.
- 10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
- 11. Datums -A- and -B- to be determined Datum plane -H-.

12 Exposed pad area in bottom side is the same as teh leadframe pad size.





(See Note 8)





N = 8L

	МІ			
Dim	Min	Nom	Max	Note
Α	-	-	1.10	
A ₁	0.05	0.10	0.15	
A ₂	0.75	0.85	0.95	
b	0.25	-	0.38	8
b ₁	0.25	0.30	0.33	8
С	0.13	-	0.23	
с ₁	0.13	0.15	0.18	
D		3.00 BSC		3
E	4.90 BSC			
E ₁	2.90	3.00	3.10	3
е	0.65 BSC			
e ₁	1.95 BSC			
L	0.40	0.55	0.70	4
Ν	8			5
x	0°	4°	6°	
ECN: T-02080—Rev. C, 15-Jul-02 DWG: 5867				



TrenchFET[®] Power MOSFETs

Application Note 808

Mounting LITTLE FOOT[®], SO-8 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/ppg?72286), for the basis of the pad design for a LITTLE FOOT SO-8 power MOSFET. In converting this recommended minimum pad to the pad set for a power MOSFET, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

In the case of the SO-8 package, the thermal connections are very simple. Pins 5, 6, 7, and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In a dual package, pins 5 and 6 are one drain, and pins 7 and 8 are the other drain. For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.





Figure 2. Dual MOSFET SO-8 Pad Pattern With Copper Spreading

The minimum recommended pad patterns for the single-MOSFET SO-8 with copper spreading (Figure 1) and dual-MOSFET SO-8 with copper spreading (Figure 2) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. These patterns use all the available area underneath the body for this purpose.

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

Application Note 826

Vishay Siliconix



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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