3 W flyback IoT off-line isolated power supply reference board using 5th generation fixed frequency CoolSET™ (ICE5AR4770AG)

REF_5AR4770AG_3W1

About this document

Scope and purpose

This document is a reference design for a 3 W IoT off-line isolated power supply using the latest Infineon fifth-generation Fixed Frequency (FF) CoolSET™ ICE5AR4770AG. The power supply is designed with a universal input compatible with most geographic regions, and isolated output (+5 V/0.6 A).

Highlights of the 3 W IoT off-line isolated power supply:

- Very small form-factor design
- Simplified circuitry with good integration of power and protection features
- Auto-restart protection scheme to minimize interruption and enhance end-user experience

Intended audience

This document is intended for power supply design or application engineers, etc. who wish to design low-cost, highly reliable off-line Switched Mode Power Supply (SMPS) systems for:

- Applications related to the Internet of Things (IoT)
  1) Standby power supply
  2) Power supply for microcontrollers
  3) Power supply for standalone sensors operating on a wired/wireless interface bus
- USB-power supply embedded in a wall plug
- Intelligent wall plug switched by wireless (with relay)
- Metering applications
- General applications with small form factor in the power range 1 W to 3 W

Table of contents

Table of contents

1 System introduction

The Internet of Things (IoT) is connecting up ever smarter devices and machines. The fast-growing market around the IoT covers a wide range of applications. All of them have one thing in common, namely the ability to collect and exchange data with each other. The microcontrollers, sensors, actuators, etc. embedded in each of the devices stay connected to the network at all times. They are supplied by an efficient low-power and low-standby power supply, to which the Infineon fifth-generation FF CoolSET™ family of integrated off-line power supply ICs is ideally suited.

Figure 1 IoT applications

Table 1 lists the system requirements for the IoT, and the corresponding Infineon solution is shown in the right-hand column.

Table 1 System requirements and Infineon solutions

	System requirement for IoT	Infineon solution – ICE5AR4770AG
1	High efficiency under light-load conditions to meet ENERGY STAR requirements	New FF control and Active Burst Mode (ABM)
2	Simplified circuitry with good integration of power and protection features	Embedded 700 V MOSFET and controller in DSO-12 package
3	Robust system and protection features	Input Over Voltage Protection (OVP) and brown-in features
4	Auto-restart protection scheme to minimize interruption and enhance end-user experience	All protections are in auto-restart

1.1 High efficiency under light-load conditions to meet ENERGY STAR requirements

During typical IoT operation, the power requirement fluctuates according to various use cases. Therefore, the efficiency should be optimized across the load range. It is crucial that the IoT power supply operates as efficiently as possible, because it will be in this particular state for most of the period. Under light-load conditions, losses incurred with the power switch are usually dominated by the switching operation. The choice of switching scheme and frequency play a crucial role in ensuring high conversion efficiency.

In this reference design, ICE5AR4770AG was primarily chosen due to its frequency-reduction switching scheme. Compared with a traditional FF flyback, the CoolSET™ reduces its switching frequency from medium to light load, thereby minimizing switching losses. Therefore, an efficiency of more than 76 percent is achievable under 25 percent loading conditions.

1.2 Simplified circuitry with good integration of power and protection features

To relieve the designer of the complexity of PCB layout and circuit design, the CoolSET™ is a highly integrated device with both a controller and HV MOSFET integrated into a single, space-saving DSO-12 package. These certainly help the designer to reduce component count as well as simplifying PCB layout for ease of manufacturing and cost.

1.3 Robust system and protection features

Comprehensive protection features are integrated into the FF CoolSET™ ICE5AR4770AG, such as input line OVP, V_{CC} OV, V_{CC} Under Voltage (UV), over-load/open-loop, over-temperature and Current Sense (CS) short-to-GND. It also has limited charging current for V_{CC} short-to-GND and brown-in protection by utilizing $R_{Brown\text{-}in}$ (R16D in Figure 3).

1.4 Auto-restart protection scheme to minimize interruption and enhance end-user experience

For an IoT power supply, it would be annoying for both the end user and the manufacturer if the system were to halt and latch after protection. To minimize interruption, the CoolSET™ implements auto-restart mode for all abnormal protections.

2 Reference design board

This document provides complete design details including specifications, schematics, Bill of Materials (BOM), PCB layout, transformer design and construction information. This information includes performance results pertaining to line/load regulation, efficiency, transient load, thermal conditions, conducted EMI scans, etc.

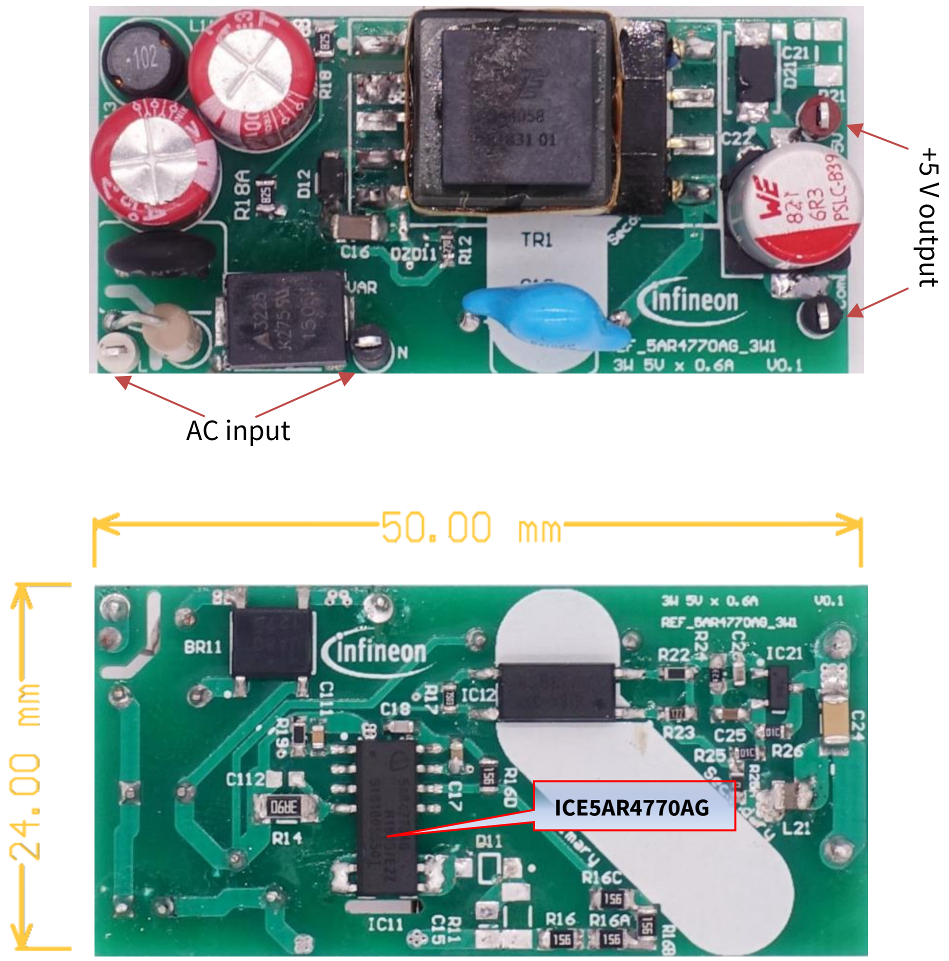


Figure 2 **REF_5AR4770AG_3W1**

3 Power supply specifications

The table below represents the minimum acceptance performance of the design. Actual performance is listed in the measurements section.

Table 2 Specifications of REF_5AR4770AG_3W1

Description	Symbol	Min.	Typ.	Max.	Units	Comments
Input						
Voltage	V_{IN}	85	–	264	V AC	Two wires (no P.E.)
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load input power	P_{stby_NL}	–	–	35	mW	230 V AC
Output						
Output voltage	V_{OUT}	–	5	–	V	±3%
Output current	I_{OUT}	0.03	0.3	0.6	A	
Output voltage ripple	V_{RIPPLE}	–	–	250	mV	20 MHz BW
Max. power output	P_{OUT_Max}	–	–	3	W	
Efficiency						
Max. load	η	–	80	–	%	115 V AC/230 V AC
Average efficiency at 25%, 50%, 75% and 100% of P_{OUT_Max}	η_{avg}	79	–	–	%	115 V AC/230 V AC
Environmental						
Conducted EMI			15		dB	Margin, CISPR 22 class B
ESD			±8		kV	EN 61000-4-2
Surge immunity						EN 61000-4-5
Differential Mode (DM)			±2		kV	See footnote 1 at 11.19
Common Mode (CM)			±4		kV	See footnote 1 at 11.19
Ambient temperature	T_{amb}	0	–	50	°C	Free conviction, sea level
Form factor		50 × 24 × 16			mm^3	L × W × H

4 Circuit diagram

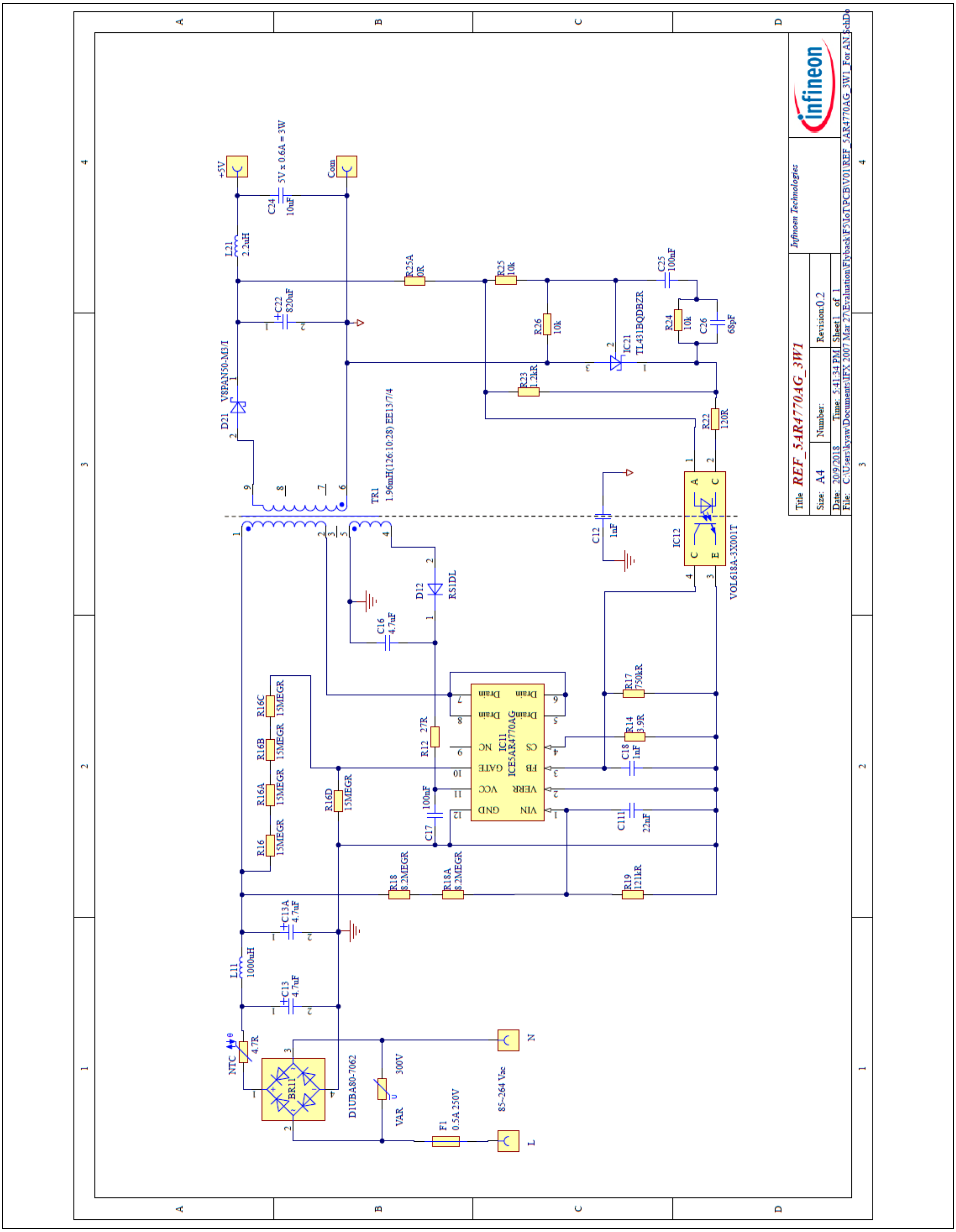


Figure 3 Schematic of REF_5AR4770AG_3W1

5 Circuit description

In this section, the design circuit for the SMPS unit will be briefly described by the different functional blocks. For details of the design procedure and component selection for the flyback circuitry please refer to the IC design guide [2] and calculation tool [3].

5.1 EMI filtering and line rectification

The input of the power supply unit is taken from the AC power grid, which is in the range of 85 V AC ~ 264 V AC. The fuse F1 is directly connected to the input line to protect the system in case of excess current entering the system circuit due to any fault. Following is the varistor VAR, which is connected across the input to absorb excessive energy during line surge transient. The resistor NTC not only reduces the in-rush current during start-up, but it also helps reduce the voltage increase on the bulk capacitors C13 and C13A during line surge transients. The bridge rectifier BR11 rectifies the AC input into DC voltage, filtered by the bulk capacitors C13 and C13A. Inductor L11 and capacitors C13 and C13A form a π filter to attenuate EMI noise.

5.2 Flyback converter power stage

The flyback converter power stage consists of C13A, transformer TR1, a primary HV MOSFET (integrated into ICE5AR4770AG), secondary rectification diodes D21, and secondary output capacitors and filtering C22, L21 and C24.

When the primary HV MOSFET turns on, some energy is stored in the transformer. When it turns off, the stored energy is released to the output capacitors and the output loading through the output diode D21.

The primary winding has two layers placed back to back for higher winding capacitance. This can reduce EMI by slowing the MOSFET switching. However, this can reduce efficiency. Winding capacitance can be tuned by adding a number of isolation tapes between the layers, depending on the EMI or efficiency need. If efficiency is a priority, interlacing primary and secondary winding is recommended, as it has lower leakage inductance. TR1 has single output windings, the V_{OUT} (5 V). The output rectification of V_{OUT} is provided by the diode D21 through filtering of C22, L21 and C24. All the secondary capacitors must be the low-ESR type, which can effectively reduce the switching ripple. Together with the Y-capacitor C12 across the primary and secondary side, the EMI noise can be further reduced to comply with CISPR 22 specifications.

5.3 Control of flyback converter through fifth-generation FF CoolSET™ ICE5AR4770AG

5.3.1 Integrated HV power MOSFET

The ICE5AR4770AG CoolSET™ is a 12-pin device in a DSO-12 package. It has been integrated with the new FF PWM controller and all necessary features and protections, and most importantly the 700 V power MOSFET, Infineon Superjunction (SJ) CoolMOS™. Hence the schematic is much simplified and the circuit design is made much easier.

5.3.2 Current Sensing (CS)

The ICE5AR4770AG is a current mode controller. The peak current is controlled cycle-by-cycle through the CS resistors R14 in the CS pin (pin 4) and so transformer saturation can be avoided and the system is more robust and reliable.

5.3.3 Feedback and compensation network

Resistor R25 is used to sense the V_{OUT} and feedback (FB) to the reference pin (pin 1) of error amplifier IC21 with reference to the voltage at resistor R26. A type 2 compensation network C25, C26 and R24 is connected between the output pin (pin 3) and the reference pin (pin 2) of the IC21 to stabilize the system. The IC21 further connects to pin 2 of the optocoupler, and IC12 with a series resistor R22 to convert the control signal to the primary side through the connection of pin 4 of the IC12 to the ICE5AR4770AG FB pin (pin 3) and complete the control loop. Both the optocoupler IC12 and the error amplifier IC21 are biased by V_{OUT}; IC12 is a direct connection while IC21 is through an R23 resistor.

The FB pin of ICE5AR4770AG is a multi-function pin which is used to select the entry burst power level (there are three levels available) through the resistor at the FB pin (R17) and also the burst-on/burst-off sense input during ABM.

5.4 Unique features of the fifth-generation FF CoolSET™ ICE5AR4770AG to support the requirements of IoT power supply

5.4.1 Fast self-start-up and sustaining of V_{CC}

The IC uses a cascode structure to fast-charge the V_{CC} capacitor. Pull-up resistors R16, R16A, R16B and R16C connected to the gate pin (pin 10) are used to initiate the start-up phase. At first, 0.2 mA is used to charge the V_{CC} capacitor from 0 V to 1.1 V. This is a protection which reduces the power dissipation of the IC during V_{CC} short-to-GND condition. Thereafter, a much higher charging current of 3.2 mA will charge the V_{CC} capacitor until the V_{CC_ON} is reached. Start-up time of less than 80 ms is achievable with a V_{CC} capacitor of 4.7 µF.

After start-up, the IC V_{CC} supply is sustained by the auxiliary winding of transformer TR1, which needs to support the V_{CC} to be above Under Voltage Lockout (UVLO) voltage (10 V typ.) through the rectifier circuit D12, R12 and C16.

5.4.2 CCM, DCM operation with frequency reduction

ICE5AR4770AG can be operated in either Discontinuous Conduction Mode (DCM) or Continuous Conduction Mode (CCM) with frequency-reduction features. This reference board is designed to operate in DCM. When the system is operating at maximum power, the controller will switch at the fixed frequency of 100 kHz. In order to achieve a better efficiency between light load and medium load, frequency reduction is implemented, and the reduction curve is shown in Figure 4. The V_{CS} is clamped by the current limitation threshold or by the PWM op-amp while the switching frequency is reduced. After the maximum frequency reduction, the minimum switching frequency is f_{OSC2_MIN} (43 kHz).

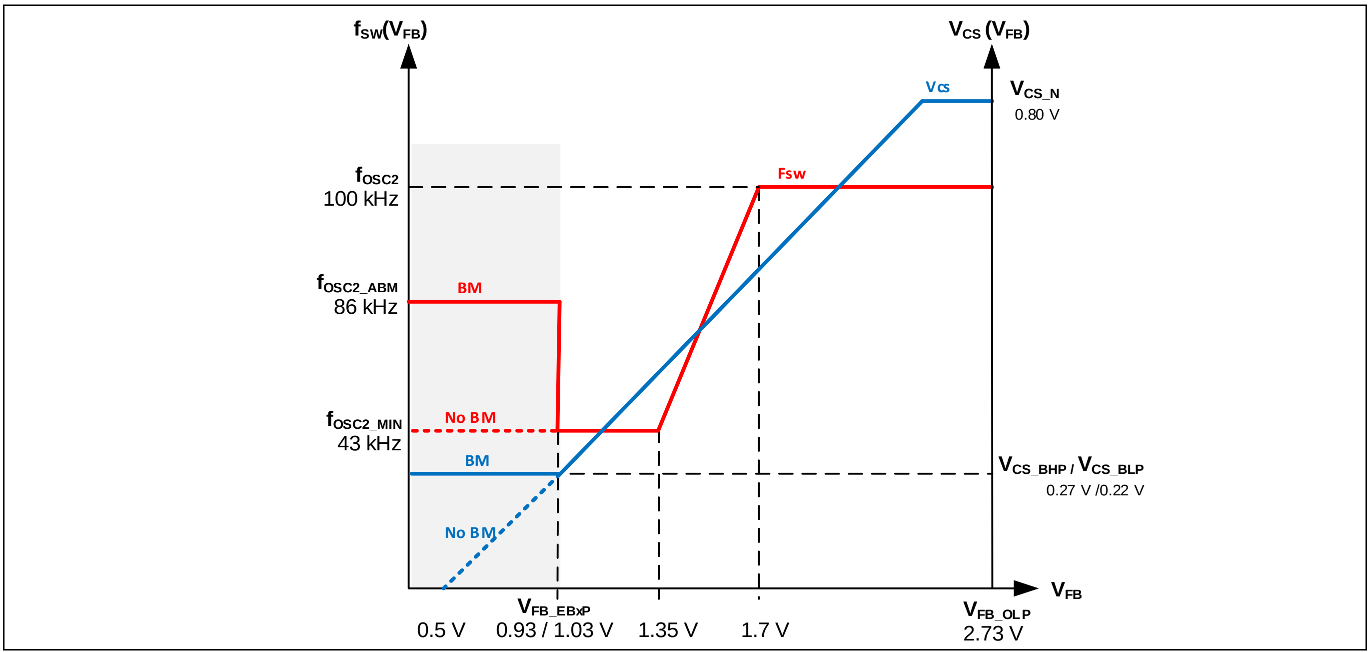


Figure 4 **Frequency-reduction curve**

5.4.3 Frequency jittering with modulated gate drive

The ICE5AR4770AG has a frequency jittering feature with modulated gate drive to reduce the EMI noise. The jitter frequency is internally set at 100 kHz (±4 kHz), and the jitter period is 4 ms.

5.4.4 System robustness and reliability through protection features

Protection is one of the major factors in determining whether the system is safe and robust – therefore sufficient protection is necessary. ICE5AR4770AG provides comprehensive protection to ensure the system is operating safely. This includes V_{IN} LOVP, brown-in, V_{CC} OV and UV, over-load, over-temperature (controller junction), CS short-to-GND and V_{CC} short-to-GND. When those faults are found, the system will enter protection mode. Once the fault is removed, the system resumes normal operation. A list of protections and failure conditions is shown in the table below.

Table 3 **Protection functions of ICE5AR4770AG**

Protection function	Failure condition	Protection mode
V_{CC} OV	V_{VCC} greater than 25.5 V	Odd-skip auto-restart
V_{CC} UV	V_{VCC} less than 10 V	Auto-restart
V_{IN} LOVP	V_{VIN} greater than 2.85 V	Non-switch auto-restart
Over-load	V_{FB} greater than 2.75 V and lasts for 54 ms	Odd-skip auto-restart
Over-temperature (junction temperature of controller chip only)	T_J greater than 140°C	Non-switch auto-restart
CS short-to-GND	V_{CS} less than 0.1 V, lasts for 0.4 µs and three consecutive pulses	Odd-skip auto-restart
V_{CC} short-to-GND (V_{VCC} = 0 V, start-up = 50 MΩ and V_{DRAIN} = 90 V)	V_{VCC} less than 1.1 V, $I_{VCC\_Charge1}$ ≈ -0.2 mA	Cannot start up
Brown-in	V_{GATE} less than 20 V	Cannot start up

5.5 Clamper circuit

A clamper RCD network normally added in parallel to the primary inductance of the transformer (pins 1 and 2 of TR1) is removed in this reference board to save on the BOM and increase efficiency. Without a clamper RCD, maximum drain voltage of the CoolMOS™ is still less, and 650 V in worst-case conditions, which gives a 7 percent margin from maximum drain-source breakdown voltage of 700 V.

5.6 PCB design tips

For a good PCB design layout, there are several points to note.

- The power loop needs to be as small as possible (see Figure 5). There are two power loops in the demo design; one from the primary side and one from the secondary side. For the primary side, it starts from the bulk capacitor (C13A) positive to the bulk capacitor negative. The power loop components include C13, the main primary transformer winding (pin 1 and pin 2 of TR1), the drain pin and the CS pin of the CoolSET™ IC11 and CS resistor. For the secondary side, the 5 V output starts from the secondary transformer windings (pin 9 of TR1), output diode D21 and output capacitors C22, L21 and C24.
- Star-ground concept should be used to avoid unexpected HF noise coupling affecting control. The ground of the small-signal components, e.g. C17, C18 and C111, and the emitter of the optocoupler (pin 3 of IC12) etc. should connect directly to the IC ground (pin 12 of IC11). Then it connects to the negative terminal of the C13A capacitor directly.

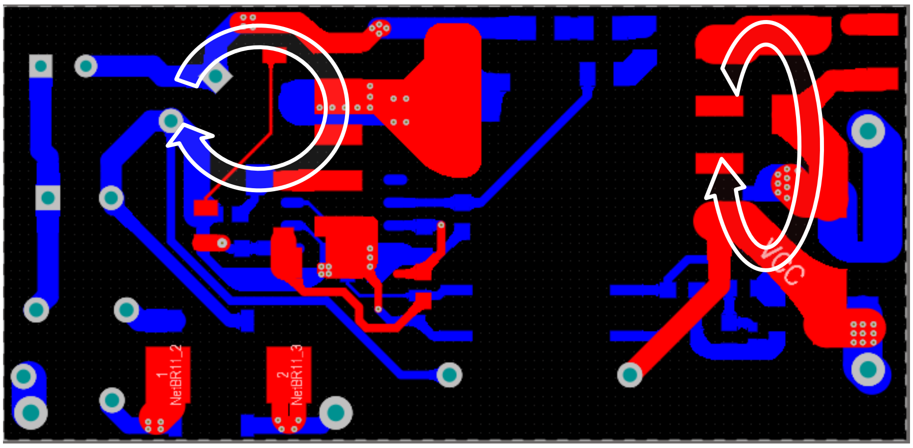


Figure 5 PCB layout tips

- Separating the HV components and LV components, e.g. V_{BUS} and CoolSET™ drain at the top part of the PCB (see Figure 5) and the other LV components at the lower part of the PCB, can reduce the spark-over chance of the high-energy surge during ESD or a lightning surge test.
- Pour the PCB copper on the drain pin of the CoolSET™ over as wide an area as possible to act as a heatsink.

5.7 EMI reduction tips

EMI compliance is always a challenge for the power supply designer. There are several critical points to consider in order to achieve satisfactory EMI performance:

- A proper transformer design can significantly reduce EMI. Low leakage inductance can incur a low switching spike and HF noise. Interlaced winding technique is the most common practice to reduce leakage inductance.[1] Winding shield, core shield and whole transformer shield are also some of the techniques that can be used to reduce EMI.

[1] Not implemented with this reference design.

- Input CMC and X-capacitor greatly reduces EMI but it is costly and impractical, especially for low-power applications.[1]
- Using a short power loop design in the PCB (as described in section 5.6) and terminating to the low-ESR capacitor such as C13A for primary-side loop and C22 for the secondary-side loop can help to reduce the switching ripple which comes out to the input terminals V_{IN}. In addition, adding a low-ESR ceramic capacitor in parallel to the C13A/C22 can help to further reduce the switching ripple.
- The Y-capacitor C12 has a function to return the HF noise to the source (negative of C13A) and reduce the overall HF noise going out to the input terminals. The larger capacitance is more effective. However, larger values would introduce larger leakage current and may fail the safety requirements.
- Adding a drain to the CS pin capacitor for the MOSFET of the CoolSET™ can reduce the high switching noise. However, it also reduces efficiency.[1]
- Adding a ferrite bead to the critical nodes of the circuit can help to reduce the HF noise, such as on the connecting path between the transformer and the drain pin, output diode D21, Y-capacitor C12, etc.[1]
- Adding additional output CMC can also help to reduce the HF noise.[1]

[1] Not implemented with this reference design.

6 PCB layout

6.1 Top side

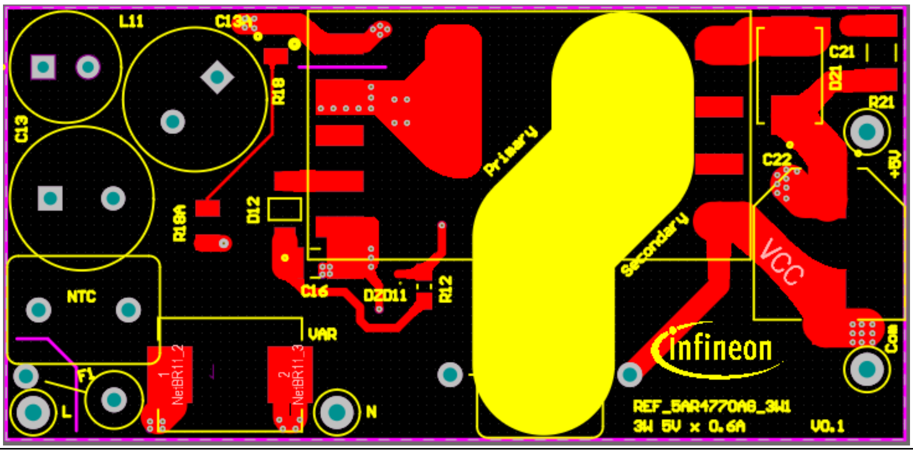


Figure 6 Top-side copper and component legend

6.2 Bottom side

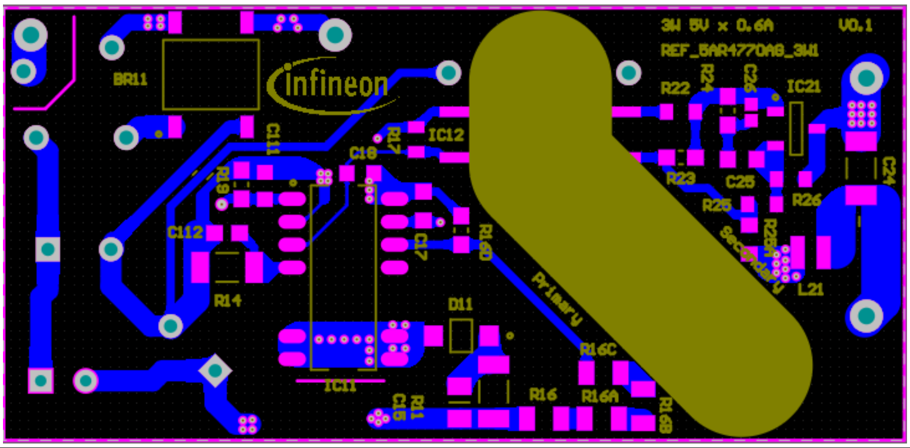


Figure 7 Bottom-side copper and component legend

6.3 Top and bottom side copper

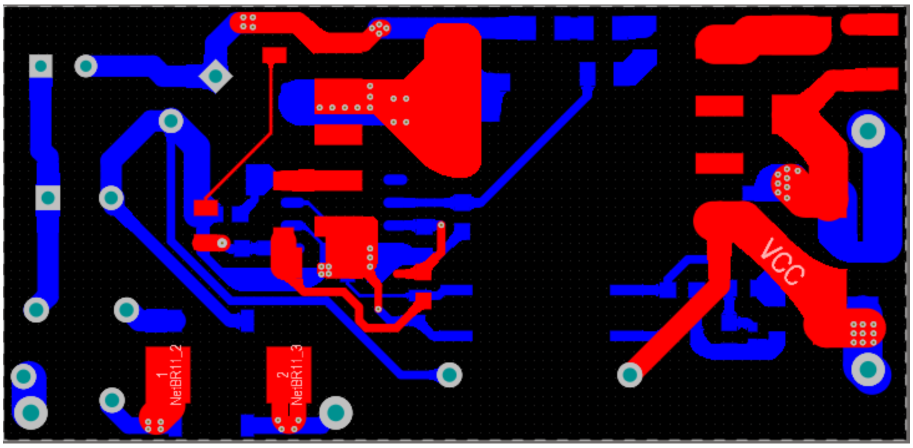


Figure 8 Top and bottom side copper

7 BOM

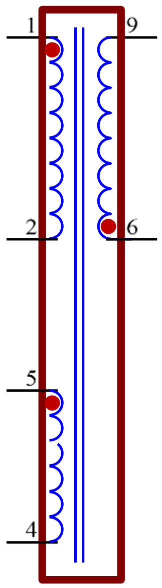
Table 4 BOM (V 0.2)

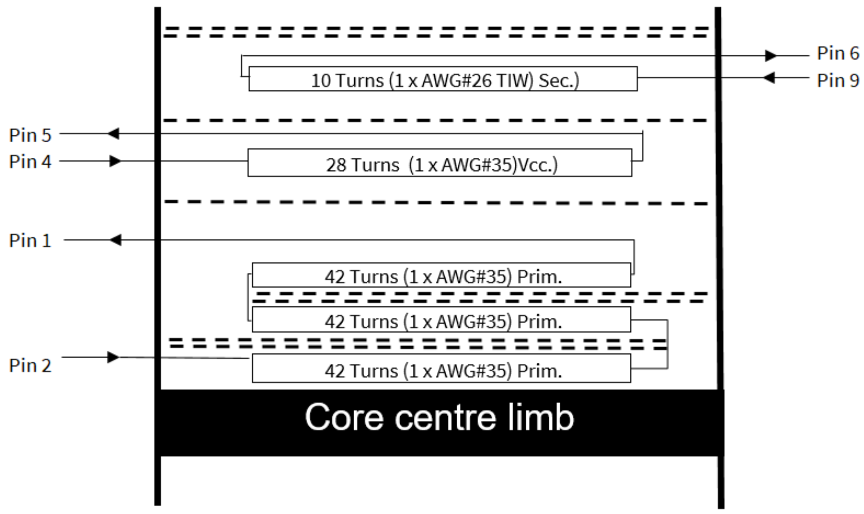
No.	Designator	Description	Part number	Manufacturer	Quantity
1	+5 V	KEY_PN5000	5000		1
2	BR11	D1UBA80-7062	D1UBA80-7062	Shindengen	1
3	C12	1 nF, 500 V	DE1E3RA102MA4BQ01F	Murata	1
4	C13, C13A	4.7 µF, 400 V	860021374008	Wurth Electronic	2
5	C16	4.7 µF, 50 V	GRM31CR71H475KA12	Murata	1
6	C17, C25	100 nF, 50 V	885012206095	Wurth Electronic	2
7	C18	1 nF, 50 V	885012206083	Wurth Electronic	1
8	C22	820 µF, 6.3 V	875075155009	Wurth Electronic	1
9	C24	10 µF, 25 V	885012208069	Wurth Electronic	1
10	C26	68 pF, 50 V	885012006056	Wurth Electronic	1
11	C111	22 nF, 50 V	885012206091	Wurth Electronic	1
12	Com, N	KEY_PN5001	5001		2
13	D12	200 V, 0.8 A	RS1DL		1
14	D21	50 V, 8 A	V8PAN50-M3/I		1
15	F1	0.5 A, 250 V	MCPMP 0.5 A 250 V		1
16	IC11	ICE5AR4770AG	ICE5AR4770AG	Infineon Technologies	1
17	IC12	VOL618A-3X001T	VOL618A-3X001T		1
18	IC21	TL431BQDBZR	TL431BQDBZR		1
19	L	KEY_PN5002	5002		1
20	L11	1000 µH	7447462102	Wurth Electronic	1
21	L21	2.2 µH	DFE201610E-2R2M=P2	Murata	1
22	NTC	4.7 R	B57153S0479M0	Epcos	1
23	R12	27 R (0603)	AC0603FR-0727RL		1
24	R14	3.9 R (1206)	ERJ8RQF3R9V		1
25	R16, R16A, R16B, R16C, R16D	15 MEGR/150 V (0805)	RC0805JR-0715ML		5
26	R17	750 kR (0603)	CRCW0603750KFK		1
27	R18, R18A	8.2 MEGR/400 V (0805)	WK08V825 JTL		2
28	R19	121 kR (0603)	ERJ3EKF1213V		1
29	R22	120 R (0603)	RC0603FR-07120RL		1
30	R23	1.2 kR (0603)	RC0603FR-071K2L		1
31	R24, R25, R26	10 k (0603)	RC0603FR-0710KL		3
32	R25A	0 R(0603)	RC0603JR-070RL		1
33	TR1	1.96 mH (126:10:28) (EE13 7 4)	750344058 (Rev. 02)	Wurth Electronic	1
34	VAR	300 V	B72650M0301K072	Epcos	1
35	PCB	50 mm × 24 mm (L × W), single layer, 1 Oz., FR-4			1

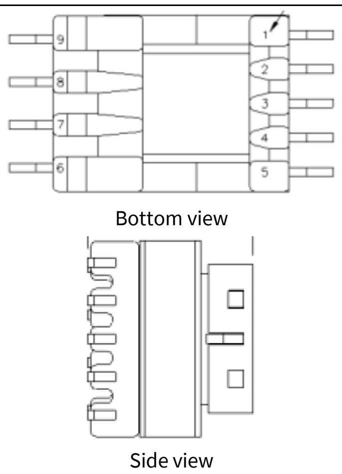
8 Transformer specification

(Refer to Appendix A for transformer design and Appendix B for WE transformer specification.)

- Core and materials: EE13/7/4, TP4A (TDG)
- Bobbin: 070-6258 (9-terminal, SMD, horizontal version)
- Primary inductance: L_p = 1.96 mH (±10 percent), measured between pin 1 and pin 2
- Manufacturer and part number: Wurth Electronics Midcom (750344058) Rev. 02







Start	Stop	Turns	Wire size	Layer
2	1	126	1 x AWG#35	Primary
4	5	28	1 x AWG#35	V_{CC}
9	6	10	1 x AWG#26 TIW	Secondary
2 mm horizontal external copper shield is added and tied to pin 5				

Figure 9 Transformer structure

9 Measurement data and graphs

Table 5 Measurement data

Input (V AC/Hz)	Description	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A)	P_{OUT} (W)	η (%)	η avg (%)	P_{in_OLP} (W)	I_{out_OLP} (A)
85/60	No load	0.019	5.01	0.000				4.89	0.79
	Min. load	0.22	5.00	0.030	0.15	68.18			
	1/10 load	0.39	5.00	0.059	0.30	75.64			
	1/4 load	0.93	4.99	0.150	0.75	80.48	81.24		
	Typ. load	1.83	4.98	0.300	1.49	81.64			
	3/4 load	2.74	4.96	0.451	2.24	81.64			
	Max. load	3.65	4.94	0.600	2.96	81.21			
115/60	No load	0.020	5.01	0.000				4.93	0.81
	Min. load	0.21	5.00	0.030	0.15	71.43			
	1/10 load	0.40	5.00	0.061	0.31	76.25			
	1/4 load	0.93	4.97	0.150	0.75	80.16	81.59		
	Typ. load	1.82	4.98	0.300	1.49	82.09			
	3/4 load	2.72	4.96	0.451	2.24	82.24			
	Max. load	3.62	4.94	0.600	2.96	81.88			
230/50	No load	0.029	5.01	0.000				5.30	0.87
	Min. load	0.23	5.00	0.030	0.15	65.22			
	1/10 load	0.43	5.00	0.061	0.31	70.93			
	1/4 load	0.96	4.99	0.150	0.75	77.97	79.88		
	Typ. load	1.86	4.98	0.300	1.49	80.32			
	3/4 load	2.78	4.96	0.451	2.24	80.47			
	Max. load	3.67	4.94	0.600	2.96	80.76			
264/50	No load	0.032	5.01	0.000				5.50	0.90
	Min. load	0.24	5.00	0.030	0.15	62.50			
	1/10 load	0.45	5.00	0.061	0.31	67.78			
	1/4 load	0.98	4.99	0.150	0.75	76.38	78.86		
	Typ. load	1.89	4.98	0.300	1.49	79.05			
	3/4 load	2.80	4.96	0.451	2.24	79.89			
	Max. load	3.70	4.94	0.600	2.96	80.11			

- No-load condition (no load) : 5 V at 0 A
- Minimum load condition (min. load) : 5 V at 30 m A
- 1/10 load condition (1/10 load) : 5 V at 60 mA
- 1/4 load condition (1/4 load) : 5 V at 0.15 A
- Typical load condition (typ. load) : 5 V at 0.3 A
- 3/4 load condition (3/4 load) : 5 V at 0.45 A
- Maximum load condition (max. load) : 5 V at 0.6 A

9.1 Load regulation

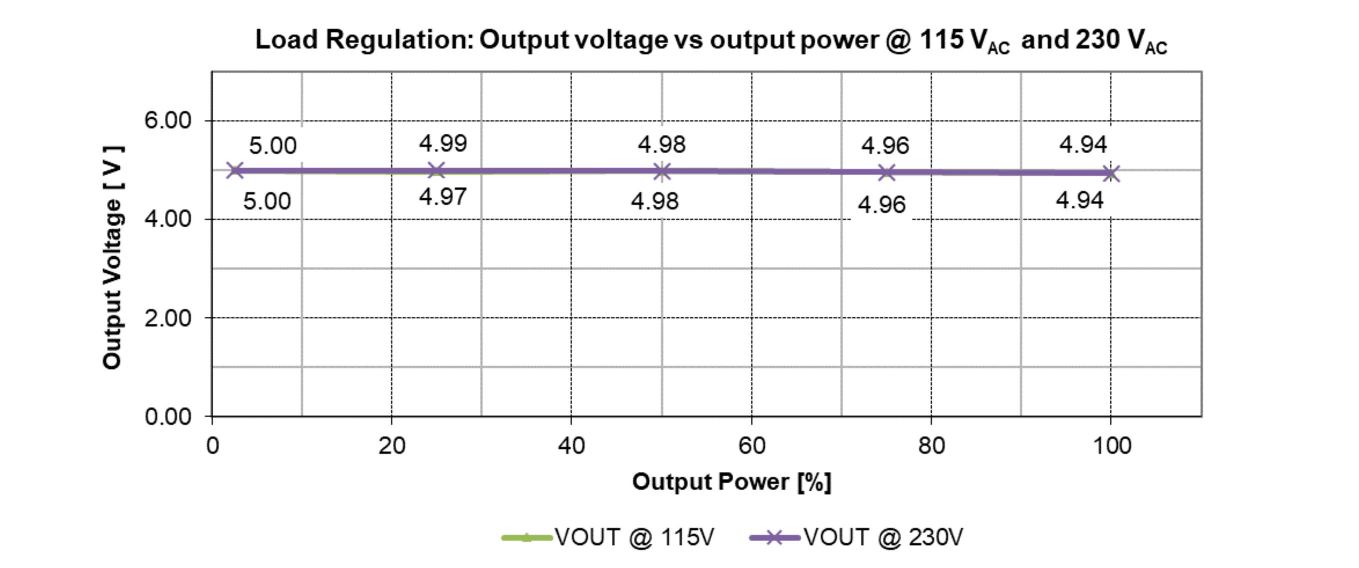


Figure 10 Load regulation V_{OUT} vs output power

9.2 Line regulation

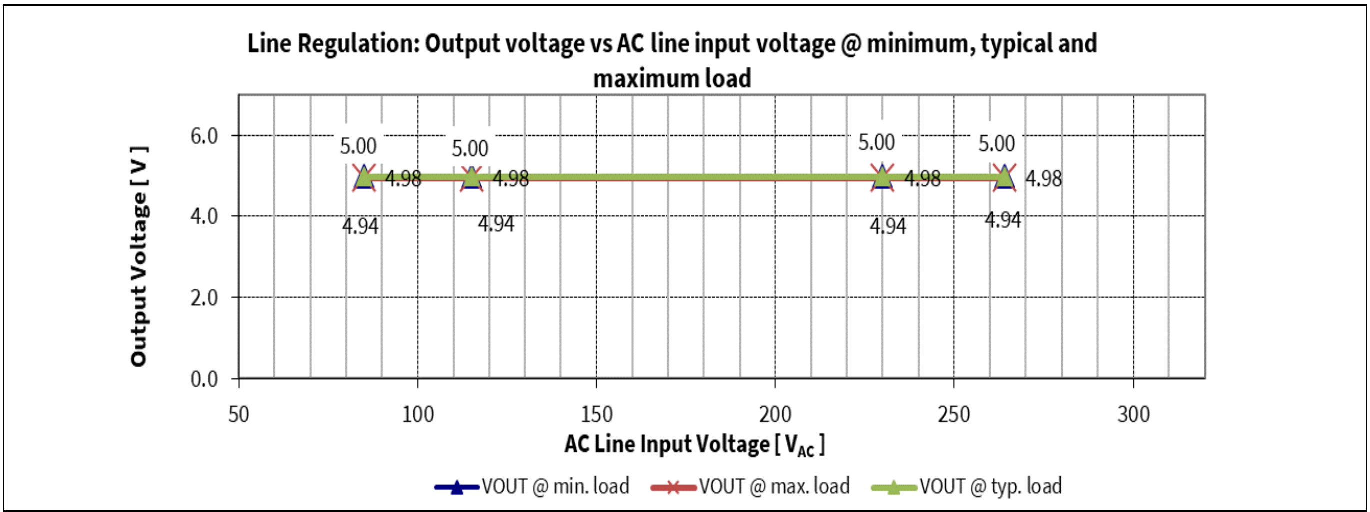


Figure 11 Line regulation: V_{OUT} vs AC-line input voltage

9.3 Efficiency vs AC-line input voltage

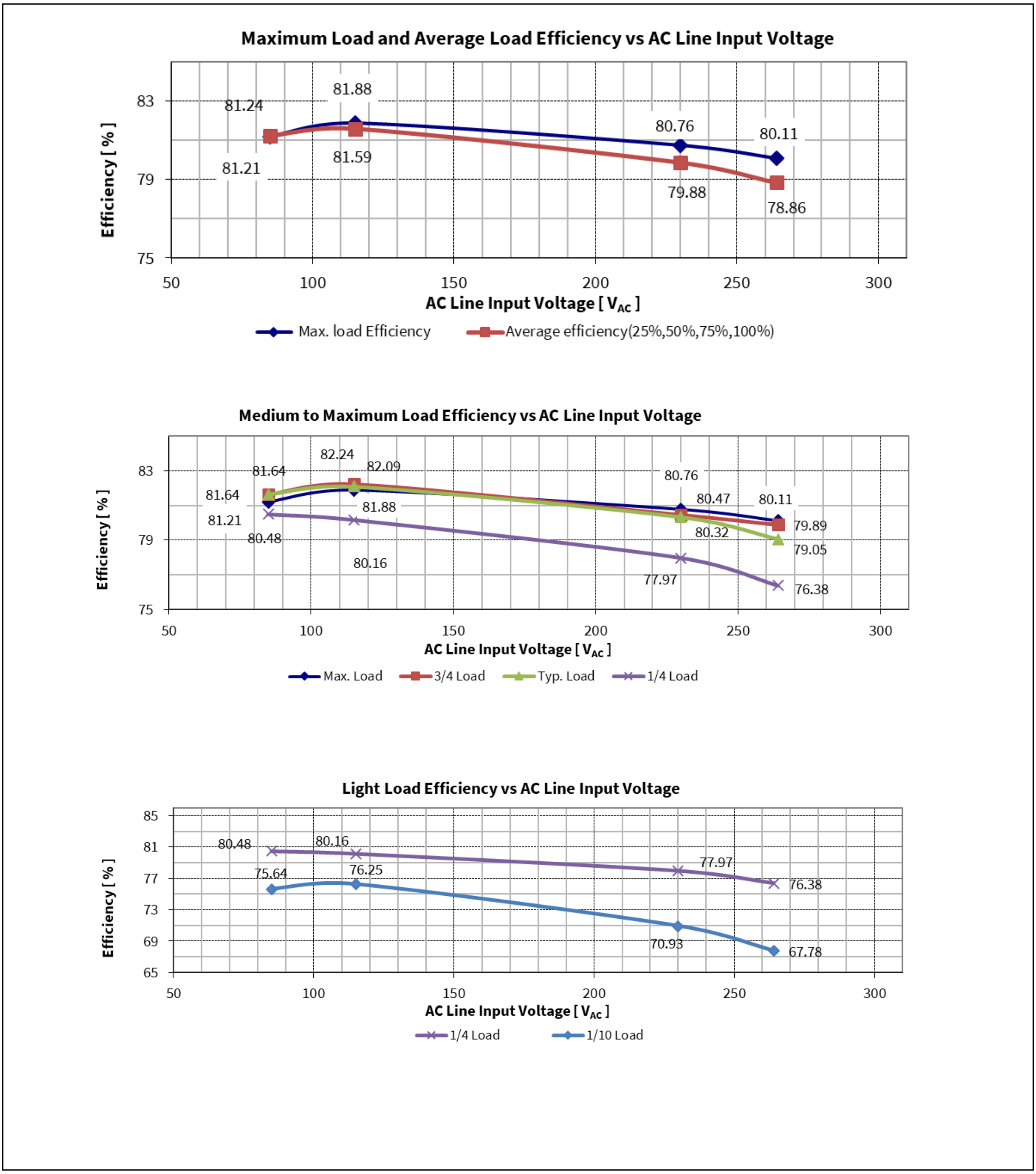


Figure 12 **Efficiency vs AC-line input voltage**

9.4 Standby power

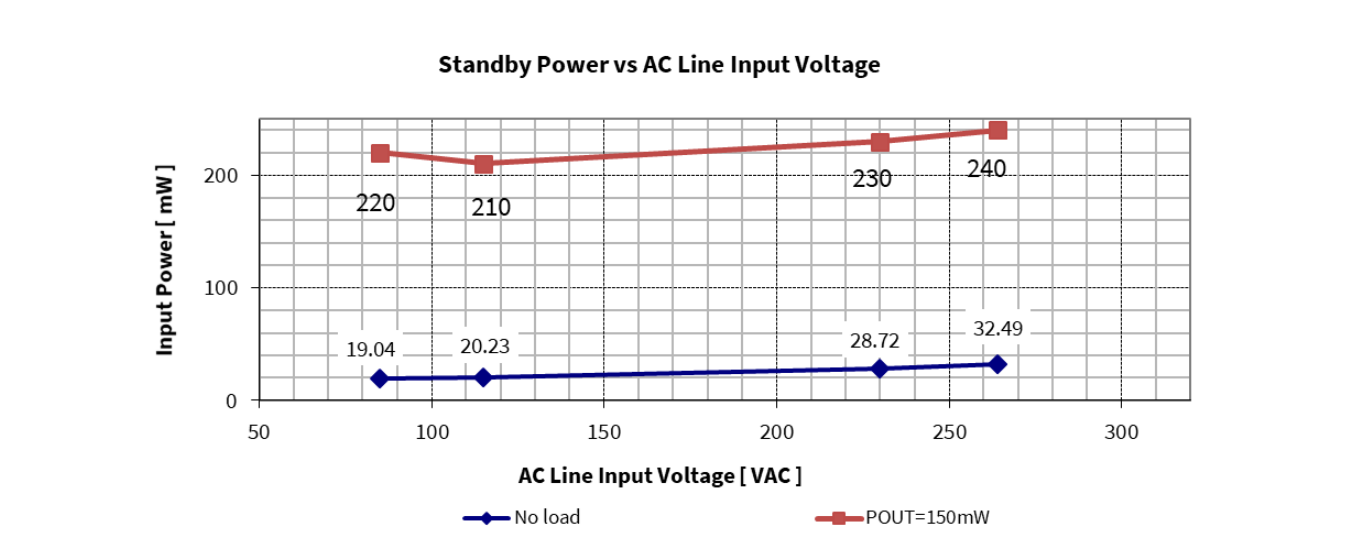


Figure 13 Standby power at no load (P_{stby_NL}) and 150 mW load vs AC-line input voltage (measured by Yokogawa WT210 power meter – integration mode)

9.5 Maximum output current

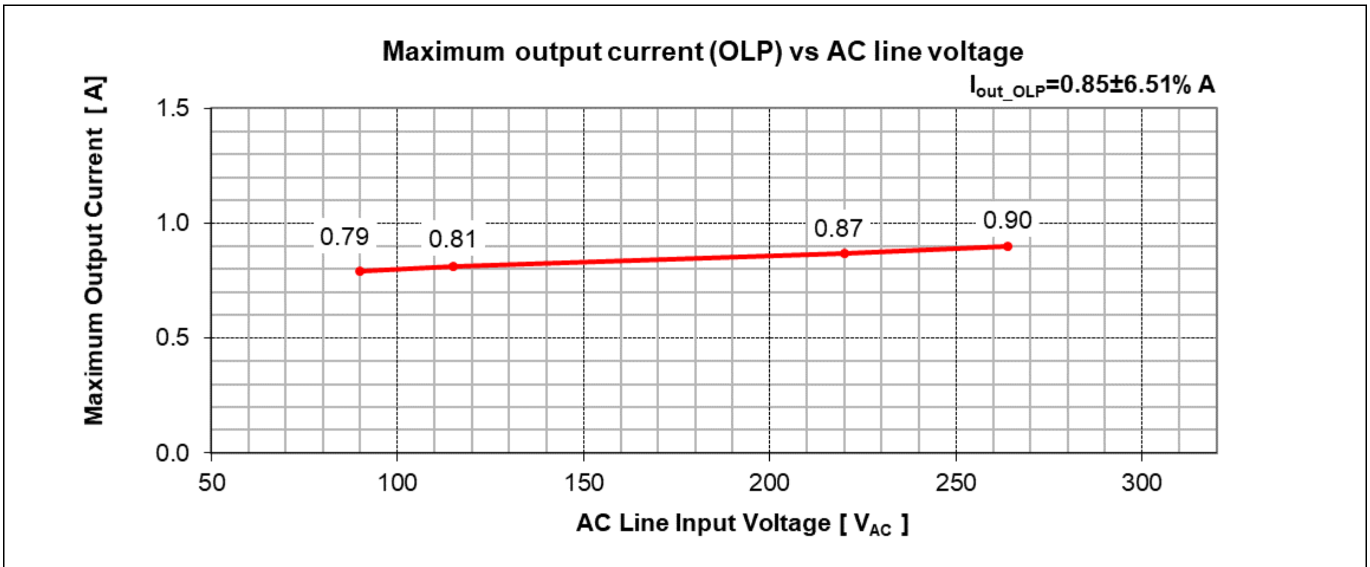


Figure 14 Maximum output current (before over-load protection) vs AC-line input voltage

10 Thermal measurement

The thermal testing of the demo board was done in the open air without forced ventilation at an ambient temperature of 25°C. An infrared thermography camera (FLIR-T62101) was used to capture the thermal reading of particular components. The measurements were taken at the maximum load running for one hour. The tested input voltage was 85 V AC and 264 V AC.

Table 6 Component temperature at full load (5 V, 0.6 A) under T_{amb} = 25°C

Circuit code	Major component	85 V AC (°C)	264 V AC (°C)
IC11	ICE5AR4770AG	39.3	46.6
TR1	Transformer	42.0	44.6
BR1	Bridge diode	34.9	31.3
D21	+5 V output diode	47.8	48.1
	Ambient	25.0	25.0

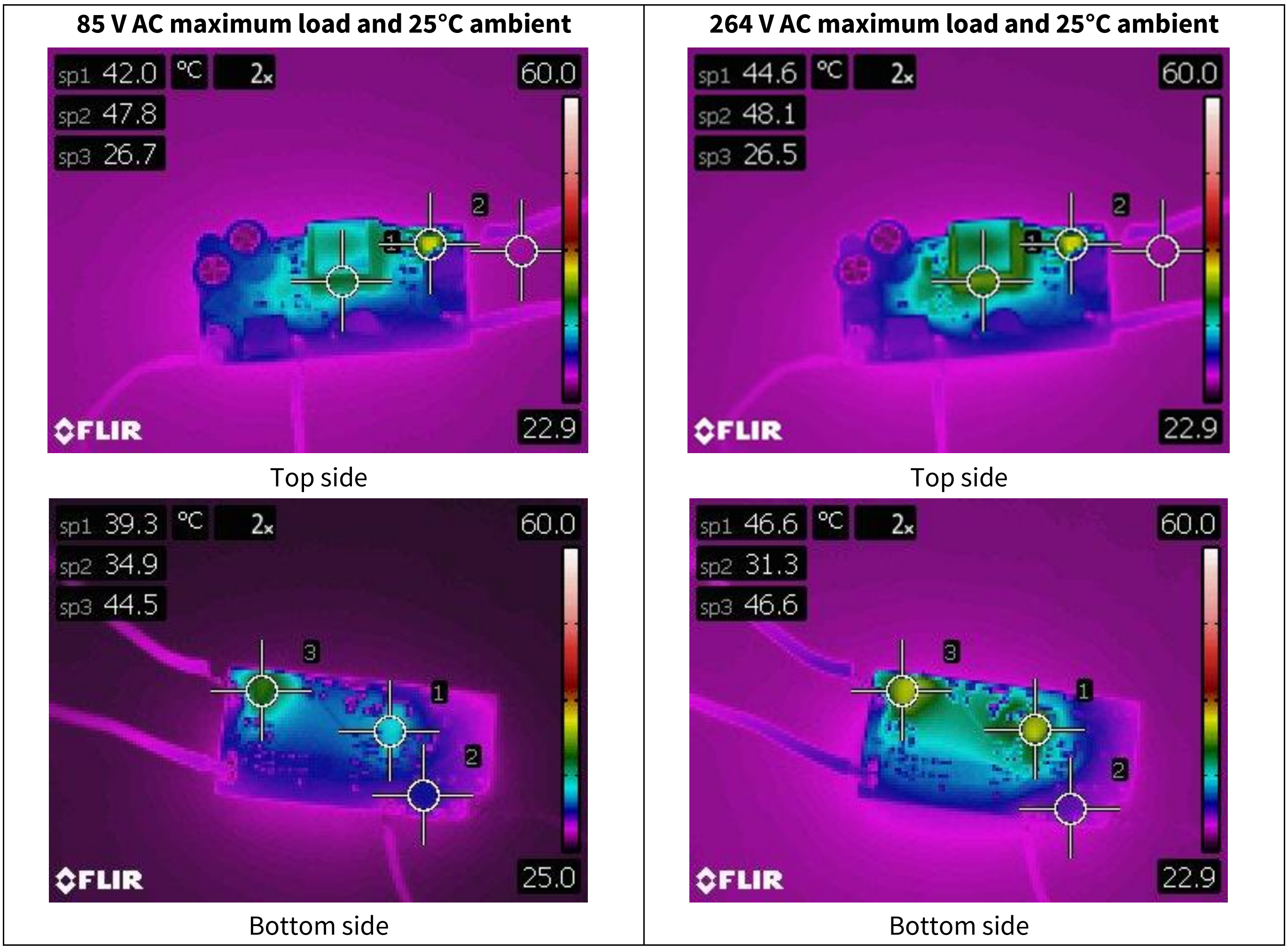


Figure 15 Infrared thermal image of REF_5AR4770AG_3W1

11 Waveforms

All waveforms and scope plots were recorded with a Teledyne LeCroy 606Zi oscilloscope.

11.1 Start-up at low/high AC-line input voltage with maximum load

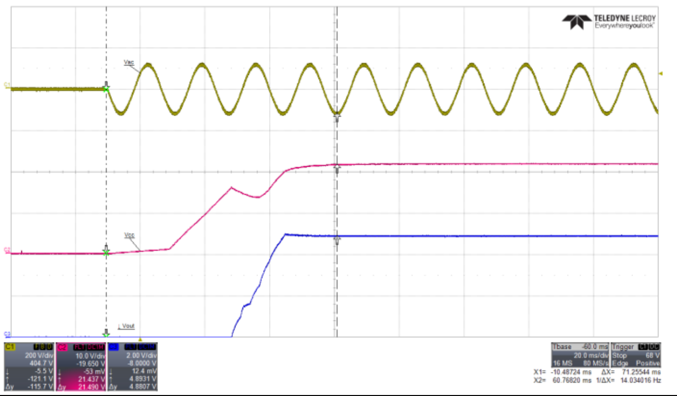
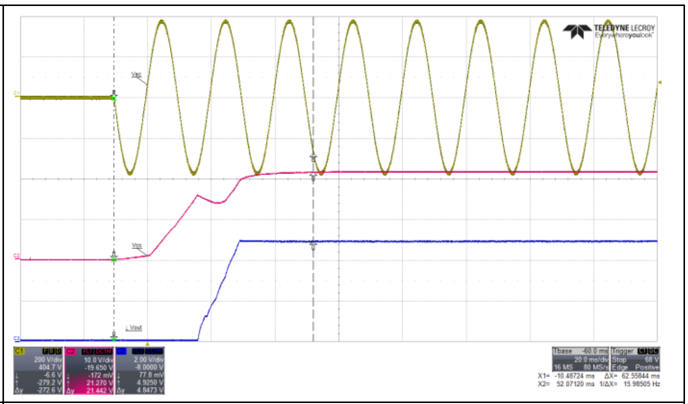
	
C1 (yellow): V AC; C2 (purple): V_{VCC}; C3 (blue): V_{OUT} (5 V)	C1 (yellow): V AC; C2 (purple): V_{VCC}; C3 (blue): V_{OUT} (5 V)
V_{IN} = 85 V AC, max. load; start-up time: ≈ 71 ms	V_{IN} = 264 V AC, max. load; start-up time: ≈ 62 ms

Figure 16 Start-up

11.2 Soft-start

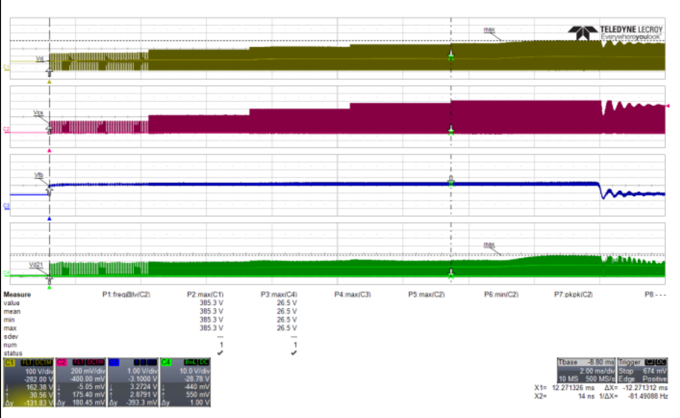
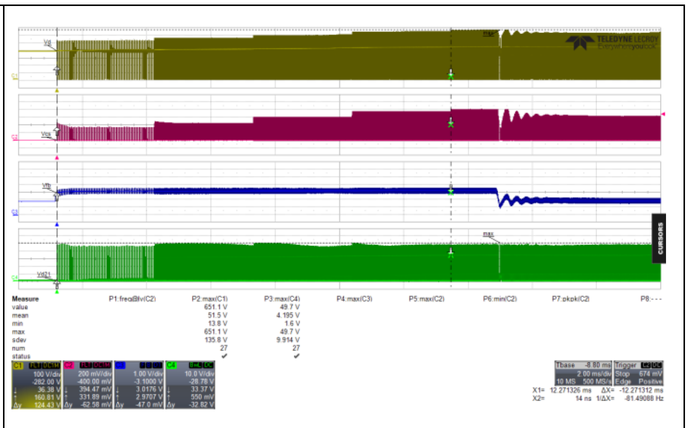
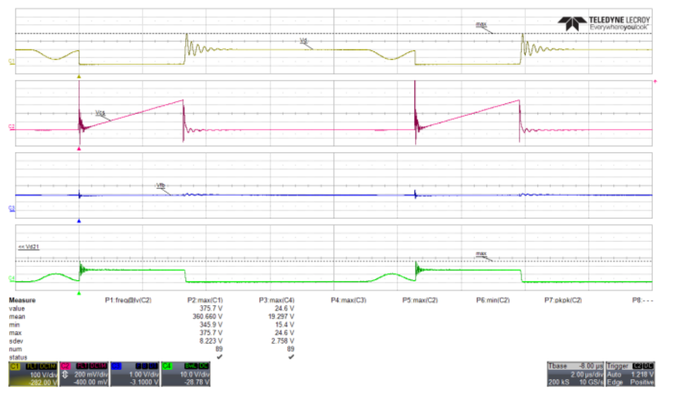
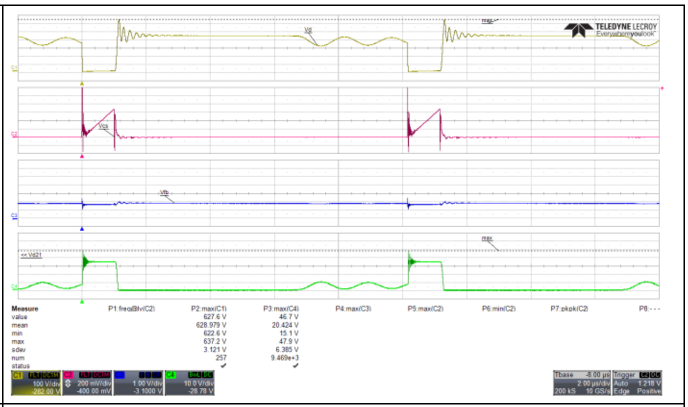
	
C1 (yellow): V_{Drain}; C2 (purple): V_{CS}; C3 (blue): V_{FB}; C4 (green): V_{D21}	C1 (yellow): V_{Drain}; C2 (purple): V_{CS}; C3 (blue): V_{FB}; C4 (green): V_{D21}
V_{IN} = 85 V AC, max. load; soft-start time: ≈ 12 ms	V_{IN} = 264 V AC, max. load; soft-start time: ≈ 12 ms

Figure 17 Soft-start

11.3 Switching waveform at maximum load

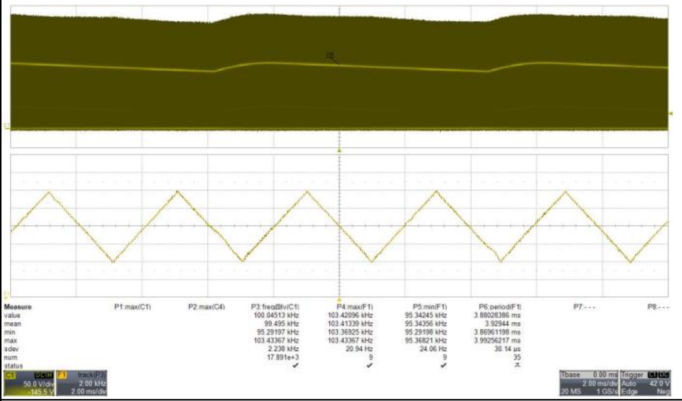


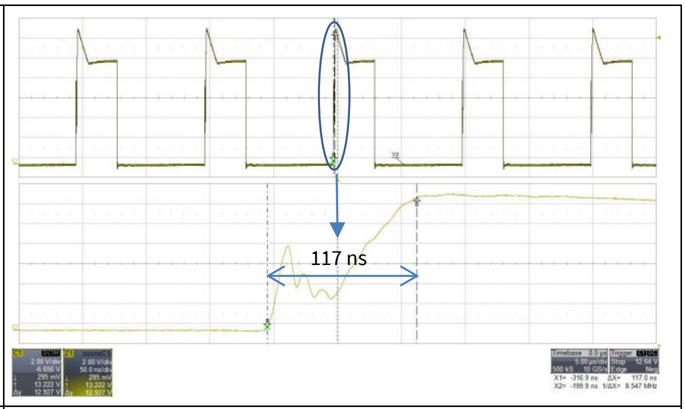


C1 (yellow): V_{Drain}; C2 (purple): V_{CS}; C3 (blue): V_{FB}; C4 (green): V_{D21}	C1 (yellow): V_{Drain}; C2 (purple): V_{CS}; C3 (blue): V_{FB}; C4 (green): V_{D21}
V_{IN} = 85 V AC, max. load; V_{Drain_max}: 375 V DC and V_{D21_max}: 24 V DC	V_{IN} = 264 V AC, max. load; V_{Drain_max}: 637 V DC and V_{D21_max}: 48 V DC

Figure 18 Drain and CS voltage at maximum load

11.4 Frequency jittering and modulated gate drive





C1 (yellow): V_{Drain}; F1 (orange): Frequency track of V_{Drain}	C1 (yellow): V_{GATE}; Z1 (orange): Zoom of V_{GATE}
V_{IN} = 85 V AC, 100 percent load; jittering frequency ≈ 95 kHz ~ 103 kHz and period ≈ 4 ms	V_{IN} = 85 V AC, 100 percent load; modulated gate drive rising-up time ≈ 117 ns

Figure 19 Frequency jittering and modulated gate drive

11.5 Output ripple voltage at maximum load

- Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz BW

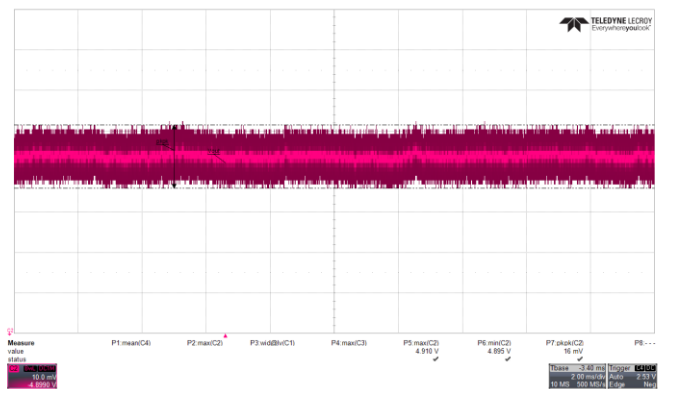
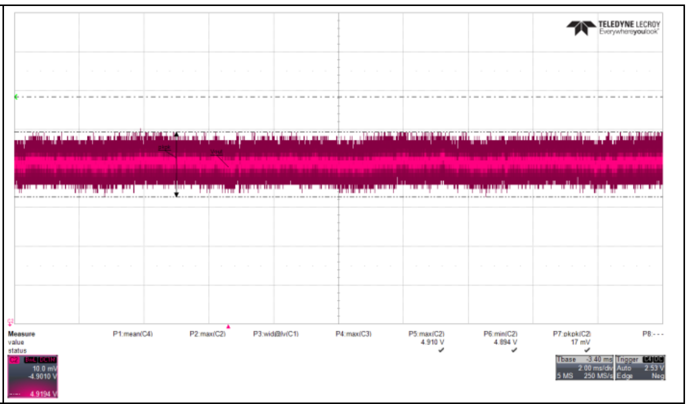
	
C2 (purple): V_{RIPPLE} (5 V)	C2 (purple): V_{RIPPLE} (5 V)
V_{IN} = 85 V AC, max. load; $V_{RIPPLE1}$ (12 V): 16 mV	V_{IN} = 264 V AC, max. load; $V_{RIPPLE1}$ (5 V): 17 mV

Figure 20 Output ripple voltage at maximum load

11.6 Output ripple voltage in ABM 50 mW load

- Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz BW
- Load: 50 mW (5 V, 10 mA)

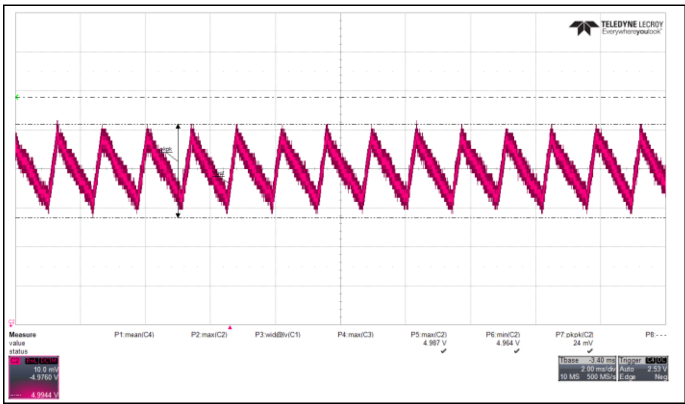
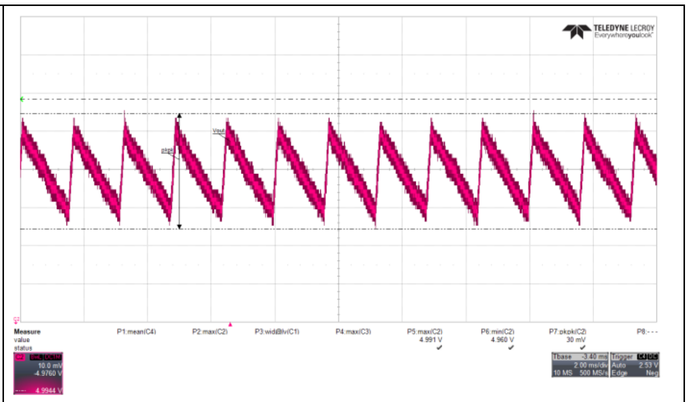
	
C2 (purple): V_{RIPPLE} (5 V)	C2 (purple): V_{RIPPLE} (5 V)
V_{IN} = 85 V AC, 50 mW load; V_{RIPPLE} (5 V): 24 mV	V_{IN} = 264 V AC, 50 mW load; $V_{RIPPLE1}$ (12 V): 30 mV

Figure 21 Output ripple voltage in ABM 50 mW load

11.7 Load transient response (dynamic load from 10 percent to 100 percent)

- Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz BW
- 5 V load change from 10 percent to 100 percent, 100 Hz, 0.4 A/µs slew rate

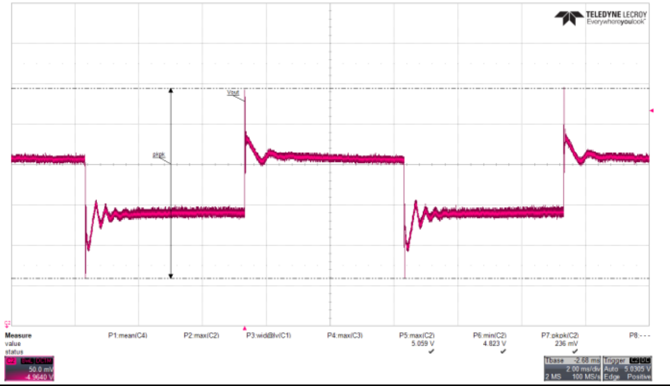
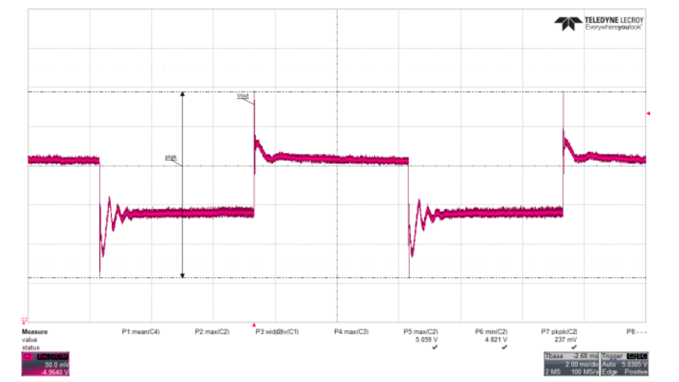
	
C2 (purple): V_{RIPPLE} (5 V)	C2 (purple): V_{RIPPLE} (5 V)
V_{IN} = 85 V AC, 10 percent to 100 percent load; V_{RIPPLE} (5 V): 236 mV	V_{IN} = 264 V AC, 10 percent to 100 percent load; V_{RIPPLE} (5 V): 237 mV

Figure 22 Load transient response

11.8 Entering ABM

- Load change from 3 W (5 V, 0.6 A) to 0.1 W (5 V, 0.02 A)

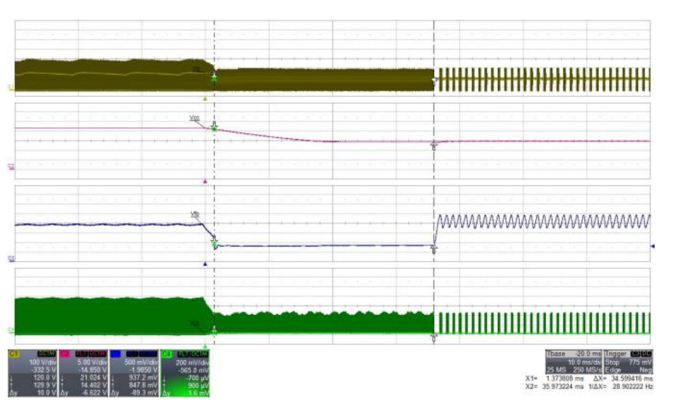
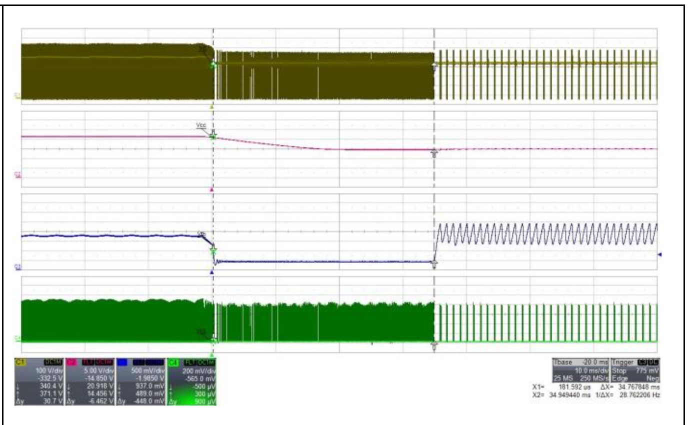
	
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}	C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}
V_{IN} = 85 V AC; system enters burst mode option 2: V_{FB} less than 0.93 V and $t_{blanking}$ = 36 ms	V_{IN} = 264 V AC; system enters burst mode option 2: V_{FB} less than 0.93 V and $t_{blanking}$ = 36 ms

Figure 23 Entering ABM

11.9 During ABM

- Load: 0.11 W (5 V, 0.022 A)

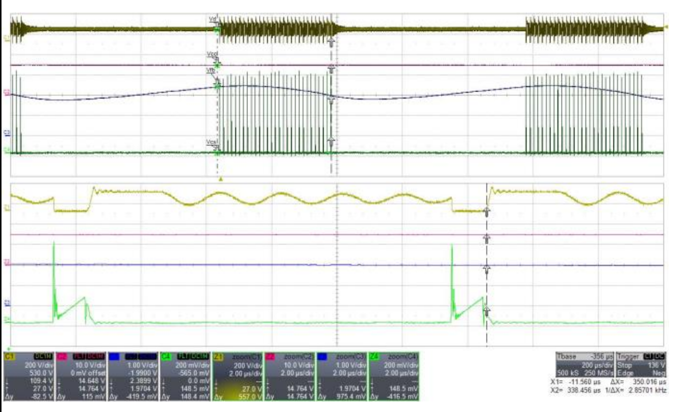
	
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}	C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}
V_{IN} = 85 V AC; burst mode option 2: V_{FB_BOn} = 2.35 V, V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.22 V, f_{OSC4_ABM} = 83 kHz	V_{IN} = 264 V AC; burst mode option 2: V_{FB_BOn} = 2.35 V, V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.22 V, f_{OSC4_ABM} = 83 kHz

Figure 24 During ABM

11.10 Leaving ABM

- Load change from 0.1 W (5 V, 0.02 A) to full load

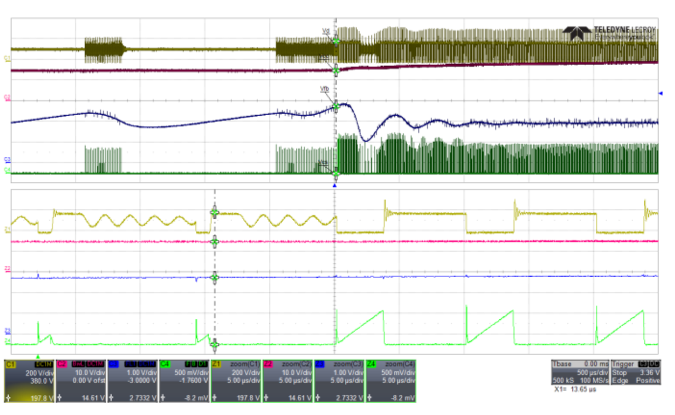
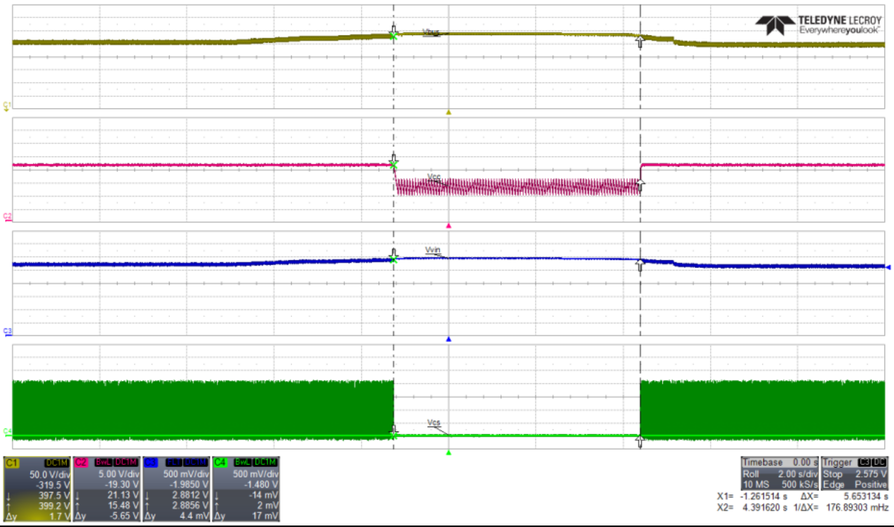
	
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}	C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{CS}
V_{IN} = 85 V AC; system leaves burst mode: V_{FB} greater than 2.73 V	V_{IN} = 264 V AC; system leaves burst mode: V_{FB} greater than 2.73 V

Figure 25 Leaving ABM

11.11 Line OVP (non-switch auto-restart)

- Increase AC-line voltage gradually at maximum load until line OVP is detected and then decrease the AC-line until line OVP reset is detected



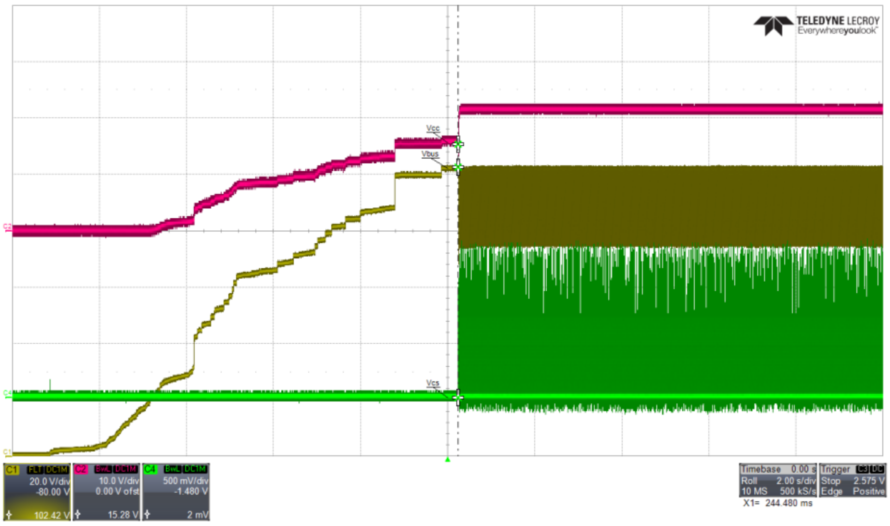
C1 (yellow): V_{Bus}; C2 (purple): V_{VCC}; C3 (blue): V_{VIN}; C4 (green): V_{CS}

Max. load; line OVP triggered: V_{BUS} greater than 398 V DC or V_{VIN} greater than 2.85 V; line OVP reset: V_{BUS} less than 398 V DC or V_{VIN} less than 2.85 V

Figure 26 Line OVP

11.12 Brown-in protection by utilizing $R_{Brown\text{-}in}$ (R16D in Figure 3)

- Increase AC-line voltage gradually at full load until the system starts up



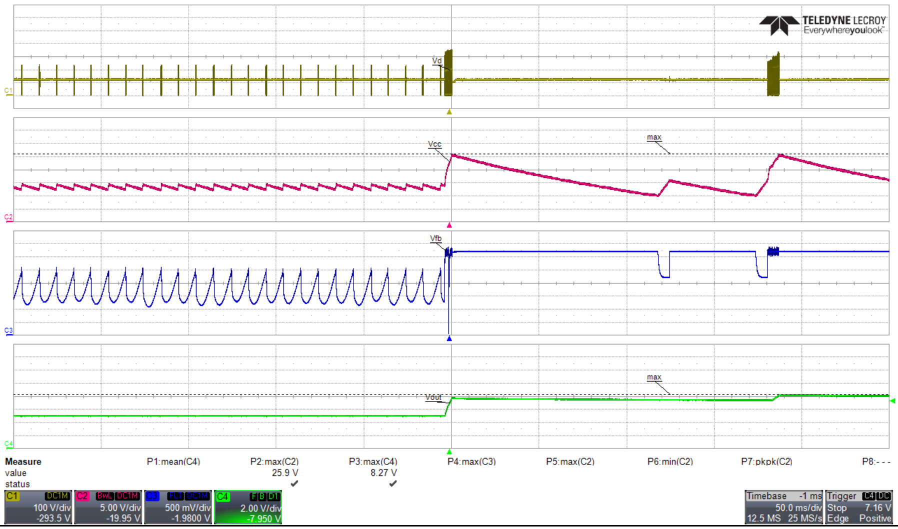
C1 (yellow): V_{Bus}; C2 (purple): V_{VCC}; C4 (green): V_{CS}

Full load; brown-in: 73 V AC (V_{BUS} greater than 102 V DC)

Figure 27 Brown-in protection

11.13 Output OVP by utilizing V_{CC} OVP (odd-skip auto-restart)

- Short R26 resistor during system operation at no load



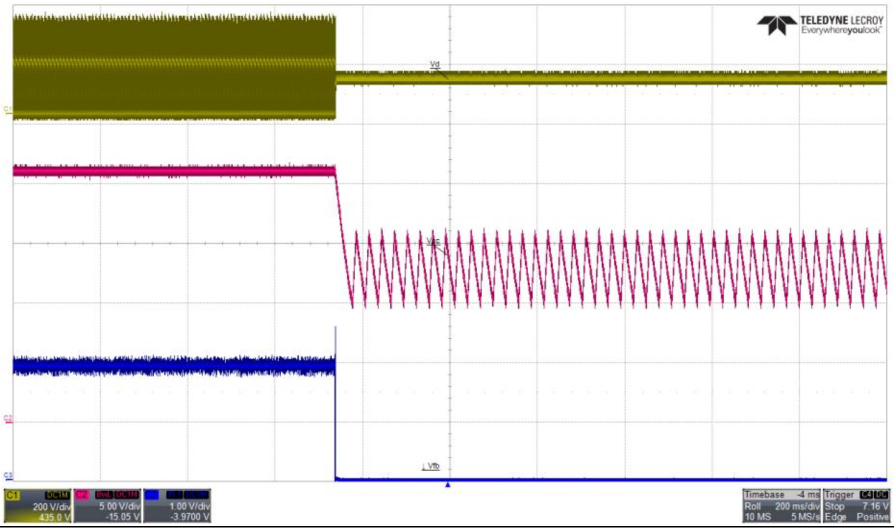
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB} (12 V); C4 (green): V_{OUT}

V_{IN} = 85 V AC; system enters output OVP by using V_{CC} OVP: V_{OUT} greater than 8 V (V_{CC} greater than 25.5 V)

Figure 28 **V_{CC} OVP**

11.14 V_{CC} UVP (auto-restart)

- Short R17 while the system is operating at full load



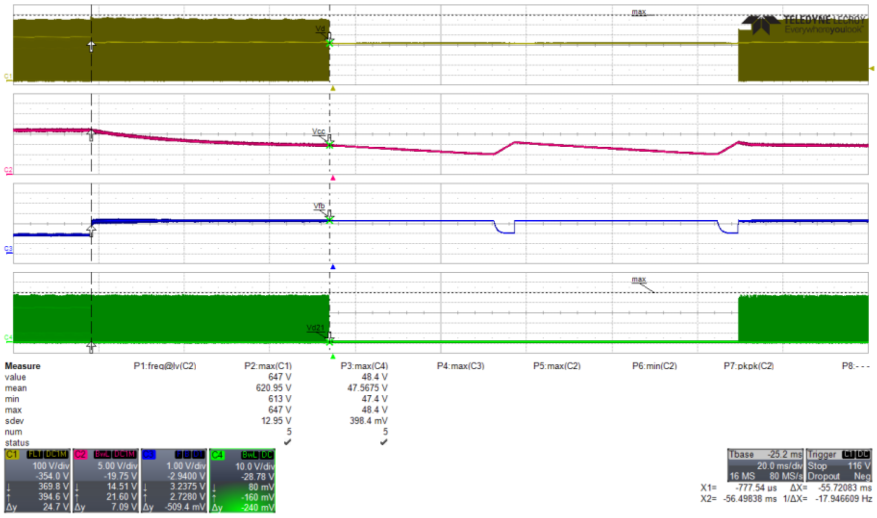
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}

V_{IN} = 85 V AC; system enters V_{CC} UVP: V_{CC} less than 10 V

Figure 29 **V_{CC} UVP**

11.15 Over-load protection (odd-skip auto-restart)

- V_{OUT} (5 V) short-to-GND at 264 V AC

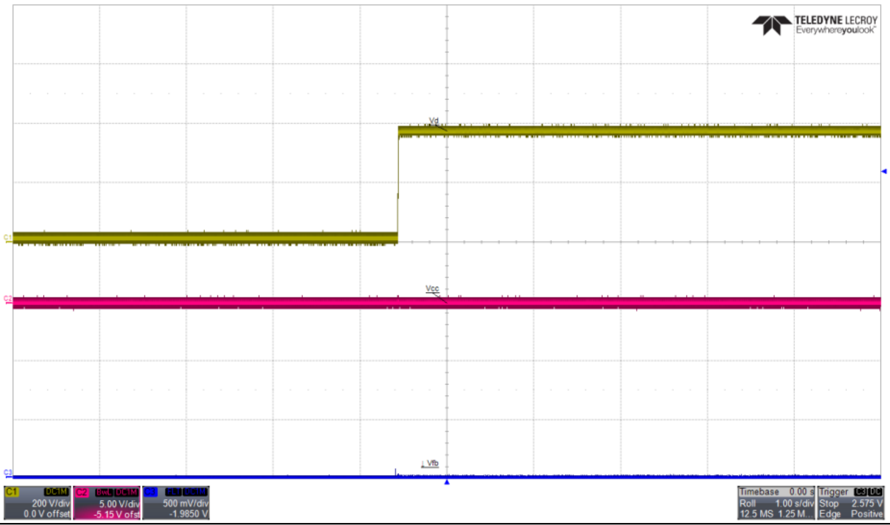


C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}; C4 (green): V_{D21}
V_{IN} = 264 V AC; system enters over-load protection: V_{FB} greater than 2.73 V and lasts for ≈ 52 ms blanking time: V_{Drain_max}: 647 V DC and V_{D21_max}: 49 V DC

Figure 30 Over-load protection and max. voltage stress for MOSFET and output diode (D21)

11.16 V_{CC} short-to-GND protection

- Short V_{CC} pin-to-GND with current meter before system start-up



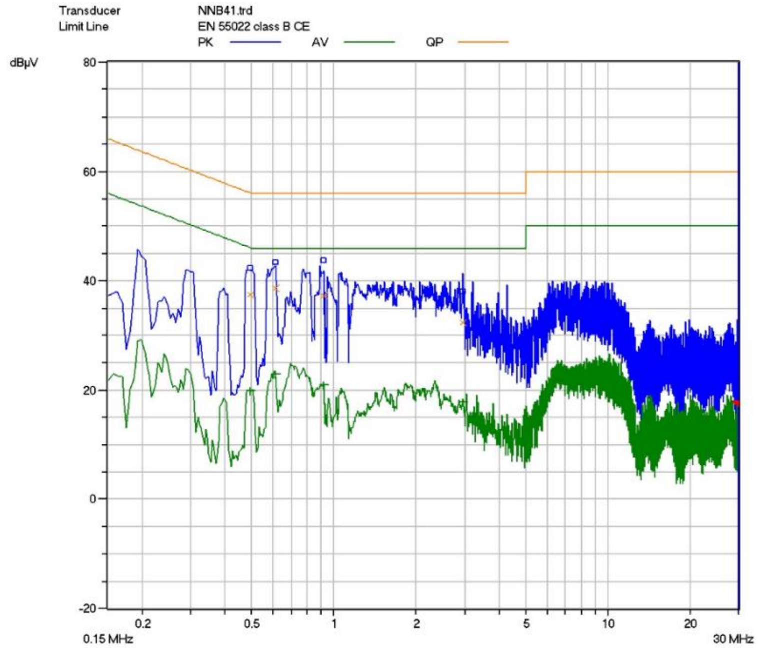
C1 (yellow): V_{Drain}; C2 (purple): V_{VCC}; C3 (blue): V_{FB}
V_{IN} = 264 V AC; system enters V_{CC} short-to-GND: V_{CC} less than V_{VCC_SCP} ➔ I_{VCC} = 430 µA (input power ≈ 140 mW)

Figure 31 V_{CC} short-to-GND protection

11.17 Conducted emissions (EN 55022 class B)

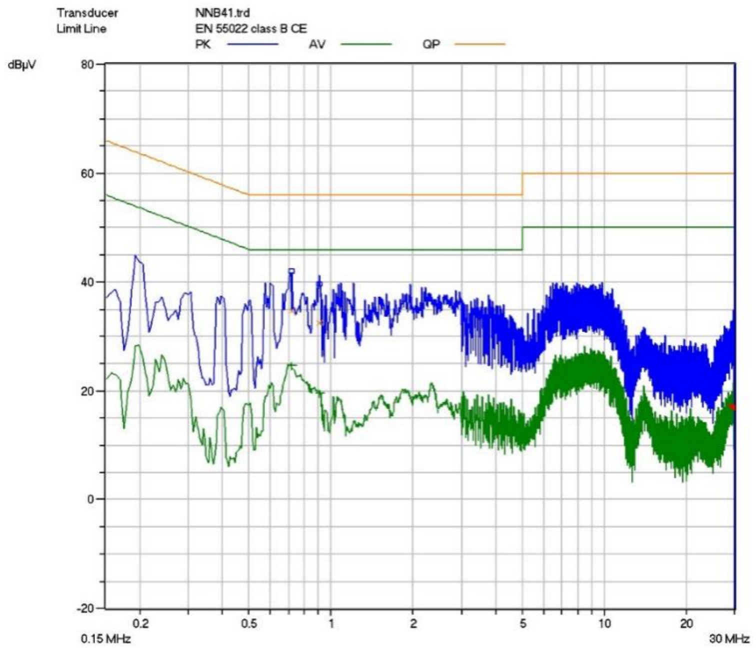
Equipment: Schaffner SMR4503 (receiver); standard: EN 55022 (CISPR 22) class B; test conditions: V_{IN} = 115 V AC and 230 V AC; load: 3 W (5 V, 8.3 Ω).

- Pass conducted emissions EN 55022 (CISPR 22) class B with greater than 16 dB margin for quasi-peak measurement.



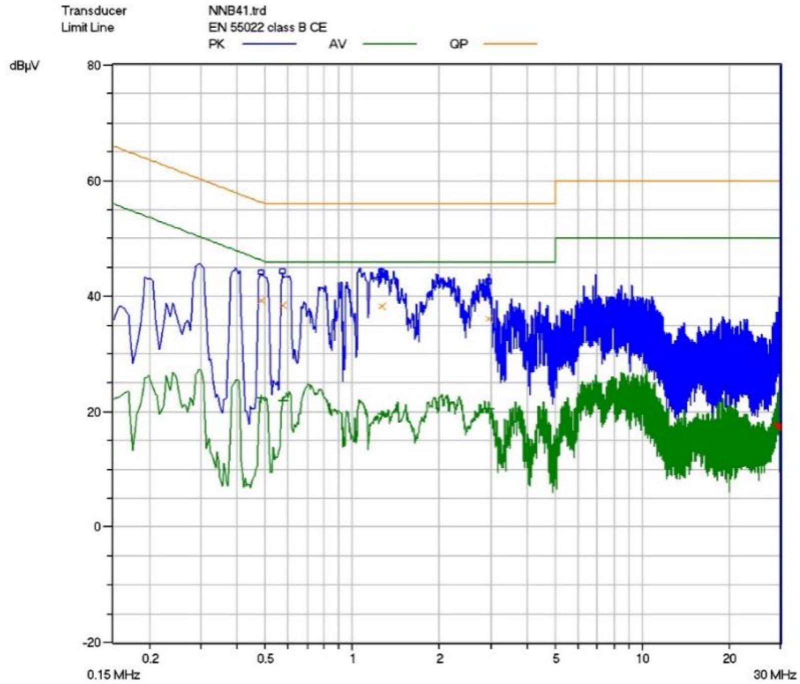
Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.4920	L	42.4	L	20.0	L	37.5	46.1	56.1
0.6120	L	43.3	L	23.0	L	38.6	46.0	56.0
0.9120	L	43.9	L	20.9	L	37.2	46.0	56.0
2.9640	L	38.1	L	17.8	L	32.3	46.0	56.0

Figure 32 Conducted emissions at 115 V AC-line and 3 W load – greater than 17 dB margin



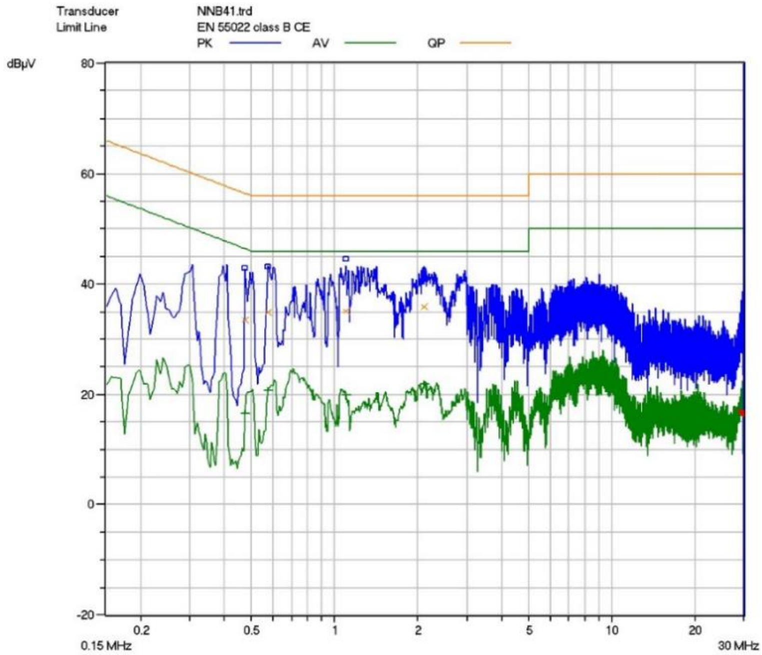
Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.7140	N	42.0	N	24.7	N	34.7	46.0	56.0
0.9060	N	39.6	N	19.5	N	32.5	46.0	56.0

Figure 33 Conducted emissions at 115 V AC-neutral and 3 W load – greater than 21 dB margin



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.4860	L	44.2	L	22.4	L	39.4	46.2	56.2
0.5760	L	44.5	L	21.9	L	38.5	46.0	56.0
1.2660	L	44.3	L	19.6	L	38.2	46.0	56.0
2.9640	L	42.5	L	20.6	L	36.1	46.0	56.0

Figure 34 Conducted emissions at 230 V AC-line and 3 W load – greater than 16 dB margin



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.4740	N	43.1	N	16.6	N	33.5	46.4	56.4
0.5760	N	43.2	N	20.8	N	35.0	46.0	56.0
1.0920	N	44.5	N	19.9	N	35.1	46.0	56.0
2.0940	N	42.0	N	22.0	N	35.8	46.0	56.0

Figure 35 Conducted emissions at 230 V AC-neutral and 3 W load – greater than 20 dB margin

11.18 ESD immunity (EN 61000-4-2)

This system was subjected to a ±8 kV ESD test according to EN 61000-4-2 for both contact and air discharge. A test failure was defined as non-recoverable.

- Air discharge: pass ±8 kV; contact discharge: pass ± 8 kV.

Table 7 System ESD test result

Description	ESD test	Level	Number of strikes		Test result
			$+V_{OUT}$	$-V_{OUT}$	
115 V AC, 3 W (5 V, 8.3 Ω)	Contact	+8 kV	10	10	Pass
		-8 kV	10	10	Pass
	Air	+8 kV	10	10	Pass
		-8 kV	10	10	Pass
230 V AC, 3 W (5 V, 8.3 Ω)	Contact	+8 kV	10	10	Pass
		-8 kV	10	10	Pass
	Air	+8 kV	10	10	Pass
		-8 kV	10	10	Pass

11.19 Surge immunity (EN 61000-4-5)

This system was subjected to a surge immunity test (±2 kV DM and ±4 kV CM) according to EN 61000-4-5. A test failure was defined as a non-recoverable.

- DM: pass ±2 kV[1]; CM: pass ±4 kV[1].

Table 8 System surge immunity test result

Description	Test	Level		Number of strikes				Test result
				0°	90°	180°	270°	
115 V AC, 3 W (5 V, 8.3 Ω)	DM	+2 kV	L → N	3	3	3	3	Pass[1]
		-2 kV	L → N	3	3	3	3	Pass[1]
	CM	+4 kV	L → G	3	3	3	3	Pass[1]
		+4 kV	N → G	3	3	3	3	Pass[1]
		-4 kV	L → G	3	3	3	3	Pass[1]
		-4 kV	N → G	3	3	3	3	Pass[1]
230 V AC, 3 W (5 V, 8.3 Ω)	DM	+2 kV	L → N	3	3	3	3	Pass[1]
		-2 kV	L → N	3	3	3	3	Pass[1]
	CM	+4 kV	L → G	3	3	3	3	Pass[1]
		+4 kV	N → G	3	3	3	3	Pass[1]
		-4 kV	L → G	3	3	3	3	Pass[1]
		-4 kV	N → G	3	3	3	3	Pass[1]

[1] 1. Change F1 to 36911600000 (300 V, 1.6 A time-lag fuse).
2. Change VAR to B72207S2301K101 (300 V, 0.25 W varistor).
3. Disable line OVP by clamping V_{IN} pin voltage less than 2.75 V (add 2.4 V Zener diode at V_{IN} pin to GND pin).

12 Appendix A: Transformer design and spreadsheet [3]

Design procedure for FF flyback converter using CoolSET™ 5xRxxxxAG/BZS (version 1.0)

Project	**ICE5AR4770AG**
Application	**85 ~ 264 V AC and 3 W (5 V, 0.6 A) single-output, isolated flyback**
CoolSET™	**ICE5AR4770AG**
Date	**18 June 2018**
Revision	**0.2**

Enter design variables in orange-colored cells

Read design results in green-colored cells

Equation numbers are according to the Design Guide.

Select component values based on standard values available.

Voltage/current rating does not include design margin, voltage spikes and transient currents.

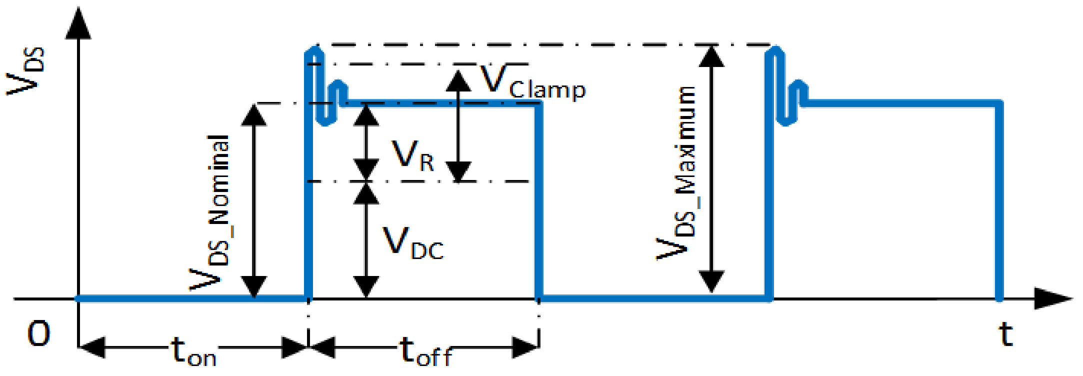
In "Output regulation", only fill in either isolated or non-isolated, whichever is applicable.

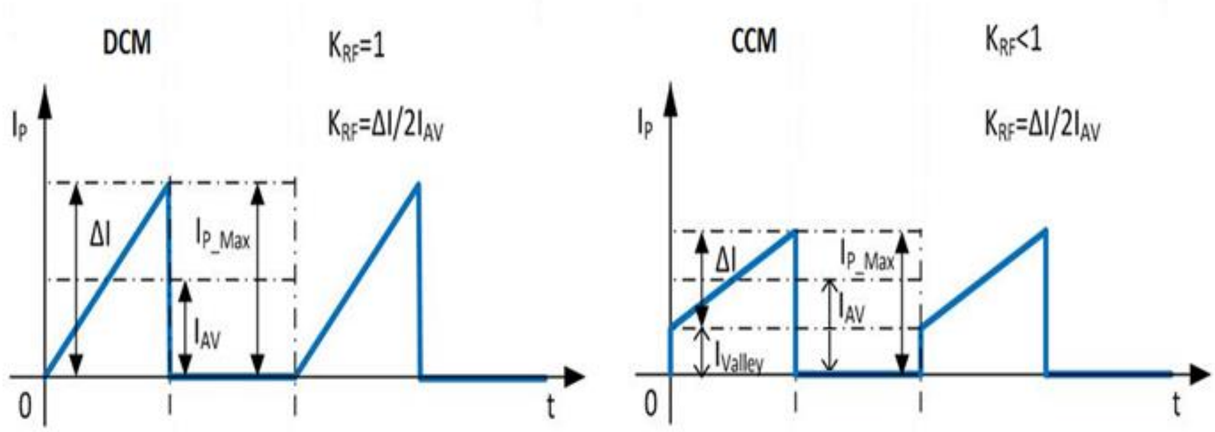
	Description	Eq. #	Parameter	Unit	Value
Input, output, CoolSET™ specs					
Line input					
Input	Minimum AC input voltage		$V\,AC_{Min}$	[V]	85
Input	Maximum AC input voltage		$V\,AC_{Max}$	[V]	264
Input	Line frequency		f_{AC}	[Hz]	60
Input	Bus capacitor DC ripple voltage		$V\,DC_{Ripple}$	[V]	27
Output 1 specs					
Input	Output voltage 1		V_{Out1}	[V]	5
Input	Output current 1		I_{Out1}	[A]	0.6
Input	Forward voltage of output diode 1		V_{FOut1}	[V]	0.6
Input	Output ripple voltage 1		$V_{OutRipple1}$	[V]	0.1
Result	Output power 1	Eq. 001	P_{Out1}	[W]	3
Auxiliary					
Input	V_{CC} voltage		V_{Vcc}	[V]	15
Input	Forward voltage of V_{CC} diode (D2)		$V_{F\,Vcc}$	[V]	0.6
Power					
Input	Efficiency		η		0.8
Result	Nominal output power	Eq. 003	P_{OutNom}	[W]	3.00
Input	Maximum output power for over-load protection		P_{OUT_Max}	[W]	3.3
Result	Maximum input power for over-load protection	Eq. 006	P_{InMax}	[W]	4.13
Input	Minimum output power		P_{OUT_Min}	[W]	0.3
Controller/CoolSET™					
	CoolSET™ -				ICE5AR4770AG
Input	Switching frequency		f_S	[Hz]	100000
Input	Targeted max. drain source voltage		V_{DSMax}	[V]	600
Input	Max. ambient temperature		T_{amax}	[°C]	50
Diode bridge and input capacitor					
Diode bridge					
Input	Power factor		cosφ		0.6
Result	Maximum AC input current	Eq. 007	I_{ACRMS}	[A]	0.081
Result	Peak voltage at $V\,AC_{Max}$	Eq. 008	$V\,DC_{MaxPk}$	[V]	373.35
Input capacitor					
Result	Peak voltage at $V\,AC_{Min}$	Eq. 009	$V\,DC_{MinPk}$	[V]	120.21
Result	Selected minimum DC input voltage	Eq. 010	$V\,DC_{MinSet}$	[V]	93.21
Result	Discharging time at each half-line cycle	Eq. 011	T_D	[ms]	6.52
Result	Required energy at discharging time of input capacitor	Eq. 012	W_{In}	[Ws]	0.03
Result	Calculated input capacitor	Eq. 013	C_{INCal}	[µF]	9.34
Input	Select input capacitor (C1)		C_{in}	[µF]	9.4
Result	Calculated minimum DC input voltage	Eq. 015	$V\,DC_{Min}$	[V]	93.42

Appendix A: Transformer design and spreadsheet [3]

Transformer design

Drain voltage and current waveform





Primary inductance and winding currents

Input	Reflection voltage		V_{RSET}	[V]	70.56
Result	Maximum duty cycle	Eq. 016	D_{Max}		0.43
Input	Select current ripple factor		K_{RF}		1
Result	Primary inductance	Eq. 017	L_P	[H]	1.96E-03
Result	Primary turn-on average current	Eq. 018	I_{AV}	[A]	0.10
Result	Primary peak-to-peak current	Eq. 019	ΔI	[A]	0.21
Result	Primary peak current	Eq. 020	I_{PMax}	[A]	0.21
Result	Primary valley current	Eq. 021	I_{Valley}	[A]	0.00
Result	Primary RMS current	Eq. 022	I_{PRMS}	[A]	0.078

Select core type

Input	Select core type				1
Result	Core type				EE13/7/4
Result	Core material				TP4A (TDG)
Result	Maximum flux density		B_{Max}	[T]	0.26
Result	Cross-sectional area		A_e	[mm²]	12.4
Result	Bobbin width		BW	[mm]	7.49
Result	Winding cross-section		A_N	[mm²]	13.48
Result	Average length of turn		l_N	[mm]	27.4

Winding calculation

Result	Calculated minimum number of primary turns	Eq. 023	N_{PCal}	Turns	124.68
Input	Select number of primary turns		N_P	Turns	126
Result	Calculated number of secondary 1 turns	Eq. 024	N_{S1Cal}	Turns	10.00
Input	Select number of secondary 1 turns		N_{S1}	Turns	10
Result	Calculated number of auxiliary turns	Eq. 026	N_{VccCal}	Turns	27.86
Input	Select number of auxiliary turns		N_{Vcc}	Turns	28

Appendix A: Transformer design and spreadsheet [3]

Result	Calculated V_{CC} voltage	Eq. 027	V_{VccCal}	[V]	15.08
Post calculation					
Result	Primary to secondary 1 turns ratio	Eq. 028	N_{PS1}		12.60
Result	Post calculated reflected voltage	Eq. 030	V_{RPost}	[V]	70.56
Result	Post calculated maximum duty cycle	Eq. 031	$D_{MaxPost}$		0.43
Result	Duty cycle prime	Eq. 032	D_{Max}'		0.57
Result	Actual flux density	Eq. 033	B_{MaxAct}	[T]	0.257
Result	Maximum DC input voltage for CCM operation	Eq. 034	$V\ DC_{maxCCM}$	[V]	93.42
Transformer winding design					
Input	Margin according to safety standard		M	[mm]	0
Input	Copper space factor		f_{Cu}		0.4
Result	Effective bobbin window	Eq. 035	BW_E	[mm]	7.5
Result	Effective winding cross-section	Eq. 036	A_{Ne}	[mm²]	13.5
Input	Primary winding area factor		AF_{NP}		0.50
Input	Secondary 1 winding area factor		AF_{NS1}		0.45
Input	Auxiliary winding area factor		AF_{NVcc}		0.05
Primary winding					
Result	Calculated wire copper cross-sectional area	Eq. 037	A_{PCal}	[mm²]	0.0214
Result	Calculated maximum wire size	Eq. 038	AWG_{PCal}		34
Input	Select wire size		AWG_P		35
Input	Select number of parallel wire		nw_P		1
Result	Wire copper diameter	Eq. 039	d_P	[mm]	0.14
Result	Wire copper cross-sectional area	Eq. 040	A_P	[mm²]	0.0163
Result	Wire current density	Eq. 041	S_P	[A/mm²]	4.77
Input	Insulation thickness		INS_P	[mm]	0.01
Result	Turns per layer	Eq. 042	NL_P	Turns/layer	45
Result	Number of layers	Eq. 043	Ln_P	Layers	3
Secondary 1 winding					
Result	Calculated wire copper cross-sectional area	Eq. 044	A_{NS1Cal}	[mm²]	0.2426
Result	Calculated maximum wire size	Eq. 045	AWG_{S1Cal}		23
Input	Select wire size		AWG_{S1}		25
Input	Select number of parallel wire		nw_{S1}		1
Result	Wire copper diameter	Eq. 046	d_{S1}	[mm]	0.4572
Result	Wire copper cross-sectional area	Eq. 047	A_{S1}	[mm²]	0.1642
Result	Peak current	Eq. 048	I_{S1Max}	[A]	2.5859
Result	RMS current	Eq. 049	I_{S1RMS}	[A]	1.1269
Result	Wire current density	Eq. 050	S_{S1}	[A/mm²]	6.86
Input	Insulation thickness		INS_{S1}	[mm]	0.01
Result	Turns per layer	Eq. 051	NL_{S1}	Turns/layer	10
Result	Number of layers	Eq. 052	Ln_{S1}	Layers	1
RCD clamper and CS resistor					
RCD clamper circuit					
Input	Leakage inductance percentage		$L_{LK\%}$	[%]	0.36
Result	Leakage inductance	Eq. 062	L_{LK}	[H]	7.05E-06
Result	Clamping voltage	Eq. 063	V_{Clamp}	[V]	156.09
Result	Calculated clamping capacitor	Eq. 064	$C_{ClampCal}$	[nF]	0.01
Input	Select clamping capacitor value (C2)		C_{clamp}	[nF]	1
Result	Calculated clamping resistor	Eq. 065	$R_{clampCal}$	[kΩ]	3123.9
Input	Select clamping resistor value (R4)		R_{clamp}	[kΩ]	3000
CS resistor					
Input	CS threshold value from datasheet		V_{CS_N}	[V]	0.8
Result	Calculated CS resistor (R8A, R8B)	Eq. 066	R_{sense}	[Ω]	3.90

Ouput rectifier

Secondary 1 output rectifier

Result	Diode reverse voltage	Eq. 067	$V_{RDiode1}$	[V]	34.63
Result	Diode RMS current		I_{S1RMS}	[A]	1.13
Input	Max. voltage undershoot at output capacitor		ΔV_{Out1}	[V]	0.15
Input	Number of clock periods		n_{cp1}		20
Result	Output capacitor ripple current	Eq. 068	$I_{Ripple1}$	[A]	0.95
Result	Calculated minimum output capacitor	Eq. 069	$C_{Out1Cal}$	[µF]	800
Input	Select output capacitor value (C152)		C_{Out1}	[µF]	820
Input	ESR (Z_{max}) value from datasheet at 100 kHz		R_{ESR1}	[Ω]	0.008
Input	Number of parallel capacitors		nc_{COut1}		1
Result	Zero frequency of output capacitor	Eq. 070	f_{ZCOut1}	[kHz]	24.26
Result	First-stage ripple voltage	Eq. 071	$V_{Ripple1}$	[V]	0.020687
Input	Select LC filter inductor value (L151)		L_{out1}	[µH]	2.2
Result	Calculated LC filter capacitor	Eq. 072	C_{LCCal1}	[µF]	19.6
Input	Select LC filter capacitor value (C153)		C_{LC1}	[µF]	20
Result	LC filter frequency	Eq. 073	f_{LC1}	[kHz]	23.99
Result	Second-stage ripple voltage	Eq. 074	$V_{2ndRipple1}$	[mV]	1.13
V_{CC} diode and capacitor					
Result	Auxiliary diode reverse voltage (D2)	Eq. 083	$V_{RDiodeVCC}$	[V]	98.05
Input	Soft-start time from datasheet		t_{ss}	[ms]	12
Input	$I_{VCC,Charge3}$ from datasheet		$I_{VCC\_Charge3}$	[mA]	3
Input	V_{CC} on-threshold		V_{VCC_ON}	[V]	16
Input	V_{CC} off-threshold		V_{VCC_OFF}	[V]	10
Result	Calculated V_{CC} capacitor	Eq. 084	C_{VCCCal}	[µF]	6.00
Input	Select V_{CC} capacitor (C3)		C_{VCC}	[µF]	4.7
Input	V_{CC} short threshold from datasheet		V_{VCC_SCP}	[V]	1.1
Input	$I_{VCC\_Charge1}$ from datasheet		$I_{VCC\_Charge1}$	[mA]	0.2
Result	Start-up time	Eq. 085	$t_{StartUp}$	[ms]	49.193
Calculation of losses					
Input diode bridge					
Input	Diode bridge forward voltage		V_{FBR}	[V]	1
Result	Diode bridge power loss	Eq. 086	P_{DIN}	[W]	0.16
Transformer copper					
Result	Primary winding copper resistance	Eq. 087	R_{PCu}	[mΩ]	3642.43
Result	Secondary 1 winding copper resistance	Eq. 088	R_{S1Cu}	[mΩ]	28.71
Result	Primary winding copper loss	Eq. 090	P_{PCu}	[mW]	22.01
Result	Secondary 1 winding copper loss	Eq. 091	P_{S1Cu}	[mW]	36.46
Result	Total transformer copper loss	Eq. 093	P_{Cu}	[W]	0.0585
Output rectifier diode					
Result	Secondary 1 diode loss	Eq. 094	P_{Diode1}	[W]	0.68
RCD clamper circuit					
Result	RCD clamper loss	Eq. 096	$P_{Clamper}$	[W]	0.02
CS resistor					
Result	CS resistor loss	Eq. 097	P_{CS}	[W]	0.02
MOSFET					
Input	R_{DSON} from datasheet		R_{DSON} at T_J = 125°C	[Ω]	8.73
Input	Co(er) from datasheet		$C_{o(er)}$	[pF]	3.4
Input	External drain-to-source capacitance		C_{DS}	[pF]	0
Result	Switch-on loss at minimum AC input voltage	Eq. 098	$P_{SONMinAC}$	[W]	0.0046
Result	Conduction loss at minimum AC input voltage	Eq. 099	$P_{condMinAC}$	[W]	0.0527
Result	Total MOSFET loss at minimum AC input voltage	Eq. 100	$P_{MOSMinAC}$	[W]	0.0573
Result	Switch-on loss at maximum AC input voltage	Eq. 101	$P_{SONMaxAC}$	[W]	0.0335
Result	Conduction loss at maximum AC input voltage	Eq. 102	$P_{condMaxAC}$	[W]	0.0132
Result	Total MOSFET loss at maximum AC input voltage	Eq. 103	$P_{MOSMaxAC}$	[W]	0.0467
Result	Total MOSFET loss (from minimum or maximum AC)		P_{MOS}	[W]	0.0573

Appendix A: Transformer design and spreadsheet [3]

Controller

Input	Controller current consumption		I_{VCC_Normal}	[mA]	0.9
Result	Controller loss	Eq. 104	P_{Ctrl}	[W]	0.0136

Efficiency after losses

Result	Total power loss	Eq. 105	P_{Losses}	[W]	1.01
Result	Post calculated efficiency	Eq. 106	η_{Post}	[%]	76.52

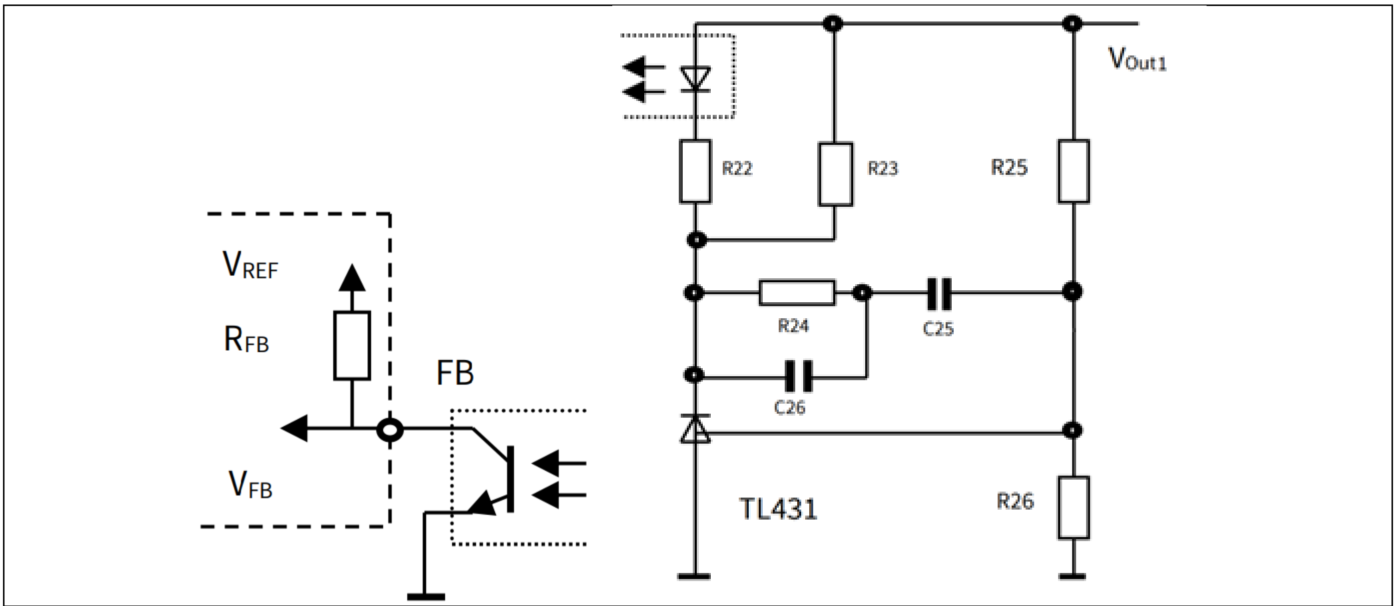
CoolSET™/MOSFET temperature

Input	Enter thermal resistance junction-ambient (include copper pour)		R_{thJA_As}	[°K/W]	104.0
Result	Temperature rise	Eq. 107	ΔT	[°K]	6.0
Result	Junction temperature at T_{amax}	Eq. 108	T_{jmax}	[°C]	56.0

Line OVP

Input	Select AC input LOVP		V_{OVP_AC}	[V AC]	275
Input	High side DC input voltage divider resistor (R3A, R3B, R3C)		R_{l1}	[MΩ]	16
Input	Controller LOVP threshold		V_{VIN_LOVP}	[V]	2.85
Result	Low side DC input voltage divider resistor	Eq 109	R_{l2Cal}	[kΩ]	121.07
Input	Select low-side DC input voltage divider resistor (R7)		R_{l2}	[kΩ]	121
Result	Post calculated LOVP	Eq 110	V_{OVP_ACPost}	[V_{AC}]	275.16

Output regulation (isolated using TL431 and optocoupler)
Isolated FB circuit



Output regulation

Input	TL431 reference voltage		V_{REF_TL}	[V]	2.5
Input	Current for voltage divider resistor R26		I_{R26}	[mA]	0.25
Result	Calculated voltage divider resistor	Eq. 111	$R26_{Cal}$	[kΩ]	10
Input	Select voltage divider resistor value		R26	[kΩ]	10
Result	Calculated voltage divider resistor	Eq. 112	$R25_{Cal}$	[kΩ]	10.00
Input	Select voltage divider resistor value		R25	[kΩ]	10.0

Optocoupler and TL431 bias

Input	Current Transfer Ratio (CTR)		G_C	[%]	100
Input	Optocoupler diode forward voltage		V_{FOpto}	[V]	1.25
Input	Maximum current for optocoupler diode		I_{Fmax}	[mA]	10
Input	Minimum current for TL431		I_{KAmin}	[mA]	1
Result	Calculated minimum optocoupler bias resistance	Eq. 114	$R22_{Cal}$	[kΩ]	0.1250
Input	Select optocoupler bias resistor		R22	[kΩ]	0.12
Input	FB pull-up reference voltage V_{REF} from datasheet		V_{REF}	[V]	3.3
Input	V_{FB_OLP} from datasheet		V_{FB_OLP}	[V]	2.75
Input	R_{FB} from datasheet		R_{FB}	[kΩ]	15
Result	Calculated maximum TL431 bias resistance	Eq. 115	$R23_{Cal}$	[kΩ]	1.25
Input	Selected TL431 bias resistor		R23	[kΩ]	1.2

Appendix A: Transformer design and spreadsheet [3]

Regulation loop

Result	FB transfer characteristic	Eq. 116	K_{FB}		125.00
Result	Gain of FB transfer characteristic	Eq. 117	G_{FB}	[db]	41.94
Result	Voltage divider transfer characteristic	Eq. 118	K_{VD}		0.500000
Result	Gain of voltage divider transfer characteristic	Eq. 119	G_{VD}	[db]	-6.02
Result	Resistance at maximum load pole	Eq. 120	R_{LH}	[Ω]	7.58
Result	Resistance at minimum load pole	Eq. 121	R_{LL}	[Ω]	83.33
Result	Poles of power stage at maximum load pole	Eq. 122	f_{OH}	[Hz]	51.24
Result	Poles of power stage at minimum load pole	Eq. 123	f_{OL}	[Hz]	4.66
Result	Zero frequency of the compensation network	Eq. 124	f_{OM}	[Hz]	15.45
Input	Zero dB crossover frequency		fg	[kHz]	3
Input	PWM-OP gain from datasheet		A_V		2.03
Result	Transient impedance	Eq. 117	Z_{PWM}	[V/A]	9.9
Result	Power stage at crossover frequency	Eq. 118	$\lvert F_{PWR}(fg)\rvert$		0.042
Result	Gain of power stage at crossover frequency	Eq. 119	$G_{PWR}(fg)$	[db]	-27.52
Result	Gain of the regulation loop at fg	Eq. 120	Gs(ω)	[db]	8.396
Result	Separated components of the regulator	Eq. 121	Gr(ω)	[db]	-8.396
Result	Calculated resistance value of compensation network	Eq. 122	$R24_{Cal}$	[kΩ]	1.90
Input	Select resistor value of compensation network		R24	[kΩ]	10
Result	Calculated capacitance value of compensation network	Eq. 123	$C26_{Cal}$	[nF]	5.305
Input	Select capacitor value of compensation network		C26	[nF]	0.068
Result	Calculated capacitance value of compensation network	Eq. 124	$C25_{Cal}$	[nF]	1030.10
Input	Select capacitor value of compensation network		C25	[nF]	100

Output regulation (non-isolated)

Final design

Electrical

Minimum AC voltage			[V]	85
Maximum AC voltage			[V]	264
Maximum input current			[A]	0.05
Minimum DC voltage			[V]	93
Maximum DC voltage			[V]	373
Maximum output power			[W]	3.3
Output voltage 1			[V]	5.0
Output ripple voltage 1			[mV]	1.1
Transformer peak current			[A]	0.21
Maximum duty cycle				0.43
Reflected voltage			[V]	71
Copper losses			[W]	0.06
MOSFET losses			[W]	0.06
Sum losses			[W]	1.01
Efficiency			[%]	76.52

Transformer

Core type				EE13/7/4
Core material				TP4A(TDG)
Effective core area			[mm^2]	12.4
Maximum flux density			[mT]	257
Inductance			[µH]	1959
Margin			[mm]	0
Primary turns			Turns	126
Primary copper wire size			AWG	35
Number of primary copper wires in parallel				1
Primary layers			Layer	3
Secondary 1 turns (N_{S1})			Turns	10
Secondary 1 copper wire size			AWG	25
Number of secondary 1 copper wires in parallel				1
Secondary 1 layers			Layer	1
Auxiliary turns			Turns	28
Leakage inductance			[µH]	7.1

Appendix A: Transformer design and spreadsheet [3]

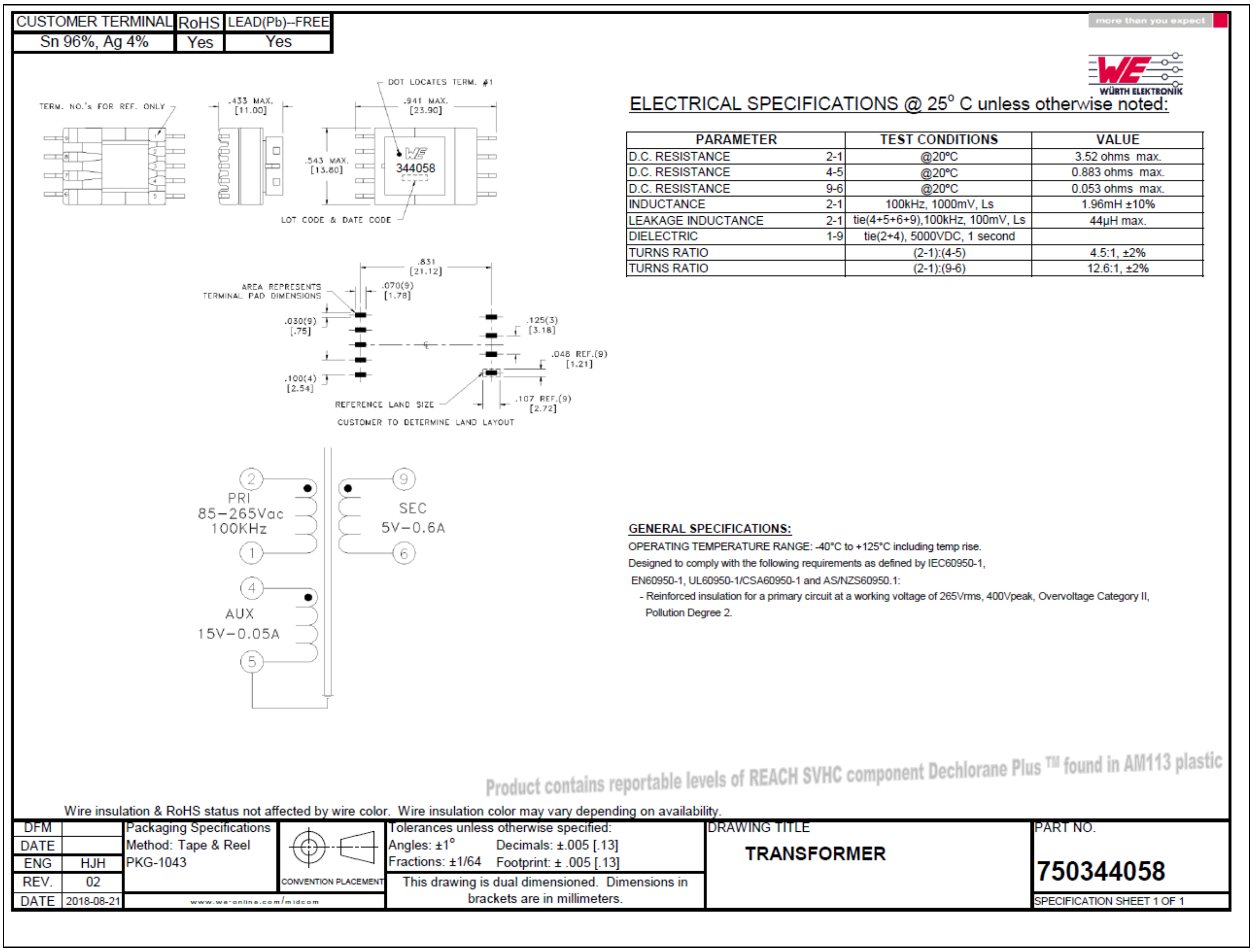
Components

Input capacitor (C1)			[µF]	9.4
Secondary 1 output capacitor (C152)			[µF]	820.0
Secondary 1 output capacitor in parallel				1.0
Secondary 1 LC filter inductor (L151)			[µH]	2.2
Secondary 1 LC filter capacitor (C153)			[µF]	10.0
V_{CC} capacitor (C3)			[µF]	4.7
Sense resistor (R8A, R8B)			[Ω]	3.90
Clamping resistor (R4)			[kΩ]	3000.0
Clamping capacitor (C2)			[nF]	1
High-side DC input voltage divider resistor (R3A, R3B, R3C)			[MΩ]	16
Low-side DC input voltage divider resistor (R7)			[kΩ]	121

Regulation components (isolated using TL431 and optocoupler)

Voltage divider		R26	[kΩ]	10.0
Voltage divider (V_{OUT1} sense)		R25	[kΩ]	10.0
Optocoupler bias resistor		R22	[kΩ]	0.12
TL431 bias resistor		R23	[kΩ]	1.2
Compensation network resistor		R24	[kΩ]	10.0
Compensation network capacitor		C26	[nF]	0.07
Compensation network capacitor		C25	[nF]	100.0

13 Appendix B: WE transformer specification



CUSTOMER TERMINAL	RoHS	LEAD(Pb)–FREE
Sn 96%, Ag 4%	Yes	Yes

ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	2-1	@20°C	3.52 ohms max.
D.C. RESISTANCE	4-5	@20°C	0.883 ohms max.
D.C. RESISTANCE	9-6	@20°C	0.053 ohms max.
INDUCTANCE	2-1	100kHz, 1000mV, Ls	1.96mH ±10%
LEAKAGE INDUCTANCE	2-1	tie(4+5+6+9),100kHz, 100mV, Ls	44µH max.
DIELECTRIC	1-9	tie(2+4), 5000VDC, 1 second	
TURNS RATIO		(2-1):(4-5)	4.5:1, ±2%
TURNS RATIO		(2-1):(9-6)	12.6:1, ±2%

GENERAL SPECIFICATIONS:
OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.
Designed to comply with the following requirements as defined by IEC60950-1, EN60950-1, UL60950-1/CSA60950-1 and AS/NZS60950.1:
- Reinforced insulation for a primary circuit at a working voltage of 265Vrms, 400Vpeak, Overvoltage Category II, Pollution Degree 2.

Product contains reportable levels of REACH SVHC component Dechlorane Plus ™ found in AM113 plastic

Wire insulation & RoHS status not affected by wire color. Wire insulation color may vary depending on availability.

DFM		Packaging Specifications	CONVENTION PLACEMENT	Tolerances unless otherwise specified:	DRAWING TITLE	PART NO.
DATE		Method: Tape & Reel		Angles: ±1° Decimals: ±.005 [.13]	TRANSFORMER	750344058
ENG	HJH	PKG-1043		Fractions: ±1/64 Footprint: ± .005 [.13]		
REV.	02			This drawing is dual dimensioned. Dimensions in brackets are in millimeters.		
DATE	2018-08-21	www.we-online.com/midcom				SPECIFICATION SHEET 1 OF 1

Figure 36 WE transformer specification

14 References

[1] ICE5AR4770AG datasheet, Infineon Technologies AG

[2] 5th-Generation Fixed-Frequency Design Guide

[3] CalculationTool_ICE5xSAG_ICE5xRxxxxAG

[4] AN-REF-3W-IOT-COOLSETM

Revision history

Document version	Date of release	Description of changes
V1.0	28 August 2018	First release

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2018-08-28

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AN_1807_PL83_1808_054829

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург, Промышленная ул, дом № 19, литера Н, помещение 100-Н Офис 331