

## N-channel 800 V, 0.470 $\Omega$ typ., 9 A MDmesh™ K5 Power MOSFETs in a TO-220FP and TO-220FP ultra narrow leads

Datasheet - production data

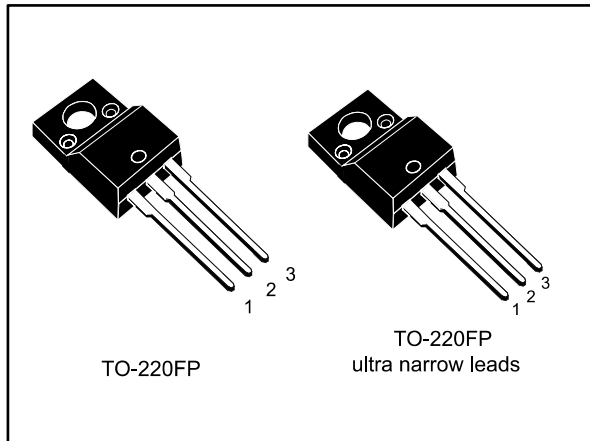


Figure 1: Internal schematic diagram

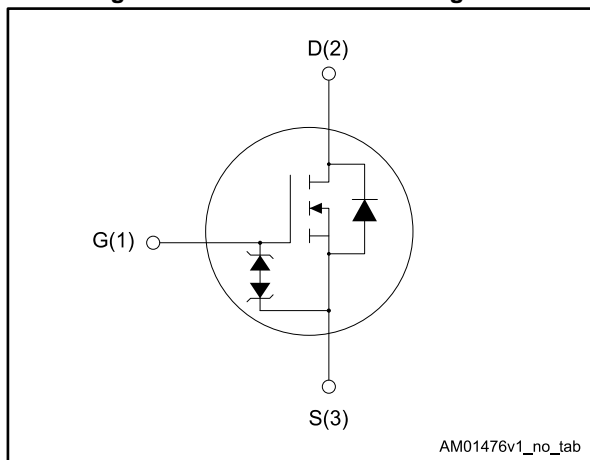


Table 1: Device summary

Order code	Marking	Package	Packing
STF10N80K5	10N80K5	TO-220FP	Tube
STFU10N80K5		TO-220FP ultra narrow leads	

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STF10N80K5	800 V	0.600 $\Omega$	9 A	30 W
STFU10N80K5				

- Industry's lowest R<sub>DS(on)</sub> x area
- Industry's best figure of merit (FoM)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	9	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	6	A
$I_{DM}^{(2)}$	Drain current pulsed	36	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	30	W
$I_{AR}$	Max. current during repetitive or single pulse avalanche (pulse width limited by $T_{Jmax.}$ )	3	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AS}$ , $V_{DD} = 50\text{ V}$ )	130	mJ
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ ; $T_C = 25\text{ }^\circ\text{C}$ )	2500	V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(4)}$	MOSFET $dv/dt$ ruggedness	50	
$T_j$	Operating junction temperature range	- 55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

**Notes:**

(1)Limited by maximum junction temperature.

(2)Pulse width limited by safe operating area.

(3) $I_{SD} \leq 9\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} \leq V_{(BR)DSS}$

(4) $V_{DS} \leq 640\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	4.2	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	$^\circ\text{C}/\text{W}$

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 4: On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	800			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 800\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 800\text{ V}$ $T_C = 125\text{ °C}$ <sup>(1)</sup>			50	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 4.5\text{ A}$		0.470	0.600	$\Omega$

**Notes:**

<sup>(1)</sup>Defined by design, no subject to production test.

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	635	-	pF
$C_{oss}$	Output capacitance		-	53	-	pF
$C_{rss}$	Reverse transfer capacitance		-	0.8	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }640\text{ V}$ , $V_{GS} = 0\text{ V}$	-	85	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related				34	-
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 640\text{ V}$ , $I_D = 9\text{ A}$ $V_{GS} = 10\text{ V}$ See <a href="#">Figure 16: "Test circuit for gate charge behavior"</a>	-	22	-	nC
$Q_{gs}$	Gate-source charge		-	5.5	-	nC
$Q_{gd}$	Gate-drain charge		-	13.2	-	nC

**Notes:**

<sup>(1)</sup>Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

<sup>(2)</sup>Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$ , $I_D = 4.5\text{ A}$ , $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ See <a href="#">Figure 15: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 20: "Switching time waveform"</a>	-	14.5	-	ns
$t_r$	Rise time		-	11	-	ns
$t_{d(off)}$	Turn-off delay time		-	35	-	ns
$t_f$	Fall time		-	14	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		36	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 9\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 9\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	370		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , see <a href="#">Figure 17: "Test circuit for inductive load switching and diode recovery times"</a> )	-	4.58		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	25		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 9\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	520		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ see <a href="#">Figure 17: "Test circuit for inductive load switching and diode recovery times"</a>	-	5.88		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	22.5		A

**Notes:**

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ , $I_D = 0\text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

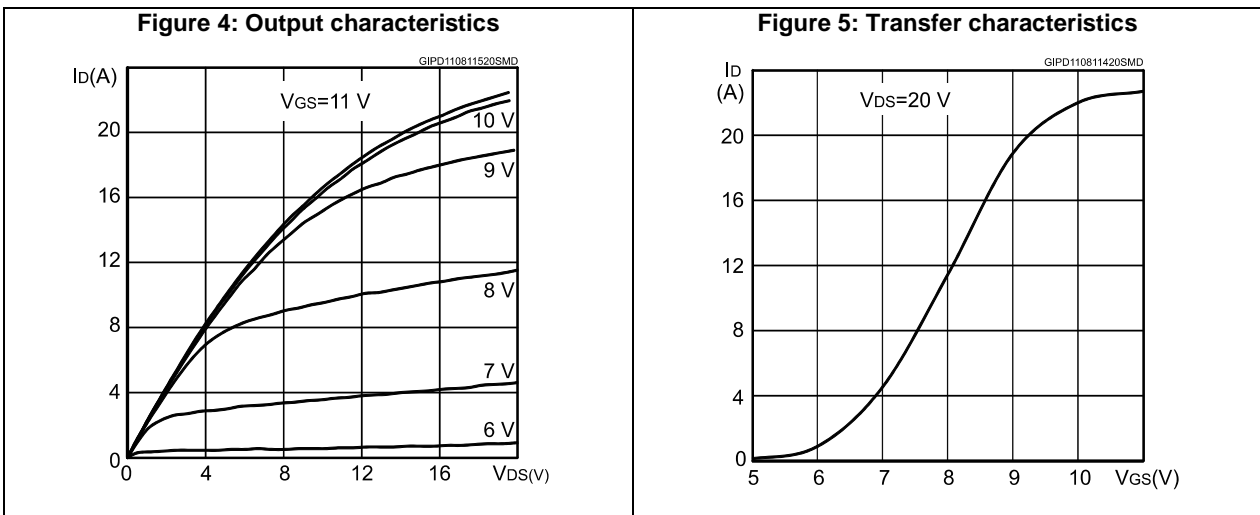
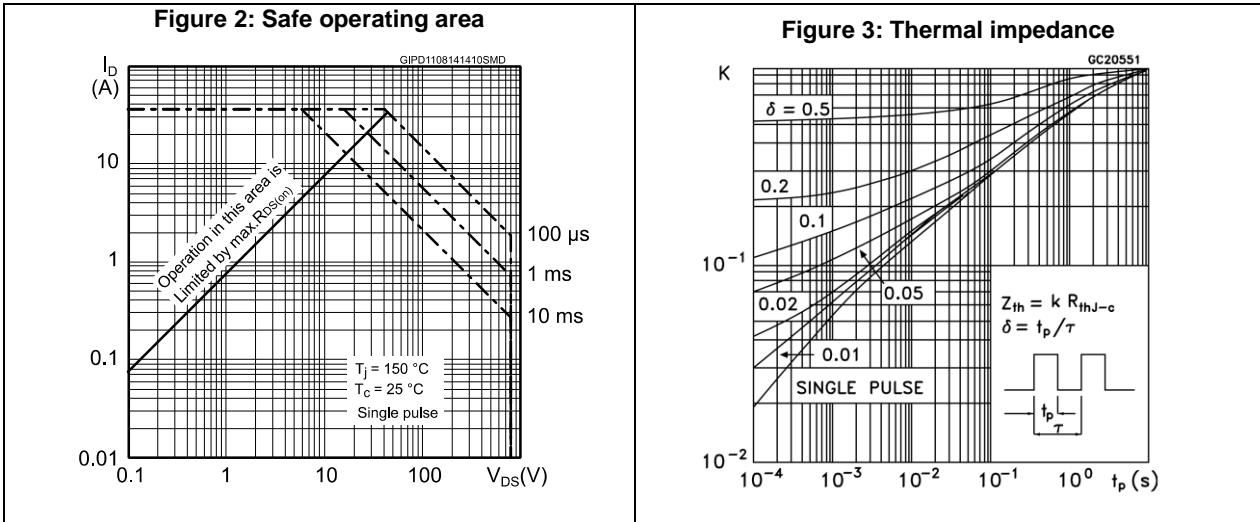


Figure 6: Gate charge vs. gate-source voltage

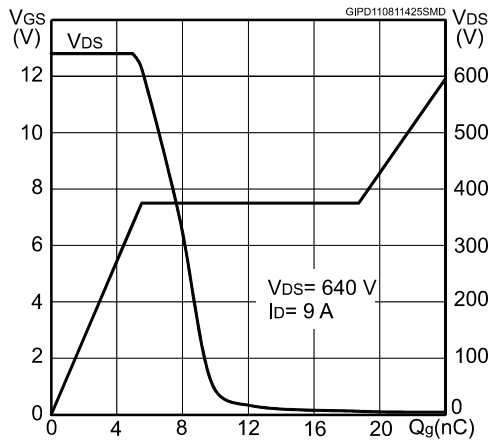


Figure 7: Static drain-source on-resistance

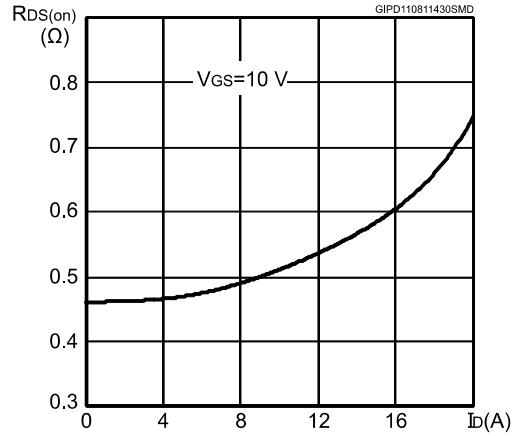


Figure 8: Capacitance variations

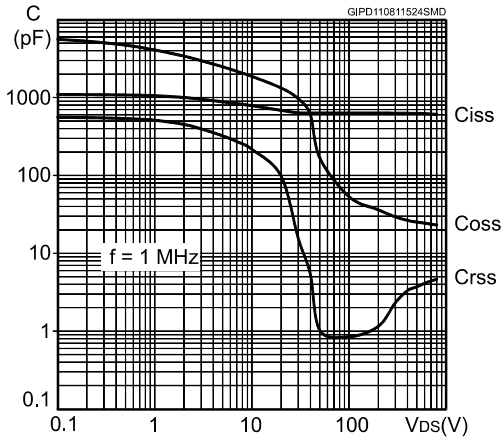


Figure 9: Source-drain diode forward characteristics

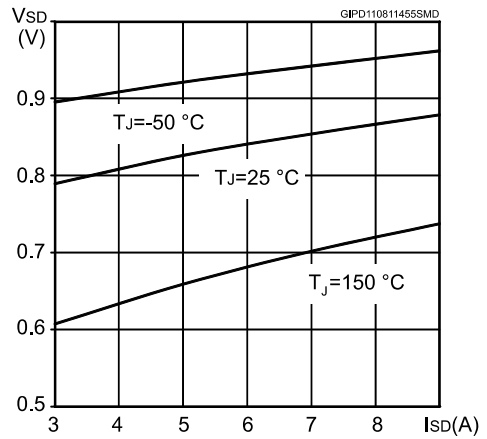


Figure 10: Normalized gate threshold voltage vs. temperature

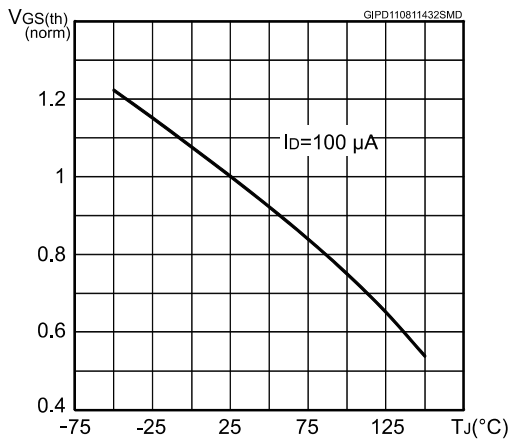


Figure 11: Normalized on-resistance vs. temperature

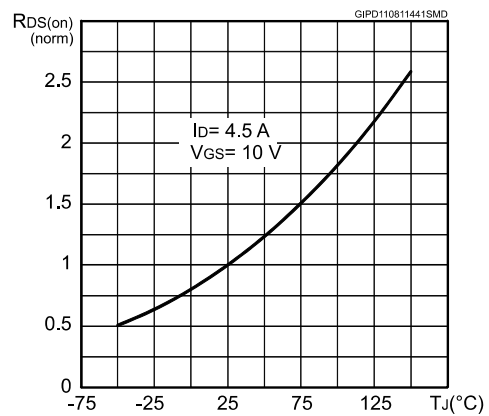


Figure 12: Normalized  $V_{(BR)DSS}$  vs. temperature

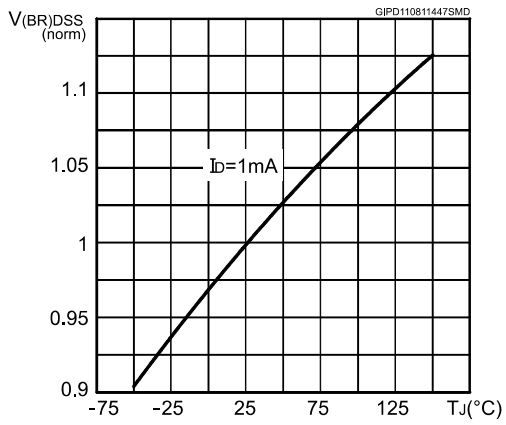


Figure 13: Maximum avalanche energy vs. starting  $T_J$

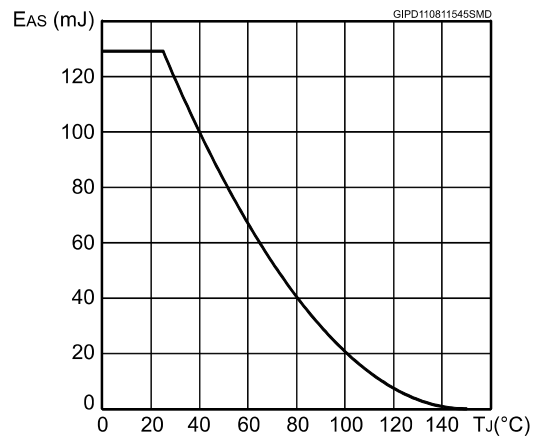
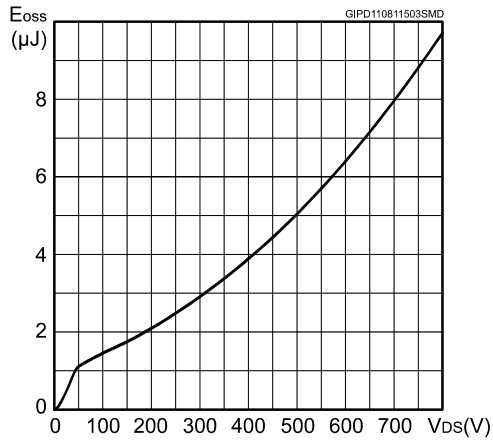


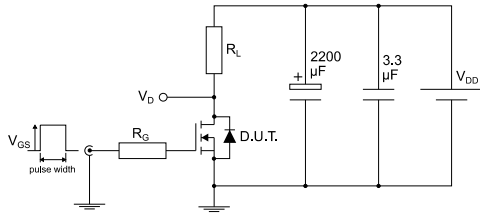
Figure 14: Output capacitance stored energy





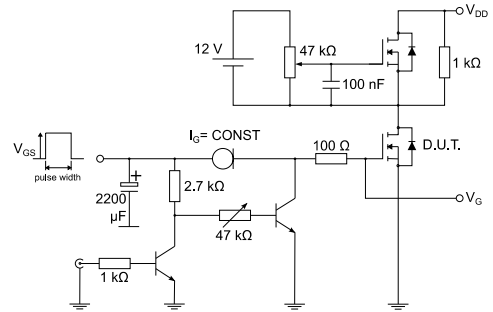
### 3 Test circuits

**Figure 15: Test circuit for resistive load switching times**



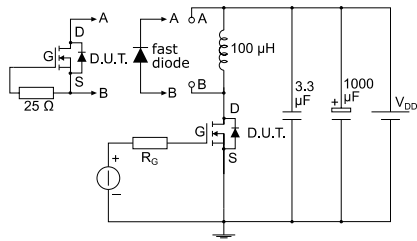
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**Figure 16: Test circuit for gate charge behavior**



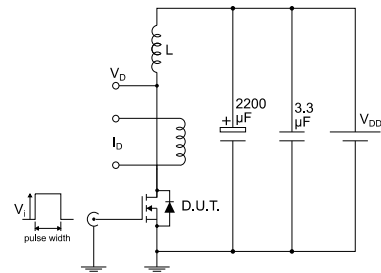
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**Figure 17: Test circuit for inductive load switching and diode recovery times**



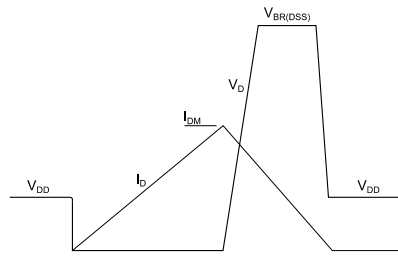
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**Figure 18: Unclamped inductive load test circuit**



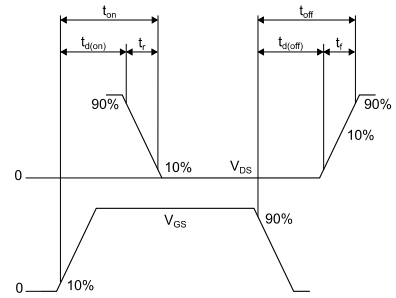
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Figure 19: Unclamped inductive waveform



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Figure 20: Switching time waveform



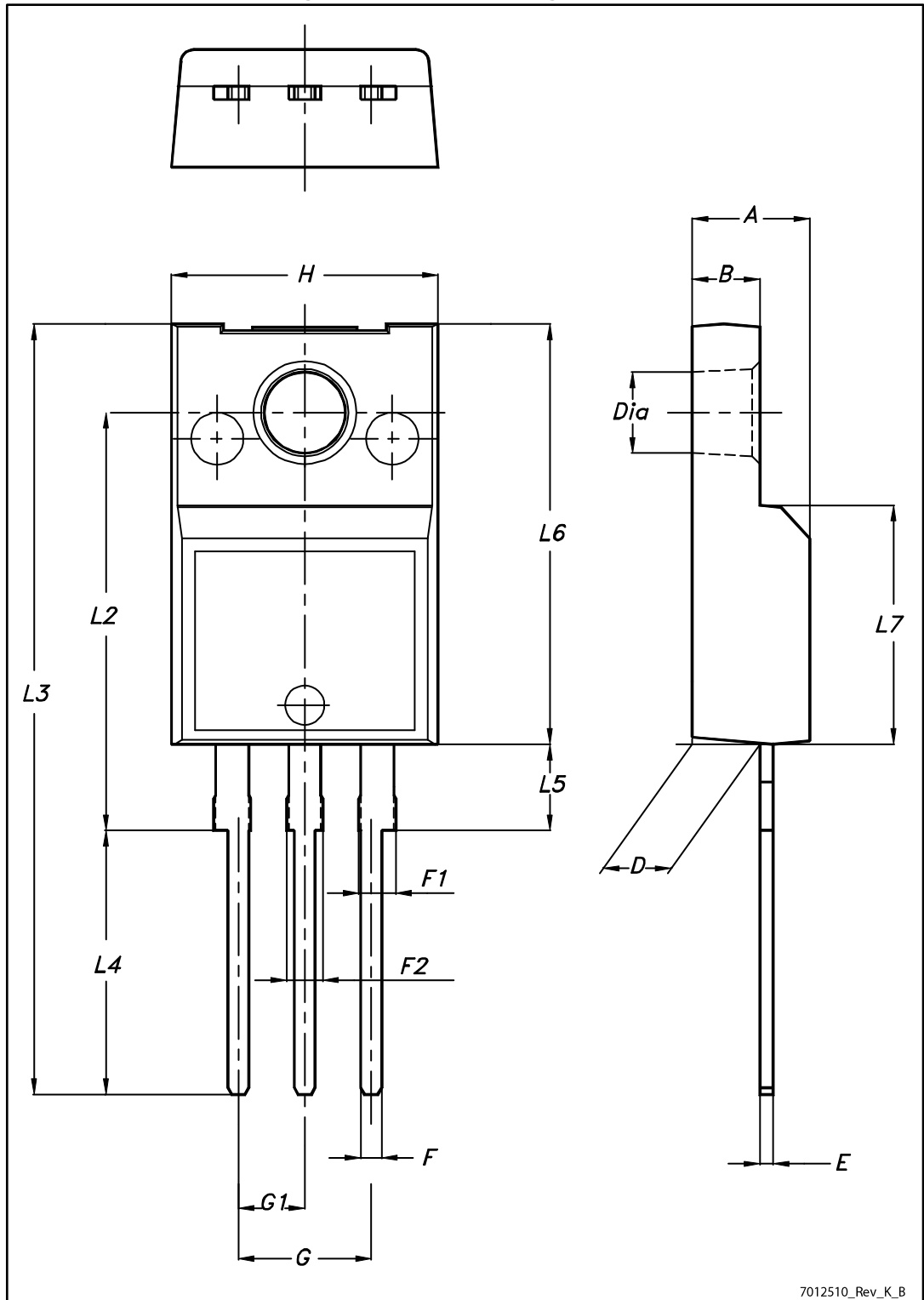
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## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 TO-220FP package information

Figure 21: TO-220FP package outline



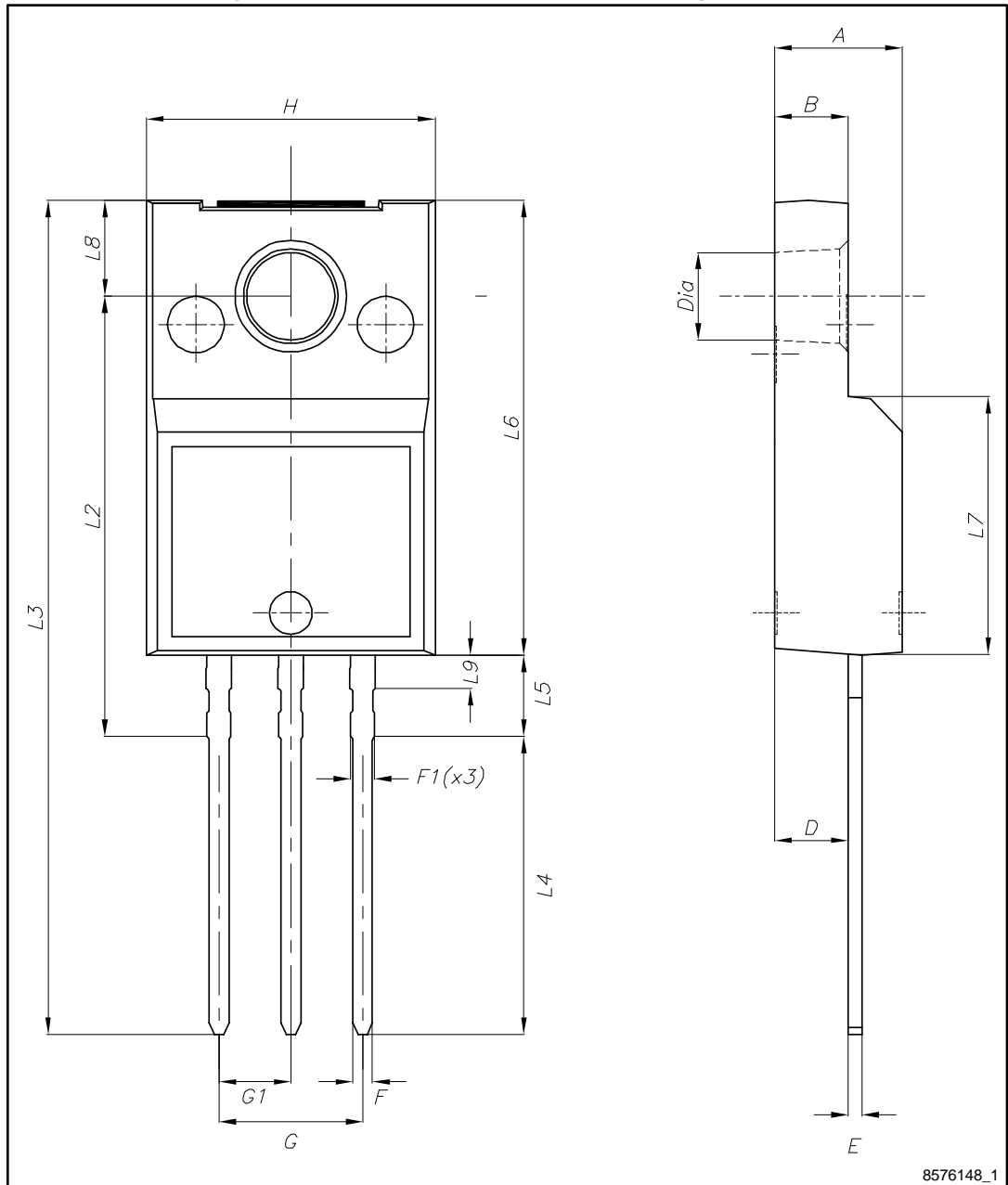
7012510\_Rev\_K\_B

Table 9: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

### 4.2 TO-220FP ultra narrow leads package information

Figure 22: TO-220FP ultra narrow leads package outline



8576148\_1

Table 10: TO-220FP ultra narrow leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.60
F	0.65		0.75
F1	-		0.90
G	4.95		5.20
G1	2.40	2.54	2.70
H	10.00		10.40
L2	15.10		15.90
L3	28.50		30.50
L4	10.20		11.00
L5	2.50		3.10
L6	15.60		16.40
L7	9.00		9.30
L8	3.20		3.60
L9	-		1.30
Dia.	3.00		3.20

## 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
23-Jun-2014	1	First release.
13-Aug-2014	2	-Document status promoted from preliminary to production data. -Inserted <i>Section 3: Electrical characteristics (curves)</i> . -Minor text changes.
17-Sep-2014	3	Updated title, features and description in cover page.
05-Nov-2014	4	Updated <i>Section 3: Electrical characteristics (curves)</i> . Minor text changes.
08-Sep-2016	5	Added the order code STF10N80K5 and the relative <a href="#">Section 4.2: "TO-220FP ultra narrow leads package information"</a> .



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