



**256K x 36, 512K x 18
3.3V Synchronous ZBT™ SRAMs
3.3V I/O, Burst Counter
Flow-Through Outputs**

**IDT71V65703
IDT71V65903**

Features

- ◆ 256K x 36, 512K x 18 memory configurations
- ◆ Supports high performance system speed - 100 MHz (7.5 ns Clock-to-Data Access)
- ◆ ZBT™ Feature - No dead cycles between write and read cycles
- ◆ Internally synchronized output buffer enable eliminates the need to control \overline{OE}
- ◆ Single R/W (READ/WRITE) control pin
- ◆ 4-word burst capability (Interleaved or linear)
- ◆ Individual byte write (\overline{BW}_1 - \overline{BW}_4) control (May tie active)
- ◆ Three chip enables for simple depth expansion
- ◆ 3.3V power supply ($\pm 5\%$)
- ◆ 3.3V ($\pm 5\%$) I/O Supply (V_{DDO})
- ◆ Power down controlled by ZZ input
- ◆ Packaged in a JEDEC standard 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array (fBGA).

Description

The IDT71V65703/5903 are 3.3V high-speed 9,437,184-bit (9 Megabit) synchronous SRAMs organized as 256K x 36 / 512K x 18. They are designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus they have been given the name ZBT™, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock

cycle, and on the next clock cycle the associated data cycle occurs, be it read or write.

The IDT71V65703/5903 contain address, data-in and control signal registers. The outputs are flow-through (no output data register). Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable (\overline{CEN}) pin allows operation of the IDT71V65703/5903 to be suspended as long as necessary. All synchronous inputs are ignored when \overline{CEN} is high and the internal device registers will hold their previous values.

There are three chip enable pins (\overline{CE}_1 , \overline{CE}_2 , \overline{CE}_2) that allow the user to deselect the device when desired. If any one of these three is not asserted when $\overline{ADV}/\overline{LD}$ is low, no new memory operation can be initiated. However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state one cycle after the chip is deselected or a write is initiated.

The IDT71V65703/5903 have an on-chip burst counter. In the burst mode, the IDT71V65703/5903 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the LBO input pin. The LBO pin selects between linear and interleaved burst sequence. The $\overline{ADV}/\overline{LD}$ signal is used to load a new external address ($\overline{ADV}/\overline{LD} = \text{LOW}$) or increment the internal burst counter ($\overline{ADV}/\overline{LD} = \text{HIGH}$).

The IDT71V65703/5903 SRAMs utilize IDT's latest high-performance CMOS process and are packaged in a JEDEC Standard 14mm x 20mm 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA) and a 165 fine pitch ball grid array (fBGA).

Pin Description Summary

A0-A18	Address Inputs	Input	Synchronous
\overline{CE}_1 , \overline{CE}_2 , \overline{CE}_2	Chip Enables	Input	Synchronous
\overline{OE}	Output Enable	Input	Asynchronous
R/W	Read/Write Signal	Input	Synchronous
\overline{CEN}	Clock Enable	Input	Synchronous
\overline{BW}_1 , \overline{BW}_2 , \overline{BW}_3 , \overline{BW}_4	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
$\overline{ADV}/\overline{LD}$	Advance Burst Address/Load New Address	Input	Synchronous
LBO	Linear/Interleaved Burst Order	Input	Static
ZZ	Sleep Mode	Input	Asynchronous
I/O0-I/O31, I/OP1-I/OP4	Data Input/Output	I/O	Synchronous
VDD, VDDO	Core Power, I/O Power	Supply	Static
VSS	Ground	Supply	Static

5298 tbl 01

Pin Definitions⁽¹⁾

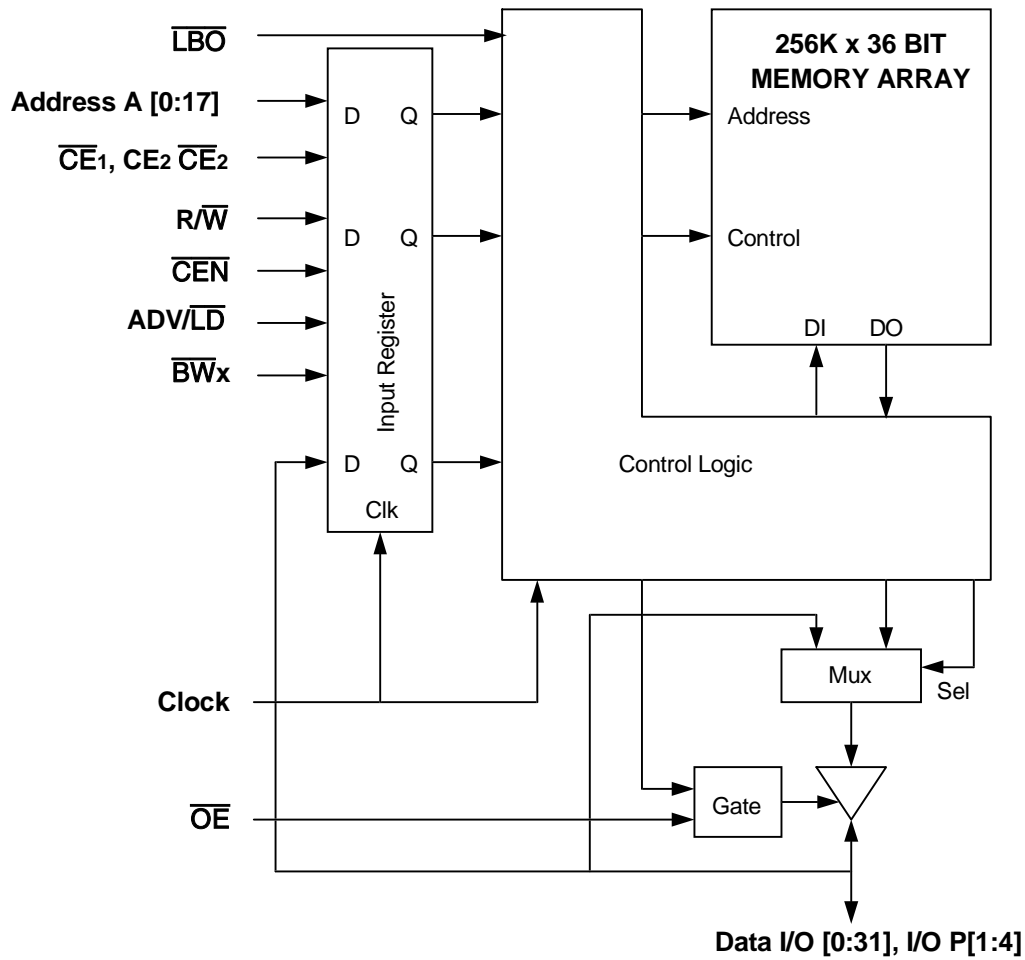
Symbol	Pin Function	I/O	Active	Description
A0-A18	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/LD low, CEN low, and true chip enables.
ADV/LD	Advance / Load	I	N/A	ADV/LD is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/LD is low with the chip deselected, any burst in progress is terminated. When ADV/LD is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/LD is sampled high.
R/W	Read / Write	I	N/A	R/W signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place one clock cycle later.
CEN	Clock Enable	I	LOW	Synchronous Clock Enable Input. When CEN is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of CEN sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, CEN must be sampled low at rising edge of clock.
BW1-BW4	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (When R/W and ADV/LD are sampled low) the appropriate byte write signal (BW1-BW4) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/W is sampled high. The appropriate byte(s) of data are written into the device one cycle later. BW1-BW4 can all be tied low if always doing write to the entire 36-bit word.
CE1, CE2	Chip Enables	I	LOW	Synchronous active low chip enable. CE1 and CE2 are used with CE2 to enable the IDT71V65703/5903 (CE1 or CE2 sampled high or CE2 sampled low) and ADV/LD low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a one cycle deselect, i.e., the data bus will tri-state one clock cycle after deselect is initiated.
CE2	Chip Enable	I	HIGH	Synchronous active high chip enable. CE2 is used with CE1 and CE2 to enable the chip. CE2 has inverted polarity but otherwise identical to CE1 and CE2.
CLK	Clock	I	N/A	This is the clock input to the IDT71V65703/5903. Except for OE, all timing references for the device are made with respect to the rising edge of CLK.
I/O0-I/O31 I/OP1-I/OP4	Data Input/Output	I/O	N/A	Data input/output (I/O) pins. The data input path is registered, triggered by the rising edge of CLK. The data output path is flow-through (no output register).
LBO	Linear Burst Order	I	LOW	Burst order selection input. When LBO is high the Interleaved burst sequence is selected. When LBO is low the Linear burst sequence is selected. LBO is a static input, and it must not change during device operation.
OE	Output Enable	I	LOW	Asynchronous output enable. OE must be low to read data from the 71V65703/5903. When OE is HIGH the I/O pins are in a high-impedance state. OE does not need to be actively controlled for read and write cycles. In normal operation, OE can be tied low.
ZZ	Sleep Mode	I	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V65703/5903 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.
VDD	Power Supply	N/A	N/A	3.3V core power supply.
VDDO	Power Supply	N/A	N/A	3.3V I/O supply.
VSS	Ground	N/A	N/A	Ground.

NOTE:

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

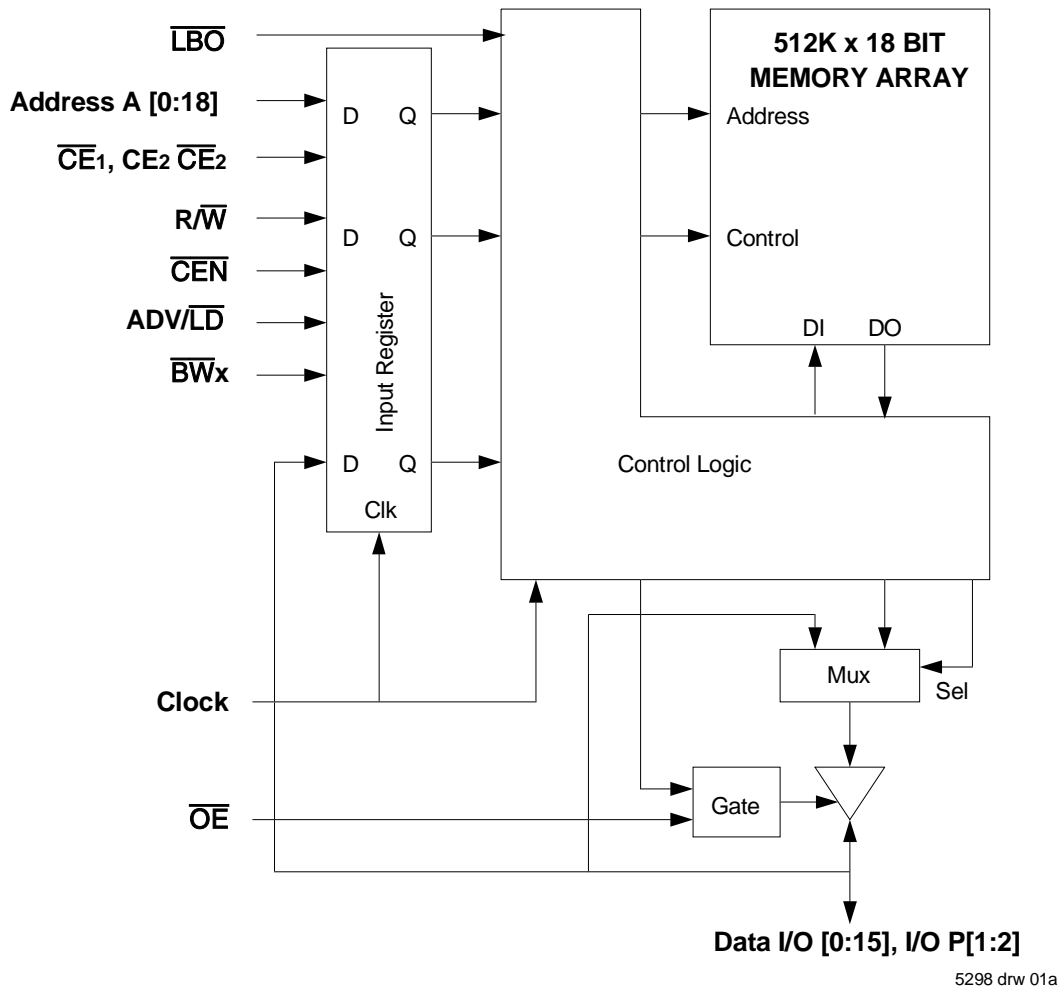
5298 tbl 02

Functional Block Diagram — 256K x 36



5298 drw 01

Functional Block Diagram — 512K x 18



Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V _{DDQ}	I/O Supply Voltage	3.135	3.3	3.465	V
V _{SS}	Ground	0	0	0	V
V _H	Input High Voltage - Inputs	2.0	—	V _{DD} + 0.3	V
V _H	Input High Voltage - I/O	2.0	—	V _{DDQ} + 0.3	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V

5298 tbl 04

NOTE:

- V_{IL} (min.) = -1.0V for pulse width less than tcvc/2, once per cycle.

Recommended Operating Temperature and Supply Voltage

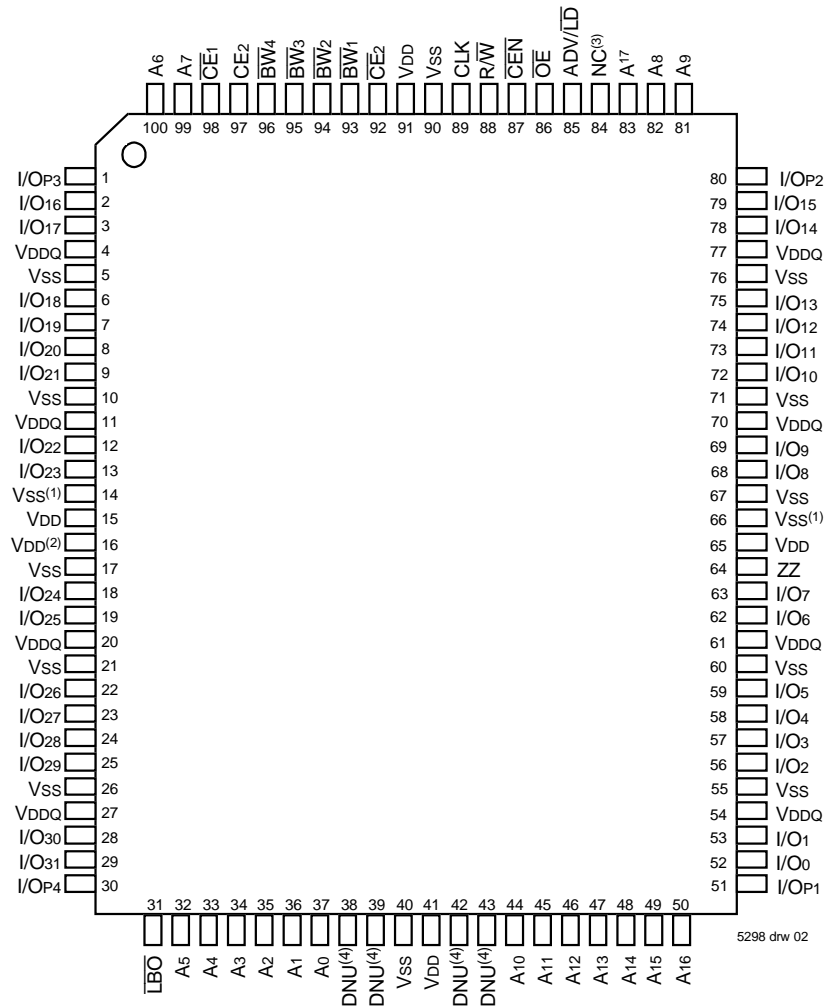
Grade	Temperature ⁽¹⁾	V _{SS}	V _{DD}	V _{DDQ}
Commercial	0°C to +70°C	0V	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	3.3V±5%

NOTES:

5298 tbl 05

1. T_A is the "instant on" case temperature.

Pin Configuration — 256K x 36

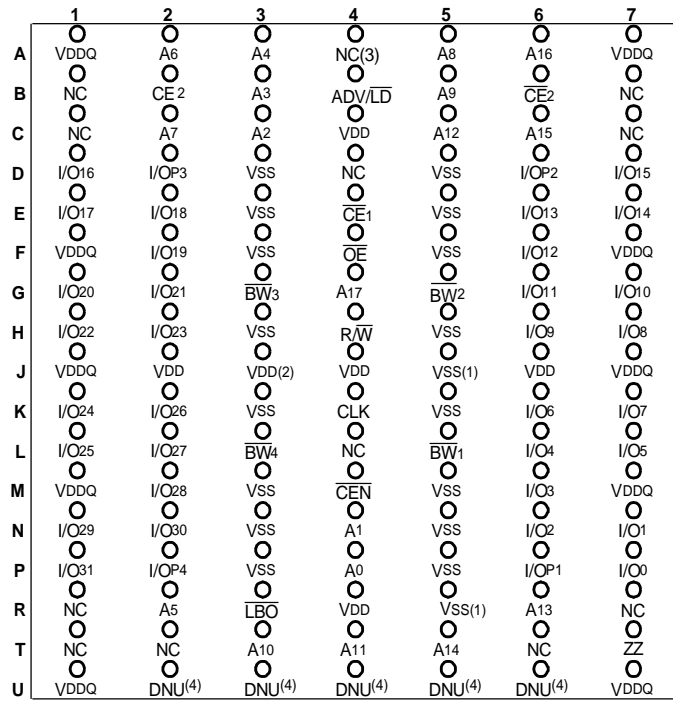


Top View 100 TQFP

NOTES:

1. Pins 14 and 66 do not have to be connected directly to V_{SS} as long as the input voltage is ≤ V_{IL}.
2. Pin 16 does not have to be connected directly to V_{DD} as long as the input voltage is ≥ V_{IH}.
3. Pin 84 is reserved for a future 16M.
4. DNU = Do not use. Pins 38, 39, 42 and 43 are reserved for respective JTAG pins TMS, TDI, TDO and TCK. The current die revision allows these pins to be left unconnected, tied LOW (V_{SS}), or tied HIGH (V_{DD}).

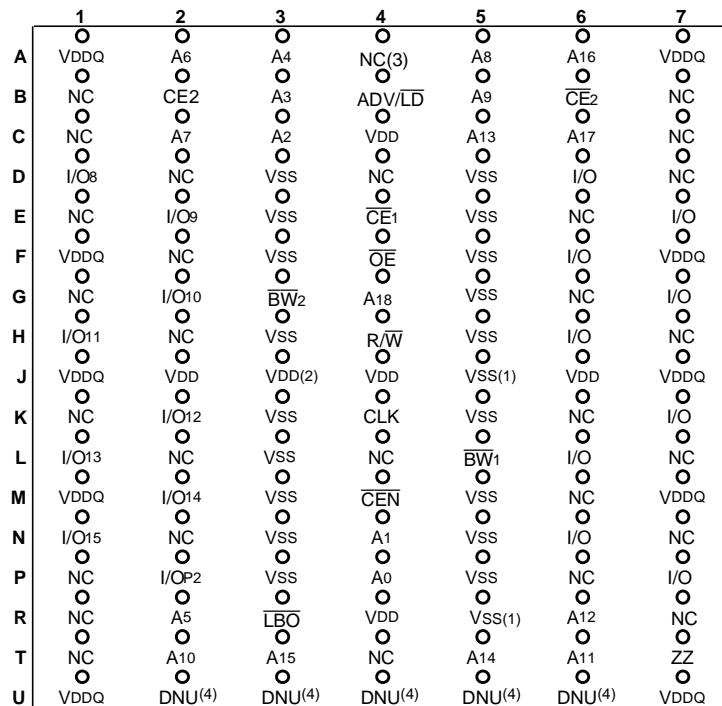
Pin Configuration — 256K x 36, 119 BGA



5298 drw 13a

Top View

Pin Configuration — 512K x 18, 119 BGA



5298 drw 13b

Top View

NOTES:

1. R5 and J5 do not have to be directly connected to Vss as long as the input voltage is $\leq V_{IL}$.
2. J3 does not have to be connected directly to VDD as long as the input voltage is $\geq V_{IH}$.
3. A4 is reserved for future 16M.
4. DNU = Do not use; Pin U2, U3, U4, U5 and U6 are reserved for respective JTAG pins: TMS, TDI, TCK, TDO and TRST. The current die revision allows these pins to be left unconnected, tied LOW (Vss), or tied HIGH (VDD).

Pin Configuration — 256K x 36, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC ⁽³⁾	A7	$\overline{CE}1$	$\overline{B\overline{W}}3$	$\overline{B\overline{W}}2$	$\overline{CE}2$	\overline{CEN}	ADV/ \overline{LD}	A17	A8	NC
B	NC	A6	CE2	$\overline{B\overline{W}}4$	$\overline{B\overline{W}}1$	CLK	R/ \overline{W}	\overline{OE}	NC ⁽³⁾	A9	NC ⁽³⁾
C	I/OP3	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP2
D	I/O17	I/O16	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O15	I/O14
E	I/O19	I/O18	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O13	I/O12
F	I/O21	I/O20	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O11	I/O10
G	I/O23	I/O22	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O9	I/O8
H	VSS ⁽¹⁾	VDD ⁽²⁾	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	I/O25	I/O24	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O7	I/O6
K	I/O27	I/O26	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O5	I/O4
L	I/O29	I/O28	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	I/O2
M	I/O31	I/O30	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	I/O0
N	I/OP4	NC	VDDQ	VSS	DNU ⁽⁴⁾	NC	VSS ⁽¹⁾	VSS	VDDQ	NC	I/OP1
P	NC	NC ⁽³⁾	A5	A2	DNU ⁽⁴⁾	A1	DNU ⁽⁴⁾	A10	A13	A14	NC
R	$\overline{LB\overline{O}}$	NC ⁽³⁾	A4	A3	DNU ⁽⁴⁾	A0	DNU ⁽⁴⁾	A11	A12	A15	A16

5298 tbl 25a

Pin Configuration — 512K x 18, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC ⁽³⁾	A7	$\overline{CE}1$	$\overline{B\overline{W}}2$	NC	$\overline{CE}2$	\overline{CEN}	ADV/ \overline{LD}	A18	A8	A10
B	NC	A6	CE2	NC	$\overline{B\overline{W}}1$	CLK	R/ \overline{W}	\overline{OE}	NC ⁽³⁾	A9	NC ⁽³⁾
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP1
D	NC	I/O8	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O7
E	NC	I/O9	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O6
F	NC	I/O10	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O5
G	NC	I/O11	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O4
H	VSS ⁽¹⁾	VDD ⁽²⁾	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	I/O12	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	NC
K	I/O13	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O2	NC
L	I/O14	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	NC
M	I/O15	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O0	NC
N	I/OP2	NC	VDDQ	VSS	DNU ⁽⁴⁾	NC	VSS ⁽¹⁾	VSS	VDDQ	NC	NC
P	NC	NC ⁽³⁾	A5	A2	DNU ⁽⁴⁾	A1	DNU ⁽⁴⁾	A11	A14	A15	NC
R	$\overline{LB\overline{O}}$	NC ⁽³⁾	A4	A3	DNU ⁽⁴⁾	A0	DNU ⁽⁴⁾	A12	A13	A16	A17

5298 tbl25b

NOTES:

1. Pins H1 and N7 do not have to be connected directly to Vss as long as the input voltage is $\leq V_{IL}$.
2. Pin H2 does not have to be connected directly to Vdd as long as the input voltage is $\geq V_{IH}$.
3. Pin B9, B11, A1, R2 and P2 are reserved for a future 18M, 36M, 72M, 144M and 288M respectively.
4. DNU = Do not use. Pins P5, R5, P7, R7 and N5 are reserved for respective JTAG pins: TDI, TMS, TDO, TCK and \overline{TRST} on future revisions. The current die revision allows these pins to be left unconnected, tied LOW (Vss), or tied HIGH (Vdd).

Synchronous Truth Table⁽¹⁾

\overline{CEN}	R/W	$\overline{CE}_1, \overline{CE}_2^{(6)}$	ADV/LD	BWx	ADDRESS USED	PREVIOUS CYCLE	CURRENT CYCLE	I/O (One cycle later)
L	L	L	L	Valid	External	X	LOAD WRITE	D ⁽⁷⁾
L	H	L	L	X	External	X	LOAD READ	Q ⁽⁷⁾
L	X	X	H	Valid	Internal	LOAD WRITE / BURST WRITE	BURST WRITE (Advance burst counter) ⁽²⁾	D ⁽⁷⁾
L	X	X	H	X	Internal	LOAD READ / BURST READ	BURST READ (Advance burst counter) ⁽²⁾	Q ⁽⁷⁾
L	X	H	L	X	X	X	DESELECT or STOP ⁽³⁾	HIZ
L	X	X	H	X	X	DESELECT / NOOP	NOOP	HIZ
H	X	X	X	X	X	X	SUSPEND ⁽⁴⁾	Previous Value

5298 tbl 08

NOTES:

- L = V_{IL}, H = V_{IH}, X = Don't Care.
- When ADV/LD signal is sampled high, the internal burst counter is incremented. The R/W signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/W signal when the first address is loaded at the beginning of the burst cycle.
- Deselect cycle is initiated when either (\overline{CE}_1 , or \overline{CE}_2 is sampled high or CE2 is sampled low) and ADV/LD is sampled low at rising edge of clock. The data bus will tri-state one cycle after deselect is initiated.
- When \overline{CEN} is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers and the I/Os remains unchanged.
- To select the chip requires $\overline{CE}_1 = L$, $\overline{CE}_2 = L$ and CE2 = H on these chip enable pins. The chip is deselected if any one of the chip enables is false.
- Device Outputs are ensured to be in High-Z during device power-up.
- Q - data read from the device, D - data written to the device.

Partial Truth Table for Writes⁽¹⁾

OPERATION	R/W	\overline{BW}_1	\overline{BW}_2	$\overline{BW}_3^{(3)}$	$\overline{BW}_4^{(3)}$
READ	H	X	X	X	X
WRITE ALL BYTES	L	L	L	L	L
WRITE BYTE 1 (I/O[0:7], I/OP1) ⁽²⁾	L	L	H	H	H
WRITE BYTE 2 (I/O[8:15], I/OP2) ⁽²⁾	L	H	L	H	H
WRITE BYTE 3 (I/O[16:23], I/OP3) ^(2,3)	L	H	H	L	H
WRITE BYTE 4 (I/O[24:31], I/OP4) ^(2,3)	L	H	H	H	L
NO WRITE	L	H	H	H	H

5298 tbl 09

NOTES:

- L = V_{IL}, H = V_{IH}, X = Don't Care.
- Multiple bytes may be selected during the same cycle.
- N/A for x18 configuration.

Interleaved Burst Sequence Table ($\overline{LBO} = V_{DD}$)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address ⁽¹⁾	1	1	1	0	0	1	0	0

5298 tbl 10

NOTE:

- Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Linear Burst Sequence Table ($\overline{\text{LBO}}=\text{Vss}$)

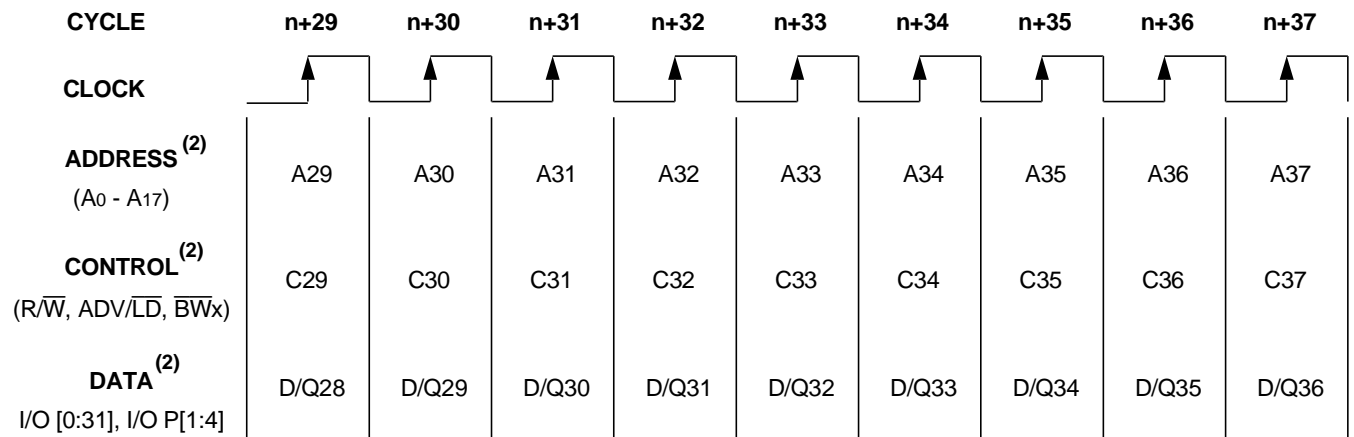
	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address ⁽¹⁾	1	1	0	0	0	1	1	0

5298 tbl 11

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Functional Timing Diagram⁽¹⁾



5298 drw 03

NOTES:

1. This assumes $\overline{\text{CEN}}$, $\overline{\text{CE}}_1$, CE_2 and $\overline{\text{CE}}_2$ are all true.
2. All Address, Control and Data_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data_Out is valid after a clock-to-data delay from the rising edge of clock.

Device Operation - Showing Mixed Load, Burst, Deselect and NOOP Cycles⁽²⁾

Cycle	Address	R/ \bar{W}	ADV/ \bar{LD}	$\bar{CE}_1^{(1)}$	\bar{CEN}	\bar{BW}_x	\bar{OE}	I/O	Comments
n	A0	H	L	L	L	X	X	D1	Load read
n+1	X	X	H	X	L	X	L	Q0	Burst read
n+2	A1	H	L	L	L	X	L	Q0+1	Load read
n+3	X	X	L	H	L	X	L	Q1	Deselect or STOP
n+4	X	X	H	X	L	X	X	Z	NOOP
n+5	A2	H	L	L	L	X	X	Z	Load read
n+6	X	X	H	X	L	X	L	Q2	Burst read
n+7	X	X	L	H	L	X	L	Q2+1	Deselect or STOP
n+8	A3	L	L	L	L	L	X	Z	Load write
n+9	X	X	H	X	L	L	X	D3	Burst write
n+10	A4	L	L	L	L	L	X	D3+1	Load write
n+11	X	X	L	H	L	X	X	D4	Deselect or STOP
n+12	X	X	H	X	L	X	X	Z	NOOP
n+13	A5	L	L	L	L	L	X	Z	Load write
n+14	A6	H	L	L	L	X	X	D5	Load read
n+15	A7	L	L	L	L	L	L	Q6	Load write
n+16	X	X	H	X	L	L	X	D7	Burst write
n+17	A8	H	L	L	L	X	X	D7+1	Load read
n+18	X	X	H	X	L	X	L	Q8	Burst read
n+19	A9	L	L	L	L	L	L	Q8+1	Load write

5298 tbl 12

NOTES:

- \bar{CE}_2 timing transition is identical to \bar{CE}_1 signal. CE_2 timing transition is identical but inverted to the \bar{CE}_1 and \bar{CE}_2 signals.
- H = High; L = Low; X = Don't Care; Z = High Impedence.

Read Operation⁽¹⁾

Cycle	Address	R \overline{W}	ADV/ \overline{LD}	$\overline{CE}_1^{(2)}$	\overline{CEN}	\overline{BW}_x	\overline{OE}	I/O	Comments
n	A ₀	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	X	X	L	Q ₀	Contents of Address A ₀ Read Out

5298 tbl 13

NOTES:

- H = High; L = Low; X = Don't Care; Z = High Impedance.
- \overline{CE}_2 timing transition is identical to \overline{CE}_1 signal. \overline{CE}_2 timing transition is identical but inverted to the \overline{CE}_1 and \overline{CE}_2 signals.

Burst Read Operation⁽¹⁾

Cycle	Address	R \overline{W}	ADV/ \overline{LD}	$\overline{CE}_1^{(2)}$	\overline{CEN}	\overline{BW}_x	\overline{OE}	I/O	Comments
n	A ₀	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	L	Q ₀	Address A ₀ Read Out, Inc. Count
n+2	X	X	H	X	L	X	L	Q ₀₊₁	Address A ₀₊₁ Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	Q ₀₊₂	Address A ₀₊₂ Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	Q ₀₊₃	Address A ₀₊₃ Read Out, Load A ₁
n+5	A ₁	H	L	L	L	X	L	Q ₀	Address A ₀ Read Out, Inc. Count
n+6	X	X	H	X	L	X	L	Q ₁	Address A ₁ Read Out, Inc. Count
n+7	A ₂	H	L	L	L	X	L	Q ₁₊₁	Address A ₁₊₁ Read Out, Load A ₂

5298 tbl 14

NOTES:

- H = High; L = Low; X = Don't Care; Z = High Impedance.
- \overline{CE}_2 timing transition is identical to \overline{CE}_1 signal. \overline{CE}_2 timing transition is identical but inverted to the \overline{CE}_1 and \overline{CE}_2 signals.

Write Operation⁽¹⁾

Cycle	Address	R \overline{W}	ADV/ \overline{LD}	$\overline{CE}_1^{(2)}$	\overline{CEN}	\overline{BW}_x	\overline{OE}	I/O	Comments
n	A ₀	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	D ₀	Write to Address A ₀

5298 tbl 15

NOTES:

- H = High; L = Low; X = Don't Care; Z = High Impedance.
- \overline{CE}_2 timing transition is identical to \overline{CE}_1 signal. \overline{CE}_2 timing transition is identical but inverted to the \overline{CE}_1 and \overline{CE}_2 signals.

Burst Write Operation⁽¹⁾

Cycle	Address	R \overline{W}	ADV/ \overline{LD}	$\overline{CE}_1^{(2)}$	\overline{CEN}	\overline{BW}_x	\overline{OE}	I/O	Comments
n	A ₀	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	D ₀	Address A ₀ Write, Inc. Count
n+2	X	X	H	X	L	L	X	D ₀₊₁	Address A ₀₊₁ Write, Inc. Count
n+3	X	X	H	X	L	L	X	D ₀₊₂	Address A ₀₊₂ Write, Inc. Count
n+4	X	X	H	X	L	L	X	D ₀₊₃	Address A ₀₊₃ Write, Load A ₁
n+5	A ₁	L	L	L	L	L	X	D ₀	Address A ₀ Write, Inc. Count
n+6	X	X	H	X	L	L	X	D ₁	Address A ₁ Write, Inc. Count
n+7	A ₂	L	L	L	L	L	X	D ₁₊₁	Address A ₁₊₁ Write, Load A ₂

5298 tbl 16

NOTES:

- H = High; L = Low; X = Don't Care; Z = High Impedance.
- \overline{CE}_2 timing transition is identical to \overline{CE}_1 signal. \overline{CE}_2 timing transition is identical but inverted to the \overline{CE}_1 and \overline{CE}_2 signals.

Read Operation with Clock Enable Used⁽¹⁾

Cycle	Address	R \overline{W}	ADV/ \overline{LD}	$\overline{CE}_1^{(2)}$	\overline{CEN}	\overline{BW}_x	\overline{OE}	I/O	Comments
n	A ₀	H	L	L	L	X	X	X	Address A ₀ and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A ₁	H	L	L	L	X	L	Q ₀	Address A ₀ Read out, Load A ₁
n+3	X	X	X	X	H	X	L	Q ₀	Clock Ignored. Data Q ₀ is on the bus.
n+4	X	X	X	X	H	X	L	Q ₀	Clock Ignored. Data Q ₀ is on the bus.
n+5	A ₂	H	L	L	L	X	L	Q ₁	Address A ₁ Read out, Load A ₂
n+6	A ₃	H	L	L	L	X	L	Q ₂	Address A ₂ Read out, Load A ₃
n+7	A ₄	H	L	L	L	X	L	Q ₃	Address A ₃ Read out, Load A ₄

5298 tbl 17

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. \overline{CE}_2 timing transition is identical to \overline{CE}_1 signal. \overline{CE}_2 timing transition is identical but inverted to the \overline{CE}_1 and \overline{CE}_2 signals.

Write Operation with Clock Enable Used⁽¹⁾

Cycle	Address	R \overline{W}	ADV/ \overline{LD}	$\overline{CE}_1^{(2)}$	\overline{CEN}	\overline{BW}_x	\overline{OE}	I/O	Comments
n	A ₀	L	L	L	L	L	X	X	Address A ₀ and Control meet setup.
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored.
n+2	A ₁	L	L	L	L	L	X	D ₀	Write data D ₀ , Load A ₁ .
n+3	X	X	X	X	H	X	X	X	Clock Ignored.
n+4	X	X	X	X	H	X	X	X	Clock Ignored.
n+5	A ₂	L	L	L	L	L	X	D ₁	Write Data D ₁ , Load A ₂
n+6	A ₃	L	L	L	L	L	X	D ₂	Write Data D ₂ , Load A ₃
n+7	A ₄	L	L	L	L	L	X	D ₃	Write Data D ₃ , Load A ₄

5298 tbl 18

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. \overline{CE}_2 timing transition is identical to \overline{CE}_1 signal. \overline{CE}_2 timing transition is identical but inverted to the \overline{CE}_1 and \overline{CE}_2 signals.

Read Operation with Chip Enable Used⁽¹⁾

Cycle	Address	R \overline{W}	ADV/ \overline{LD}	\overline{CE}_1 ⁽²⁾	\overline{CEN}	\overline{BW}_x	\overline{OE}	I/O ⁽³⁾	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	Z	Deselected.
n+2	A ₀	H	L	L	L	X	X	Z	Address A ₀ and Control meet setup.
n+3	X	X	L	H	L	X	L	Q ₀	Address A ₀ read out, Deselected.
n+4	A ₁	H	L	L	L	X	X	Z	Address A ₁ and Control meet setup.
n+5	X	X	L	H	L	X	L	Q ₁	Address A ₁ read out, Deselected.
n+6	X	X	L	H	L	X	X	Z	Deselected.
n+7	A ₂	H	L	L	L	X	X	Z	Address A ₂ and Control meet setup.
n+8	X	X	L	H	L	X	L	Q ₂	Address A ₂ read out, Deselected.
n+9	X	X	L	H	L	X	X	Z	Deselected.

5298 tbl 19

NOTES:

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. \overline{CE}_2 timing transition is identical to \overline{CE}_1 signal. CE₂ timing transition is identical but inverted to the \overline{CE}_1 and \overline{CE}_2 signals.
3. Device outputs are ensured to be in High-Z during device power-up.

Write Operation with Chip Enable Used⁽¹⁾

Cycle	Address	R \overline{W}	ADV/ \overline{LD}	\overline{CE}_1 ⁽²⁾	\overline{CEN}	\overline{BW}_x	\overline{OE}	I/O	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	Z	Deselected.
n+2	A ₀	L	L	L	L	L	X	Z	Address A ₀ and Control meet setup
n+3	X	X	L	H	L	X	X	D ₀	Data D ₀ Write In, Deselected.
n+4	A ₁	L	L	L	L	L	X	Z	Address A ₁ and Control meet setup
n+5	X	X	L	H	L	X	X	D ₁	Data D ₁ Write In, Deselected.
n+6	X	X	L	H	L	X	X	Z	Deselected.
n+7	A ₂	L	L	L	L	L	X	Z	Address A ₂ and Control meet setup
n+8	X	X	L	H	L	X	X	D ₂	Data D ₂ Write In, Deselected.
n+9	X	X	L	H	L	X	X	Z	Deselected.

5298 tbl 20

NOTES:

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE} = L$ is defined as $\overline{CE}_1 = L$, $\overline{CE}_2 = L$ and CE₂ = H. $\overline{CE} = H$ is defined as $\overline{CE}_1 = H$, $\overline{CE}_2 = H$ or CE₂ = L.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V±5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I _L	Input Leakage Current	V _{DD} = Max., V _{IN} = 0V to V _{DD}	—	5	μA
I _L	$\overline{\text{LBO}}$ Input Leakage Current ⁽¹⁾	V _{DD} = Max., V _{IN} = 0V to V _{DD}	—	30	μA
I _O	Output Leakage Current	V _{OUT} = 0V to V _{CC}	—	5	μA
V _{OL}	Output Low Voltage	I _{OL} = +8mA, V _{DD} = Min.	—	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -8mA, V _{DD} = Min.	2.4	—	V

NOTE:

5298 tbl 21

1. The $\overline{\text{LBO}}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ pin will be internally pulled to V_{SS} if not actively driven.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽¹⁾ (V_{DD} = 3.3V±5%)

Symbol	Parameter	Test Conditions	7.5ns		8ns		8.5ns		Unit
			Com'l	Ind	Com'l	Ind	Com'l	Ind	
I _{DD}	Operating Power Supply Current	Device Selected, Outputs Open, ADV/ $\overline{\text{LD}}$ = X, V _{DD} = Max., V _{IN} ≥ V _{IH} or ≤ V _{IL} , f = f _{MAX} ⁽²⁾	275	295	250	60	225	60	mA
I _{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V _{DD} = Max., V _{IN} ≥ V _{IH} or ≤ V _{IL} , f = 0 ^(2,3)	40	60	40	60	40	60	mA
I _{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, V _{DD} = Max., V _{IN} ≥ V _{IH} or ≤ V _{IL} , f = f _{MAX} ^(2,3)	105	125	100	120	95	115	mA
I _{SB3}	Idle Power Supply Current	Device Selected, Outputs Open, $\overline{\text{CEN}} \geq V_{IH}$, V _{DD} = Max., V _{IN} ≥ V _{IH} or ≤ V _{IL} , f = f _{MAX} ^(2,3)	40	60	40	60	40	60	mA
I _{ZZ}	Full Sleep Mode Supply Current	Device Selected, Outputs Open, $\overline{\text{CEN}} \leq V_{IL}$, V _{DD} = Max., ZZ ≥ V _{IH} , V _{IN} ≥ V _{IH} or ≤ V _{IL} , f = f _{MAX} ^(2,3)	40	60	40	60	40	60	mA

NOTES:

5298 tbl 22

- All values are maximum guaranteed values.
- At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/tcvc; f=0 means no input lines are changing.
- For I/Os V_{IH} = V_{DD} - 0.2V, V_{IL} = 0.2V. For other inputs V_{IH} = V_{DD} - 0.2V, V_{IL} = 0.2V.

AC Test Load

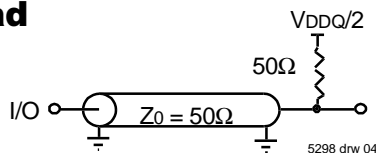


Figure 1. AC Test Load

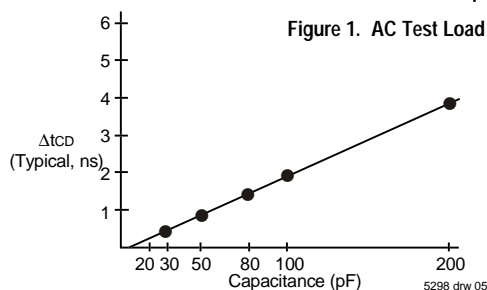


Figure 2. Lumped Capacitive Load, Typical Derating

AC Test Conditions

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figure 1

5298 tbl 23

AC Electrical Characteristics (VDD = 3.3V±5%, Commercial and Industrial Temperature Ranges)

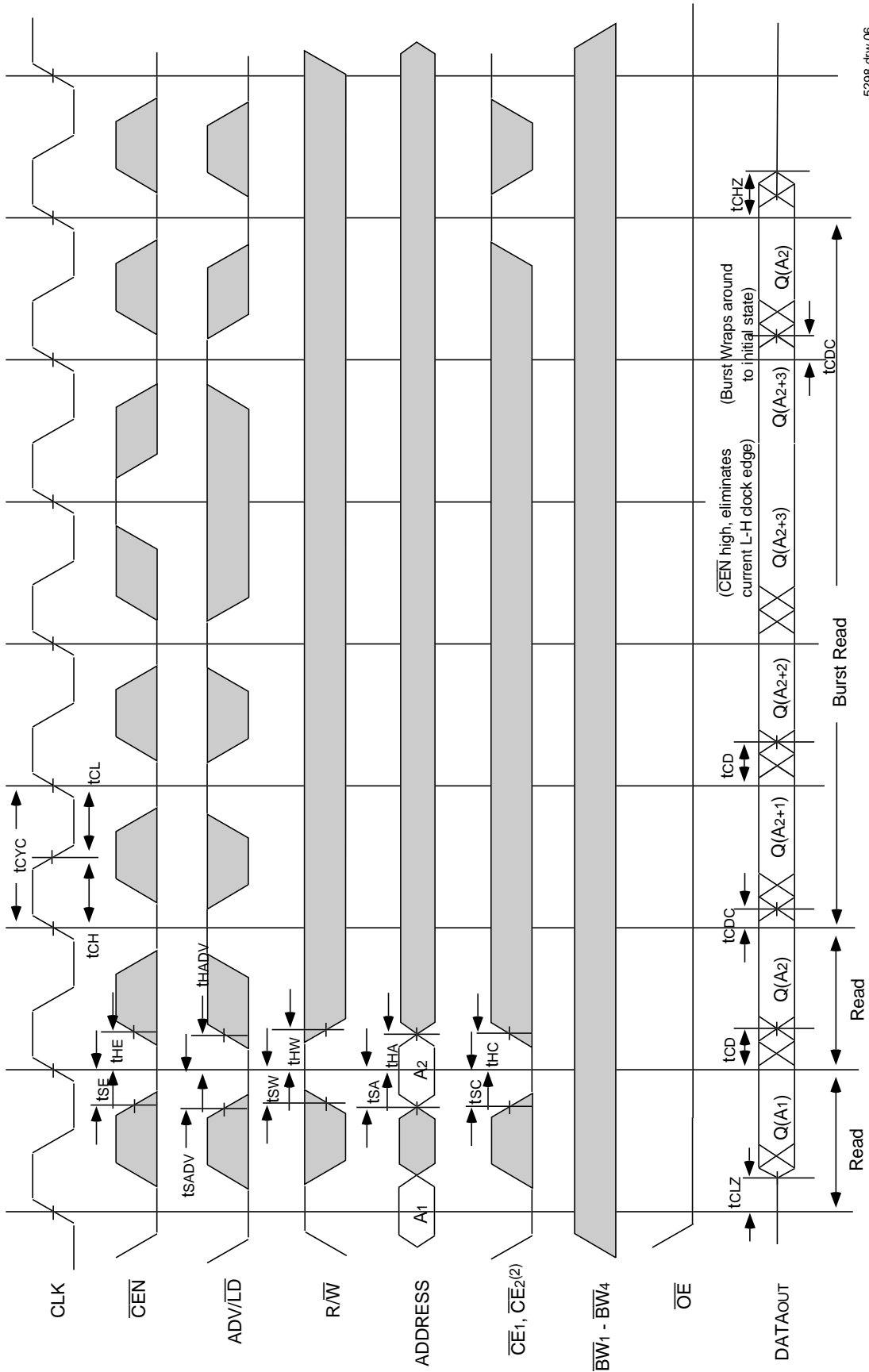
Symbol	Parameter	7.5ns		8ns		8.5ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC}	Clock Cycle Time	10	—	10.5	—	11	—	ns
t _{CH} ⁽¹⁾	Clock High Pulse Width	2.5	—	2.7	—	3.0	—	ns
t _{CL} ⁽¹⁾	Clock Low Pulse Width	2.5	—	2.7	—	3.0	—	ns
Output Parameters								
t _{CD}	Clock High to Valid Data	—	7.5	—	8	—	8.5	ns
t _{CDc}	Clock High to Data Change	2	—	2	—	2	—	ns
t _{CLZ} ^(2,3,4)	Clock High to Output Active	3	—	3	—	3	—	ns
t _{CHZ} ^(2,3,4)	Clock High to Data High-Z	—	5	—	5	—	5	ns
t _{OE}	Output Enable Access Time	—	5	—	5	—	5	ns
t _{OLZ} ^(2,3)	Output Enable Low to Data Active	0	—	0	—	0	—	ns
t _{OHZ} ^(2,3)	Output Enable High to Data High-Z	—	5	—	5	—	5	ns
Set Up Times								
t _{SE}	Clock Enable Setup Time	2.0	—	2.0	—	2.0	—	ns
t _{SA}	Address Setup Time	2.0	—	2.0	—	2.0	—	ns
t _{SD}	Data In Setup Time	2.0	—	2.0	—	2.0	—	ns
t _{SW}	Read/Write (R/W) Setup Time	2.0	—	2.0	—	2.0	—	ns
t _{ADV}	Advance/Load (ADV/LD) Setup Time	2.0	—	2.0	—	2.0	—	ns
t _{SC}	Chip Enable/Select Setup Time	2.0	—	2.0	—	2.0	—	ns
t _{SB}	Byte Write Enable (BWx) Setup Time	2.0	—	2.0	—	2.0	—	ns
Hold Times								
t _{HE}	Clock Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{HW}	Read/Write (R/W) Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{HADV}	Advance/Load (ADV/LD) Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{HB}	Byte Write Enable (BWx) Hold Time	0.5	—	0.5	—	0.5	—	ns

5298 tbl 24

NOTES:

1. Measured as HIGH above 0.6V_{DD0} and LOW below 0.4V_{DD0}.
2. Transition is measured ±200mV from steady-state.
3. These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
4. To avoid bus contention, the output buffers are designed such that t_{CHZ} (device turn-off) is about 1ns faster than t_{CLZ} (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because t_{CLZ} is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 3.465V) than t_{CHZ}, which is a Max. parameter (worse case at 70 deg. C, 3.135V).

Timing Waveform of Read Cycle(1,2,3,4)

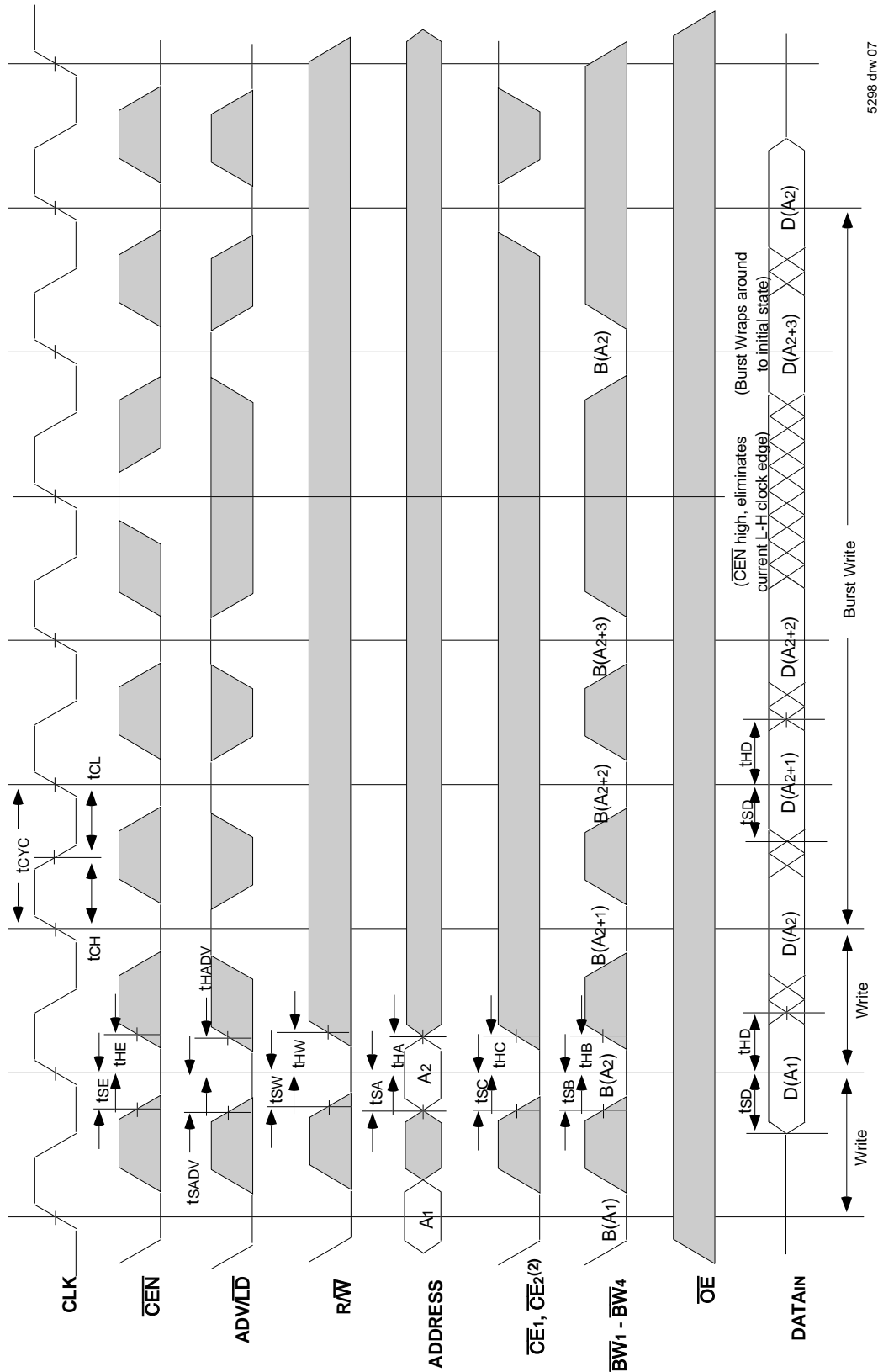


5298 drw 06

NOTES:

1. $Q(A_1)$ represents the first output from the external address A_1 . $Q(A_2)$ represents the first output from the external address A_2 . $Q(A_2+1)$ represents the next output data in the burst sequence of the base address A_2 , etc. where address bits A_0 and A_1 are advancing for the four word burst in the sequence defined by the state of the \overline{LBO} input.
2. CE_2 timing transitions are identical but inverted to the $\overline{CE_1}$ and $\overline{CE_2}$ signals. For example, when $\overline{CE_1}$ and $\overline{CE_2}$ are LOW on this waveform, CE_2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD LOW.
4. R/W is don't care when the SRAM is bursting (ADV/LD sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/W signal when new address and control are loaded into the SRAM.

Timing Waveform of Write Cycles(1,2,3,4,5)

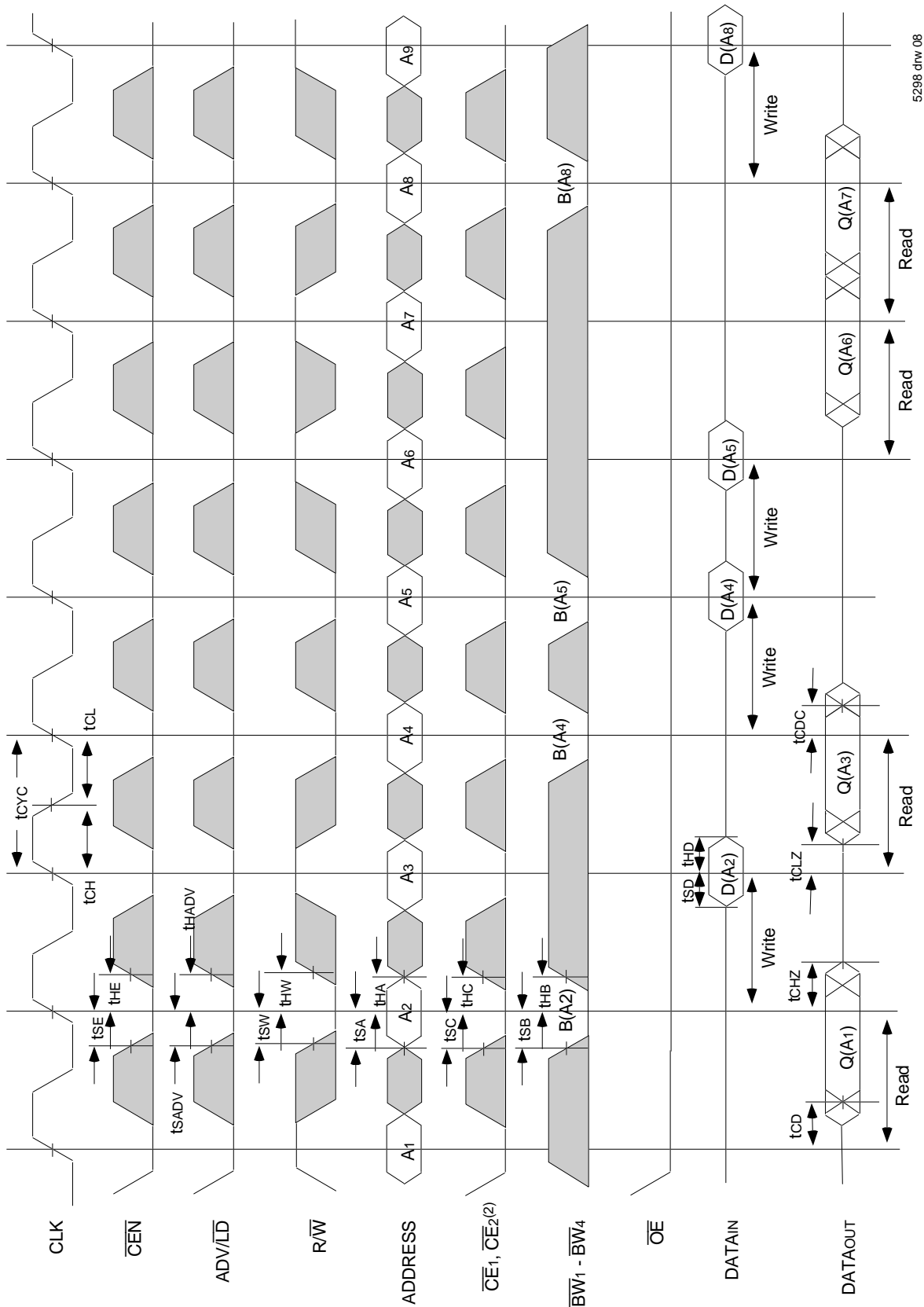


5298 dnw 07

NOTES:

1. $D(A_1)$ represents the first input to the external address A_1 . $D(A_2)$ represents the first input to the external address A_2 . $D(A_2+1)$ represents the next input data in the burst sequence of the base address A_2 , etc. where address bits A_0 and A_1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. CE_2 limiting transitions are identical but inverted to the CE_1 and CE_2 signals. For example, when CE_1 and CE_2 are LOW on this waveform, CE_2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling $ADVLD$ LOW.
4. RW is don't care when the SRAM is bursting ($ADVLD$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the RW signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals (BWx) must be valid on all write and burst-write cycles. A write cycle is initiated when RW signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

Timing Waveform of Combined Read and Write Cycles^(1,2,3)

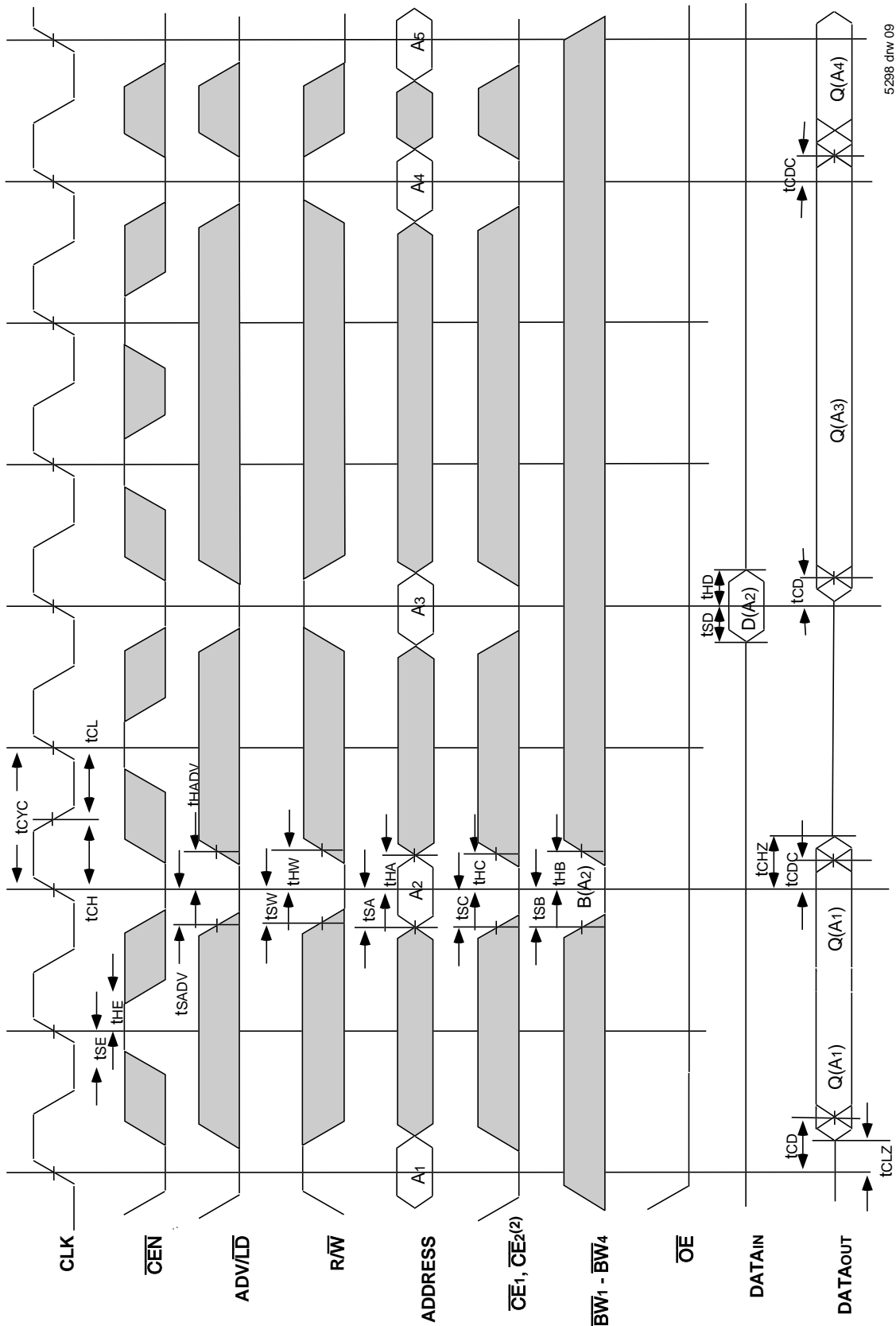


5298 drw 08

NOTES:

1. Q(A₁) represents the first output from the external address A₁. D(A₂) represents the input data to the SRAM corresponding to address A₂. CE₁ timing transitions are identical but inverted to the CE₁ and CE₂ signals. For example, when CE₁ and CE₂ are LOW on this waveform, CE₂ is HIGH.
2. Individual Byte Write signals (BW_x) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.
3. Individual Byte Write signals (BW_x) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

Timing Waveform of $\overline{\text{CEN}}$ Operation(1,2,3,4)

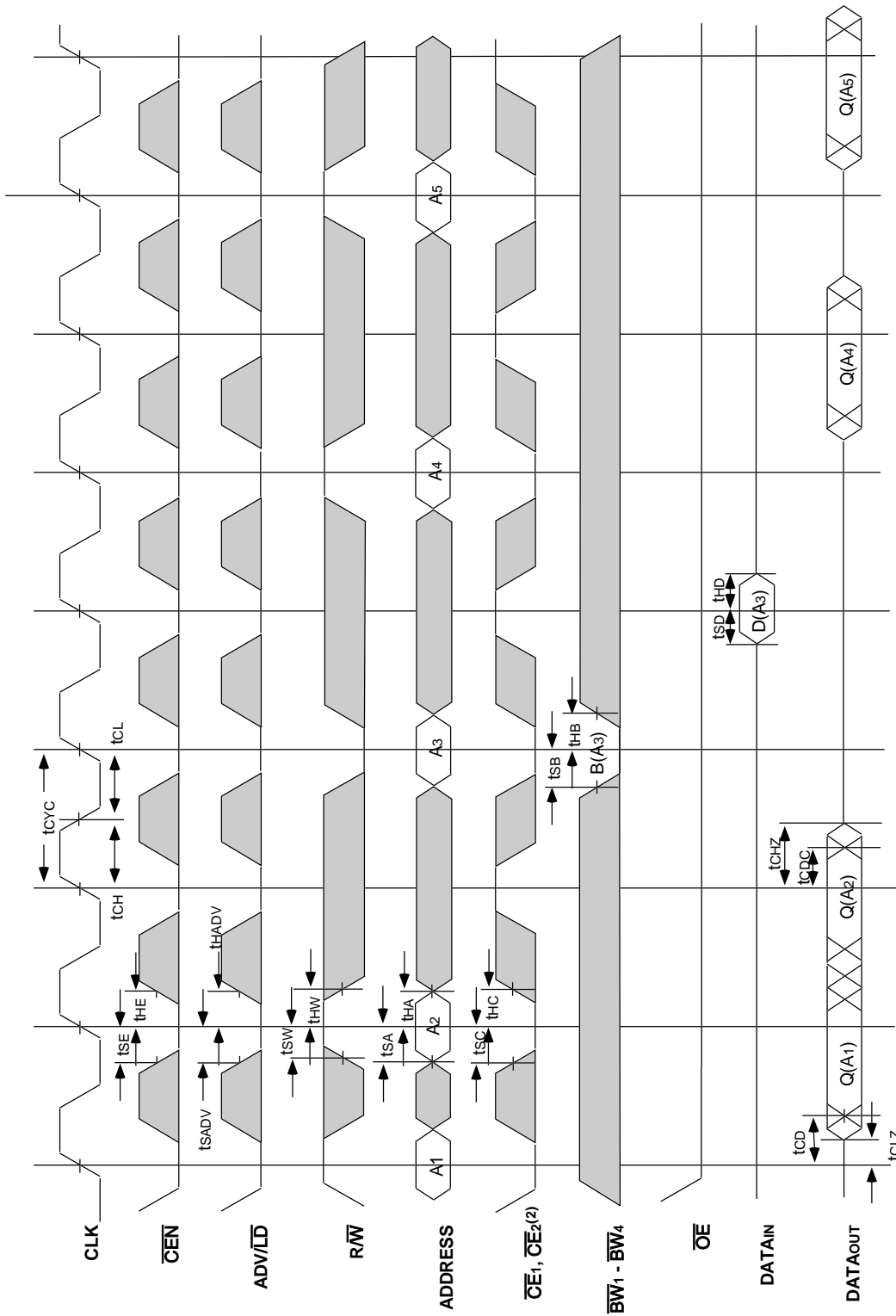


5298 dhw 09

NOTES:

1. O (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. CEz timing transitions are identical but inverted to the $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ signals. For example, when $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ are LOW on this waveform, CEz is HIGH.
3. $\overline{\text{CEN}}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{\text{BW}}_x$) must be valid on all write and burst-write cycles. A write cycle is initiated when $\overline{\text{RW}}$ signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

Timing Waveform of $\overline{\text{CS}}$ Operation(1,2,3,4)

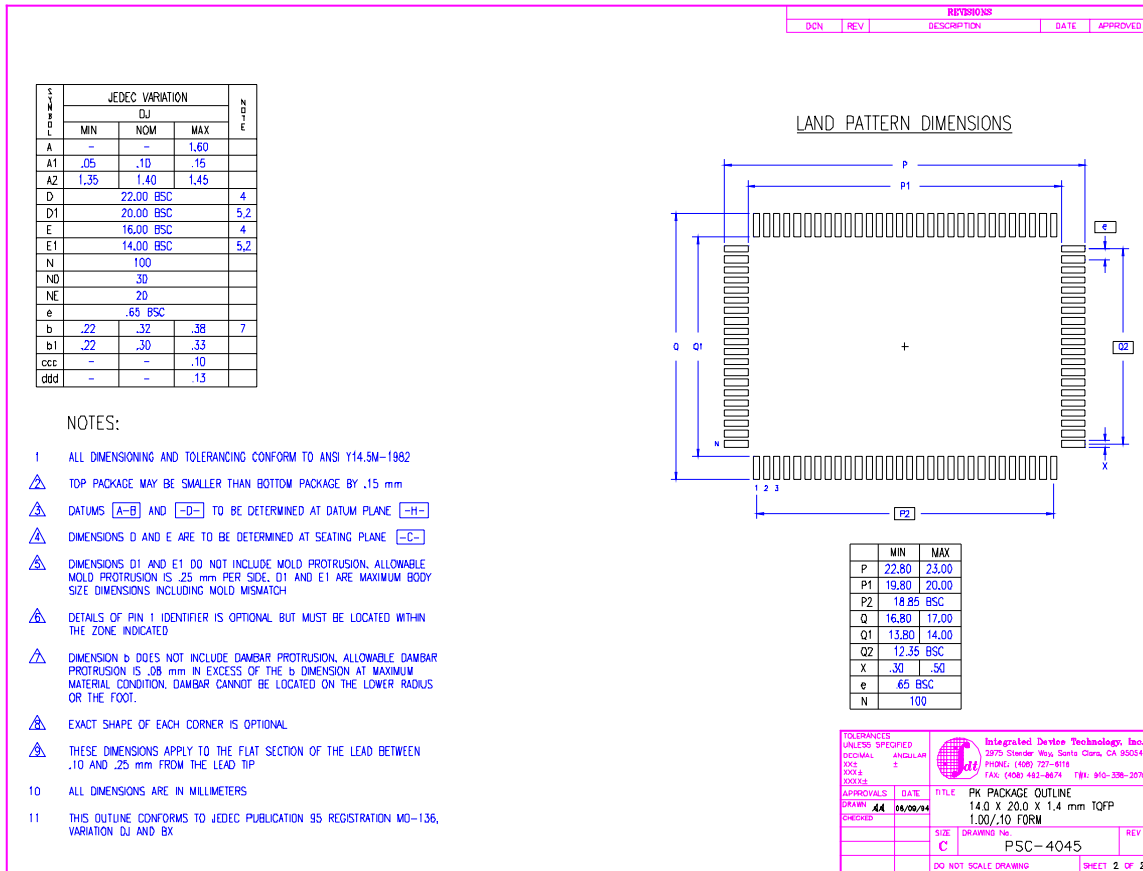
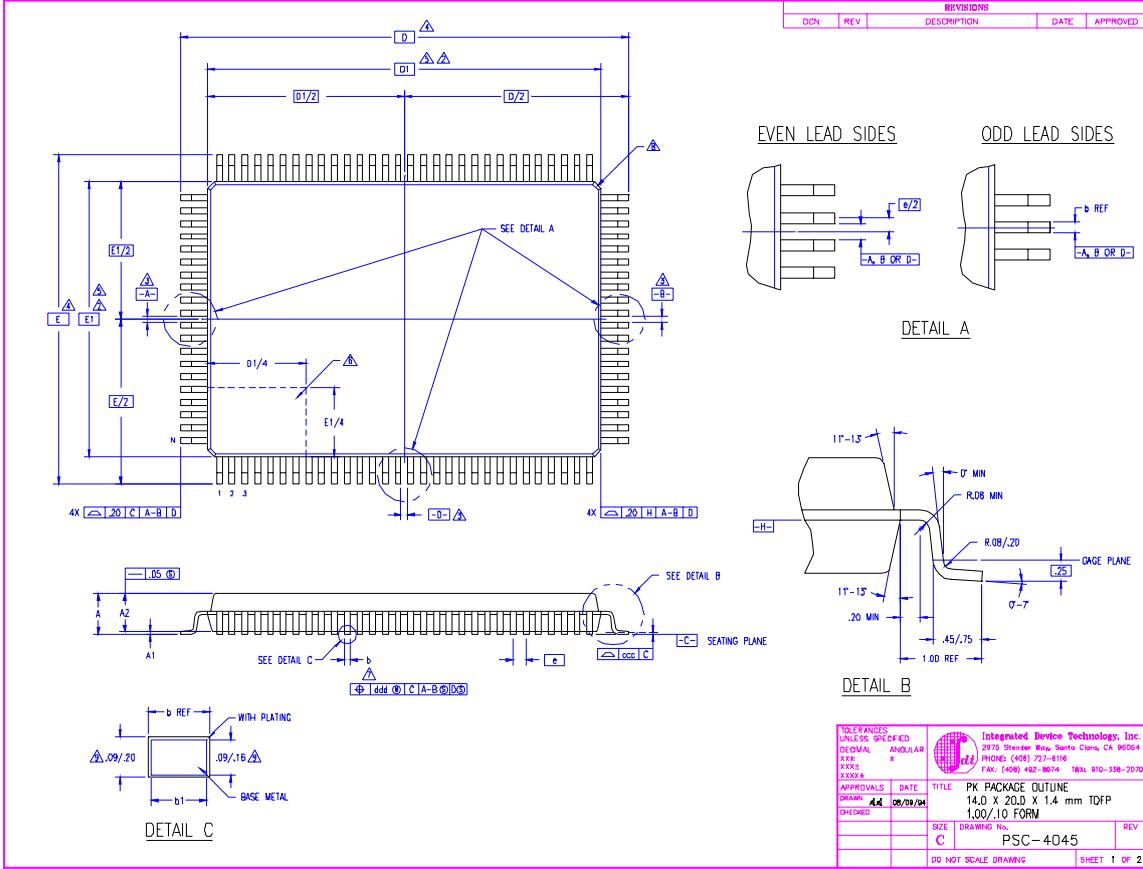


5298 drw 10

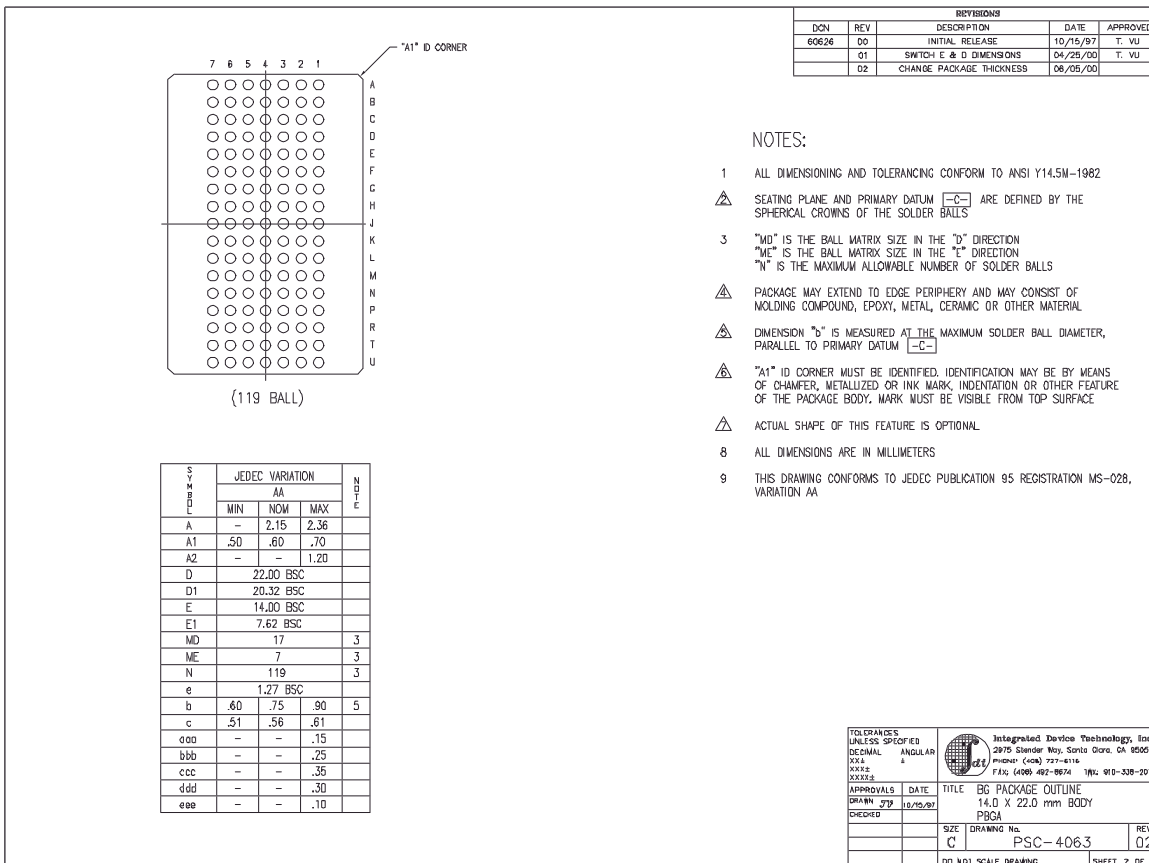
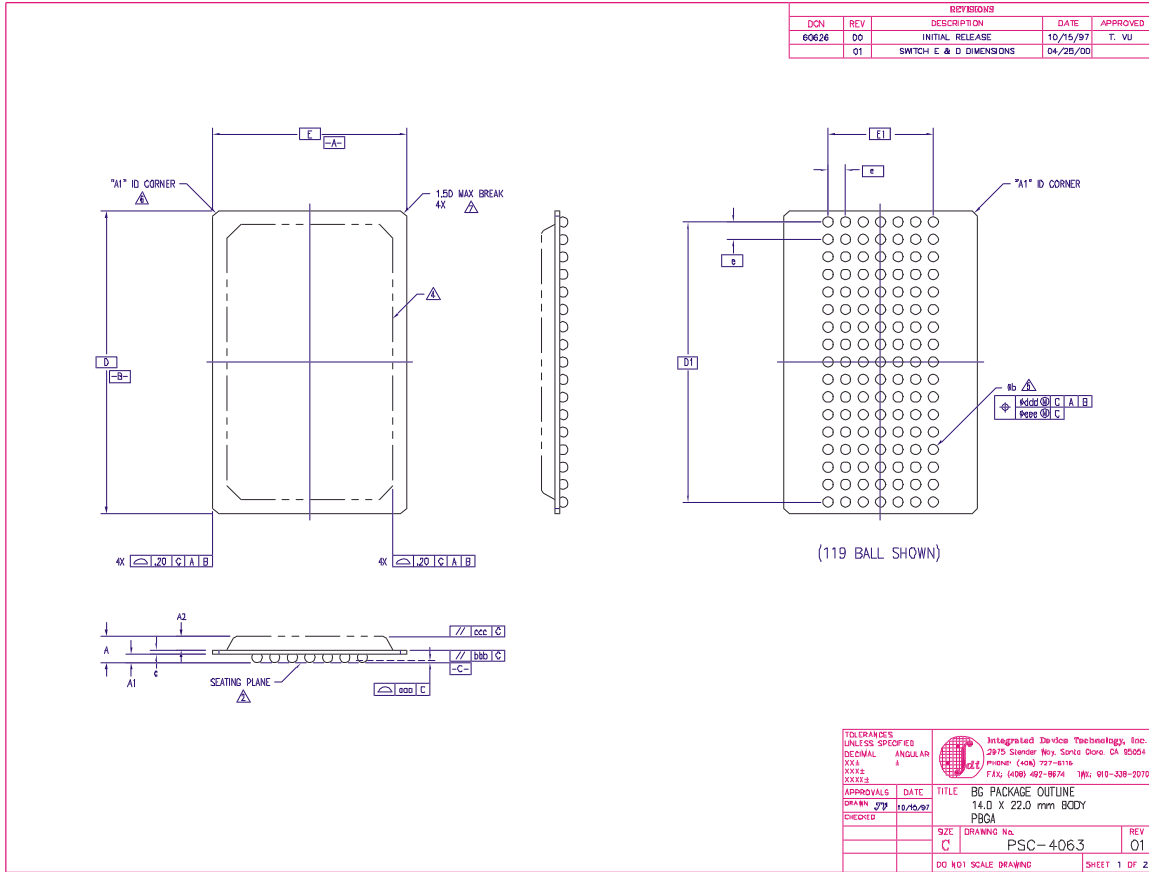
NOTES:

1. $Q(A_1)$ represents the first output from the external address A_1 . $D(A_3)$ represents the input data to the SRAM corresponding to address A_3 etc.
2. CE_2 timing transitions are identical but inverted to the $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ signals. For example, when $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ are LOW on this waveform, CE_2 is HIGH.
3. When either one of the Chip enables (CE_1 , CE_2 , $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$) is sampled inactive at the rising clock edge, a deselect cycle is initiated. The data-bus tri-states one cycle after the initiation of the deselect cycle. This allows for any pending data transfers (reads or writes) to be completed.
4. Individual Byte Write signals ($\overline{\text{BW}}_x$) must be valid on all write and burst-write cycles. A write cycle is initiated when $\overline{\text{RW}}$ signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

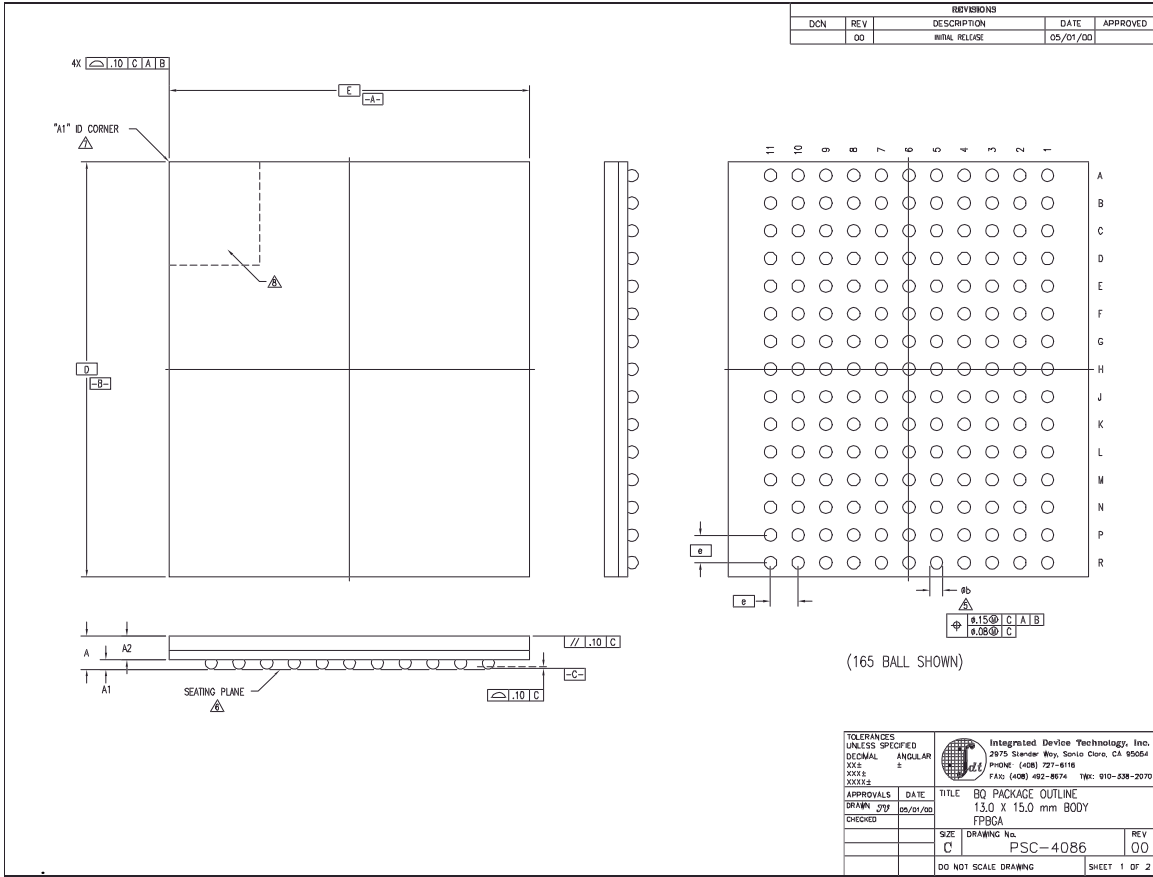
100-Pin Plastic Thin Quad Flatpack (TQFP) Package Diagram Outline



119 Ball Grid Array (BGA) Package Diagram Outline



165 Ball Grid Array (fBGA) Package Diagram Outline



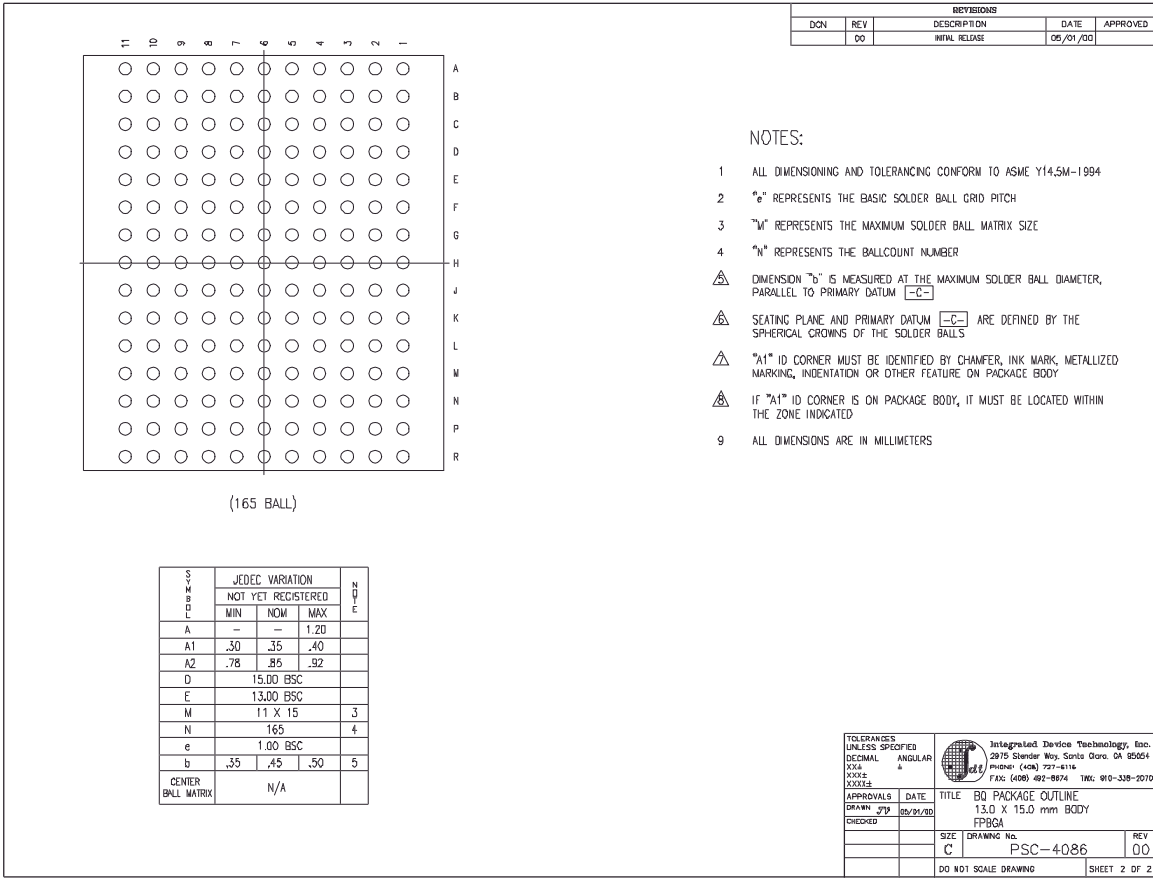
TOLERANCES UNLESS SPECIFIED
 DECIMAL ANGULAR
 XXXX &
 XXXX
 XXXX

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 2875 Slender Way, Santa Clara, CA 95054
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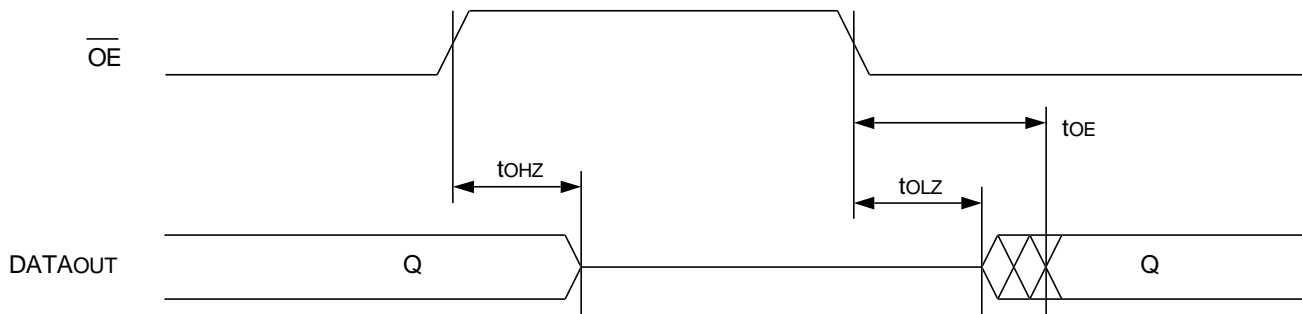
APPROVALS DATE TITLE
 DRAWN JTP 05/01/00 BO PACKAGE OUTLINE
 CHECKED 13.0 X 15.0 mm BODY
 FFBGA

SIZE DRAWING No. REV
 C PSC-4086 00

DO NOT SCALE DRAWING SHEET 1 OF 2



Timing Waveform of \overline{OE} Operation⁽¹⁾

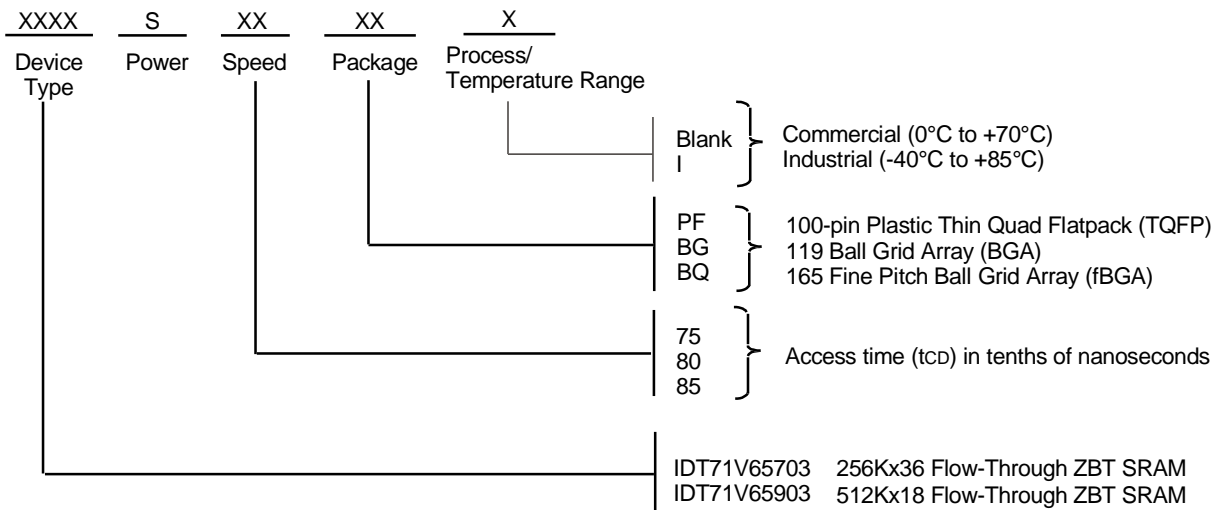


5298 drw 11

NOTE:

1. A read operation is assumed to be in progress.

Ordering Information



5298 drw 12

Datasheet Document History

12/31/99		Created new part number and datasheet from 71V657/59 to 71v65703/5903
04/20/00	Pg.5,6	Add JTAG reset pins to TQFP pin configuration; removed footnote
	Pg. 7	Add clarification note to Recommended Operating Temperature and Absolute Max Ratings tables
	Pg. 21	Add note to BGA pin configuration; corrected typo within pinout
05/23/00		Insert TQFP Package Diagram Outline
	Pg. 23	Add new package offering: 13mm x 15mm, 165 fine pitch ball grid array
	Pg. 23	Correction on 119 Ball Grid Array Package diagram Outline
07/28/00	Pg. 5-8	Remove JTAG pins from TQFP, BG119 and BQ165 pinouts, refer to IDT71V656xx and IDT71V658xx device errata sheet
	Pg. 7,8	Correct error in pinout, B2 on BG119 and B1 on BQ165 pinout
	Pg. 23	Update BG119 package diagram dimensions
11/04/00	Pg. 8	Add reference note to pin N5 on the BQ165 pinout, reserved for JTAG $\overline{\text{TRST}}$
	Pg. 15	Add I _{zz} to DC Electrical Characteristics
12/04/02	Pg. 1-25	Changed datasheet from Preliminary to final release.
	Pg. 5,6,15,16,25	Added I _{temp} to datasheet
12/18/02	Pg. 1,2,5,6,7,8	Removed JTAG functionality for current die revision.
	Pg. 7	Corrected pin configuration on the x36, 119 BGA. Switched pins I/O0 and I/OP1.
03/02/09	Pg. 25	Removed "IDT" from orderable part number.



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Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

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