# LINEAR TECHNOLOGY

## LTC1606
## 16-Bit, 250ksps, Single Supply ADC

## FEATURES

- **Sample Rate: 250ksps**
- **Single 5V Supply**
- **Bipolar Input Range: ±10V**
- **Signal-to-Noise Ratio: 90dB Typ**
- **Power Dissipation: 75mW Typ**
- **Guaranteed No Missing Codes**
- Integral Nonlinearity: ±2.0LSB Max
- Operates with Internal or External Reference
- Internal Synchronized Clock
- 28-Pin SSOP and SO Packages
- 100ksps Version (LTC1605)
- Improved 2nd Source to AD976A and ADS7805
- Available in 28-Lead Plastic SSOP and SO Packages

## APPLICATIONS

- Industrial Process Control
- Multiplexed Data Acquisition Systems
- High Speed Data Acquisition for PCs
- Digital Signal Processing

## DESCRIPTION

The LTC®1606 is a 250ksps, sampling 16-bit A/D converter that draws only 75mW (typical) from a single 5V supply. This easy-to-use device includes sample-and-hold, precision reference, switched capacitor successive approximation A/D and trimmed internal clock.

The LTC1606's input range is an industry standard ±10V. Maximum DC specs include ±2.0LSB INL and 16 bits no missing codes over temperature. An external reference can be used if greater accuracy over temperature is needed.

The 90dB signal-to-noise ratio offers an improvement of 3dB over competing devices, and the RMS transition noise is reduced (0.65LSB vs 1LSB) relative to competitive parts.

The ADC has a microprocessor compatible, 16-bit or two byte parallel output port. A convert start input and a data ready signal (BUSY) ease connections to FIFOs, DSPs and microprocessors.
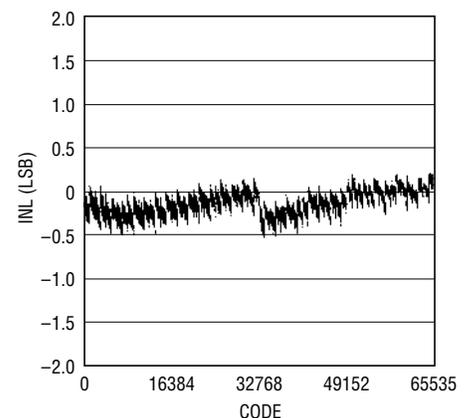
## BASIC CONFIGURATION

**Low Power, 250kHz, 16-Bit Sampling ADC on 5V Supply**



1606 TA01
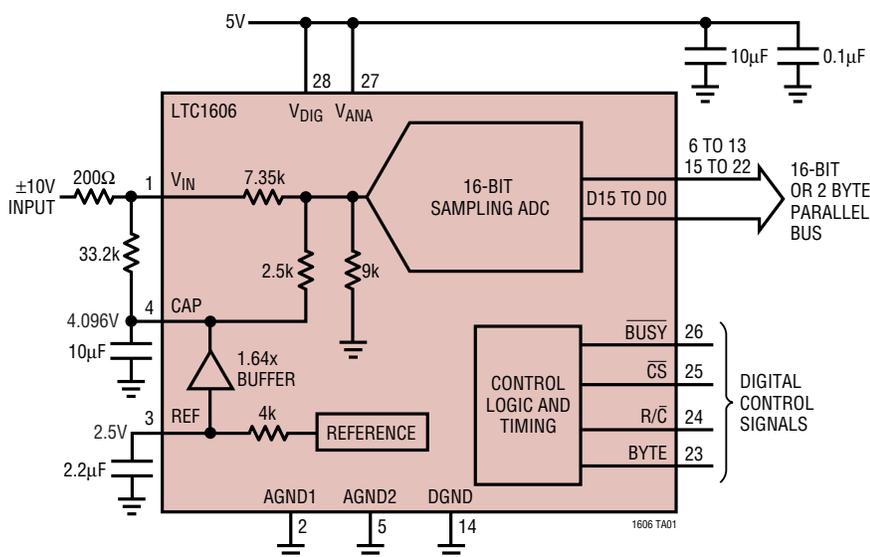
**Typical INL Curve**



1606 G04

# ABSOLUTE MAXIMUM RATINGS

**(Notes 1, 2)**

$V_{ANA}$ ................................................................. 7V
$V_{DIG}$ to $V_{ANA}$ ............................................... 0.3V
$V_{DIG}$ ............................................................... 7V
Ground Voltage Difference
   DGND, AGND1 and AGND2 ............................. ±0.3V
Analog Inputs (Note 3)
   $V_{IN}$ ............................................................ ±25V
   CAP ............................ $V_{ANA}$ + 0.3V to AGND2 – 0.3V
   REF ...................................... Indefinite Short to AGND2
                     Momentary Short to $V_{ANA}$
Digital Input Voltage (Note 4) ........ $V_{DGND}$ – 0.3V to 10V
Digital Output Voltage ........ $V_{DGND}$ – 0.3V to $V_{DIG}$ + 0.3V
Power Dissipation ............................................. 500mW
Operating Ambient Temperature Range
   LTC1606AC/LTC1606C ............................. 0°C to 70°C
   LTC1606AI/LTC1606I ......................... –40°C to 85°C
Storage Temperature Range ................. –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ................. 300°C

# PACKAGE/ORDER INFORMATION

TOP VIEW

| | | | |
|---|---|---|---|
| $V_{IN}$ | 1 | 28 | $V_{DIG}$ |
| AGND1 | 2 | 27 | $V_{ANA}$ |
| REF | 3 | 26 | $\overline{BUSY}$ |
| CAP | 4 | 25 | $\overline{CS}$ |
| AGND2 | 5 | 24 | R/$\overline{C}$ |
| D15 (MSB) | 6 | 23 | BYTE |
| D14 | 7 | 22 | D0 |
| D13 | 8 | 21 | D1 |
| D12 | 9 | 20 | D2 |
| D11 | 10 | 19 | D3 |
| D10 | 11 | 18 | D4 |
| D9 | 12 | 17 | D5 |
| D8 | 13 | 16 | D6 |
| DGND | 14 | 15 | D7 |

G PACKAGE
28-LEAD PLASTIC SSOP

SW PACKAGE
28-LEAD PLASTIC SO

$T_{JMAX} = 125°C, \theta_{JA} = 95°C/W$ (G)
$T_{JMAX} = 125°C, \theta_{JA} = 130°C/W$ (SW)

# CONVERTER CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Notes 5, 6)

| PARAMETER | CONDITIONS | | LTC1606 MIN | TYP | MAX | LTC1606A MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Resolution | | ● | 16 | | | 16 | | | Bits |
| No Missing Codes | | ● | 15 | | | 16 | | | Bits |
| Transition Noise | | | | 0.65 | | | 0.65 | | LSB$_{RMS}$ |
| Integral Linearity Error | (Note 7) | ● | | | ±3 | | | ±2 | LSB |
| Bipolar Zero Error | Ext. Reference = 2.5V (Note 8) | ● | | | ±10 | | | ±10 | mV |
| Bipolar Zero Error Drift | | | | ±2 | | | ±2 | | ppm/°C |
| Full-Scale Error Drift | | | | ±7 | | | ±5 | | ppm/°C |
| Full-Scale Error | Ext. Reference = 2.5V (Notes 12, 13) | ● | | | ±0.50 | | | ±0.25 | % |
| Full-Scale Error Drift | Ext. Reference = 2.5V | | | ±2 | | | ±2 | | ppm/°C |
| Power Supply Sensitivity $V_{ANA} = V_{DIG} = V_{DD}$ | $V_{DD} = 5V ±5%$ (Note 9) | | | | ±8 | | | ±8 | LSB |

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## ANALOG INPUT
The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5)

| SYMBOL | PARAMETER | CONDITIONS | | LTC1606/LTC1606A MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Analog Input Range (Note 9) | $4.75V \leq V_{ANA} \leq 5.25V$, $4.75V \leq V_{DIG} \leq 5.25V$ | ● | | ±10 | | V |
| $C_{IN}$ | Analog Input Capacitance | | | | 10 | | pF |
| $R_{IN}$ | Analog Input Impedance | | | | 10 | | kΩ |

## DYNAMIC ACCURACY (Notes 5, 14)

| SYMBOL | PARAMETER | CONDITIONS | LTC1606 MIN | TYP | MAX | LTC1606A MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| S/(N + D) | Signal-to-(Noise + Distortion) Ratio | 1kHz Input Signal (Note 14)<br>10kHz Input Signal<br>20kHz, −60dB Input Signal | 83 | 90<br>90<br>30 | | 87 | 90<br>90<br>30 | | dB<br>dB<br>dB |
| THD | Total Harmonic Distortion | 1kHz Input Signal, First 5 Harmonics<br>10kHz Input Signal, First 5 Harmonics | −87 | −102<br>−94 | | −89 | −102<br>−94 | | dB<br>dB |
| | Peak Harmonic or Spurious Noise | 1kHz Input Signal<br>10kHz Input Signal | | −102<br>−94 | | | −102<br>−94 | | dB<br>dB |
| | Full-Power Bandwidth | (Note 15) | | 275 | | | 275 | | kHz |
| | Aperture Delay | | | 40 | | | 40 | | ns |
| | Aperture Jitter | | Sufficient to Meet AC Specs | | | Sufficient to Meet AC Specs | | | |
| | Transient Response | Full-Scale Step (Note 9) | | 1 | | | 1 | | µs |
| | Overvoltage Recovery | (Note 16) | | 150 | | | 150 | | ns |

## INTERNAL REFERENCE CHARACTERISTICS
The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5)

| PARAMETER | CONDITIONS | | LTC1606/LTC1606A MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{REF}$ Output Voltage | $I_{OUT} = 0$ | ● | 2.470 | 2.500 | 2.520 | V |
| $V_{REF}$ Output Tempco | $I_{OUT} = 0$ | | | ±5 | | ppm/°C |
| Internal Reference Source Current | | | | 1 | | µA |
| External Reference Voltage for Specified Linearity | (Notes 9, 10) | | 2.30 | 2.50 | 2.70 | V |
| External Reference Current Drain | Ext. Reference = 2.5V (Note 9) | ● | | | 100 | µA |
| CAP Output Voltage | $I_{OUT} = 0$ | | | 4.096 | | V |

## DIGITAL INPUTS AND DIGITAL OUTPUTS  The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5)

| SYMBOL | PARAMETER | CONDITIONS | | | LTC1606/LTC1606A MIN | TYP | MAX | UNITS |
|--------|-----------|------------|---|---|-----|-----|-----|-------|
| $V_{IH}$ | High Level Input Voltage | $V_{DD} = 5.25V$ | | ● | 2.4 | | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{DD} = 4.75V$ | | ● | | | 0.8 | V |
| $I_{IN}$ | Digital Input Current | $V_{IN} = 0V$ to $V_{DD}$ | | ● | | | ±10 | μA |
| $C_{IN}$ | Digital Input Capacitance | | | | | 5 | | pF |
| $V_{OH}$ | High Level Output Voltage | $V_{DD} = 4.75V$ | $I_O = -10μA$ | | | 4.5 | | V |
| | | | $I_O = -200μA$ | ● | 4.0 | | | V |
| $V_{OL}$ | Low Level Output Voltage | $V_{DD} = 4.75V$ | $I_O = 160μA$ | | | 0.05 | | V |
| | | | $I_O = 1.6mA$ | ● | | 0.10 | 0.4 | V |
| $I_{OZ}$ | Hi-Z Output Leakage D15 to D0 | $V_{OUT} = 0V$ to $V_{DD}$, $\overline{CS}$ High | | ● | | | ±10 | μA |
| $C_{OZ}$ | Hi-Z Output Capacitance D15 to D0 | $\overline{CS}$ High (Note 9) | | ● | | | 15 | pF |
| $I_{SOURCE}$ | Output Source Current | $V_{OUT} = 0V$ | | | | −10 | | mA |
| $I_{SINK}$ | Output Sink Current | $V_{OUT} = V_{DD}$ | | | | 10 | | mA |

## TIMING CHARACTERISTICS  The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5)

| SYMBOL | PARAMETER | CONDITIONS | | LTC1606/LTC1606A MIN | TYP | MAX | UNITS |
|--------|-----------|------------|---|-----|-----|-----|-------|
| $f_{SAMPLE(MAX)}$ | Maximum Sampling Frequency | | ● | 250 | | | kHz |
| $t_{CONV}$ | Conversion Time | | ● | | | 2.5 | μs |
| $t_{ACQ}$ | Acquisition Time | | ● | | | 1.5 | μs |
| $t_1$ | Convert Pulse Width | (Note 11) | ● | 40 | | | ns |
| $t_2$ | Data Valid Delay After R/$\overline{C}$↓ | (Note 9) | ● | | | 2.5 | μs |
| $t_3$ | $\overline{BUSY}$ Delay from R/$\overline{C}$↓ | $C_L = 30pF$ | ● | | | 65 | ns |
| $t_4$ | $\overline{BUSY}$ Low | | ● | | | 2.5 | μs |
| $t_5$ | $\overline{BUSY}$ Delay After End of Conversion | | | | 100 | | ns |
| $t_6$ | Aperture Delay | | | | 40 | | ns |
| $t_7$ | Bus Relinquish Time | | ● | | 15 | 50 | ns |
| $t_8$ | $\overline{BUSY}$ Delay After Data Valid | | ● | 20 | 90 | | ns |
| $t_9$ | Previous Data Valid After R/$\overline{C}$↓ | | | | 2 | | μs |
| $t_{10}$ | R/$\overline{C}$ to $\overline{CS}$ Setup Time | (Notes 9, 10) | ● | 5 | | | ns |
| $t_{11}$ | Time Between Conversions | | ● | 4 | | | μs |
| $t_{12}$ | Bus Access | $C_L = 30pF$ | ● | | 15 | 60 | ns |
| | Byte Delay | $C_L = 30pF$ (Notes 9, 10) | ● | | 15 | 60 | ns |

# POWER REQUIREMENTS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5)

| SYMBOL | PARAMETER | CONDITIONS | | LTC1606/LTC1606A MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Positive Supply Voltage | (Notes 9, 10) | | 4.75 | | 5.25 | V |
| $I_{DD}$ | Positive Supply Current | | ● | | 15 | 20 | mA |
| $P_{DIS}$ | Power Dissipation | | ● | | 75 | 100 | mW |

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All voltage values are with respect to ground with DGND, AGND1 and AGND2 wired together (unless otherwise noted).

**Note 3:** When these pin voltages are taken below ground or above $V_{ANA} = V_{DIG} = V_{DD}$, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below ground or above $V_{DD}$ without latch-up.

**Note 4:** When these pin voltages are taken below ground, they will be clamped by internal diodes. This product can handle input currents of 90mA below ground without latchup. These pins are not clamped to $V_{DD}$.

**Note 5:** $V_{DD}$ = 5V, $f_{SAMPLE}$ = 250kHz, $t_r = t_f$ = 5ns unless otherwise specified.

**Note 6:** Linearity, offset and full-scale specifications apply for a $V_{IN}$ input with respect to ground.

**Note 7:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual end points of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 8:** Bipolar offset is the offset voltage measured from −0.5 LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111.

**Note 9:** Guaranteed by design, not subject to test.

**Note 10:** Recommended operating conditions.

**Note 11:** With $\overline{CS}$ low the falling R/$\overline{C}$ edge starts a conversion. If R/$\overline{C}$ returns high at a critical point during the conversion, it can create errors. For best results, ensure that R/$\overline{C}$ returns high within 1μs after the start of the conversion.

**Note 12:** As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer.

**Note 13:** Full-scale error is the worst-case of −FS or +FS untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error.
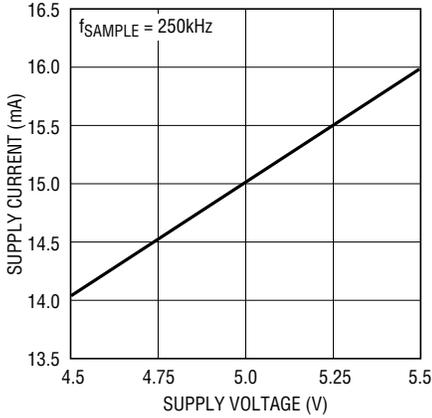
**Note 14:** All specifications in dB are referred to a full-scale ±10V input.

**Note 15:** Full-power bandwidth is defined as full-scale input frequency at which a signal-to-(noise + distortion) degrades to 60dB or 10 bits of accuracy.

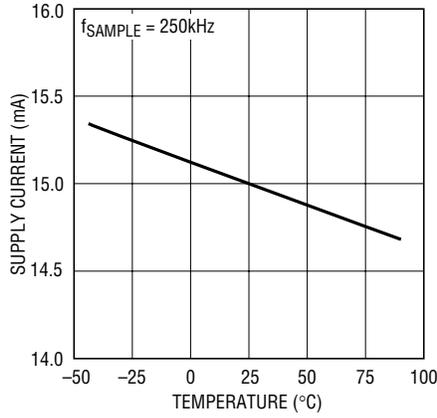**Note 16:** Recovers to specified performance after (2 • FS) input overvoltage.

# TYPICAL PERFORMANCE CHARACTERISTICS
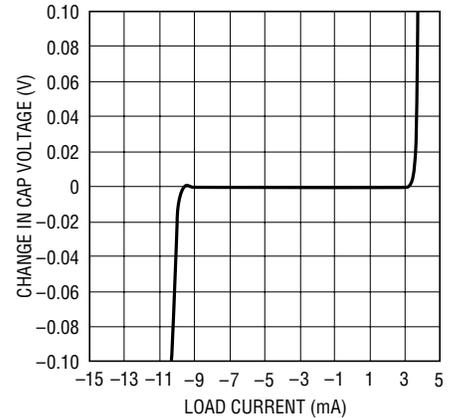
**Supply Current vs Supply Voltage**



1606 G01
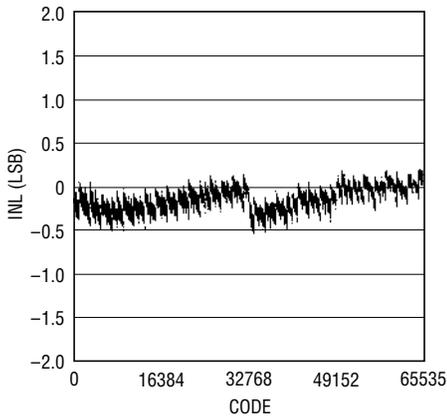
**Supply Current vs Temperature**
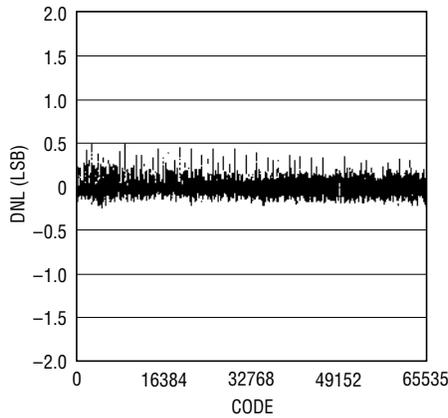


1606 G02

**Change in CAP Voltage vs Load Current**
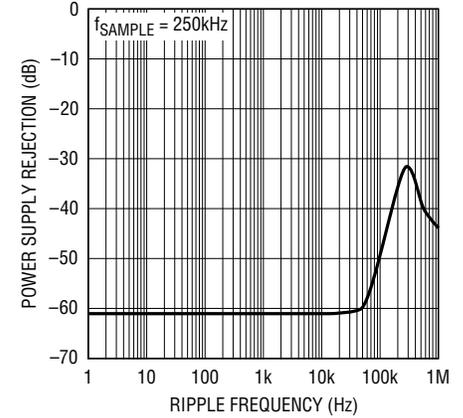


1606 G03

**Typical INL Curve**



1606 G04

**Typical DNL Curve**



1606 G04

**Power Supply Rejection vs Ripple Frequency**



LT1606 G06

**Nonaveraged 4096 Point FFT Plot**

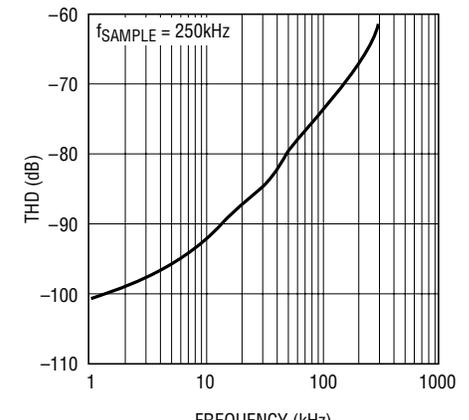

$f_{SAMPLE}$ = 250kHz
$f_{IN}$ = 1.04kHz
SINAD = 90dB
THD = −100dB
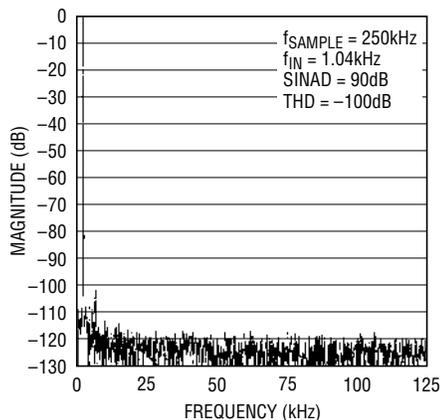
1606 G07

**SINAD vs Input Frequency**
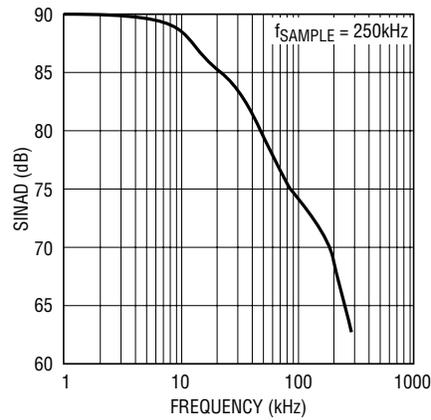


1606 G08

**Total Harmonic Distortion (THD) vs Input Frequency**



1606 G09

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# PIN FUNCTIONS

**V$_{IN}$ (Pin 1):** Analog Input. Connect through a 200Ω resistor to the analog input. Full-scale input range is ±10V.

**AGND1 (Pin 2):** Analog Ground. Tie to analog ground plane.

**REF (Pin 3):** 2.5V Reference Output. Bypass with 2.2µF tantalum capacitor. Can be driven with an external reference.

**CAP (Pin 4):** Reference Buffer Output. Bypass with 10µF tantalum capacitor. The capacitor output voltage is 4.096V when REF = 2.5V.

**AGND2 (Pin 5):** Analog Ground. Tie to analog ground plane.

**D15 to D8 (Pins 6 to 13):** Three-State Data Outputs. Hi-Z state when $\overline{CS}$ is high or when R/$\overline{C}$ is low.

**DGND (Pin 14):** Digital Ground.

**D7 to D0 (Pins 15 to 22):** Three-State Data Outputs. Hi-Z state when $\overline{CS}$ is high or when R/$\overline{C}$ is low.

**BYTE (Pin 23):** Byte Select. With BYTE low, data will be output with Pin 6 (D15) being the MSB and Pin 22 (D0)

being the LSB. With BYTE high, the upper eight bits and the lower eight bits will be switched. The MSB is output on Pin 15 and bit 8 is output on Pin 22. Bit 7 is output on Pin 6 and the LSB is output on Pin 13.

**R/$\overline{C}$ (Pin 24):** Read/$\overline{Convert}$ Input. With $\overline{CS}$ low, a falling edge on R/$\overline{C}$ puts the internal sample-and-hold into the hold state and starts a conversion. With $\overline{CS}$ low, a rising edge on R/$\overline{C}$ enables the output data bits.

**$\overline{CS}$ (Pin 25):** Chip Select. Internally OR'd with R/$\overline{C}$. With R/$\overline{C}$ low, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ high, a falling edge on $\overline{CS}$ will enable the output data.

**$\overline{BUSY}$ (Pin 26):** Output Shows Converter Status. It is low when a conversion is in progress. Data valid on the rising edge of $\overline{BUSY}$. $\overline{CS}$ or R/$\overline{C}$ must be high when BUSY rises or another conversion will start without time for signal acquisition.

**V$_{ANA}$ (Pin 27):** 5V Analog Supply. Bypass to ground with a 0.1µF ceramic and a 10µF tantalum capacitor.

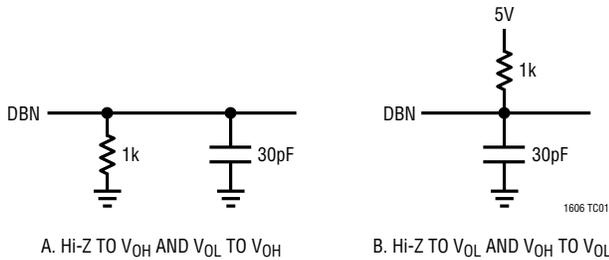**V$_{DIG}$ (Pin 28):** 5V Digital Supply. Connect directly to Pin 27.
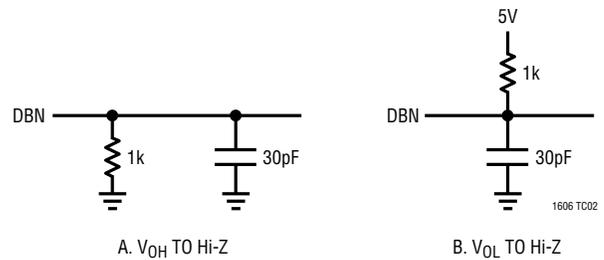
# FUNCTIONAL BLOCK DIAGRAM
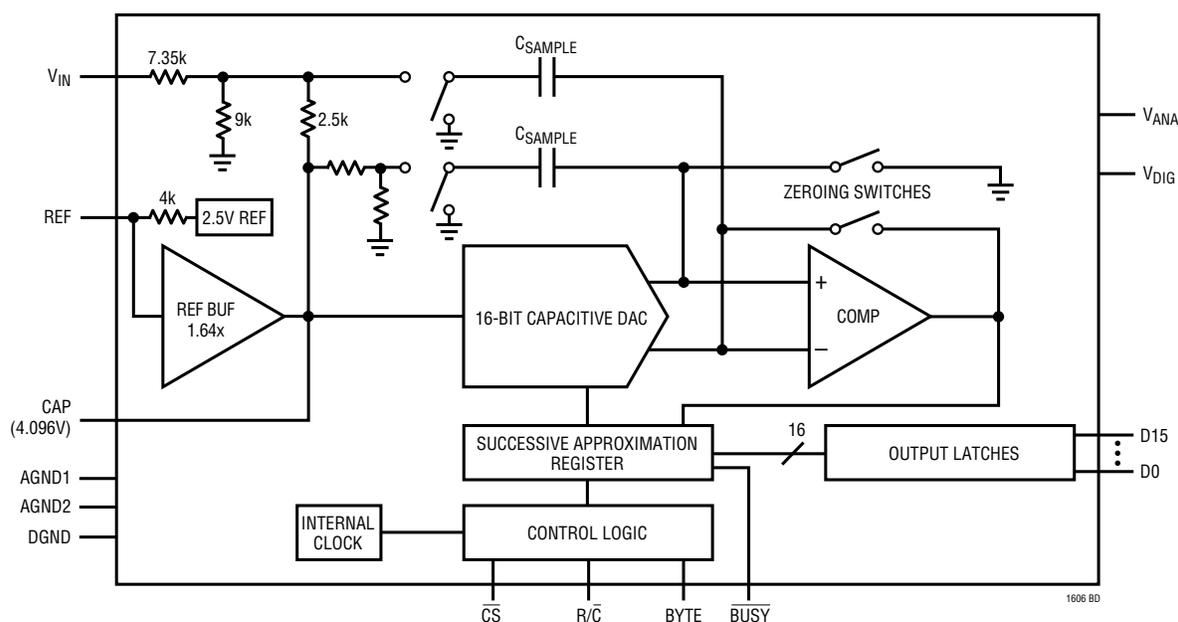
1606fa

# TEST CIRCUITS

**Load Circuit for Access Timing**

**Load Circuit for Output Float Delay**



A. Hi-Z TO $V_{OH}$ AND $V_{OL}$ TO $V_{OH}$

B. Hi-Z TO $V_{OL}$ AND $V_{OH}$ TO $V_{OL}$

1606 TC01

A. $V_{OH}$ TO Hi-Z

B. $V_{OL}$ TO Hi-Z

1606 TC02

# APPLICATIONS INFORMATION

## Conversion Details

The LTC1606 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 16-bit or two byte parallel output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

Conversion start is controlled by the $\overline{CS}$ and R/$\overline{C}$ inputs. At the start of conversion, the successive approximation register (SAR) is reset. Once a conversion cycle has begun, it cannot be restarted.

During the conversion, the internal 16-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, $V_{IN}$ is connected through the resistor divider to

the sample-and-hold capacitor during the acquire phase and the comparator offset is nulled by the autozero switches. In this acquire phase, a minimum delay of 1.5µs will provide enough time for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the autozero switches open, putting the comparator into the compare mode. The input switch switches $C_{SAMPLE}$ to ground, injecting the analog input charge onto the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the DAC output balances the $V_{IN}$ input charge. The SAR contents (a 16-bit data word) that represents the $V_{IN}$ are loaded into the 16-bit output latches.

## Driving the Analog Inputs

The nominal input range for the LTC1606 is ±10V or ($\pm 4 \bullet V_{REF}$) and the input is overvoltage protected to ±25V. The input impedance is typically 10kΩ, therefore, it should be driven with a low impedance source. Wideband noise coupling into the input can be minimized by placing a 1000pF capacitor at the input as shown in Figure 2. An NPO-type capacitor gives the lowest distortion. Place the
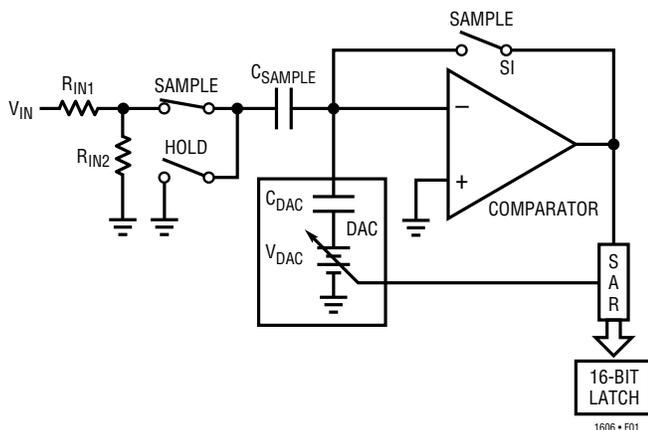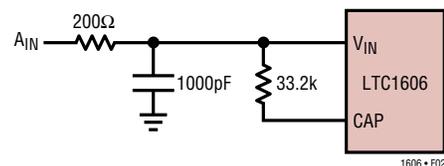


Figure 1. LTC1606 Simplified Equivalent Circuit



Figure 2. Analog Input Filtering

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# APPLICATIONS INFORMATION

capacitor as close to the device input pin as possible. If an amplifier is to be used to drive the input, care should be taken to select an amplifier with adequate accuracy, linearity and noise for the application. The following list is a summary of the op amps that are suitable for driving the LTC1606. More detailed information is available in the Linear Technology data books and LinearView™ CD-ROM.

LT1007: Low noise precision amplifier. 2.7mA supply current ±5V to ±15V supplies. Gain bandwidth product 8MHz. DC applications.

LT1097: Low cost, low power precision amplifier. 300µA supply current. ±5V to ±15V supplies. Gain bandwidth product 0.7MHz. DC applications.

LT1227: 140MHz video current feedback amplifier. 10mA supply current. ±5V to ±15V supplies. Low noise and low distortion.

LT1360: 37MHz voltage feedback amplifier. 3.8mA supply current. ±5V to ±15V supplies. Good AC/DC specs.

LT1363: 50MHz voltage feedback amplifier. 6.3mA supply current. Good AC/DC specs.

LT1364/LT1365: Dual and quad 50MHz voltage feedback amplifiers. 6.3mA supply current per amplifier. Good AC/DC specs.

LT1468: 90MHz 22V/µs 16-bit accurate amplifier.

LT1469: Dual LT1468

## Internal Voltage Reference

The LTC1606 has an on-chip, temperature compensated, curvature corrected, bandgap reference, which is factory trimmed to 2.50V. The full-scale range of the ADC is equal to (±4 • $V_{REF}$) or nominally ±10V. The output of the reference is connected to the input of a buffer (1.64x) through a 4k resistor (see Figure 3). The input to the buffer or the output of the reference is available at REF (Pin 3). The internal reference can be overdriven with an external reference if more accuracy is needed. The buffer output drives the internal DAC and is available at CAP (Pin 4). The CAP pin can be used to drive a steady DC load of less than 2mA. Driving an AC load is not recommended because it can cause the performance of the converter to degrade.

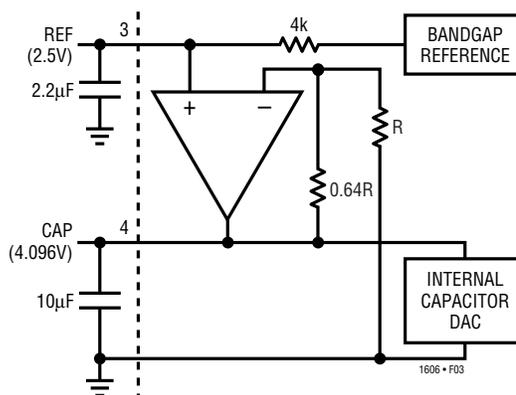LinearView is a trademark of Linear Technology Corporation



Figure 3. Internal or External Reference Source

For minimum code transition noise, the REF pin and the CAP pin should each be decoupled with a capacitor to filter wideband noise from the reference and the buffer (2.2µF tantalum for the REF pin and 10µF tantalum for the CAP pin). To prevent the 10µF bypass capacitor from discharging through the CAP pin if the positive supply ($V_{DIG}$ and $V_{ANA}$) were to drop, a diode (1N4148 or equivalent) can be placed between the CAP pin and the positive supply.

## Offset and Gain Adjustments

The LTC1606 offset and full-scale errors have been trimmed at the factory with the external resistors shown in Figure 4. This allows for external adjustment of offset and full scale in applications where absolute accuracy is important. See Figure 5 for the offset and gain trim circuit. The 100k resistor in parallel with the 33.2k is only needed for externally trimming the offset. First, adjust the offset to zero by adjusting resistor R3. Apply an input voltage of –152.6µV (–0.5LSB) and adjust R3 so the code is
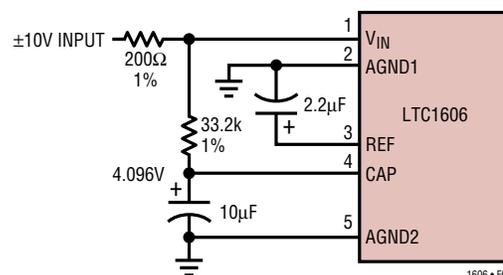


Figure 4. ±10V Input Without Trim

# APPLICATIONS INFORMATION

changing between 1111 1111 1111 1111 and 0000 0000 0000 0000. The gain error is trimmed by adjusting resistor R4. An input voltage of 9.999542V (+FS − 1.5LSB) is applied to $V_{IN}$ and R4 is adjusted until the output code is changing between 0111 1111 1111 1110 and 0111 1111 1111 1111. Figure 6 shows the bipolar transfer characteristic of the LTC1606.
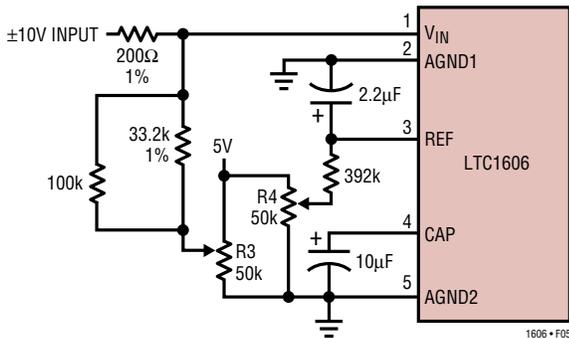


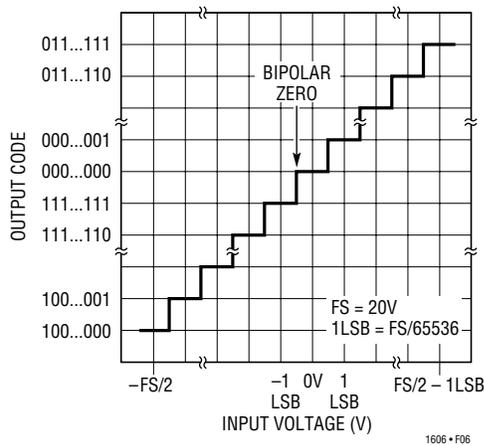**Figure 5. ±10V Input with Offset and Gain Trim**



**Figure 6. LTC1606 Bipolar Transfer Characteristics**

If the external resistors are not used, the resulting offset and gain error ranges are shown in Table 1.

## DC Performance

One way of measuring the transition noise associated with a high resolution ADC is to use a technique where a DC signal is applied to the input of the ADC and the resulting output codes are collected over a large number of conversions. For example in Figure 7, the distribution of output code is shown for a DC input that has been digitized 4096 times. The distribution is Gaussian and the RMS code transition is about 0.65LSB.

## DIGITAL INTERFACE

### Internal Clock

The ADC has an internal clock that is trimmed to achieve a typical conversion time of 2.3μs. No external adjustments are required and, with the typical acquisition time of 1μs, throughput performance of 250ksps is assured.
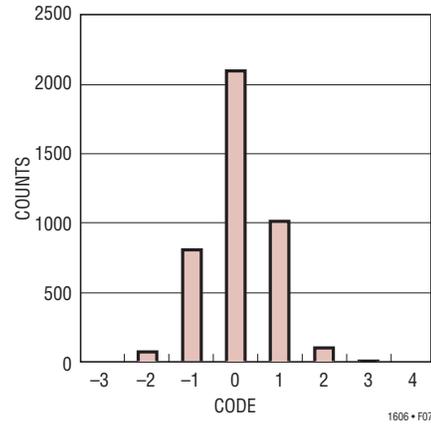


**Figure 7. Histogram for 4096 Conversions**

**Table 1**

| ERROR TERM | WITH BOTH EXTERNAL RESISTORS INCLUDED | WITHOUT THE EXTERNAL 33.2k RESISTOR | WITHOUT EITHER EXTERNAL RESISTOR INCLUDED |
|---|---|---|---|
| Offset Error | −10mV < Error < 10mV | 10mV < Error< 55mV | 54mV < Error < 155mV |
| +Full-Scale Error | −0.25% < Error < 0.25% <br> −0.50% < Error < 0.50% | −1.3% < Error < −0.10% | −3.40% < Error < −0.85% |
| −Full-Scale Error | −0.25% < Error < 0.25% <br> −0.50% < Error < 0.50% | 0.25% < Error < 1.40% | 2.10% < Error < 6.15% |

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# APPLICATIONS INFORMATION

**Timing and Control**

Conversion start and data read are controlled by two digital inputs: $\overline{CS}$ and R/$\overline{C}$. To start a conversion and put the sample-and-hold into the hold mode, bring $\overline{CS}$ and R/$\overline{C}$ low for no less than 40ns. Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output and this is low while the conversion is in progress.

There are two modes of operation. The first mode is shown in Figure 8. The digital input R/$\overline{C}$ is used to control the start of conversion. $\overline{CS}$ is tied low. When R/$\overline{C}$ goes low, the sample-and-hold goes into the hold mode and a conversion is started. $\overline{BUSY}$ goes low and stays low during the conversion and will go back high after the conversion has been completed and the internal output shift registers have been updated. R/$\overline{C}$ should remain low for no less than 40ns. During the time R/$\overline{C}$ is low, the digital outputs are in a Hi-Z state. R/$\overline{C}$ should be brought back high within 1µs after the start of the conversion to ensure that no errors occur in the digitized result. The second mode, shown in

Figure 9, uses the $\overline{CS}$ signal to control the start of a conversion and the reading of the digital output. In this mode the R/$\overline{C}$ input signal should be brought low no less than 10ns before the falling edge of $\overline{CS}$. The minimum pulse width for $\overline{CS}$ is 40ns. When $\overline{CS}$ falls, $\overline{BUSY}$ goes low and will stay low until the end of the conversion. $\overline{BUSY}$ will go high after the conversion has been completed. The new data is valid when $\overline{CS}$ is brought back low again to initiate a read. Again, it is recommended that both R/$\overline{C}$ and $\overline{CS}$ return high within 1µs after the start of the conversion.

**Output Data**

The output data can be read as a 16-bit word or it can be read as two 8-bit bytes. The format of the output data is two's complement. The digital input pin BYTE is used to control the two byte read. With the BYTE pin low, the first eight MSBs are output on the D15 to D8 pins and the eight LSBs are output on the D7 to D0 pins. When the BYTE pin is taken high, the eight LSBs replace the eight MSBs (Figure 10).



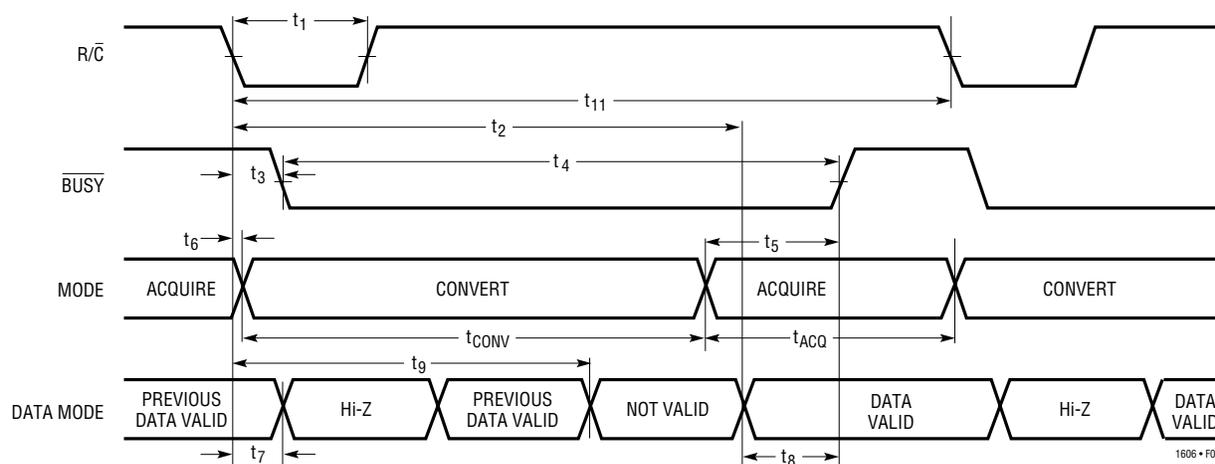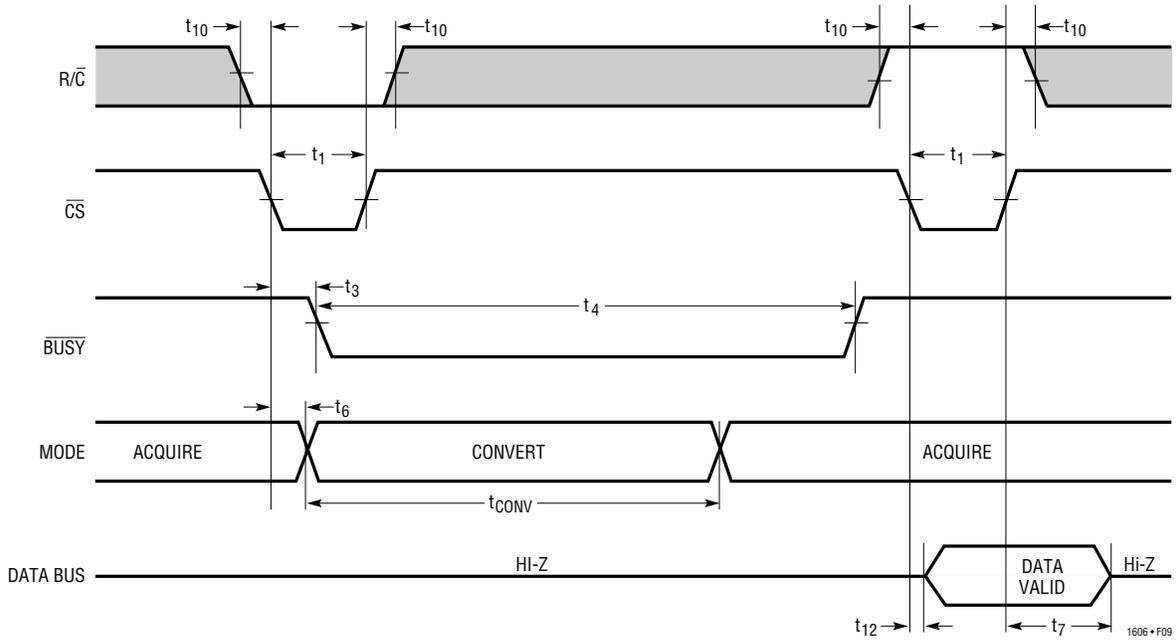**Figure 8. Conversion Timing with Outputs Enabled After Conversion ($\overline{CS}$ Tied Low)**

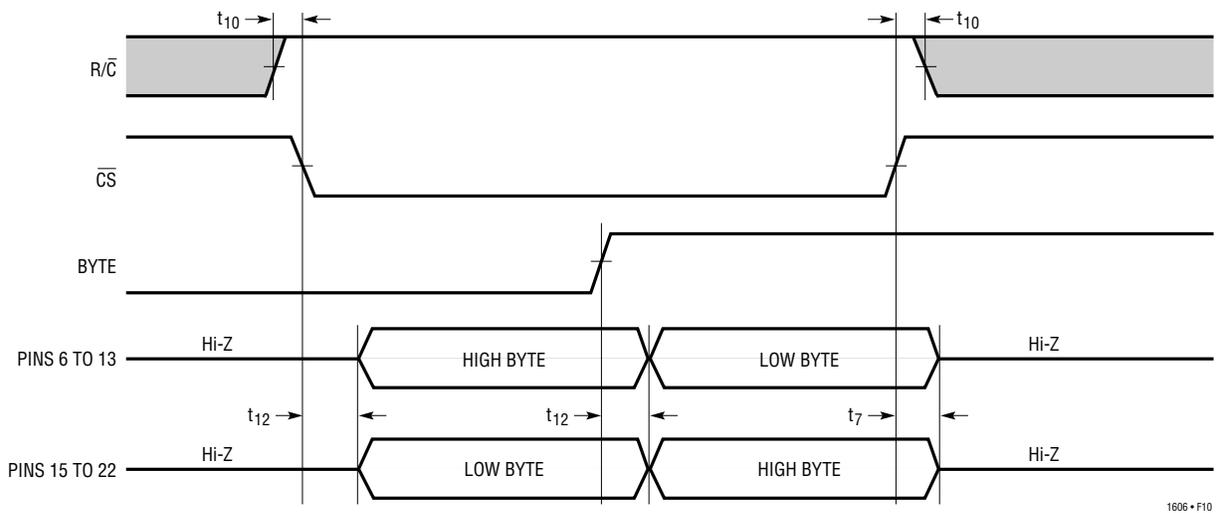**Figure 9. Using $\overline{CS}$ to Control Conversion and Read Timing**



**Figure 10. Using $\overline{CS}$ and BYTE to Control Data Bus Read Timing**

# APPLICATIONS INFORMATION

## Dynamic Performance

FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental.

## Signal-to-Noise Ratio

The Signal-to-Noise and Distortion Ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. A typical LTC1606 has a SINAD of 90dB and THD of –100dB with a 250kHz sampling rate and a 1kHz input.

## Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 ... + V_N^2}}{V_1}$$

where $V_1$ is the RMS amplitude of the fundamental frequency and $V_2$ through $V_N$ are the amplitudes of the second through Nth harmonics.
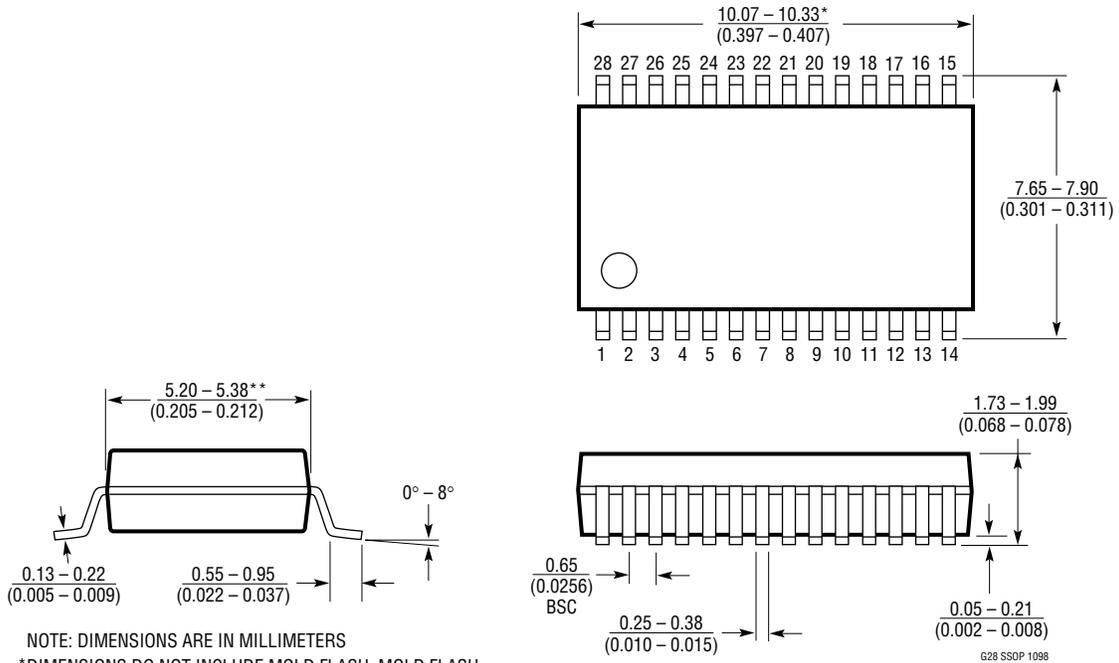
## Board Layout, Power Supplies and Decoupling

Wire wrap boards and molded sockets are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1606, a printed circuit board is required. Layout for the printed circuit board should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by AGND.

Pay particular attention to the design of the analog and digital ground planes. The DGND pin of the LTC1606 should be tied to the analog ground plane. Placing the bypass capacitor as close as possible to the power supply, the reference and reference buffer output is very important. Low impedance common returns for these bypass capacitors are essential to low noise operation of the ADC, and the foil width for these tracks should be as wide as possible. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedance as much as possible.

# PACKAGE DESCRIPTION
Dimensions in inches (millimeters) unless otherwise noted.

**G Package**
**28-Lead Plastic SSOP (0.209)**
(LTC DWG # 05-08-1640)

10.07 – 10.33*
(0.397 – 0.407)

28 27 26 25 24 23 22 21 20 19 18 17 16 15

7.65 – 7.90
(0.301 – 0.311)

1 2 3 4 5 6 7 8 9 10 11 12 13 14

5.20 – 5.38**
(0.205 – 0.212)

0° – 8°

0.13 – 0.22
(0.005 – 0.009)

0.55 – 0.95
(0.022 – 0.037)

NOTE: DIMENSIONS ARE IN MILLIMETERS
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH
 SHALL NOT EXCEED 0.152mm (0.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD
 FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

1.73 – 1.99
(0.068 – 0.078)

0.65
(0.0256)
BSC

0.25 – 0.38
(0.010 – 0.015)

0.05 – 0.21
(0.002 – 0.008)

G28 SSOP 1098

LINEAR
TECHNOLOGY

# PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

**SW Package**
**28-Lead Plastic Small Outline (Wide 0.300)**
(LTC DWG # 05-08-1620)

0.697 – 0.712*
(17.70 – 18.08)

28 27 26 25 24 23 22 21 20 19 18 17 16 15

NOTE 1

0.394 – 0.419
(10.007 – 10.643)

1 2 3 4 5 6 7 8 9 10 11 12 13 14

0.291 – 0.299**
(7.391 – 7.595)

0.010 – 0.029 × 45°
(0.254 – 0.737)

0° – 8° TYP

0.009 – 0.013
(0.229 – 0.330)

NOTE 1

0.016 – 0.050
(0.406 – 1.270)

0.093 – 0.104
(2.362 – 2.642)

0.037 – 0.045
(0.940 – 1.143)

0.050
(1.270)
BSC

0.014 – 0.019
(0.356 – 0.482)
TYP

0.004 – 0.012
(0.102 – 0.305)

S28 (WIDE) 1098
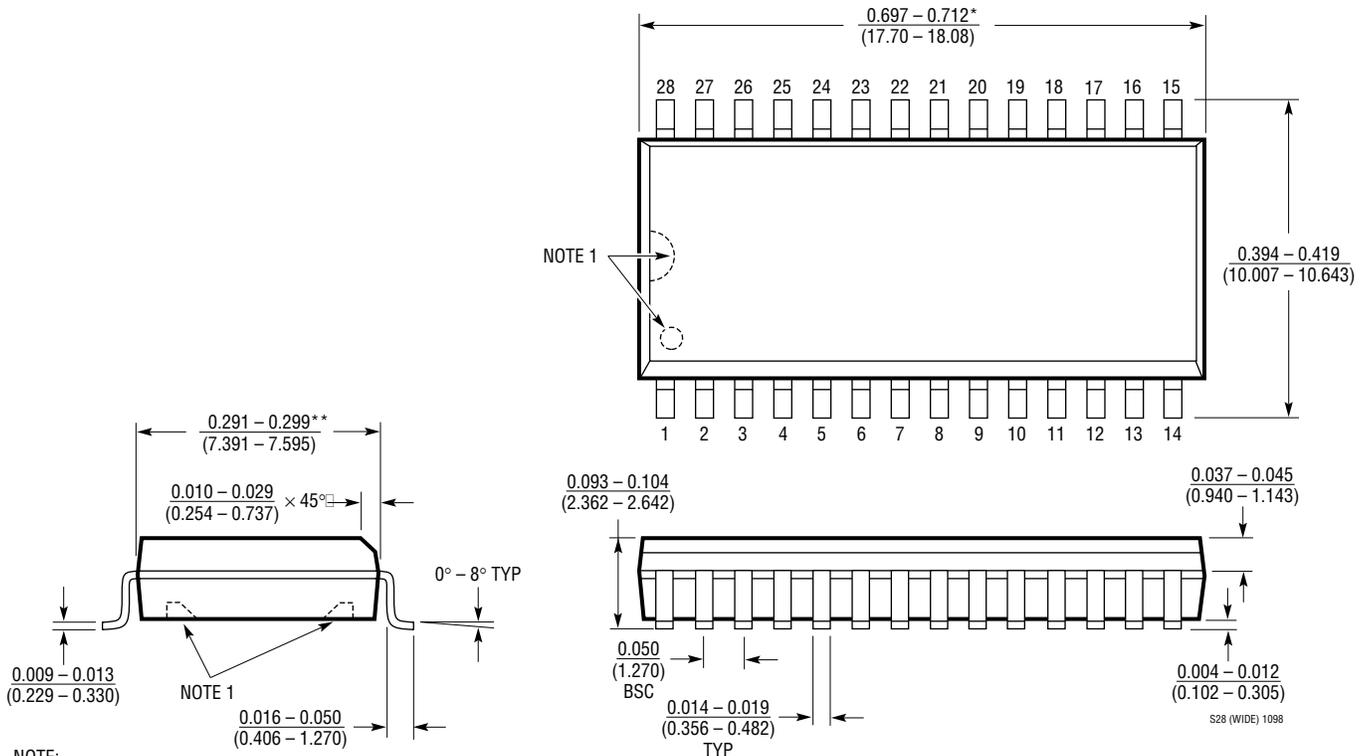
NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
   THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

 *DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

 **DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

# TYPICAL APPLICATION

**High Impedance Buffered Input Exhibits 100dB SFDR and 98dB THD Performance**



1606 TA02
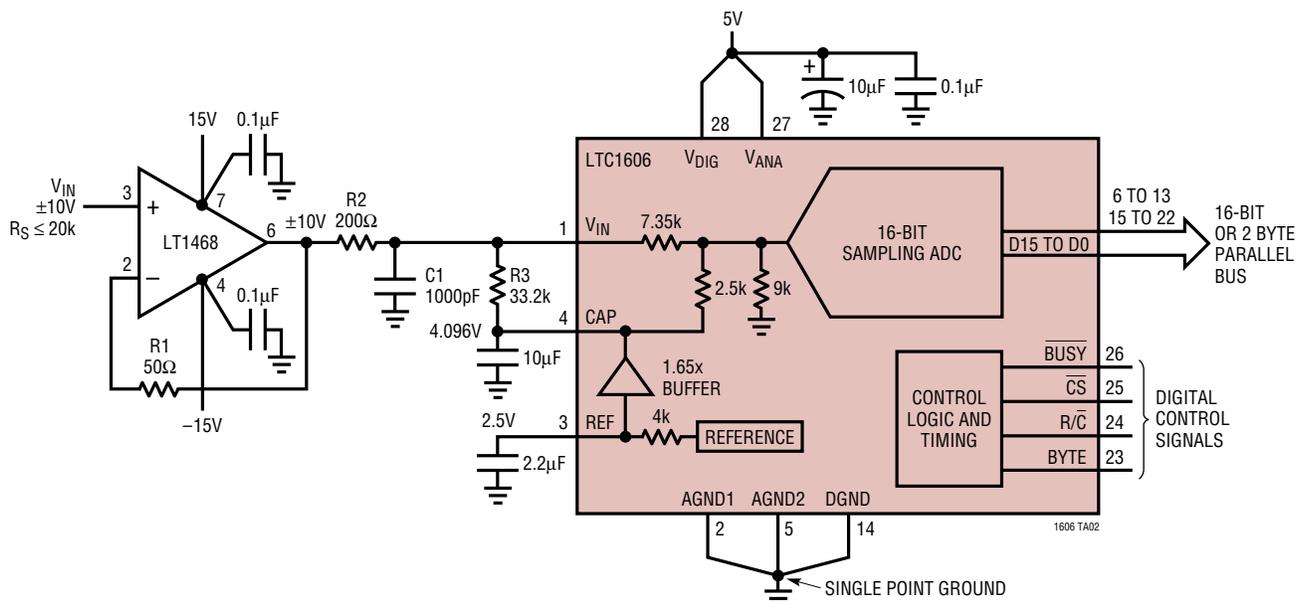
# RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1274/LTC1277 | Low Power 12-Bit, 100ksps ADCs | 10mW Power Dissipation, Parallel/Byte Interface |
| LTC1415 | Single 5V, 12-Bit, 1.25Msps ADC | 55mW Power Dissipation, 72dB SINAD |
| LTC1418 | 14-Bit, 200ksps ADC | 15mW, Serial or Parallel Interface |
| LTC1419 | Low Power 14-Bit, 800ksps ADC | True 14-Bit Linearity, 81.5dB SINAD, 150mW Dissipation |
| LT1460-2.5 | Micropower Precision Series Reference | 0.075% Max, 10ppm/°C Max, Only 130μA Supply Current |
| LT1461 | Precision Bandgap Reference | 0.04% Max, 3ppm/°C Max |
| LTC1594/LTC1598 | Micropower 4-/8-Channel 12-Bit ADCs | Serial I/O, 3V and 5V Versions |
| LTC1604 | 16-Bit, 333ksps ADC | ±2.5V Input, 90dB SINAD, 100dB THD, No Missing Codes |
| LTC1605 | 16-Bit, 100kHz ADC | Pin Compatible with LTC1606 |
| LTC1605-1/LTC1605-2 | 16-Bit, 100kHz ADC | 0V to 4V/±4V Input Range, Pin Compatible with LTC1606 |
| LTC1608 | 16-Bit, 500ksps ADC | ±2.5V Input, No Missing Codes, Pin Compatible with LTC1604 |

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