CY62162G/CY62162GE MoBL®

16-Mbit (512 K × 32) Static RAM with Error-Correcting Code (ECC)

Features

- Ultra-low standby power
  - Typical standby current: 5.5 µA
  - Maximum standby current: 16 µA
- High speed: 45 ns / 55 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Wide voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- ERR pin to indicate 1-bit error detection and correction
- Easy memory expansion with $\overline{CE}_1$ and CE_2 features
- Available in Pb-free 119-ball PBGA package, 512 K × 32 bits SRAM

Functional Description

The CY62162G and CY62162GE devices are high performance CMOS MoBL SRAM organized as 512K words by 32-bits. Both CY62162G and CY62162GE are available with dual chip enables. CY62162GE includes an error indication pin that signals the host processor in the case of a single bit error-detection and correction event. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or $\overline{B}_{A-D}$ HIGH). The input and output pins (I/O_0 through I/O_{31}) are placed in a high impedance state when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW) or outputs are disabled ($\overline{OE}$ HIGH) or the byte selects are disabled ($\overline{B}_{A-D}$ HIGH).

To write to the device, take chip enables ($\overline{CE}_1$ LOW, CE_2 HIGH) and write enable ($\overline{WE}$) input LOW. If byte enable A ($\overline{B}_A$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{18}). If byte enable B ($\overline{B}_B$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}). Likewise, $\overline{B}_C$ and $\overline{B}_D$ correspond with the I/O pins I/O_{16} to I/O_{23} and I/O_{24} to I/O_{31}, respectively.

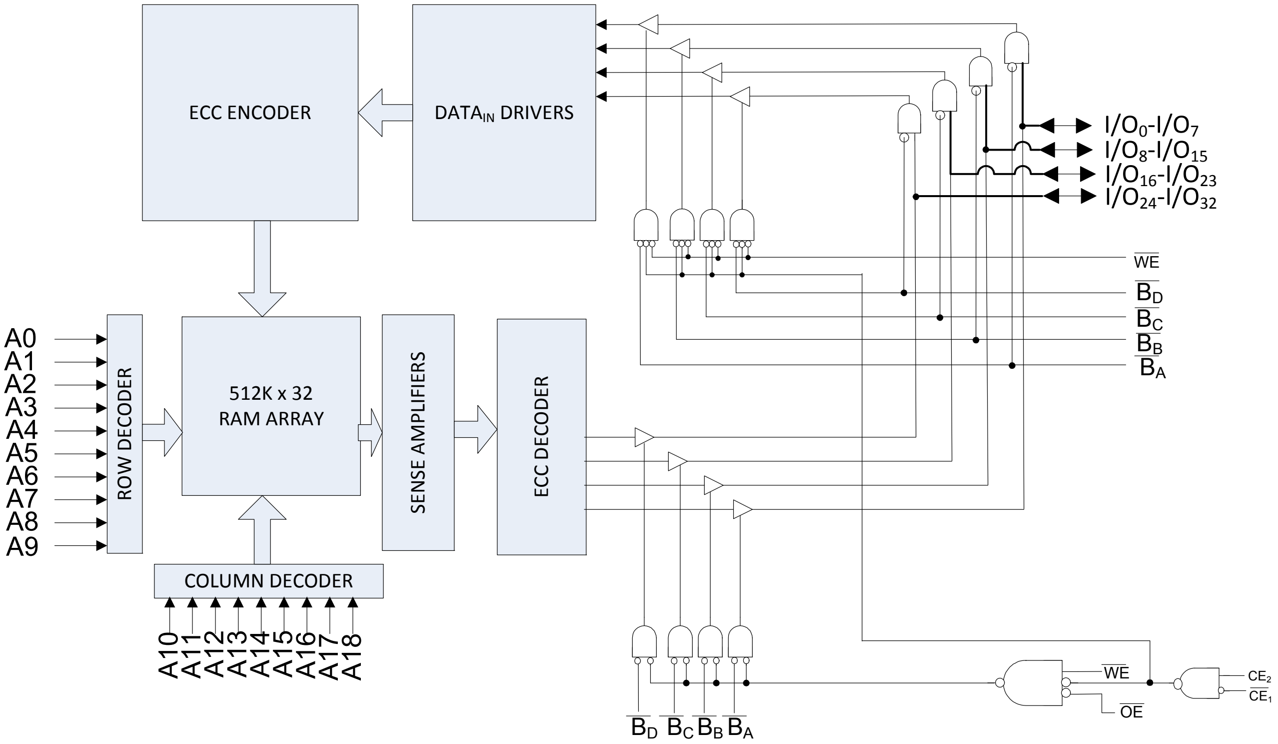
To read from the device, take chip enables ($\overline{CE}_1$ LOW, CE_2 HIGH), and output enable ($\overline{OE}$) LOW while forcing the write enable ($\overline{WE}$) HIGH. If the first byte enable ($\overline{B}_A$) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If byte enable ($\overline{B}_B$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. Likewise, $\overline{B}_C$ and $\overline{B}_D$ correspond to the third and fourth bytes. During Read operation, in case of a single bit error detection and correction, ERR is asserted HIGH[1]. See the Truth Table – CY62162G / CY62162GE on page 15 for a complete description of read and write modes.

CY62162G and CY62162GE devices are available in a 119-ball PBGA package with center power and ground pinout.

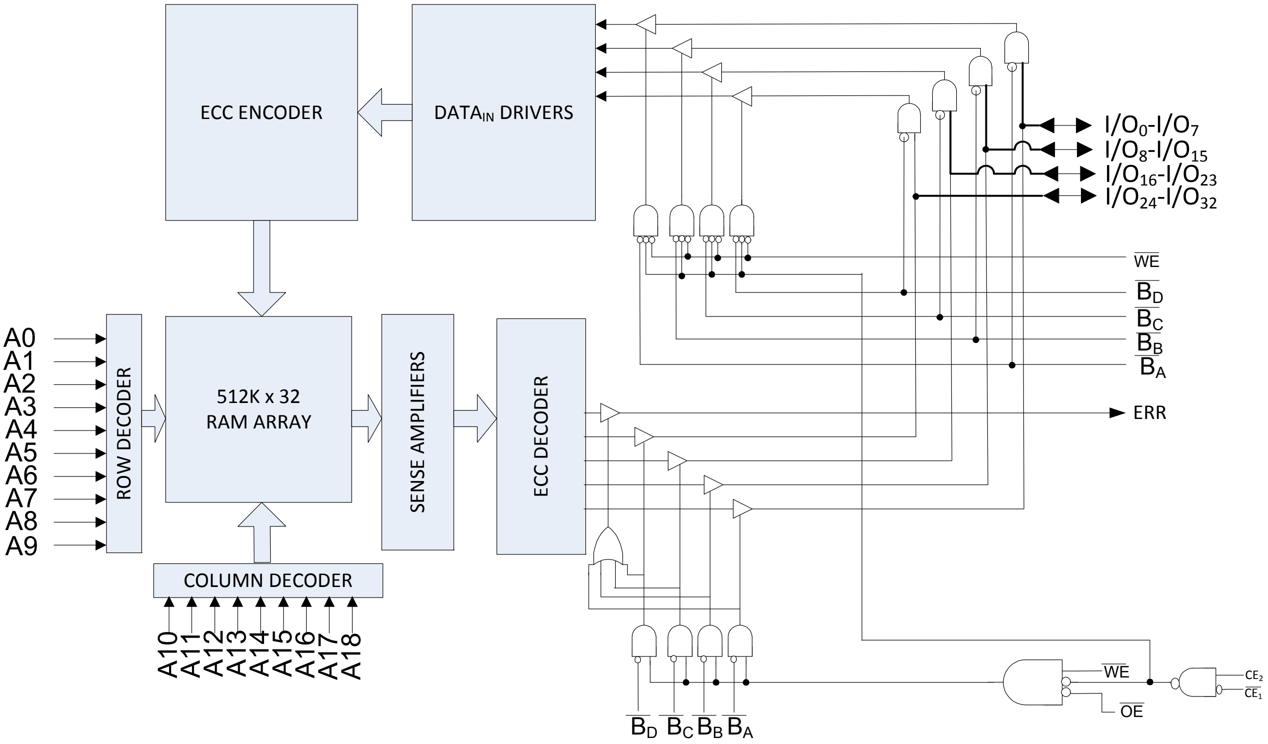
Note

[1] This device does not support automatic write-back on error detection.

Logic Block Diagram – CY62162G



Logic Block Diagram – CY62162GE



Contents

Pin Configurations

Figure 1. 119-ball FBGA pinout [2]
CY62162G (512 K × 32)

	1	2	3	4	5	6	7
A	I/O_{16}	A_4	A_3	A_2	A_1	A_0	I/O_0
B	I/O_{17}	A_{18}	A_{17}	$\overline{CE}_1$	A_{16}	A_{15}	I/O_1
C	I/O_{18}	$\overline{B}_c$	CE_2	NC	NC	$\overline{B}_a$	I/O_2
D	I/O_{19}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_3
E	I/O_{20}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_4
F	I/O_{21}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_5
G	I/O_{22}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_6
H	I/O_{23}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_7
J	NC	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	NC
K	I/O_{24}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_8
L	I/O_{25}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_9
M	I/O_{26}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{10}
N	I/O_{27}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_{11}
P	I/O_{28}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{12}
R	I/O_{29}	A_{14}	$\overline{B}_d$	NC	$\overline{B}_b$	A_{13}	I/O_{13}
T	I/O_{30}	A_{12}	A_{11}	$\overline{WE}$	A_{10}	A_9	I/O_{14}
U	I/O_{31}	A_8	A_7	$\overline{OE}$	A_6	A_5	I/O_{15}

Figure 2. 119-ball FBGA pinout [2, 3]
CY62162GE (512 K × 32)

	1	2	3	4	5	6	7
A	I/O_{16}	A_4	A_3	A_2	A_1	A_0	I/O_0
B	I/O_{17}	A_{18}	A_{17}	$\overline{CE}_1$	A_{16}	A_{15}	I/O_1
C	I/O_{18}	$\overline{B}_c$	CE_2	NC	NC	$\overline{B}_a$	I/O_2
D	I/O_{19}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_3
E	I/O_{20}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_4
F	I/O_{21}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_5
G	I/O_{22}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_6
H	I/O_{23}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_7
J	ERR	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	NC
K	I/O_{24}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_8
L	I/O_{25}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_9
M	I/O_{26}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{10}
N	I/O_{27}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_{11}
P	I/O_{28}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{12}
R	I/O_{29}	A_{14}	$\overline{B}_d$	NC	$\overline{B}_b$	A_{13}	I/O_{13}
T	I/O_{30}	A_{12}	A_{11}	$\overline{WE}$	A_{10}	A_9	I/O_{14}
U	I/O_{31}	A_8	A_7	$\overline{OE}$	A_6	A_5	I/O_{15}

Note

[2] NC pins are not connected internally to the die.

[3] ERR is an Output pin. If not used, this pin should be left floating.

Product Portfolio

Product	Features and Options (see the Pin Configurations Section)	Range	V_{CC} Range (V)	Speed (ns)	Power Dissipation			
					Operating I_{CC}, (mA) $f = f_{max}$		Standby, I_{SB2} (µA)	
					Typ[4]	Max	Typ[4]	Max
CY62162G(E)18	Dual Chip Enable Optional Error indication on ERR pinout	Industrial	1.65 V–2.2 V	55	29	32	7	26
CY62162G(E)30			2.2 V–3.6 V	45	29	36	5.5	16

Note

4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power applied .... –55 °C to +125 °C

Supply voltage to ground potential .....–0.5 V to V_{CC} + 0.5 V

DC voltage applied to outputs in high Z State[6] ....–0.5 V to V_{CC} + 0.5 V

DC input voltage [6] ....–0.5 V to V_{CC}+ 0.5 V

Output current into outputs (LOW) .... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) .... > 2001 V

Latch-up current .... > 140 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[7]
CY62162G	Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description		Test Conditions		Min	Typ [8]	Max	Unit
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OH} = –0.1 mA		1.4	–	–	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.0	–	–	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.2	–	–	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.2	
		2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 2 mA		–	–	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 8 mA		–	–	0.4	
V_{IH}	Input HIGH voltage	1.65 V to 2.2 V	–		1.4	–	V_{CC} + 0.2	
		2.2 V to 2.7 V	–		2.0	–	V_{CC} + 0.3	
		2.7 V to 3.6 V	–		2.0	–	V_{CC} + 0.3	
V_{IL}	Input LOW voltage [6]	1.65 V to 2.2 V	–		–0.2	–	0.4	
		2.2 V to 2.7 V	–		–0.3	–	0.6	
		2.7 V to 3.6 V	–		–0.3	–	0.8	
I_{IX}	Input leakage current		GND $\leq V_{IN} \leq V_{CC}$		–1.0	–	+1.0	µA
I_{OZ}	Output leakage current		GND $\leq V_{OUT} \leq V_{CC}$, Output disabled		–1.0	–	+1.0	
I_{CC}	V_{CC} operating supply current		f = 22.22 MHz (45 ns)	$V_{CC} = V_{CC(max)}$, I_{OUT} = 0 mA CMOS levels	–	29.0	36.0	mA
			f = 18.18 MHz (55 ns)		–	29.0	32.0	
			f = 1 MHz		–	7.0	9.0	
I_{SB1}[9]	Automatic power down current – CMOS inputs; V_{CC} = 2.2 to 3.6 V		$\overline{CE}_1 \geq V_{CC}$ – 0.2 V or $CE_2 \leq$ 0.2 V or $\overline{B}_{A–D} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V, $V_{IN} \leq$ 0.2 V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), $V_{CC} = V_{CC(max)}$		–	5.5	16.0	µA
	Automatic power down current – CMOS inputs; V_{CC} = 1.65 to 2.2 V				–	7.0	26.0	
I_{SB2}[9]	Automatic power down current – CMOS inputs; V_{CC} = 2.2 to 3.6 V		$\overline{CE}_1 \geq V_{CC}$ – 0.2V or $CE_2 \leq$ 0.2 V or $\overline{B}_{A–D} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, $V_{CC} = V_{CC(max)}$		–	5.5	16.0	
	Automatic power down current – CMOS inputs; V_{CC} = 1.65 to 2.2 V				–	7.0	26.0	

Notes

5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), T_A = 25 °C.
6. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 2 ns.
7. Full device AC operation assumes a 100-µs ramp time from 0 to V_{CC} (min) and 200-µs wait time after V_{CC} stabilizes to its operational value.
8. Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested.
9. Chip enables ($\overline{CE}_1$ and CE_2) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

Parameter [10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance			

Thermal Resistance

Parameter [10]	Description	Test Conditions	119-ball BGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, 2-layer printed circuit board	20.92	°C/W
Θ_{JC}	Thermal resistance (junction to case)		15.84	

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms

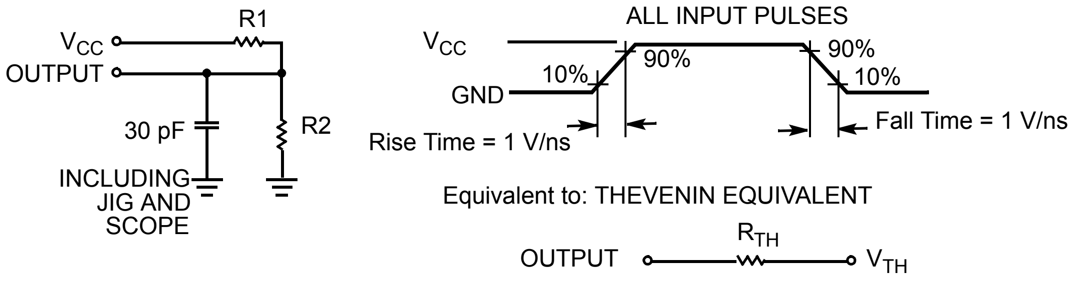


Table 1. AC Test Loads

Parameter	1.8 V	2.5 V	3.0 V	Unit
R1	13500	16667	1103	Ω
R2	10800	15385	1554	
R_{TH}	6000	8000	645	
V_{TH}	0.8	1.2	1.75	V

Note

10. Tested initially and after any design or process changes that may affect these parameters.

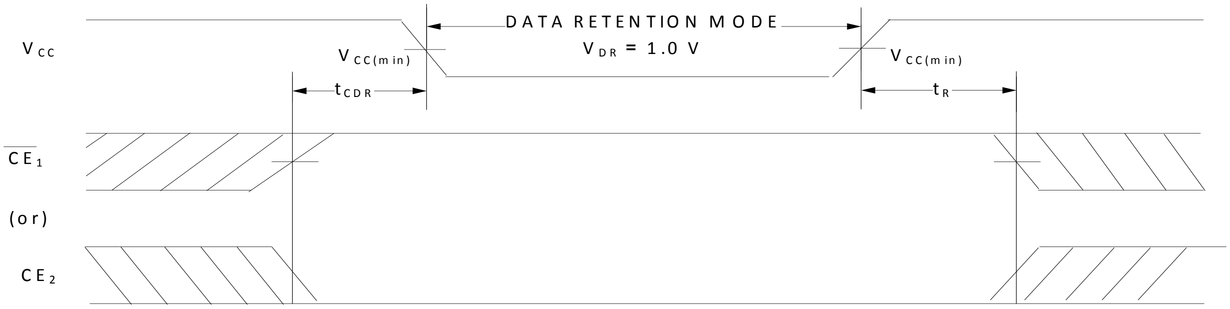
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [11]	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	–	V
I_{CCDR} [12, 13]	Data retention current	$1.0\ V \le V_{CC} \le 2.2\ V$, $\overline{CE}_1 \ge V_{CC} - 0.2\ V$ or $CE_2 \le 0.2\ V$ or $\overline{B}_{A–D} \ge V_{CC} - 0.2\ V$, $V_{IN} \ge V_{CC} - 0.2\ V$ or $V_{IN} \le 0.2\ V$	–	7.0	26.0	µA
		$2.2\ V < V_{CC} \le 3.6\ V$, $\overline{CE}_1 \ge V_{CC} - 0.2\ V$ or $CE_2 \le 0.2\ V$ or $\overline{B}_{A–D} \ge V_{CC} - 0.2\ V$, $V_{IN} \ge V_{CC} - 0.2\ V$ or $V_{IN} \le 0.2\ V$	–	5.5	16.0	
t_{CDR}[14]	Chip deselect to data retention time	–	0	–	–	ns
t_R[14, 15]	Operation recovery time	–	45 / 55	–	–	

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V for the range 1.7 V to 2.2 V; 3 V for the range 2.2 V to 3.6 V, T_A = 25 °C.

12. Only chip enables ($\overline{CE}_1$ and CE_2) and all byte enables ($\overline{B}_{A\text{-}D}$) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

13. $\overline{B}_{A\text{-}D}$ is the AND of $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$ and $\overline{B}_D$. Chip is deselected by either disabling the chip enable signals or by disabling all byte enables together.
14. These parameters are guaranteed by design and are not tested.
15. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \ge 100\ \mu s$ or stable at $V_{CC(min)} \ge 100\ \mu s$.

Switching Characteristics

Over the Operating Range

Parameter [16, 17]	**Description**	**45 ns**		**55 ns**		**Unit**
		Min	**Max**	**Min**	**Max**	
Read Cycle						
t_{RC}	Read cycle time	45.0	–	55.0	–	ns
t_{AA}	Address to data/ERR valid	–	45.0	–	55.0	
t_{OHA}	Data/ERR hold from address change	10	–	10.0	–	
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data/ERR valid	–	45.0	–	55.0	
t_{DOE}	$\overline{OE}$ LOW to data/ERR valid	–	22.0	–	25.0	
t_{LZOE}	$\overline{OE}$ LOW to low Z [17, 18]	5.0	–	5.0	–	
t_{HZOE}	$\overline{OE}$ HIGH to high Z [17, 18, 19]	–	18.0	–	18.0	
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to low Z [17, 18]	10.0	–	10.0	–	
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to high Z [17, 18, 19]	–	18.0	–	18.0	
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up [20]	0	–	0	–	
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power-down [20]	–	45.0	–	55.0	
t_{DBE}	Byte enable LOW to data valid	–	45.0	–	55.0	
t_{LZBE}	Byte enable LOW to low Z [17]	5.0	–	5.0	–	
t_{HZBE}	Byte enable HIGH to high Z [17, 19]	–	18.0	–	18.0	
Write Cycle [21, 22]						
t_{WC}	Write cycle time	45.0	–	55.0	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35.0	–	40.0	–	
t_{AW}	Address setup to write end	35.0	–	40.0	–	
t_{HA}	Address hold from write end	0	–	0	–	
t_{SA}	Address setup to write start	0	–	0	–	
t_{PWE}	$\overline{WE}$ pulse width	35.0	–	40.0	–	
t_{BW}	Byte enable LOW to write end	35.0	–	40.0	–	
t_{SD}	Data setup to write end	25.0	–	25.0	–	
t_{HD}	Data hold from write end	0	–	0	–	
t_{HZWE}	$\overline{WE}$ LOW to high Z [17, 19, 18]	–	18.0	–	20.0	
t_{LZWE}	$\overline{WE}$ HIGH to low Z [17, 18]	10.0	–	10.0	–	

Notes

16. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of V_{TH}, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in Table 1 on page 8.
17. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
18. Tested initially and after any design or process changes that may affect these parameters.
19. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedence state.
20. These parameters are guaranteed by design and are not tested.
21. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ LOW. Chip enable must be active and $\overline{WE}$ and byte enables must be LOW to initiate a write, and the transition of any of these signals terminate the write. The input data setup and hold timing are referenced to the leading edge of the signal that terminates the write.
22. The minimum write cycle pulse width for Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{HZWE} and t_{SD}.

Switching Waveforms

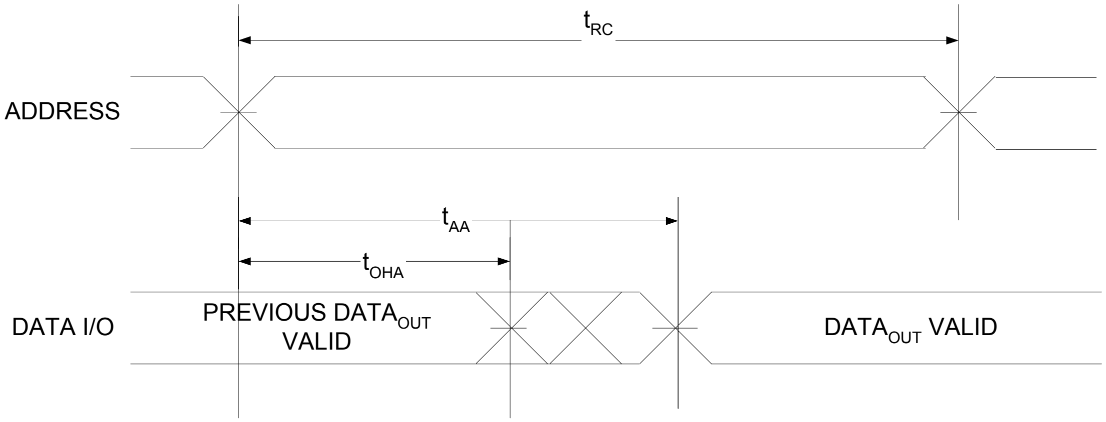


Figure 5. Read Cycle No. 1 of CY62162G (Address Transition Controlled) [23, 24]

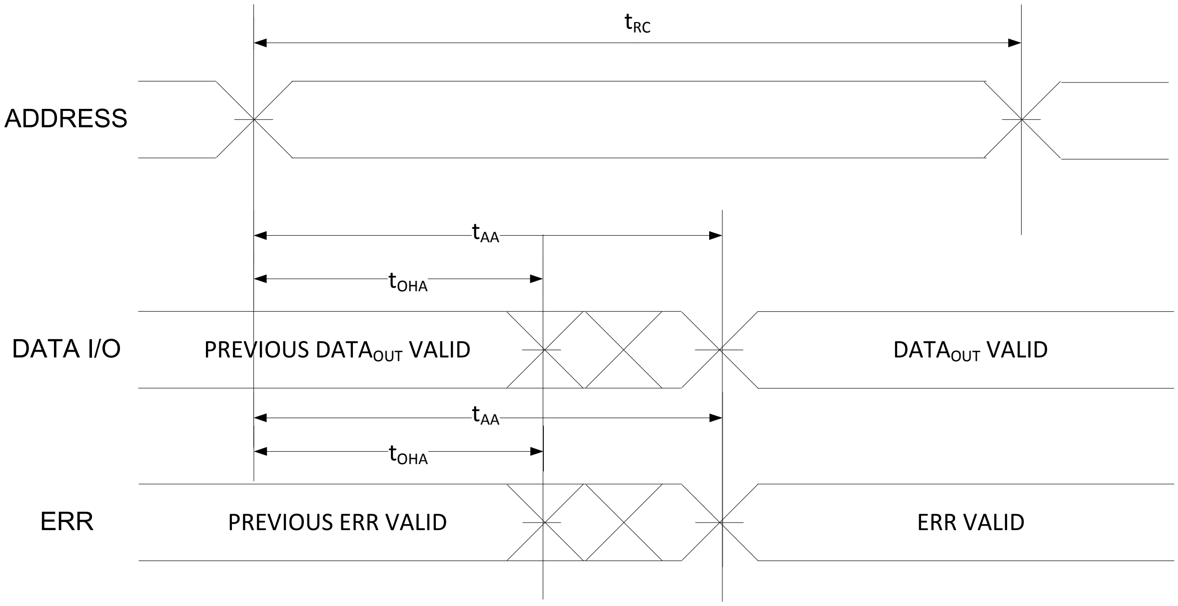


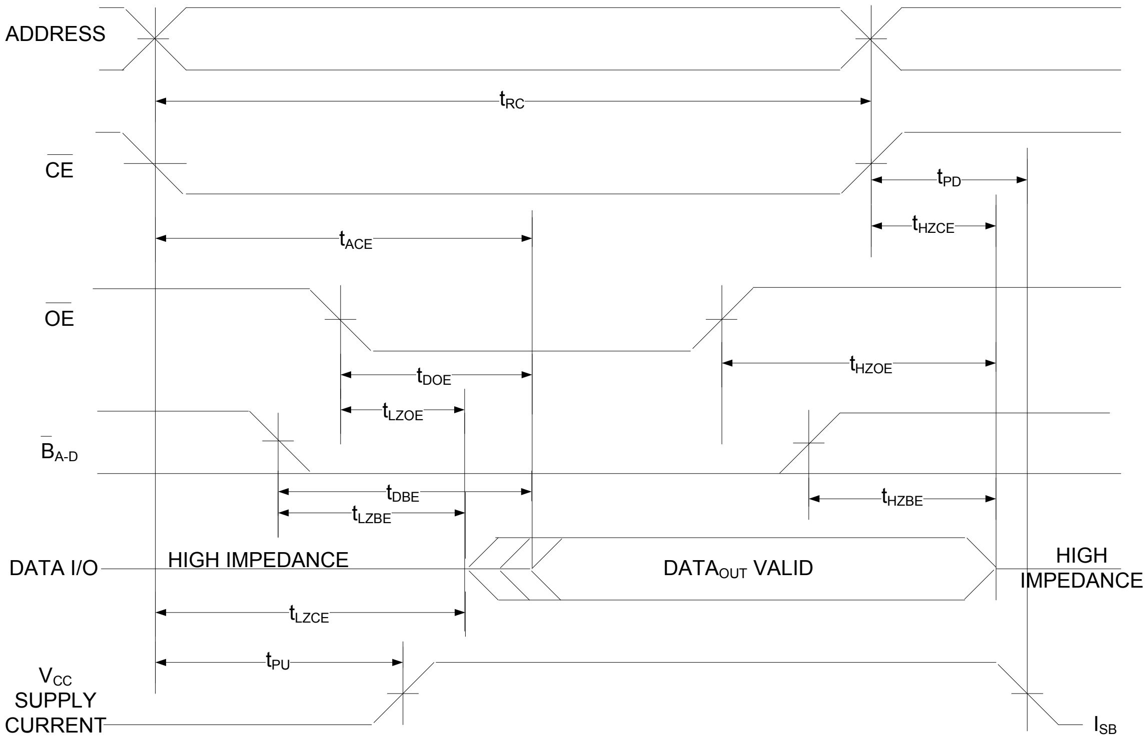
Figure 6. Read Cycle No. 1 of CY62162GE (Address Transition Controlled) [23, 24]

Notes

[23] Device is continuously selected. $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$.
[24] $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms *(continued)*

Figure 7. Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled) [25, 26, 27]



Notes

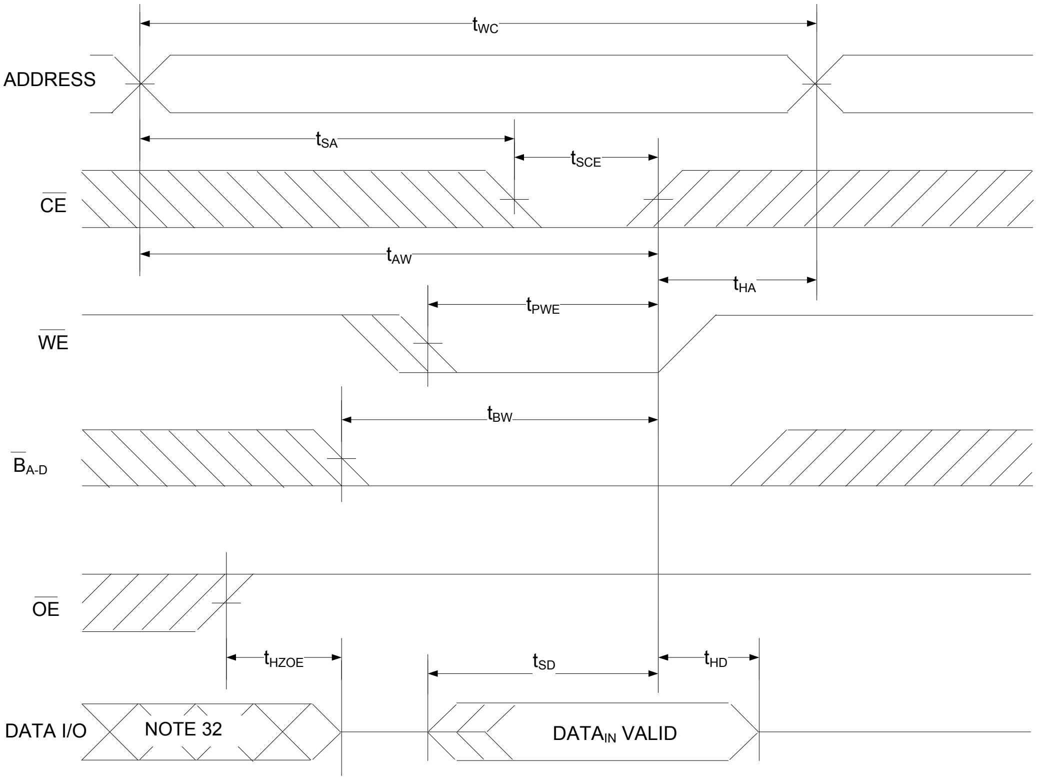
[25] $\overline{\text{WE}}$ is HIGH for read cycle.

[26] Address valid before or similar to $\overline{\text{CE}}$ transition LOW.

[27] $\overline{\text{CE}}$ refers to a combination of $\overline{\text{CE}}_1$ and CE_2. $\overline{\text{CE}}$ is LOW when $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH. $\overline{\text{CE}}$ is HIGH when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW.

Switching Waveforms *(continued)*

Figure 8. Write Cycle No. 1 ($\overline{CE}$ Controlled) [28, 29, 30, 31]



Notes

28. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ LOW. Chip enable must be active and $\overline{WE}$ and byte enables must be LOW to initiate a write, and the transition of any of these signals terminate the write. The input data setup and hold timing are referenced to the leading edge of the signal that terminates the write.
29. Data I/O is high impedance if $\overline{OE}$ or $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D = V_{IH}$.
30. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.
31. $\overline{CE}$ refers to a combination of $\overline{CE}_1$ and CE_2. $\overline{CE}$ is LOW when $\overline{CE}_1$ is LOW and CE_2 is HIGH. $\overline{CE}$ is HIGH when $\overline{CE}_1$ is HIGH or CE_2 is LOW.
32. During this period the I/Os are in output state and input signals should not be applied.

Switching Waveforms *(continued)*

Figure 9. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [33, 34, 35]

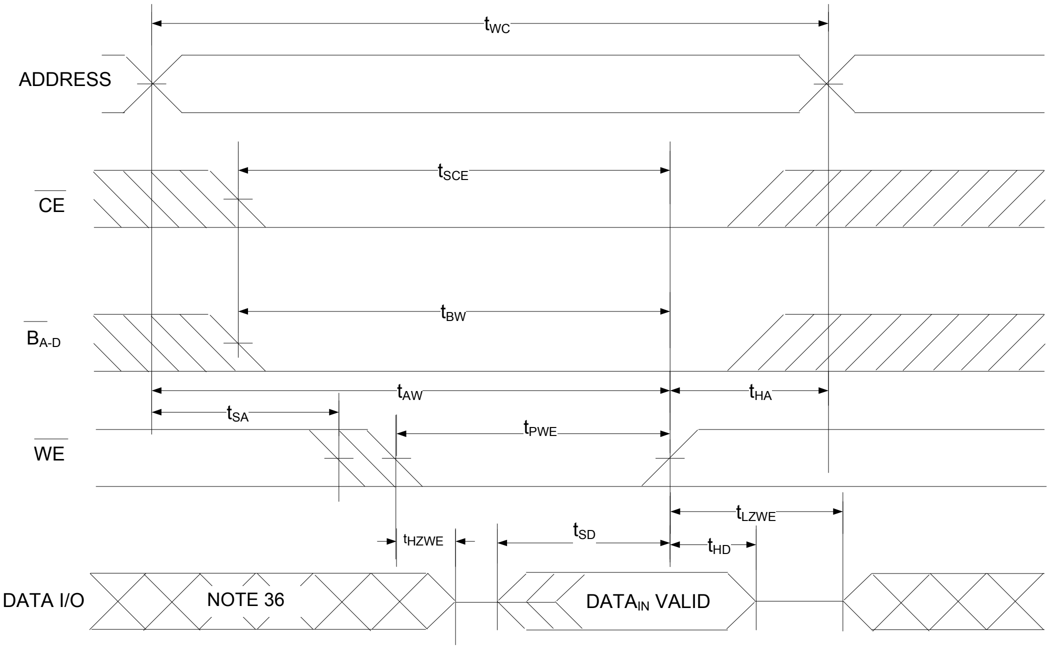
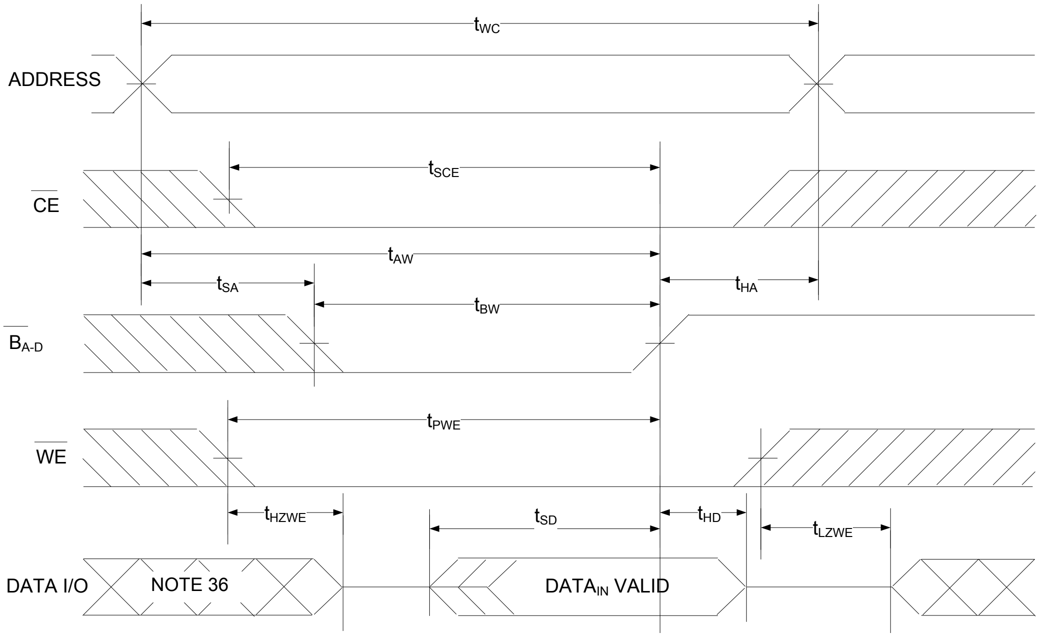


Figure 10. Write Cycle No. 3 ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ Controlled, $\overline{OE}$ LOW) [33, 34]



Notes

[33] If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

[34] $\overline{CE}$ refers to a combination of $\overline{CE}_1$ and CE_2. $\overline{CE}$ is LOW when $\overline{CE}_1$ is LOW and CE_2 is HIGH. $\overline{CE}$ is HIGH when $\overline{CE}_1$ is HIGH or CE_2 is LOW.

[35] The minimum write cycle pulse width should be equal to the sum of t_{HZWE} and t_{SD}.

[36] During this period the I/Os are in output state and input signals should not be applied.

Truth Table – CY62162G / CY62162GE

$\overline{CE}$[37]	$\overline{OE}$	$\overline{WE}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$	I/O_0–I/O_7	I/O_8–I/O_{15}	I/O_{16}–I/O_{23}	I/O_{24}–I/O_{31}	Mode	Power
H	X	X	X[38]	X[38]	X[38]	X[38]	High Z	High Z	High Z	High Z	Standby	(I_{SB})
X[38]	X	X	H	H	H	H	High Z	High Z	High Z	High Z	Standby	(I_{SB})
L	L	H	L	L	L	L	Data out	Data out	Data out	Data out	Read all bits	(I_{CC})
L	L	H	L	H	H	H	Data out	High Z	High Z	High Z	Read byte A bits only	(I_{CC})
L	L	H	H	L	H	H	High Z	Data out	High Z	High Z	Read byte B bits only	(I_{CC})
L	L	H	H	H	L	H	High Z	High Z	Data out	High Z	Read byte C bits only	(I_{CC})
L	L	H	H	H	H	L	High Z	High Z	High Z	Data out	Read byte D bits only	(I_{CC})
L	X	L	L	L	L	L	Data in	Data in	Data in	Data in	Write all bits	(I_{CC})
L	X	L	L	H	H	H	Data in	High Z	High Z	High Z	Write byte A bits only	(I_{CC})
L	X	L	H	L	H	H	High Z	Data in	High Z	High Z	Write byte B bits only	(I_{CC})
L	X	L	H	H	L	H	High Z	High Z	Data in	High Z	Write byte C bits only	(I_{CC})
L	X	L	H	H	H	L	High Z	High Z	High Z	Data in	Write byte D bits only	(I_{CC})
L	H	H	X[38]	X[38]	X[38]	X[38]	High Z	High Z	High Z	High Z	Selected, outputs disabled	(I_{CC})

ERR Output – CY62162GE

Output [39]	Mode
0	Read Operation, no single bit error in the stored data.
1	Read Operation, single bit error detected and corrected.
Z	Device deselected / Outputs disabled / Write Operation.

Note

37. $\overline{CE}$ refers to a combination of $\overline{CE_1}$ and CE_2. $\overline{CE}$ is LOW when $\overline{CE_1}$ is LOW and CE_2 is HIGH. $\overline{CE}$ is HIGH when $\overline{CE_1}$ is HIGH or CE_2 is LOW.
38. ‘X’ refers to V_{IL} or V_{IH}. For CMOS voltage levels refer to I_{SB2} test conditions in Electrical Characteristics on page 7. Chip enables ($\overline{CE_1}$ and CE_2) and all Byte Enables ($\overline{B_{A-D}}$) must be in CMOS voltage levels to meet the I_{SB2}/I_{CCDR} spec.
39. ERR is an Output pin. If not used, this pin should be left floating.

Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (All Pb-free)	Operating Range
45	2.2 V–3.6 V	CY62162G30-45BGXI	51-85115	119-ball PBGA (14 × 22 × 2.4 mm)	Industrial
55	1.65 V–2.2 V	CY62162G18-55BGXI			Industrial

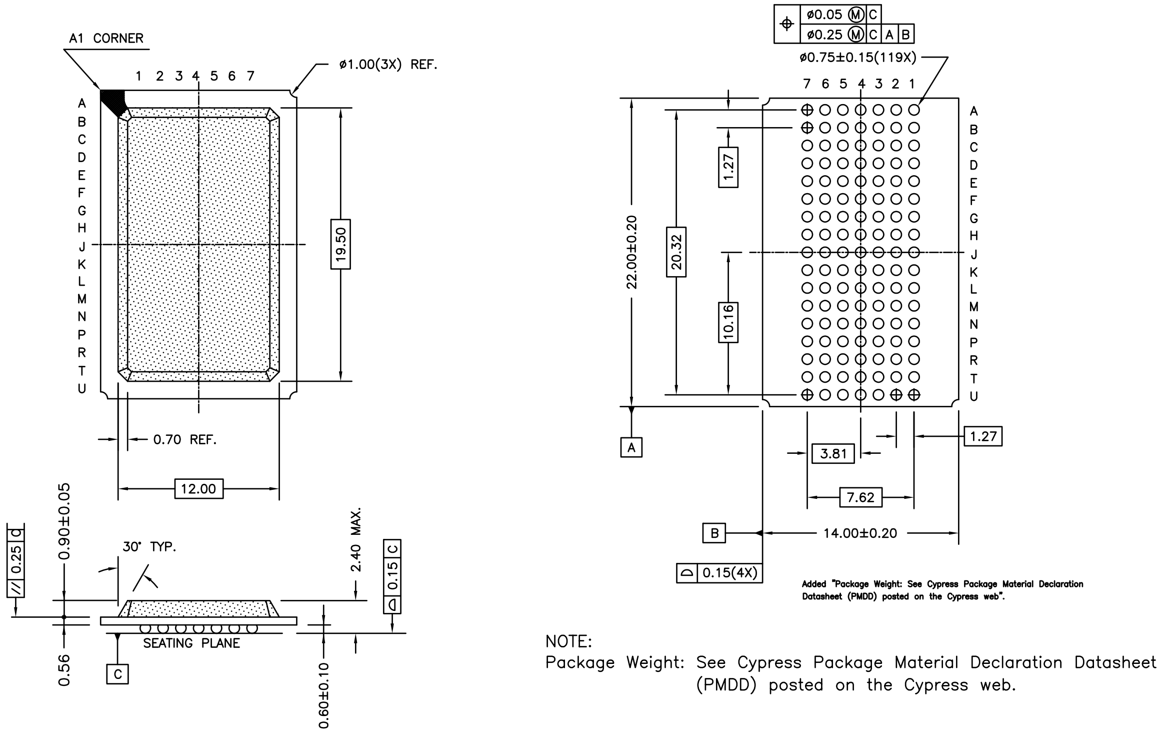
Ordering Code Definitions

CY 621 6 2 G E XX – 45 BG X I

Temperature Grade: I = Industrial
Pb-free
Package Type: BG = 119-ball PBGA
Speed grade XX: 45 = 45 ns, 55 = 55 ns
Voltage Range: 30 = 3.3 V typ, 18 = 1.8 V typ
E = ECC flag
Process Technology: G = 65 nm
Bus Width: 2 = × 32
Density: 6 = 16-Mbit
Family Code: 621 = MoBL SRAM family
Company ID: CY = Cypress

Package Diagram

Figure 11. 119-ball PBGA (14 × 22 × 2.4 mm) BG119 Package Outline, 51-85115



Added "Package Weight: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web".

NOTE:
Package Weight: See Cypress Package Material Declaration Datasheet
(PMDD) posted on the Cypress web.

51-85115 *D

Acronyms

Acronym	Description
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
mA	milliampere
MHz	megahertz
mm	millimeter
µA	microampere
µs	microsecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62162G/CY62162GE MoBL®, 16-Mbit (512 K × 32) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81598				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*C	4863821	NILE	07/31/2015	Changed status from Preliminary to Final.
*D	6012120	AESATMP9	01/03/2018	Updated logo and copyright.

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