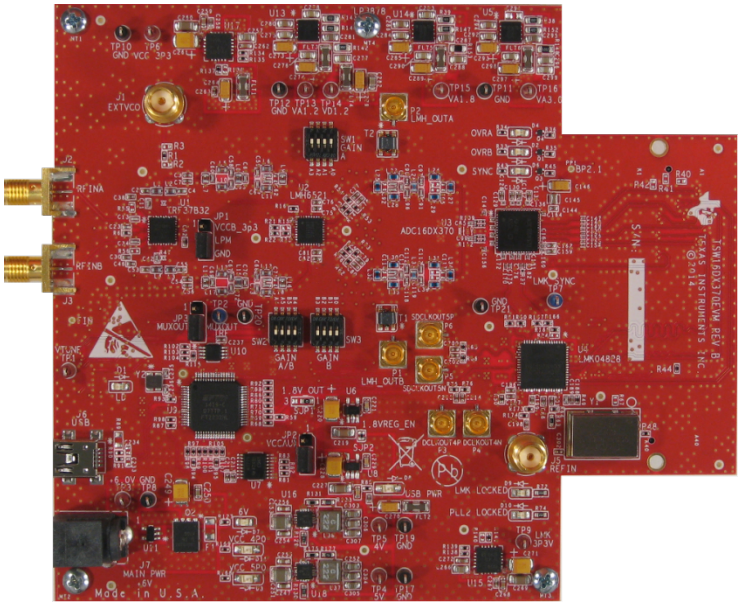
TSW16DX370EVM Rev. B

This user's guide describes the characteristics, operation, and use of TI's TSW16DX370EVM Rev B. The equipment required, setup procedures, device configuration, and an evaluation and troubleshooting section are also included.



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References

1. ADC16DX370 datasheet (SNVSA18C)
2. LMH6521 datasheet (SNOSB47D)
3. TRF37B32 datasheet (SLASE37A)
4. LMX2581 datasheet (SNAS601G)
5. LMK04828 datasheet (SNAS605A)
6. TSW14J56EVM user's guide (SLWU086A)
7. *High Speed Data Converter Pro* software user's guide, available here: DATACONVERTERPRO-SW
8. FTD245 Driver Installation Manual http://www.ftdichip.com/Support/Documents/InstallGuides.htm

1 Introduction

The TSW16DX370EVM is a reference design board used to evaluate the receiver IF subsystem solution with over 100-MHz usable bandwidth including the following products from Texas Instruments:

- ADC16DX370 dual channel 16-bit analog-to-digital converter (ADC) sampling at 368.64 MSPS
- LMH6521 dual digitally controlled variable gain amplifier (DVGA)
- TRF37B32 dual down-converting mixer with integrated IF amplifier
- LMX2581 wideband frequency synthesizer with integrated VCO
- LMK04828 ultra low jitter synthesizer and jitter cleaner

This evaluation board also includes the following important features:

- High speed serial JESD204B data output over a standard FMC interface connector.
- Device register programming via USB connector and FTDI USB-to-SPI bus translator for all devices.

The digital data from the TSW16DX370EVM board can be quickly and easily captured with the TSW14J56EVM data capture board. The TSW14J56EVM captures the high speed serial data, decodes the data, stores the data in memory, and then uploads it for analysis to a connected PC via a USB interface. The High Speed Data Converter Pro (HSDC Pro) software on the PC communicates with the hardware and processes the data.

With proper hardware selection in the HSDC Pro software, the TSW14J56 is automatically configured to support a data capture from the ADC16DX370EVM at the default sampling rate of 368.64 MSPS and serial data rate of 7.3728 Gbps.

For the rest of this document, the following references apply:

- The TSW16DX370EVM evaluation board is referred to only as 'EVM'
- The ADC16DX370 device is referred to only as 'ADC'
- The LMH6521 device is referred to only as 'LMH'
- The TRF37B32 device is referred to only as 'TRF'
- The LMX2581 is referred to only as 'LMX'
- The LMK04828 is referred to only as 'LMK'

2 Equipment

This section describes how to setup the EVM on the bench with the proper equipment to evaluate the full performance of the reference design.

2.1 Evaluation Board Feature Identification Summary

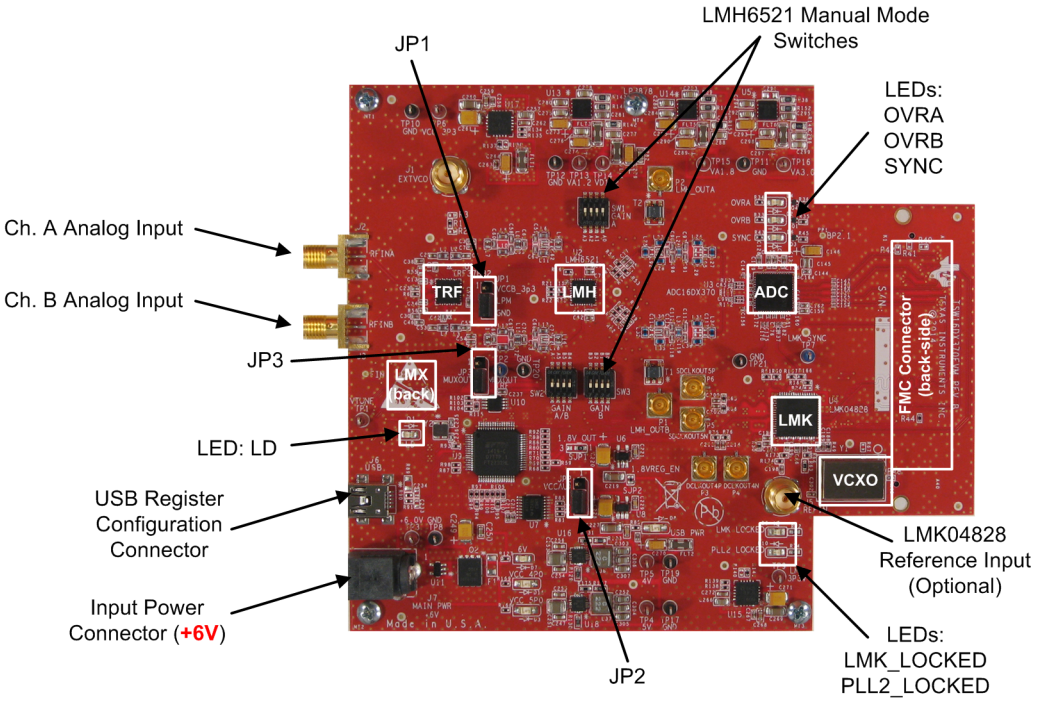


Figure 1. EVM Feature Locations

2.2 Required Equipment

The following equipment and documents are included in the EVM evaluation kit:

- Evaluation board (EVM)
- User's guide (this document)
- **+6-V** wall-mounted power supply
- Mini-USB cable

CAUTION

The +6-V supply for the EVM and +5-V supply for the TSW14J56EVM look similar but cannot be interchanged. Take care to prevent switching the supplies and causing damage to the boards.

The following list of equipment contains items that are **not** included in the EVM evaluation kit but the items are required for evaluation of this product:

- TSW14J56EVM data capture board plus +5-V power supply and mini-USB cable
- *High Speed Data Converter Pro* software
- PC computer running Microsoft® Windows® 8, Windows 7, or Windows XP
- One (1) Low-Noise Signal Generator. The following generators are recommended:
  - RF generator, > +17 dBm, ≤ 40 dBc harmonics, < 500 fs jitter 20 kHz – 20 MHz, 10 MHz – 2 GHz frequency range

  - HP HP8644B
  - Rohde & Schwarz SMA100A
- Bandpass filter for analog input for desired RF input frequency from 700–2700MHz. The following filters are recommended:
  - Bandpass filter, ≥ 60-dB harmonic attenuation, ≤ 5% bandwidth, > +18-dBm power, < 5-dB insertion loss
  - Trilithic 5VH-series Tunable BPF
  - K&L BT-series Tunable BPF
  - TTE KC6 or KC7-series Fixed BPF
- 3-dB resistive attenuator, SMA, 50 Ω
- Signal path cables, SMA or BNC

3 Setup Procedure

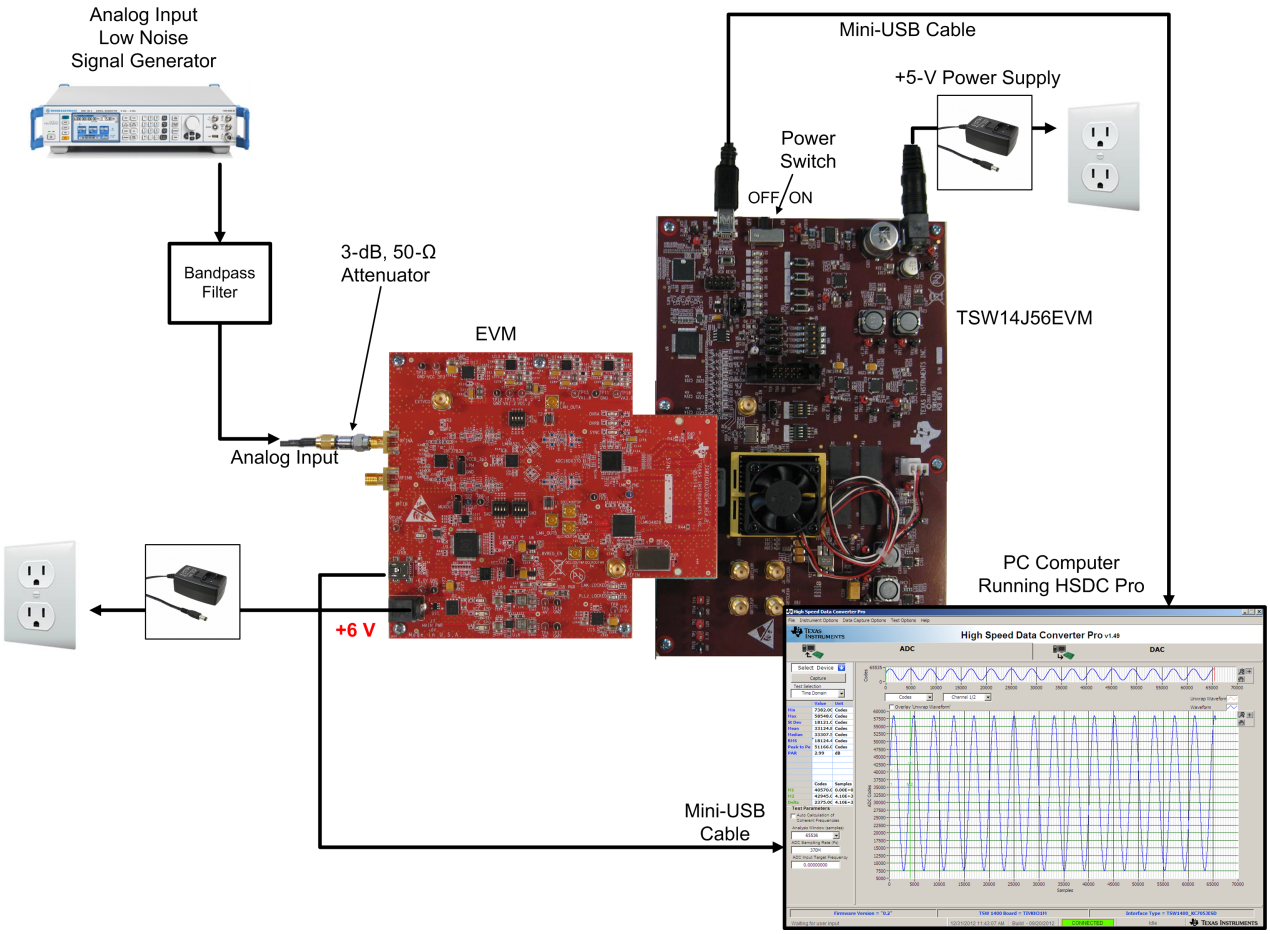


Figure 2. EVM Test Setup

3.1 Install the High Speed Data Converter Pro (HSDC Pro) Software

Download the most recent version of the HSDP software from the High Speed Data Converter Pro Software product page. Follow the installation instructions to install the software.

CAUTION

The HSDC Pro software must be installed before connecting the TSW14J56EVM to the PC for the first time.

3.2 Install the Configuration GUI Software

1. Download the configuration GUI software from the TSW16DX370EVM product page at www.ti.com
2. Extract files from the zip file
3. Run *setup.exe* and follow the installation instructions

3.3 Connect the EVM and TSW14J56EVM

With the power off, connect the EVM to the TSW14J56EVM via the FMC connector as shown in Figure 2. Check that the standoffs provide the proper height for robust connector connections.

3.4 Connect the Power Supplies to the Boards (Power OFF)

1. Confirm that the power switch on the TSW14J56EVM is in the OFF position. Connect the +5-V Power supply adapter to the TSW14J56EVM.
2. Turn the power switch of the TSW14J56EVM to the ON position.
3. Connect the +6-V power supply to the EVM.

CAUTION

The +6-V supply for the EVM and +5-V supply for the TSW14J56EVM look similar but cannot be interchanged. Take care to prevent switching the supplies and causing damage to the boards.

3.5 Connect the Signal Generators to the EVM (RF Signal OFF)

1. Connect a signal generator to the **RFINA** input of the EVM through a bandpass filter and attenuator at the SMA connector. This must be a low noise signal generator. A trilithic tunable bandpass filter is recommended to filter the signal from the generator. Configure the signal generator for **–25 dBm, 1750 MHz**.
   - Important: Coherent sampling of the input signal is not possible with the default hardware configuration of this EVM. A windowing function must be used in HSDC Pro for FFT analysis
2. **Do not yet** turn on the RF output of the signal generator.

CAUTION

This TRF device at the input of this reference design has an IP1dB = +29 dBm, but the signal path gain **may cause saturation for sinusoidal signals as low as –24 dBm**.

3.6 Connect the EVM and TSW14J56EVM to the PC

1. Connect the EVM to the PC with the Mini-USB cable
2. Connect a Mini-USB cable from the PC to the TSW14J56EVM.
3. If this is the first time connecting the TSW14J56EVM to the PC, then follow the on-screen instructions to automatically install the device drivers. See the TSW14J56EVM user's manual for more specific instructions.

3.7 Open the HSDP Software and Load the FPGA Image to the TSW14J56EVM

1. Open the HSDP software
2. Press OK to confirm the serial number of the TSW14J56EVM device
3. Select the '**TSW16DX370EVM**' device from the ADC select drop-down in the top left corner and Press YES to update the firmware.
   - Important: Configuring the ADC16DX370 with options other than the default register values may require different instructions for selecting the device in HSDC Pro. See the appendix for more details.

NOTE: Depending on the quality of the signal generator used for the input signal, a bandpass filter may not be required. The EVM achieves ~70 dB of selectivity outside the IF passband, attenuating the spurs of most signal generators to insignificant levels.

4. Enter the ADC sampling rate (Fs) as '368.64M' or the desired sampling rate
   - This number should be equal to the actual sampling rate of the device and must be updated if the sampling rate changes.

3.8 Program the EVM Using the Configuration GUI in the HSDC Pro Software

1. Note that selecting the 'TSW16DX370EVM' in the ADC select drop-down menu made an additional 'TSW16DX370EVM' tab appear in HSDC Pro. Select the TSW16DX370EVM tab in the HSDC Pro software.
2. Navigate to the INTRO tab in the GUI
3. Press the 'Program LMK04828' button.
4. Verify that the 'PLL2 LOCKED' (D10) and 'LMK LOCKED' (D9) LEDs become lit on the EVM.
5. Press the 'Calibrate ADC16DX370' button.
6. Press the 'Program LMX2581' button.
7. Verify that the 'LD' LED, next to the LMX2581, becomes lit.
8. Press the 'Program LMH6521' button.

3.9 Verify the TSW14J56EVM Switch Settings, Initialize the JESD204B Link (CPU_RESET), and Verify TSW14J56EVM Status LEDs

1. Observe the switches and jumpers on the TSW14J56EVM and verify that they are in the correct position. The required switch settings are shown in Table 5.
2. Press the **CPU_RESET** button (SW7) on the TSW14J56EVM. This button is used to reset the JESD204B receiver core in the receiving FPGA and should be pressed after power up, after changing the test setup, or after changing particular device configuration registers.
3. Verify the status of the D1–D8 LEDs on the TSW14J56EVM. See the appendix for more information regarding the status LEDs.

Table 1. Default State of LEDs on the TSW14J56EVM During Normal Operation

LED	Status
D1	N/A
D2	Blinking
D3	ON
D4	Blinking
D5	ON
D6	OFF
D7	OFF
D8	ON
FPGA_DONE	ON

3.10 Turn the Signal Generator RF Outputs ON

Turn on the RF signal outputs of the signal generators connector to **RFINA.**

3.11 Capture Data Using the HSDP Software

The following settings are made in the HSDC Pro window (Figure 3):

1. Verify that 'TSW16DX370EVM' is the selected device.
2. Verify the 'ADC sampling rate (Fs)' as '368.64M'. This value must be equal to the operating sampling rate of the device.
3. Select the Test to perform.
4. Select the data view.
5. Select the channel to view.
6. When viewing FFT results, verify that an appropriate windowing function such as 'Blackman' is selected.
7. Press the capture button to capture new data.
8. Additional Tips:
   - Use the 'Notch Frequency Bins' from the Test Options file menu to remove bins around DC (eliminate DC noise, offset) or the fundamental (eliminate phase noise from signal generators).
   - Open the 'Capture Option' dialog from the Data Capture Options file menu to change the capture depth or to enable FFT averaging.
   - For analyzing only a portion of the spectrum, use the 'Single Tone' Test with the 'Bandwidth Integration Markers' from the 'Test Options' file menu. The 'Channel Power' test may also be useful.
   - For analyzing only a subset of the captured data, set the 'Analysis Window (samples)' setting to a value less than the number total samples captured and move the green/red markers in the small transient data window at the top of the screen to select the data sub-set of interest.

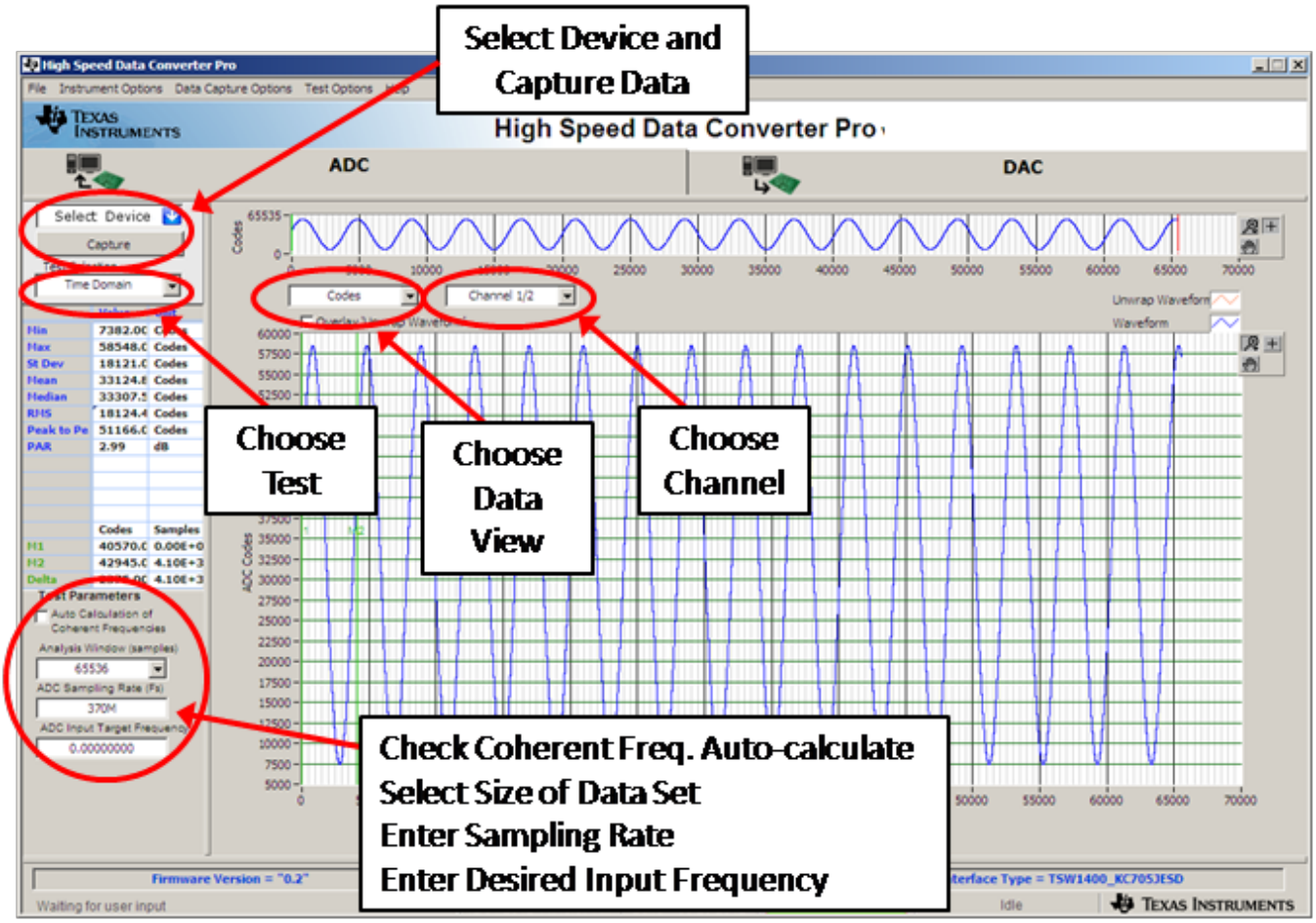


Figure 3. High Speed Data Converter Pro (HSDP) GUI

3.12 Re-Verify TSW14J56EVM Status LEDs

Verify the status of the D1–D8 LEDs on the TSW14J56EVM. Note that D4 has changed to indicate that the JESD204B link is established. See the appendix for more information regarding the status LEDs

Table 2. Default State of LEDs on the TSW14J56EVM During Normal Operation

LED	Status
D1	N/A
D2	Blinking
D3	OFF
D4	Blinking
D5	ON
D6	OFF
D7	OFF
D8	ON
FPGA_DONE	ON

4 Device Configuration

The ADC device is programmable via the serial programming interface (SPI) bus accessible through the FTDI USB to SPI converter located on the EVM. A GUI is provided to write instructions on the bus and program the registers of the ADC device.

For more information about the registers of a particular device, see the device datasheet.

4.1 Supported JESD204B Features

The ADC device supports some configuration of the JESD204B interface. Due to limitations in the TSW14J56EVM firmware, all JESD204B link features of the ADC device are not supported. The following table describes the supported and non-supported features.

JESD204B Feature	Supported by ADC16DX370 Device	Supported by TSW14J56
Number of lanes per channel (L)	L = 1 or 2	L = 1 supported L = 2 supported with special instructions for configuring HSDC Pro software
Number of Frames per Multiframe (K)	K = 9 to 32	K = 32 supported Other K values not supported at this time.
Scrambling	Scrambling supported	Scrambling not supported at this time
Test Patterns	PRBS7, PRBS15, PRBS23 supported D21.5, K28.5, ILA, Ramp patterns supported	ILA and RAMP supported PRBS7, PRBS15, PRBS23, D21.5, K28.5 not supported at this time
Speed	Lane rates from 7.4 Gbps down to 1 Gbps	Lane rates from 7.4 Gbps (Fs = 370 MSPS) down to 1 Gbps (Fs = 170 MSPS). The Fs parameter must be properly set in HSDC Pro.

4.2 Using the Device Configuration GUI

The Device Configuration GUI must be installed separately from the HSDC Pro installation, but the Configuration GUI automatically integrates into the HSDC Pro Software. If HSDC Pro is opened and the device is selected corresponding to a Configuration GUI that is already installed, then the Configuration GUI will automatically load as a selectable tab. If the Configuration GUI is opened before HSDC Pro, it will open as a standalone GUI.

Figure 4 and Figure 5 show the GUI open to the INTRO tab and ADC CORE tab, respectively. Tabs at the top of the panel organize the configuration into device and EVM features with user-friendly controls and a low-level tab for directly configuring the registers. The EVM has four (4) configurable devices, namely the ADC, LMH, LMX, and LMK. The Register Map for each device is provided in the respective device datasheet.

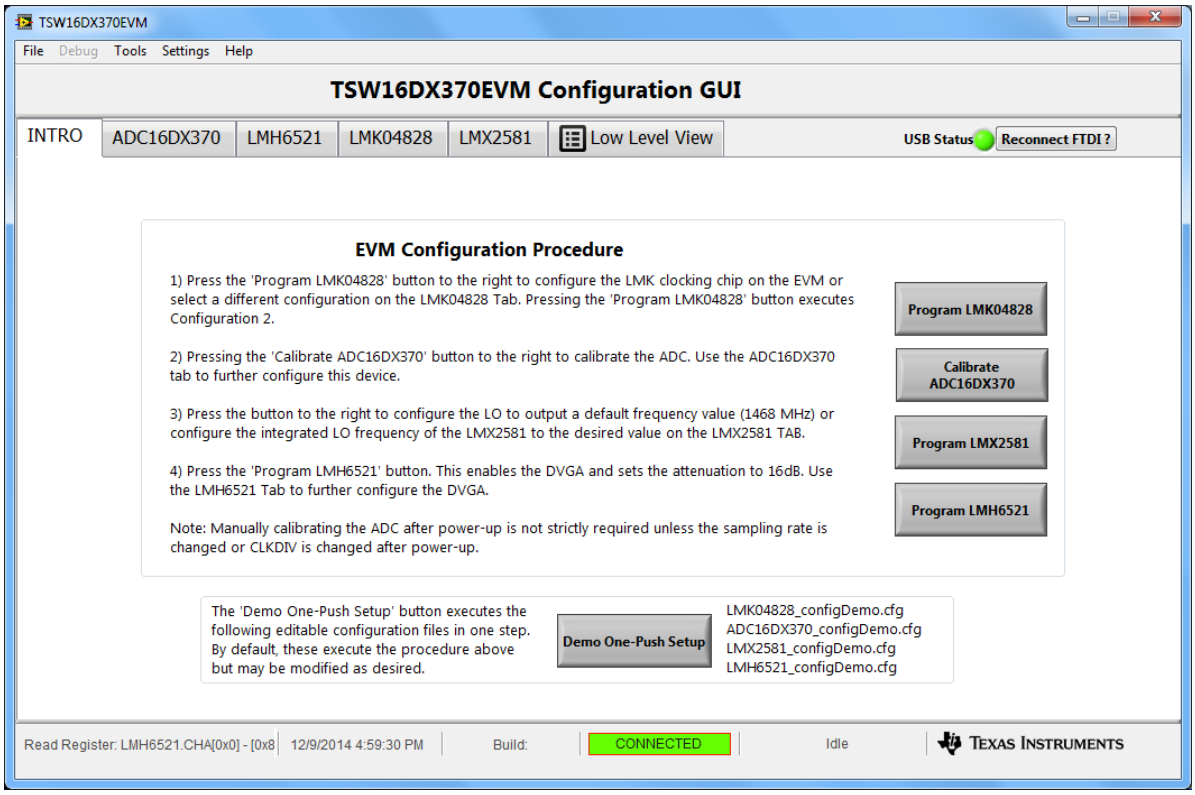


Figure 4. Configuration GUI INTRO Tab

Control	Description
Program LMK04828	Executes the ‘LMK04828_config2.cfg’ script
Calibrate ADC16DX370	Executes the ‘ADC16DX370_CalDIVCLK1.cfg’ script, running the calibration procedure required by the device
Program LMX2581	Executes the configuration script pointed to by the selection menu on the LMX2581→MACRO_CONFIG tab
Program LMH6521	Enables both LMH6521 channels and sets the attenuation to 24 dB
Demo One-Push Setup	Executes the following series of configuration scripts: LMK04828_configDemo.cfg ADC16DX370_configDemo.cfg LMX2581_configDemo.cfg LMH6521_configDemo.cfg

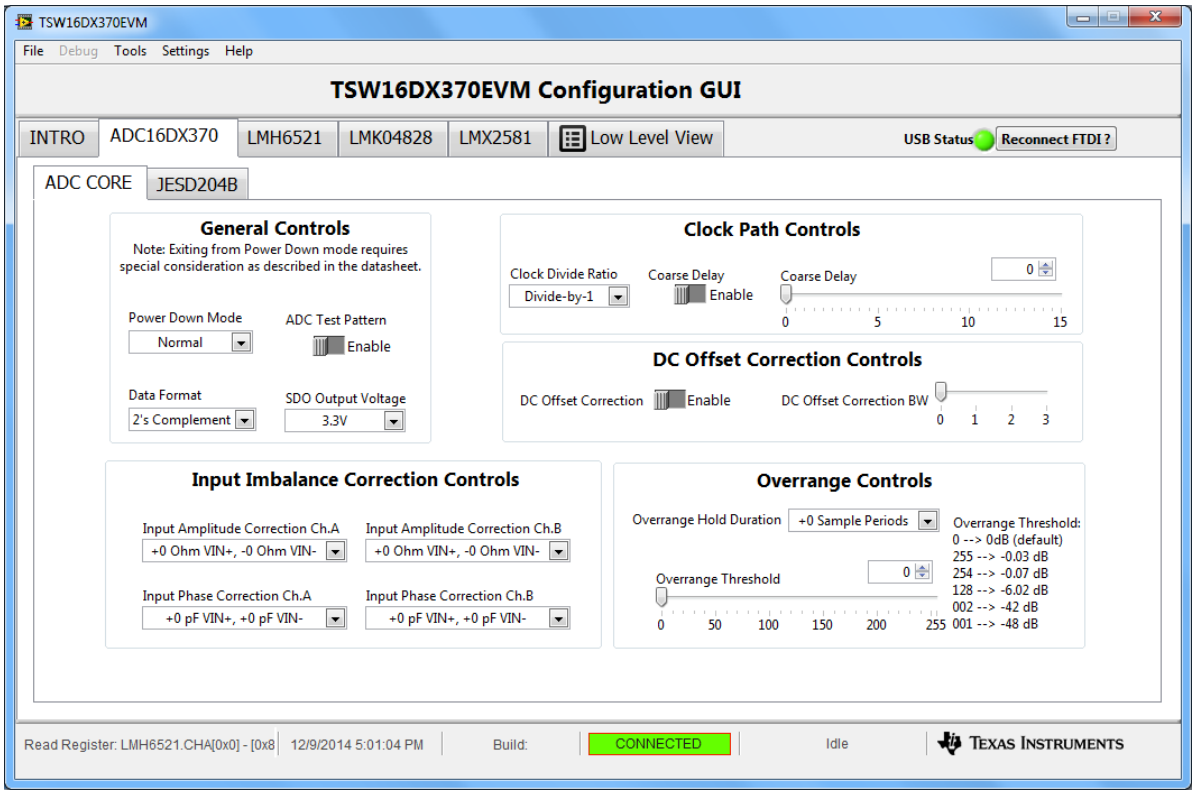


Figure 5. Configuration GUI ADC CORE Tab

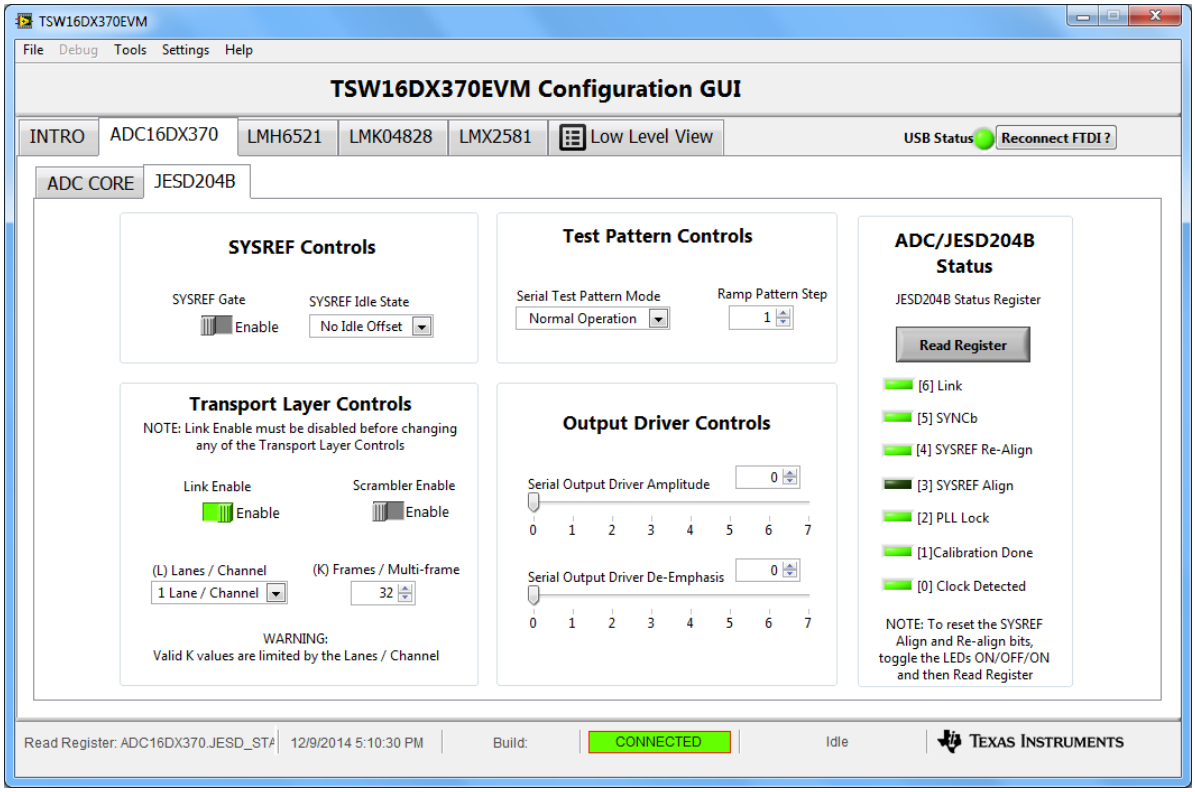


Figure 6. Configuration GUI JESD240B Tab

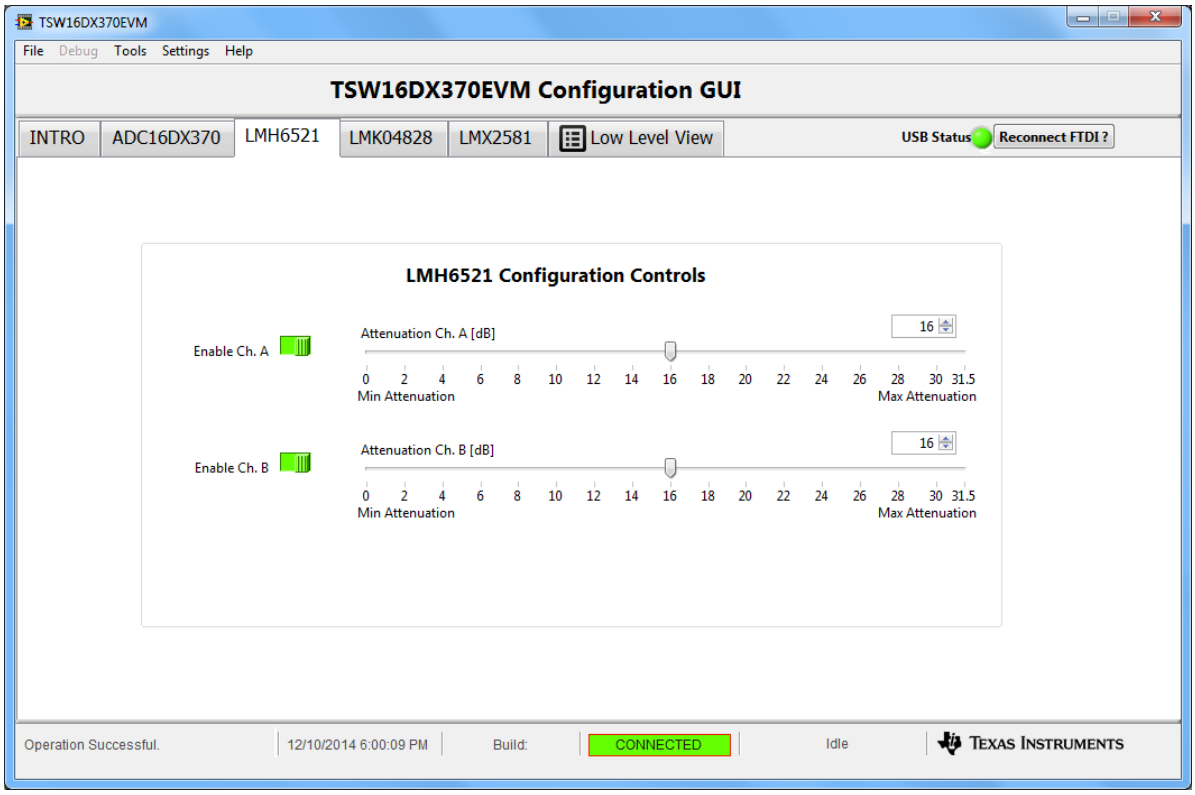


Figure 7. LMH6521 Tab

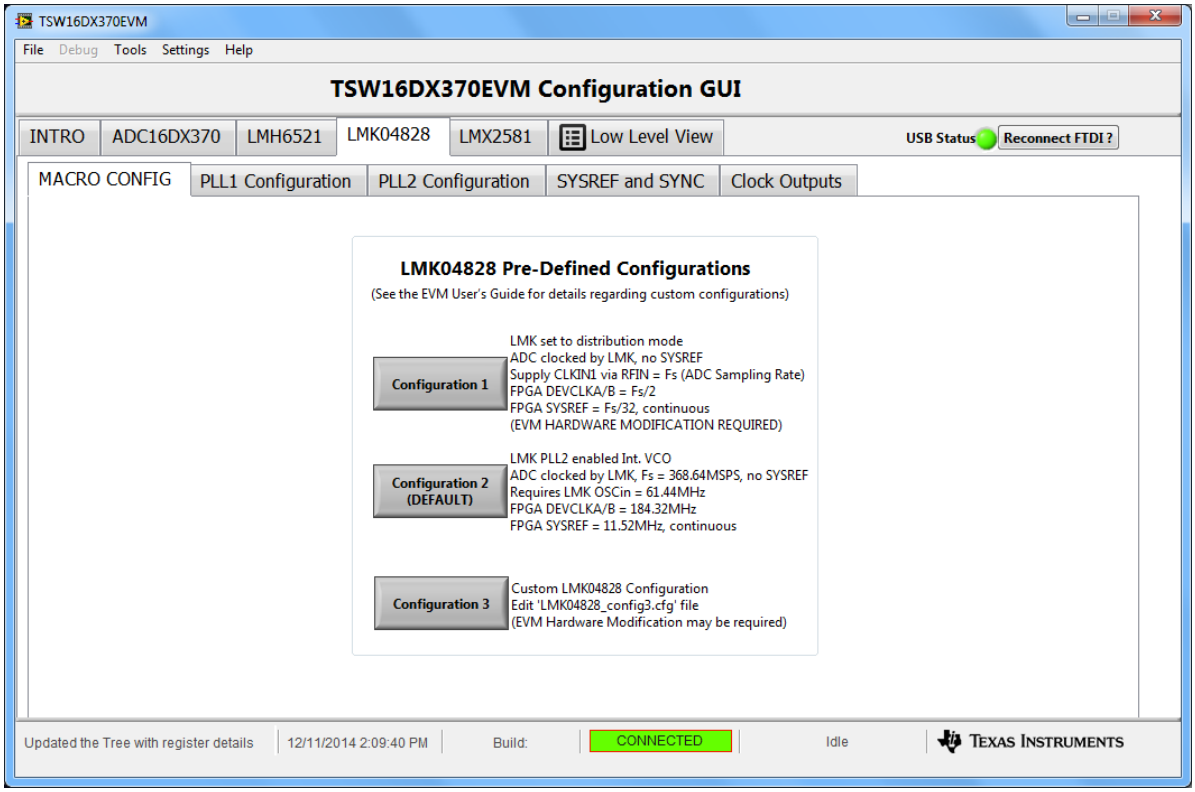
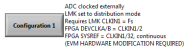
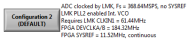


Figure 8. LMK04828 MACRO CONFIG Tab

Control	Description
	**Used to set the ADC sampling rate to a value different than the default value** ● Executes 'LMK04828_config1.cfg' script ● LMK set in clock distribution mode ● Reference signal must be applied to REFIN SMA between 100 MHz and 370 MHz (F_{REFIN}), +6 dBm ● ADC clocked by LMK, Sampling rate = F_{REFIN} ● No ADC SYSREF ● Reference frequency sent to FPGA = F_{REFIN} / 2 ● SYSREF frequency sent to FPGA = F_{REFIN} / 32 ● LMX2581 OSCin reference frequency = F_{REFIN} **NOTE:** This impacts the frequency plan and noise optimization of the LMX2581 ● EVM hardware must be changed to remove power to Y1 (Remove FB18)
	**Used to set the default ADC sampling rate** ● Appropriate configuration for default hardware ● Executes 'LMK04828_config2.cfg' script ● LMK PLL1 disabled, PLL2 with internal PLL enabled ● LMK reference provided by Y1, 61.44 MHz ● ADC clocked by LMK, Sampling rate = 368.64 MSPS ● No ADC SYSREF ● Reference frequency send to FPGA = 184.32 MHz ● SYSREF frequency sent to FPGA = 11.52 MHz ● LMX2581 OSCin reference frequency = 368.64 MHz
	**Used for LMK04828 development** ● Executes 'LMK04828_config3.cfg' script. ● By default, this script is the same script as LMK04828_config2.cfg ● Intended for editing

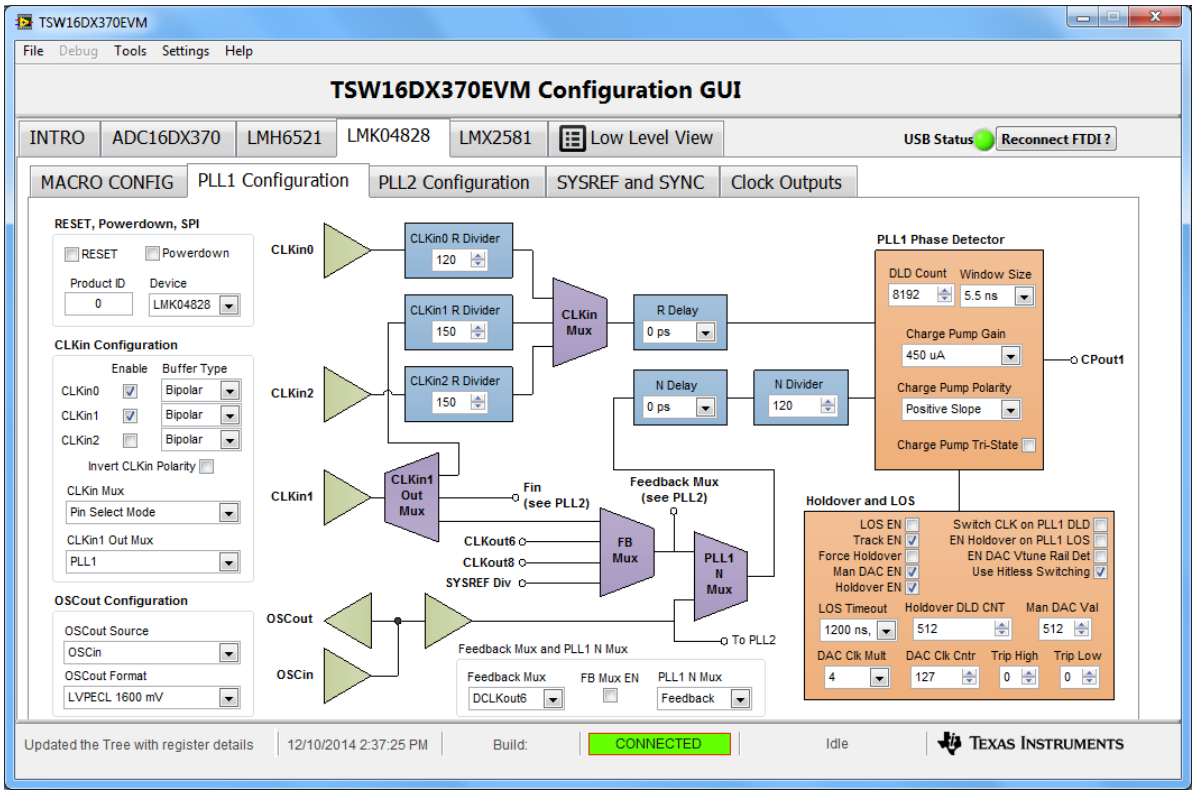


Figure 9. LMK04828 PLL1 Config Tab

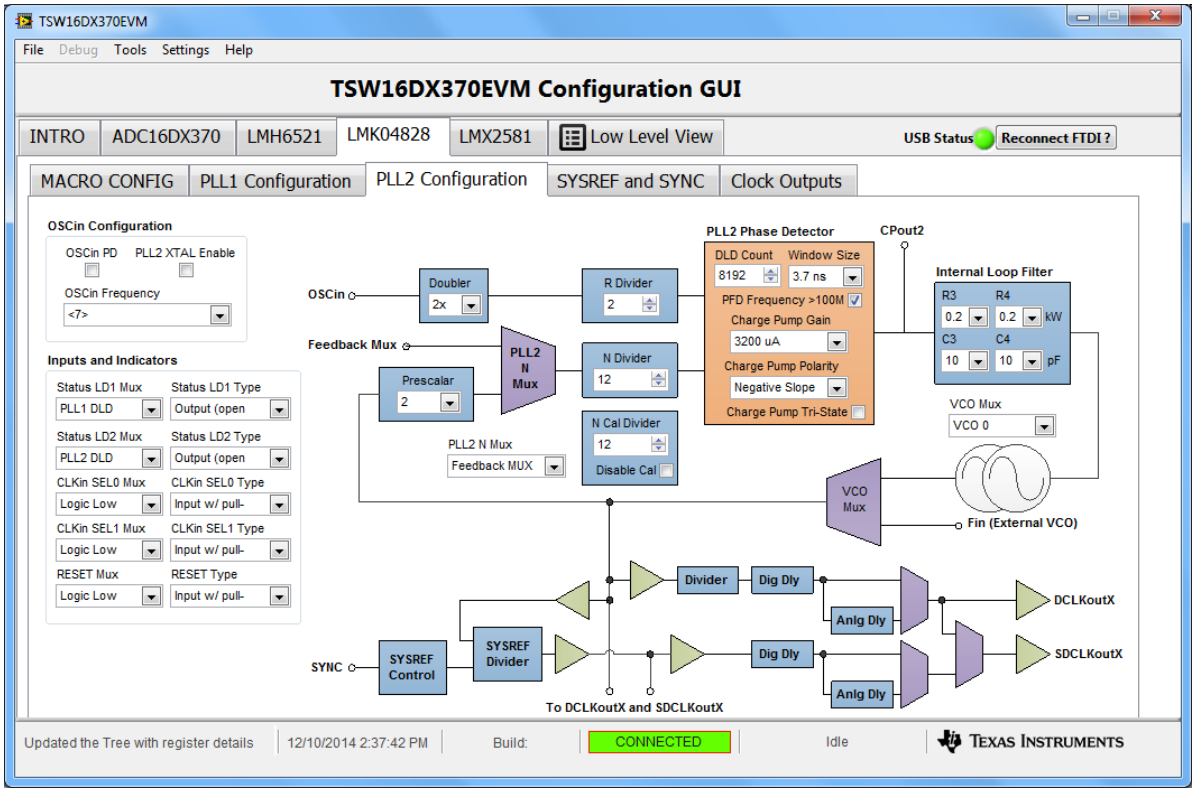


Figure 10. LMK04828 PLL2 Config Tab

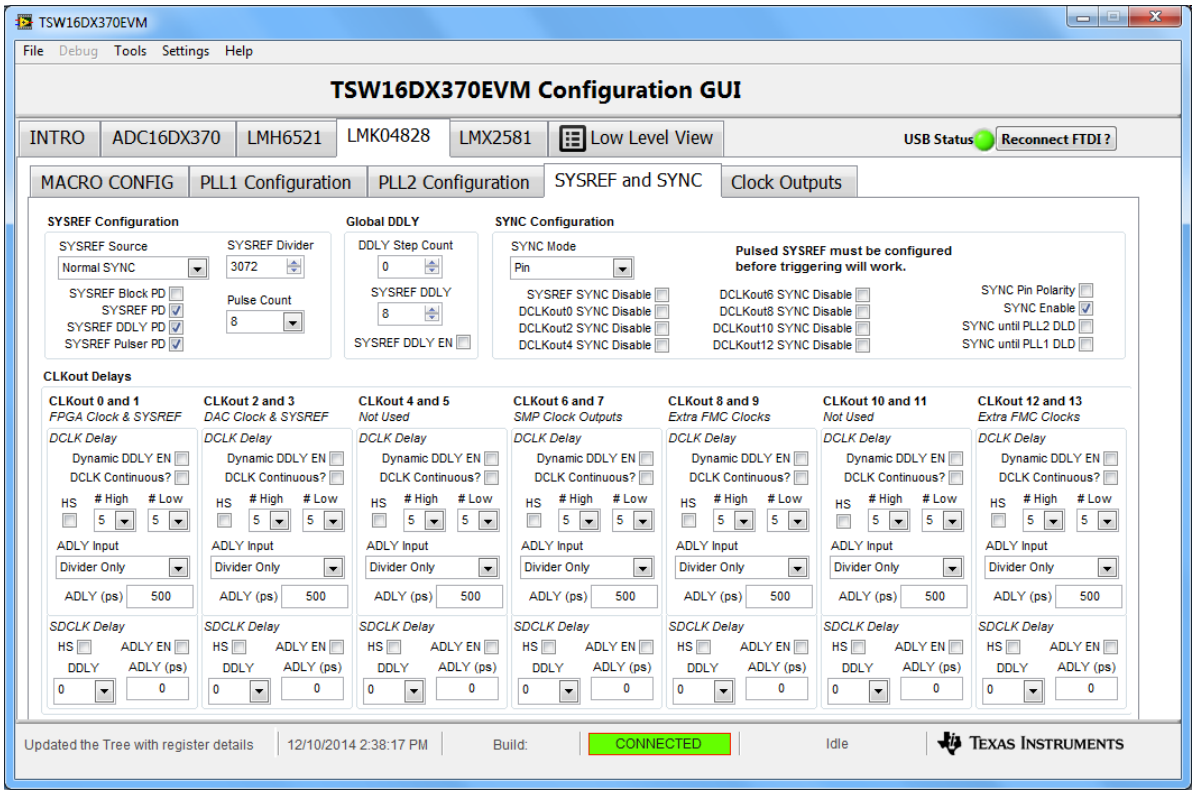


Figure 11. LMK04828 SYSREF and SYNC Tab

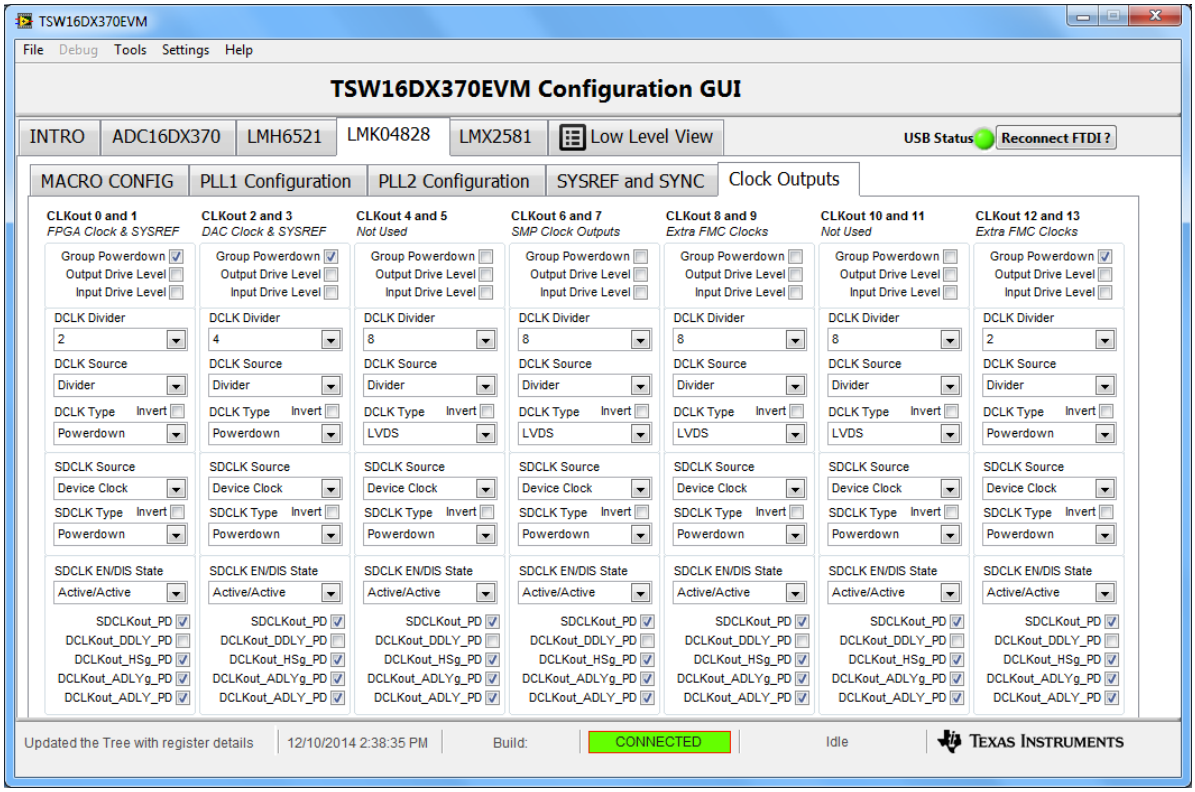


Figure 12. LMK04828 Clock Outputs Tab

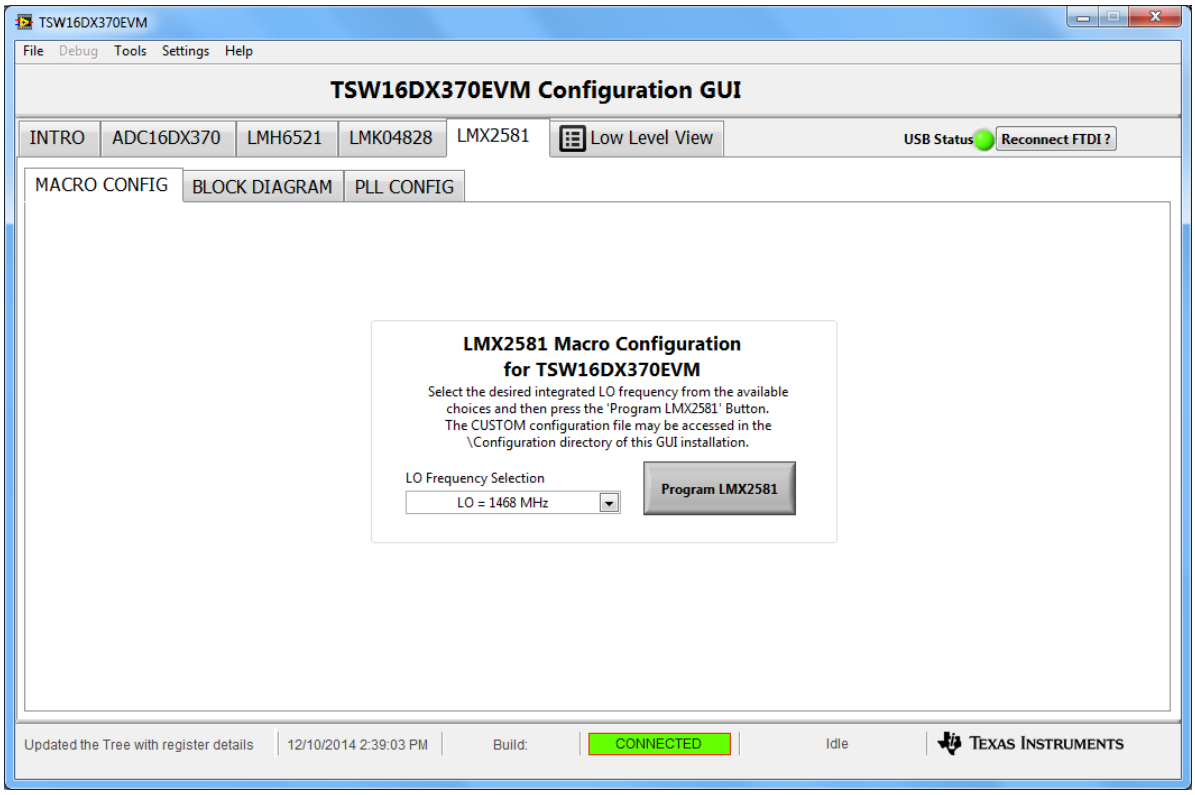


Figure 13. LMX2581 MACRO CONFIG Tab

Control	Description
	• Executes the configuration script 'LMX2581_XXX.cfg' where XXX is the RF output frequency • Requires OSCin reference frequency = 368.64 MHz which occurs for the default LMK04828 configuration • CUSTOM script intended for editing and development

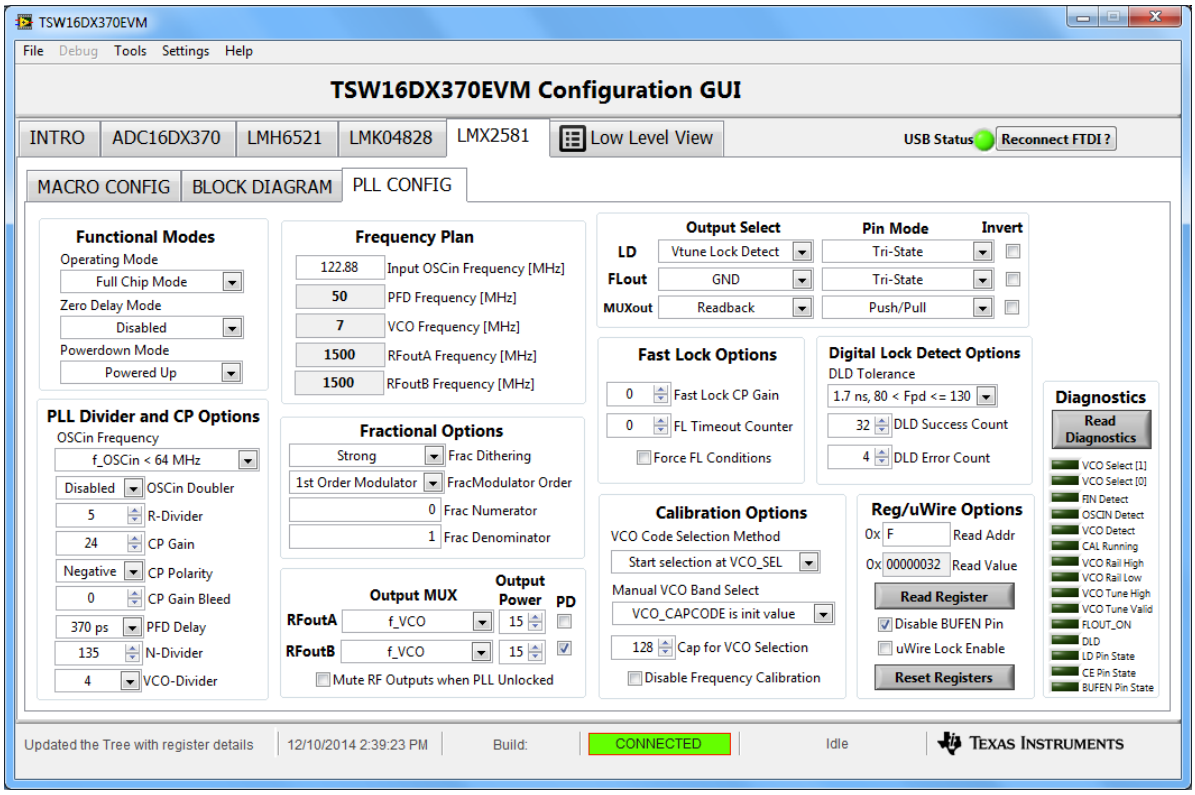


Figure 14. LMX2581 PLL Config Tab

4.3 Low-Level Control

The Low-Level View tab, shown in Figure 15, allows configuration of the devices at the bit-field level. At any time, the following controls may be used to configure or read from the device:

Control	Description
Register Map Summary	Displays the devices on the EVM, registers for those devices, and the states of the registers • Clicking on a register field allows individual bit manipulation in the Register Data Cluster • The Value column shows the value of the register at the time the GUI was last updated • The LR column shows the value of the register at the time the register was last read
Write Register Button	Write to the register highlighted in the Register Map Summary with the value in the Write Data field
Write All Button	Update all registers shown in the Register Map Summary with the values shown in the Register Map Summary • Can be used to re-synchronize the GUI with the state of the hardware
Read Register Button	Read from the register highlighted in the Register Map Summary and display the results in the Read Data field
Read All Button	Read from all registers in the Register Map Summary and display the current state of the hardware
Load Config Button	Load a Configuration File from disk and execute the commands in the file
Save Config Button	Save a Configuration File to disk that contains the current state of configuration
Register Data Cluster	Manipulate individual accessible bits of the register highlighted in the Register Map Summary
Individual Register Cluster with Read/Write Register Buttons	Perform a generic read or write command to the device shown in the 'Block' drop-down box using the Address and Write Data information

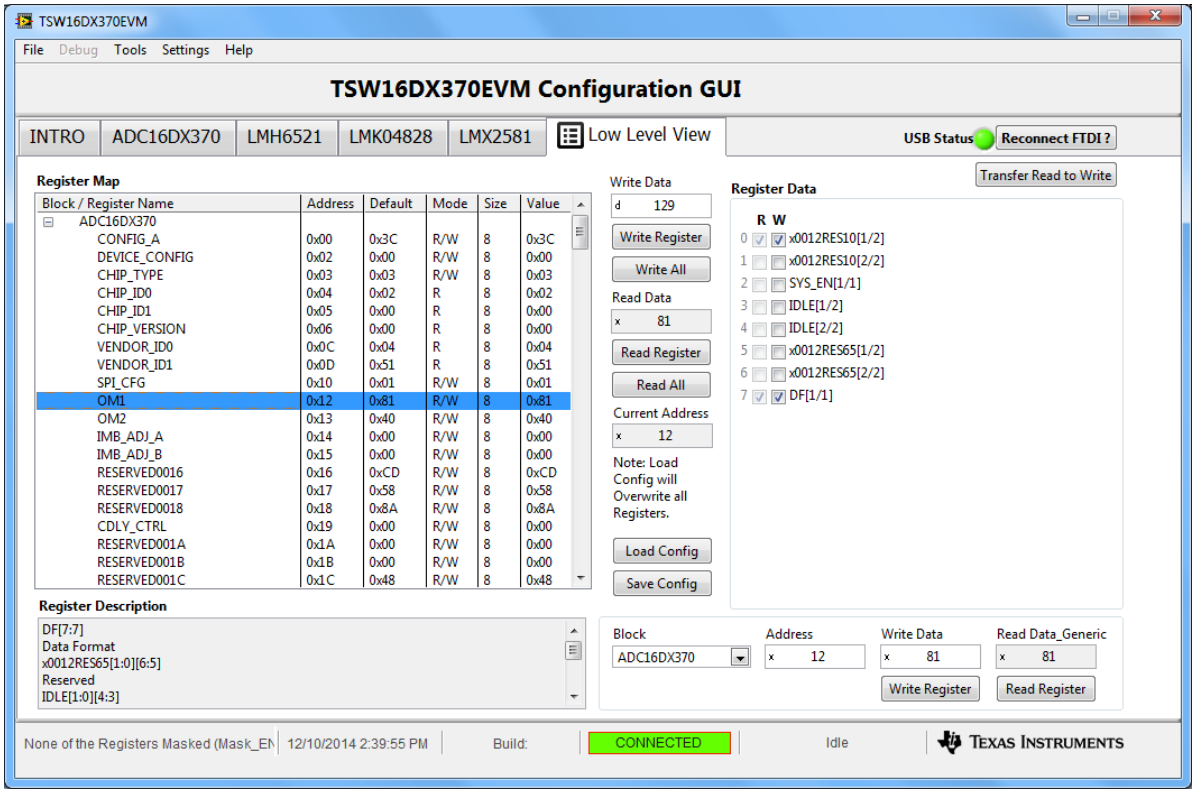


Figure 15. Low-Level Register Control Tab

5 Evaluation Troubleshooting

Table 3 provides troubleshooting procedures for several issues.

Table 3. Troubleshooting Procedures

Issue	Troubleshoot
General Problem	**Verify the test setup shown in Figure 2 and repeat the setup procedure as described in this document.**
	Check power supply to EVM and TSW14J56EVM. Verify that the power switches are in the ON position.
	Check signal and clock connections to EVM.
	Visually check the top and bottom layers of the board to verify that nothing looks discolored or damaged.
	Check the connection of all boards together.
	Try pressing the CPU_RESET button on the TSW14J56EVM.
	Try power-cycling the external power supply to the EVM and re-program the LMK and ADC devices.
TSW14J56 LEDs are not correct	Verify the settings of the configuration switches on the TSW14J56EVM.
	Verify that the EVM configuration GUI is communicating with the USB and that the configuration procedure has been followed.
	(LEDs Not Blinking) Reprogram the LMK devices.
	Try pressing the CPU_RESET button on the TSW14J56EVM.
	Try capturing data in HSDC Pro to force an LED status update.
Configuration GUI is not working properly	Verify that the USB cable is plugged into the EVM and the PC.
	Check the computer's Device Manager and verify that a 'USB Serial Device' is recognized when the EVM is connected to the PC.
	Verify that the green 'USB Status' LED light in the top right corner of the GUI is lit. If it is not lit, press 'Reconnect FTDI' button.
	Try restarting the configuration GUI.
Configuration GUI is not able to connected to the EVM	Use the free FT_PROG software from FTDI Chip and verify that the on-board FTDI chip is programmed with a Product Description that reflects the name of the EVM.
HSDP Software is not capturing good data or analysis results are incorrect.	Verify that the TSW14J56EVM is properly connected to the PC with a mini-USB cable and that the board serial number is properly identified by the HSDP software.
	Check that the proper ADC device is selected.
	Check that the analysis parameters are properly configured.
HSDP Software gives a Time-Out error when capturing data	Try to reprogram the LMK device and reset the JESD204 Link.
	Verify that the ADC sampling rate is correctly set in the HSDP software.
Sub-Optimal Measured Performance	Try pressing the 'Calibrate ADC' button on the INTRO tab or repeating the configuration GUI procedure for programming the EVM.
	Check that the spectral analysis parameters are properly configured.
	Verify that bandpass filters are used in the clock and input signal paths and that low-noise signal sources are used.

EVM Jumper Settings

The TSW16DX370EVM has three different jumpers with the following functions.

EVM Jumper Settings

Jumper	Function	Default Setting
JP1	TRF37B32 Low Power Mode Select Short 1-2: Low Power Mode enabled Short 2-3: Low Power Mode disabled	Short 2-3
JP2	ADC16DX370 SPI Bus Level Translator Interface Voltage. Set to be consistent with the SDO output interface voltage of the ADC16DX370. Short 1-2: 3.3V Short 2-3: 1.8V	Short 1-2
JP3	LMX2581 Readback Routing Short 1-2: Register readback routed to testpoint TP2 Short 2-3: Register readback routed via FTDI chip to computer	Short 2-3

A.1 TSW14J56EVM LED Bank and Switch Configuration

The LEDs on the TSW14J56EVM indicate the status of the capture board as well as status of the JESD204B link. The LEDs have the following meaning:

Table 4. Meaning of LEDs on the TSW14J56EVM

FPGA_DONE	**FPGA Programming** ON: FPGA has been programmed OFF: FPGA has NOT been programmed or is being programmed
D1	**TX SYNC~** ON: Synchronization being requested (code group synchronization phase of link initialization) OFF: Synchronization not requested (code group synchronization complete) Note: The status of this LED is only valid after attempting a data capture in HSDC Pro
D2	**TX Device Clock** BLINKING: Device clock is being received from the LMK device on the EVM NOT BLINKING: Device clock not received
D3	**SYNC~** ON: Synchronization being requested (code group synchronization phase of link initialization) OFF: Synchronization not requested (code group synchronization complete) Note: The status of this LED is only valid after attempting a data capture in HSDC Pro
D4	**RX Device Clock** BLINKING: Device clock is being received from the LMK device on the EVM NOT BLINKING: Device clock not received
D5	No Function
D6	**DDR3 Memory Calibration Done** ON: Calibration not done OFF: Calibration done, normal operation
D7	**DDR3 Memory Calibration Success** ON: Calibration not successful OFF: Calibration successful, normal operation
D8	**DDR3 Memory Calibration Fail** ON: Calibration not failed, normal operation OFF: Calibration failed

Table 5. Required State of Switches on the TSW14J56EVM

Switch	Status
SW1[1]	OFF
SW1[2]	OFF
SW1[3]	OFF
SW1[4]	OFF
SW4[1]	OFF
SW4[2]	OFF
SW4[3]	OFF
SW4[4]	OFF
SW8, MSEL0–MSEL4	All ON
TDI, TDO, TCK, TMS jumpers	All should be shorting pins 1-2
JP1 (Y1 PWR)	Short pins 1-2 (HI Setting)
J8 (USB PWR)	Short pins 1-2
JP9 (U8 ENB)	Short pins 2-3

A.2 HSDC Pro Settings for Optional ADC16DX370 Configuration

A.2.1 Changing the Number of Serial Output Lanes (L)

The ADC16DX370 outputs data on two lanes (one lane/channel) by default but the device may also be configured to output on four total lanes. This option is selected using the 'L' parameter on the JESD204B tab in the Configuration GUI. Changing the lane configuration from the default requires special HSDC Pro configuration. Contact TI for more information.

A.2.2 Changing the Number of Frames per Multi-Frame (K)

Changing the number of frames per multi-frame output by the JESD204 transmitted (ADC16DX370) is configured using the 'K' parameter on the JESD204B tab in the Configuration GUI. This parameter must be matched by the receiving device. Changing K from the default requires special HSDC Pro configuration. Contact TI for more information.

A.3 Exercising the SYSREF Input of the ADC

The SYSREF input is used to align the phase of the ADC's internal local multi-frame clock (LMFC) according to the JESD204B interface specification but it is not required to establish a link and evaluate the analog performance of the ADC with this EVM. Upon power-up, the ADC assumes a default alignment for its LMFC and proceeds to synchronize with the receiving device without requiring a SYSREF input event.

A SYSREF signal may be applied to the ADC from the LMK04828 to validate the response of the ADC to a SYSREF event. The SYSREF signal path is AC coupled, therefore only periodic signals with frequencies larger than 5 MHz are supported. Note that continuously running an SYSREF signal to the ADC during normal operating will degrade the spurious performance of the ADC.

A.4 Customizing the EVM Frequency Plan

A.4.1 Signal Path Considerations

The signal path of the TSW16DX370EVM includes two separate LC bandpass filters (BPF). These filters, in conjunction with the LO frequency and the ADC sampling rate set the frequency plan of this design which is intended for a ~100-MHz channel bandwidth and 276.48-MHz intermediate frequency (IF).

The default bandpass filters restrict the signal path frequency plan, but they may be changed. The footprints provide optimal support for a 10-pole BPF with a standard architecture. An optimal re-design of the filters should include modeling of the PCB.

A.4.2 Configuring the LMK04828

By default, the LMK04828 is configured to use PLL2 with an internal VCO and a 61.44-MHz reference from Y1. This reference is multiplied to derive the ADC sampling clock, ADC SYSREF, FPGA reference, FPGA SYSREF, and LMX2581 reference.

The LMK04828 may optionally be configured as a clock distributer and divider. A reference signal may be applied to the REFIN input (~+6 dBm) which is then divided down or passed through to generate the necessary clocks. Basic support for this configuration is available using GUI controls. Script-based customized of this mode is possible using the configuration scripts also supported by the GUI. Hardware changes are required to turn off the Y1 reference by removing FB18.

A.4.3 Configuring the LMX2581

By default, the LMX2581 can be configured to support a wide range of LO frequencies using the configuration GUI. Configuration may be performance with the MACRO configurations, CUSTOM script, or the controls present on the more detailed tabs. Care must be taken to consider the OSCin reference frequency coming from the LMK04828.

Revision History

Changes from Original (February 2015) to A Revision	Page
• Changed DVGA from LMH6517 to LMH6521	3

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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