



# TwinDie™ 1.2V DDR4 SDRAM

## MT40A1G16 – 64 Meg x 16 x 16 Banks x 1 Ranks

### Description

The 16Gb (TwinDie™) DDR4 SDRAM uses Micron’s 8Gb DDR4 SDRAM die; two x8s combined to make one x16. Similar signals as mono x16, there is one extra ZQ connection for faster ZQ Calibration and a BG1 control required for x8 addressing. Refer to Micron’s 8Gb DDR4 SDRAM data sheet (x8 option) for the specifications not included in this document. Specifications for base part number MT40A1G8 correlate to TwinDie manufacturing part number MT40A1G16.

### Features

- Uses two x8 8Gb Micron die to make one x16
- Single rank TwinDie
- $V_{DD} = V_{DDQ} = 1.2V$  (1.14–1.26V)
- 1.2V  $V_{DDQ}$ -terminated I/O
- JEDEC-standard ball-out
- Low-profile package
- $T_C$  of 0°C to 95°C
  - 0°C to 85°C: 8192 refresh cycles in 64ms
  - 85°C to 95°C: 8192 refresh cycles in 32ms

### Options

- Configuration
  - 64 Meg x 16 x 16 banks x 1 rank 1G16
- 96-ball FBGA package (Pb-free)
  - 9.5mm x 14mm x 1.2mm Die Rev :A HBA
  - 8.0mm x 14mm x 1.2mm Die Rev :B, D WBU
  - 7.5mm x 13.5mm x 1.2mm Die Rev :E KNR
- Timing – cycle time<sup>1</sup>
  - 0.625ns @ CL = 22 (DDR4-3200) -062E
  - 0.682ns @ CL = 21 (DDR4-2933) -068
  - 0.750ns @ CL = 19 (DDR4-2666) -075
  - 0.750ns @ CL = 18 (DDR4-2666) -075E
  - 0.833ns @ CL = 17(DDR4-2400) -083
  - 0.833ns @ CL = 16 (DDR4-2400) -083E
  - 0.937ns @ CL = 15 (DDR4-2133) -093E
  - 1.071ns @ CL = 13 (DDR4-1866) -107E
- Self refresh
  - Standard None
- Operating temperature
  - Commercial (0°C ≤  $T_C$  ≤ 95°C) None
- Revision
  - :A
  - :B, D
  - :E

Note: 1. CL = CAS (READ) latency.

**Table 1: Key Timing Parameters**

Speed Grade <sup>1</sup>	Data Rate (MT/s)	Target <sup>t</sup> RCD- <sup>t</sup> RP-CL	<sup>t</sup> RCD (ns)	<sup>t</sup> RP (ns)	CL (ns)
-062Y	3200	22-22-22	13.75 (13.32)	13.75 (13.32)	13.75 (13.32)
-062E	3200	22-22-22	13.75	13.75	13.75
-068	2933	21-21-21	14.32 (13.75)	14.32 (13.75)	14.32 (13.75)
-075E	2666	18-18-18	13.50	13.50	13.50
-075	2666	19-19-19	14.25	14.25	14.25
-083E	2400	16-16-16	13.32	13.32	13.32
-083	2400	17-17-17	14.16 (13.75)	14.16 (13.75)	14.16 (13.75)
-093E	2133	15-15-15	14.06 (13.50)	14.06 (13.50)	14.06 (13.50)
-093	2133	16-16-16	15.00	15.00	15.00
-107E	1866	13-13-13	13.92 (13.50)	13.92 (13.50)	13.92 (13.50)

Note: 1. Refer to Speed Bin Tables for additional details.



**Table 2: Addressing**

Parameter	1024 Meg x 16
Configuration	64 Meg x 16 x 16 banks x 1 rank
Bank group address	BG[1:0]
Bank count per group	4
Bank address in bank group	BA[1:0]
Row addressing	64K (A[15:0])
Column addressing	1K (A[9:0])
Page size	1KB

Note: 1. Page size is per bank, calculated as follows:  
Page size =  $2^{\text{COLBITS}} \times \text{ORG}/8$ , where COLBIT = the number of column address bits and ORG = the number of DQ bits.

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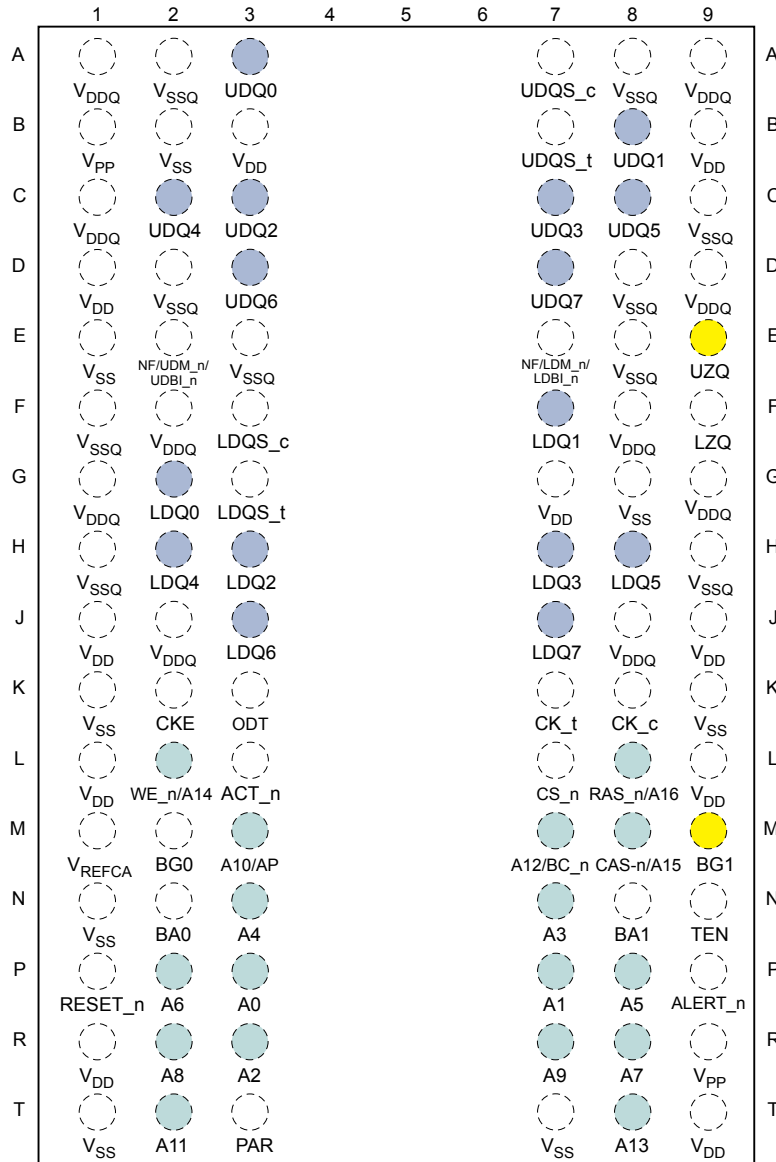
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## Ball Assignments

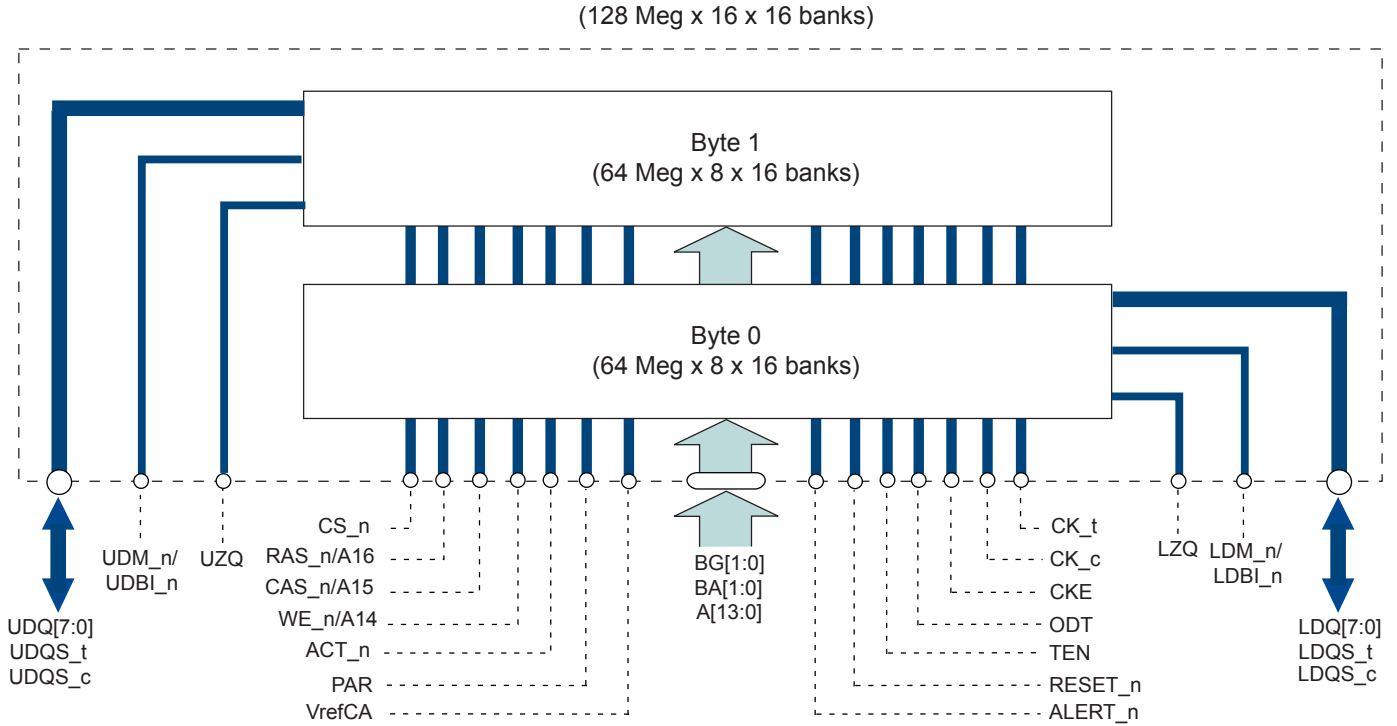
Figure 1: 96-Ball x16 SR DDP Ball Assignments



- Notes:
1. See Ball Descriptions in the monolithic data sheet.
  2. A slash "/" defines a selectable function. For example: Ball E2 = NF/UDM\_n/UDBI\_n where either NF, UDM\_n, or UDBI\_n is defined via MRS.

## Functional Block Diagrams

**Figure 2: Functional Block Diagram (128 Meg x 16 x 16 Banks x 1 Rank)**



## Connectivity Test Mode

Connectivity test (CT) mode for the x16 TwinDie single rank (SR) device is the same as two mono x8 devices connected in parallel. The mapping is restated for clarity.

### Minimum Terms Definition for Logic Equations

The test input and output pins are related by the following equations, where INV denotes a logical inversion operation and XOR a logical exclusive OR operation:

$MT0 = \text{XOR}(A1, A6, PAR)$   
 $MT1 = \text{XOR}(A8, ALERT\_n, A9)$   
 $MT2 = \text{XOR}(A2, A5, A13)$   
 $MT3 = \text{XOR}(A0, A7, A11)$   
 $MT4 = \text{XOR}(CK\_c, ODT, CAS\_n/A15)$   
 $MT5 = \text{XOR}(CKE, RAS\_n/A16, A10/AP)$   
 $MT6 = \text{XOR}(ACT\_n, A4, BA1)$   
 $MT7L = \text{XOR}(BG1, LDM\_n/LDBI\_n, CK\_t)$   
 $MT7U = \text{XOR}(BG1, UDM\_n/UDBI\_n, CK\_t)$   
 $MT8 = \text{XOR}(WE\_n/A14, A12 / BC, BA0)$   
 $MT9 = \text{XOR}(BG0, A3, RESET\_n \text{ and } TEN)$

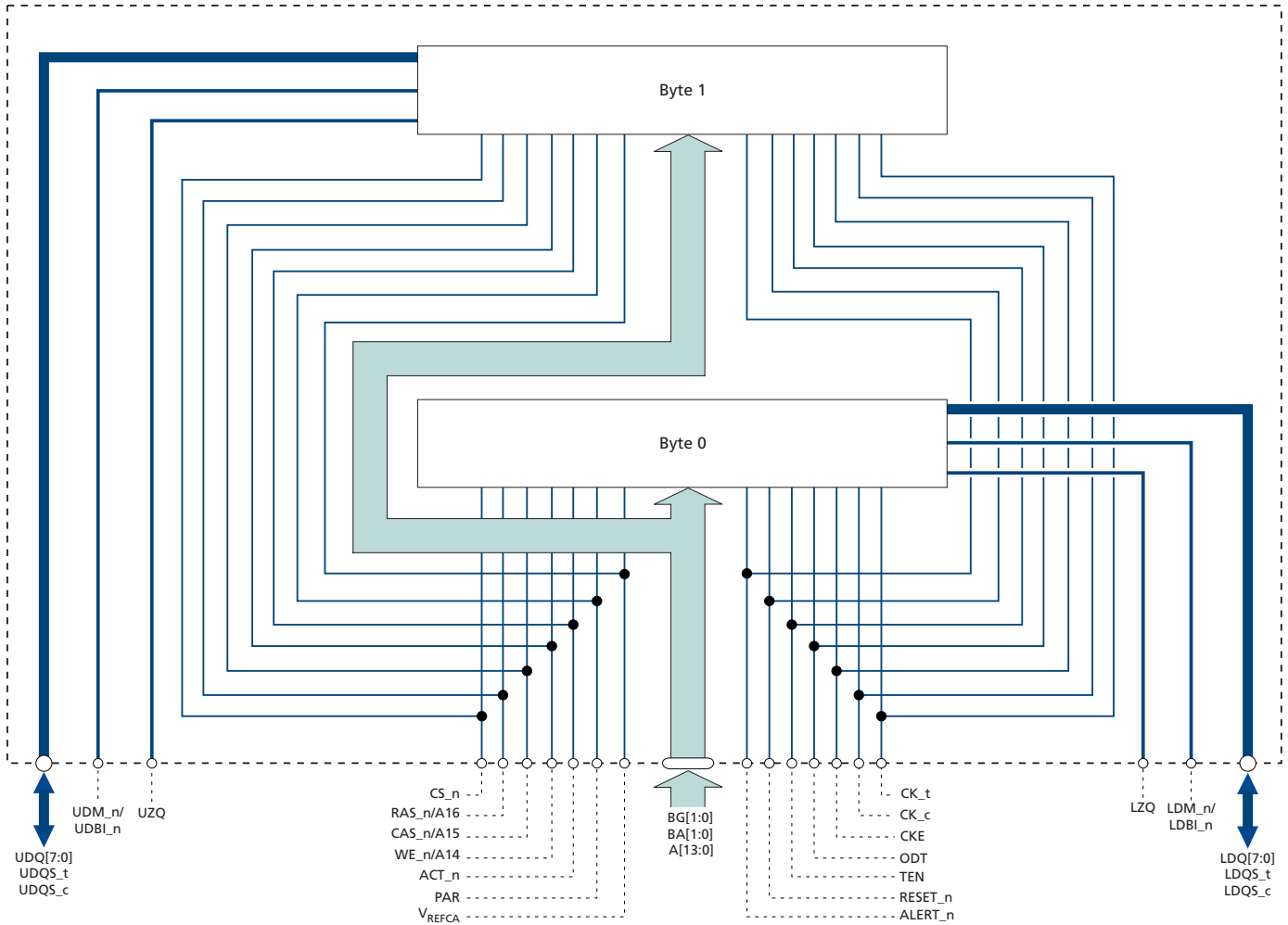
### Logic Equations for a x16 TwinDie, SR Device

Byte 0	Byte 1
LDQ0 = MT0	UDQ0 = MT0
LDQ1 = MT1	UDQ1 = MT1
LDQ2 = MT2	UDQ2 = MT2
LDQ3 = MT3	UDQ3 = MT3
LDQ4 = MT4	UDQ4 = MT4
LDQ5 = MT5	UDQ5 = MT5
LDQ6 = MT6	UDQ6 = MT6
LDQ7 = MT7L	UDQ7 = MT7U
LDQS_t = MT8	UDQS_t = MT8
LDQS_c = MT9	UDQS_c = MT9

### x16 TwinDie, SR Internal Connections

The figure below shows the internal connections of the x16 TwinDie, SR. The diagram shows why byte 0 and byte 1 outputs have the same logic equations except LDQ7 and UDQ7; they are different because the DM\_n/DBI\_n pins are not common for each byte.

**Figure 3: x16 TwinDie, SR**



## Electrical Specifications – Leakages

**Table 3: Input and Output Leakages**

Symbol	Parameter	Min	Max	Units	Notes
$I_I$	Input leakage current Any input $0V \leq V_{IN} \leq V_{DD}$ , $V_{REF}$ pin $0V \leq V_{IN} \leq 1.1V$ (All other pins not under test = 0V)	-4	4	$\mu A$	1
$I_{VREF}$	$V_{REF}$ supply leakage current $V_{REFDQ} = V_{DD}/2$ or $V_{REFCA} = V_{DD}/2$ (All other pins not under test = 0V)	-4	4	$\mu A$	2
$I_{ZQ}$	Input leakage on ZQ pin	-50	10	$\mu A$	
$I_{TEN}$	Input leakage on TEN pin	-12	20	$\mu A$	
$I_{OZPD}$	Output leakage: $V_{OUT} = V_{DDQ}$	-	10	$\mu A$	3
$I_{OZPU}$	Output leakage: $V_{OUT} = V_{SSQ}$	-50	-	$\mu A$	3, 4

- Notes:
1. Any input  $0V < V_{in} < 1.1V$
  2.  $V_{REFCA} = V_{DD}/2$ ,  $V_{DD}$  at valid level.
  3. DQs are disabled.
  4. ODT is disabled with the ODT input HIGH.

## Temperature and Thermal Impedance

It is imperative that the DDR4 SDRAM device's temperature specifications, shown in the following table, be maintained in order to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances listed in Table 5 (page 9) apply to the current die revision and packages.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications," prior to using the values listed in the thermal impedance table. For designs that are expected to last several years and require the flexibility to use several DRAM die shrinks, consider using final target theta values (rather than existing values) to account for increased thermal impedances from the die size reduction.

The DDR4 SDRAM device's safe junction temperature range can be maintained when the  $T_C$  specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required to satisfy the case temperature specifications.



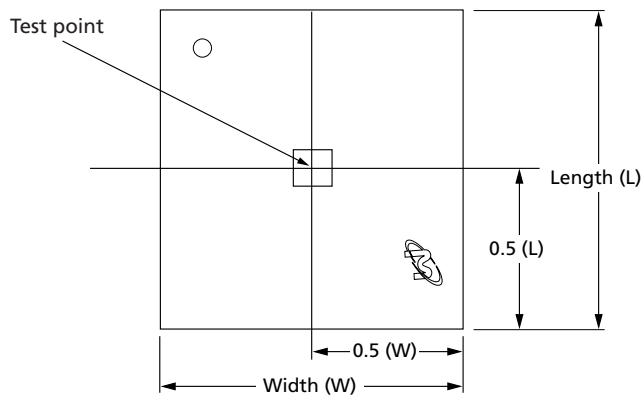
**Table 4: Thermal Characteristics**

Notes 1–3 apply to entire table

Parameter	Symbol	Value	Units	Notes
Operating temperature	$T_C$	0 to 85	°C	
		0 to 95	°C	4

- Notes:
1. MAX operating case temperature  $T_C$  is measured in the center of the package, as shown below.
  2. A thermal solution must be designed to ensure that the device does not exceed the maximum  $T_C$  during operation.
  3. Device functionality is not guaranteed if the device exceeds maximum  $T_C$  during operation.
  4. If  $T_C$  exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9µs interval refresh rate. The use of self refresh temperature (SRT) or automatic self refresh (ASR), if available, must be enabled.

**Figure 4: Temperature Test Point Location**



**Table 5: Thermal Impedance**

Die Rev.	Substrate conductivity	$\Theta_{JA}$ (°C/W) Airflow = 0m/s	$\Theta_{JA}$ (°C/W) Airflow = 1m/s	$\Theta_{JA}$ (°C/W) Airflow = 2m/s	$\Theta_{JB}$ (°C/W)	$\Theta_{JC}$ (°C/W)	Notes
A	Low	TBD	TBD	TBD	N/A	TBD	1
	High	TBD	TBD	TBD	TBD	N/A	
B, D	Low	43.9	33.0	29.5	N/A	3.3	1
	High	27.1	21.7	20.1	10.5	N/A	
E	Low	TBD	TBD	TBD	N/A	TBD	1
	High	TBD	TBD	TBD	TBD	N/A	

- Note:
1. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.



## DRAM Package Electrical Specifications

**Table 6: DRAM Package Electrical Specifications for x16 Devices**

Notes 1–4 apply to the entire table

Parameter		Symbol	DDR4-1600, -1866		DDR4-2133, -2400		DDR4-2666, -2933		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Input/ output	Zpkg	$Z_{IO}$	30	50	30	50	30	50	ohm	5, 6
	Package delay	$Td_{IO}$	60	120	60	120	60	120	ps	6, 7
	Lpkg	$L_{IO}$	–	5.0	–	5.0	–	5.0	nH	
	Cpkg	$C_{IO}$	–	3.0	–	3.0	–	3.0	pF	
DQSL_t/ DQSL_c/ DQSU_t/ DQSU_c	Zpkg	$Z_{IO\ DQS}$	30	50	30	50	30	50	ohm	5
	Package delay	$Td_{IO\ DQS}$	60	120	60	120	60	120	ps	7
	Lpkg	$L_{IO\ DQS}$	–	5.0	–	5.0	–	5.0	nH	
	Cpkg	$C_{IO\ DQS}$	–	3.0	–	3.0	–	3.0	pF	
DQSL_t/ DQSL_c, DQSU_t/ DQSU_c,	Delta Zpkg	$DZ_{IO\ DQS}$	–	20	–	20	–	20	ohm	5, 8
	Delta delay	$DTd_{IO\ DQS}$	–	45	–	45	–	45	ps	7, 8
Input CTRL pins	Zpkg	$Z_{I\ CTRL}$	35	65	35	65	35	65	ohm	5, 9
	Package delay	$Td_{I\ CTRL}$	75	120	75	120	75	120	ps	7, 9
	Lpkg	$L_{I\ CTRL}$	–	6.5	–	6.5	–	6.5	nH	
	Cpkg	$C_{I\ CTRL}$	–	2.5	–	2.5	–	2.5	pF	
Input CMD ADD pins	Zpkg	$Z_{I\ ADD\ CMD}$	35	65	35	65	35	65	ohm	5, 10
	Package delay	$Td_{I\ ADD\ CMD}$	70	125	70	125	70	125	ps	7, 10
	Lpkg	$L_{I\ ADD\ CMD}$	–	6.5	–	6.5	–	6.5	nH	
	Cpkg	$C_{I\ ADD\ CMD}$	–	3.0	–	3.0	–	3.0	pF	
CK_t, CK_c	Zpkg	$Z_{CK}$	30	55	30	55	30	55	ohm	5
	Package delay	$Td_{CK}$	80	135	80	135	80	135	ps	7
	Delta Zpkg	$DZ_{DCK}$	–	0.5	–	0.5	–	0.5	ohm	5, 11
	Delta delay	$DTd_{DCK}$	–	1.2	–	1.2	–	1.2	ps	7, 11
Input CLK	Lpkg	$L_{I\ CLK}$	–	6.0	–	6.0	–	6.0	nH	
	Cpkg	$C_{I\ CLK}$	–	3.0	–	3.0	–	3.0	pF	
ZQ Zpkg		$Z_{O\ ZQ}$	–	40	–	40	–	40	ohm	5
ZQ delay		$Td_{O\ ZQ}$	30	135	30	135	30	135	ps	7
ALERT Zpkg		$Z_{O\ ALERT}$	30	55	30	55	30	55	ohm	5
ALERT delay		$Td_{O\ ALERT}$	65	110	65	110	65	110	ps	7

- Notes:
1. The package parasitic (L and C) are not subject to production testing. If the package parasitic (L and C) are measured, the capacitance is measured with  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ , and  $V_{SSQ}$  shorted with all other signal pins floating. The inductance is measured with  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ , and  $V_{SSQ}$  shorted and all other signal pins shorted at the die, not pin, side.
  2. Package implementations should satisfy targets if the Zpkg and package delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum



# 16Gb: x16 TwinDie Single Rank DDR4 SDRAM DRAM Package Electrical Specifications

values shown. The package design targets are provided for reference, system signal simulations should not use these values but use the Micron package model.

3. It is assumed that Lpkg can be approximated as  $L_{pkg} = Z_O \times T_d$ .
4. It is assumed that Cpkg can be approximated as  $C_{pkg} = T_d/Z_O$ .
5. Package-only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where: Zpkg (total per pin) =  $\text{SQRT}(L_{pkg}/C_{pkg})$ .
6.  $Z_{IO}$  and  $T_{dIO}$  apply to DQ, DM, DQS\_c, DQS\_t, TDQS\_t, and TDQS\_c.
7. Package-only delay (Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where:  $T_{dpkg}$  (total per pin) =  $\text{SQRT}(L_{pkg} \times C_{pkg})$ .
8. Absolute value of  $Z_{IO}$  (DQS\_t),  $Z_{IO}$  (DQS\_c) for impedance (Z) or absolute value of  $T_{dIO}$  (DQS\_t),  $T_{dIO}$  (DQS\_c) for delay (Td).
9.  $Z_{I\_CTRL}$  and  $T_{dI\_CTRL}$  apply to ODT, CS\_n, and CKE.
10.  $Z_{I\_ADD\_CMD}$  and  $T_{dI\_ADD\_CMD}$  apply to A[17:0], BA[1:0], BG[1:0], RAS\_n CAS\_n, and WE\_n.
11. Absolute value of ZCK\_t, ZCK\_c for impedance (Z) or absolute value of  $T_{dCK\_t}$ ,  $T_{dCK\_c}$  for delay (Td).

**Table 7: Pad Input/Output Capacitance**

Parameter	Symbol	DDR4-1600, -1866, -2133		DDR4-2400, -2666		DDR4-2933		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Input/output capacitance: DQ, DM, DQS_t, DQS_c, TDQS_t, TDQS_c	$C_{IO}$	1.8	2.8	1.8	2.8	1.8	2.8	pF	1, 2, 3
Input capacitance: CK_t and CK_c	$C_{CK}$	2.1	2.9	2.1	2.9	2.1	2.9	pF	1, 2, 3, 4
Input capacitance delta: CK_t and CK_c	$C_{DCK}$	0	0.05	0	0.05	0	0.05	pF	1, 2, 3, 5
Input/output capacitance delta: DQS_t and DQS_c	$C_{DDQS}$	0	0.05	0	0.05	0	0.05	pF	1, 3
Input capacitance: CTRL, ADD, CMD input-only pins	$C_I$	1.6	2.6	1.6	2.6	1.6	2.6	pF	1, 3, 6
Input capacitance delta: All CTRL input-only pins	$C_{DI\_CTRL}$	-0.9	0.9	-0.9	0.9	-0.9	0.9	pF	1, 3, 7
Input capacitance delta: All ADD/CMD input-only pins	$C_{DI\_ADD\_CMD}$	-0.9	0.9	-0.9	0.9	-0.9	0.9	pF	1, 3, 8, 9
Input/output capacitance delta: DQ, DM, DQS_t, DQS_c, TDQS_t, TDQS_c	$C_{DIO}$	-0.16	0.16	-0.16	0.16	-0.16	0.16	pF	1, 2, 10, 11
Input/output capacitance: ALERT pin	$C_{ALERT}$	1.1	2.3	1.1	2.3	1.1	2.3	pF	1, 3
Input/output capacitance: ZQ pin	$C_{ZQ}$	-	3.7	-	3.7	-	3.7	pF	1, 3, 12
Input/output capacitance: TEN pin	$C_{TEN}$	0.2	2.3	0.2	2.3	0.2	2.3	pF	1, 3, 13

Notes: 1. Although the DM, TDQS\_t, and TDQS\_c pins have different functions, the loading matches DQ and DQS.

2. This parameter is not subject to a production test; it is verified by design and characterization and are provided for reference; system signal simulations should not use these values but use the Micron package model. The capacitance, if and when, is measured according to the JEP147 specification, "Procedure for Measuring Input Capacitance Using a Vector Network Analyzer (VNA)," with  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ , and  $V_{SSQ}$  applied and all other pins floating (except the pin under test, CKE, RESET\_n and ODT, as necessary).  $V_{DD} = V_{DDQ} = 1.5V$ ,  $V_{BIAS} = V_{DD}/2$  and on-die termination off.
3. This parameter applies to SR x16 TwinDie, obtained by de-embedding the package L and C parasitics.
4.  $C_{DIO} = C_{IO}(DQ, DM) - 0.5 \times (C_{IO}(DQS\_t) + C_{IO}(DQS\_c))$ .
5. Absolute value of  $C_{IO}(DQS\_t)$ ,  $C_{IO}(DQS\_c)$
6. Absolute value of  $CCK\_t$ ,  $CCK\_c$
7.  $C_i$  applies to ODT, CS\_n, CKE, A[15:0], BA[1:0], RAS\_n, CAS\_n, and WE\_n.
8.  $C_{DL\_CTRL}$  applies to ODT, CS\_n, and CKE.
9.  $C_{DL\_CTRL} = C_i(CTRL) - 0.5 \times (C_i(CLK\_t) + C_i(CLK\_c))$ .
10.  $C_{DL\_ADD\_CMD}$  applies to A[15:0], BA[1:0], RAS\_n, CAS\_n and WE\_n.
11.  $C_{DL\_ADD\_CMD} = C_i(ADD\_CMD) - 0.5 \times (C_i(CLK\_t) + C_i(CLK\_c))$ .
12. Maximum external load capacitance on ZQ pin: 5pF.
13. Only applicable if TEN pin does not have an internal pull-up.



## Current Specifications – Limits

Table 8: x16 I<sub>DD</sub>, I<sub>PP</sub>, and I<sub>DDQ</sub> Current Limits – Rev. A

Symbol	DDR4-2133 <sup>1</sup>	DDR4-2400	DDR4-2666	DDR4-2933	Unit	Notes
I <sub>DD0</sub> : One bank ACTIVATE-to-PRECHARGE current	110	120	130	TBD	mA	2, 3, 4
I <sub>PP0</sub> : One bank ACTIVATE-to-PRECHARGE I <sub>PP</sub> current	6	6	6	TBD	mA	
I <sub>DD1</sub> : One bank ACTIVATE-to-READ-to-PRECHARGE current	140	150	160	TBD	mA	3, 4, 5
I <sub>DD2N</sub> : Precharge standby current	90	100	110	TBD	mA	4, 6, 7, 8, 9, 10, 11
I <sub>DD2NT</sub> : Precharge standby ODT current	110	120	130	TBD	mA	4, 11
I <sub>DD2P</sub> : Precharge power-down current	50	60	70	TBD	mA	4, 11
I <sub>DD2Q</sub> : Precharge quiet standby current	90	90	100	TBD	mA	4, 11
I <sub>DD3N</sub> : Active standby current	110	110	120	TBD	mA	4, 11
I <sub>PP3N</sub> : Active standby I <sub>PP</sub> current	6	6	6	TBD	mA	
I <sub>DD3P</sub> : Active power-down current	70	80	80	TBD	mA	4, 11
I <sub>DD4R</sub> : Burst read current	300	300	350	TBD	mA	4, 14, 13, 11
I <sub>DD4W</sub> : Burst write current	300	320	350	TBD	mA	4, 11, 15, 16, 17, 18
I <sub>DD5R</sub> : Distributed refresh current (1X REF)	128	128	136	TBD	mA	4, 19, 20
I <sub>PP5R</sub> : Distributed refresh I <sub>PP</sub> current (1X REF)	10	10	10	TBD	mA	
I <sub>DD6N</sub> : Self refresh current; 0–85°C	60	60	60	TBD	mA	11, 21
I <sub>DD6E</sub> : Self refresh current; 0–95°C	70	70	70	TBD	mA	11, 22
I <sub>DD6R</sub> : Self refresh current; 0–45°C	50	50	50	TBD	mA	11, 23, 24
I <sub>DD6A</sub> : Auto self refresh current (25°C)	40	40	40	TBD	mA	11, 24
I <sub>DD6A</sub> : Auto self refresh current (45°C)	50	50	50	TBD	mA	11, 24
I <sub>DD6A</sub> : Auto self refresh current (75°C)	70	70	70	TBD	mA	11, 24
I <sub>PP6X</sub> : Auto self refresh current I <sub>PP</sub> current	10	10	10	TBD	mA	11, 24
I <sub>DD7</sub> : Bank interleave read current	400	410	430	TBD	mA	4
I <sub>PP7</sub> : Bank interleave read I <sub>PP</sub> current	30	30	30	TBD	mA	
I <sub>DD8</sub> : Maximum power-down current	40	40	40	TBD	mA	11

- Notes:
1. DDR4-1600 and DDR4-1866 use the same I<sub>DD</sub> limits as DDR4-2133.
  2. When additive latency is enabled for I<sub>DD0</sub>, current changes by approximately 0%.
  3. I<sub>PP0</sub> test and limit is applicable for I<sub>DD0</sub> and I<sub>DD1</sub> conditions.
  4. The I<sub>DD</sub> values must be derated (increased) when operated outside of the range 0°C ≤ T<sub>C</sub> ≤ 85°C:



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When  $T_C < 0^\circ\text{C}$ :  $I_{DD2P}$  and  $I_{DD3P}$  must be derated by 6%;  $I_{DD4R}$  and  $I_{DD4W}$  must be derated by +4%; and  $I_{DD7}$  must be derated by +11%.

When  $T_C > 85^\circ\text{C}$ :  $I_{DD0}$ ,  $I_{DD1}$ ,  $I_{DD2N}$ ,  $I_{DD2NT}$ ,  $I_{DD2Q}$ ,  $I_{DD3N}$ ,  $I_{DD3P}$ ,  $I_{DD4R}$ ,  $I_{DD4W}$ , and  $I_{DD5R}$  must be derated by +3%;  $I_{DD2P}$  must be derated by +40%.

5. When additive latency is enabled for  $I_{DD1}$ , current changes by approximately +4%.
6. When additive latency is enabled for  $I_{DD2N}$ , current changes by approximately 0%.
7. When DLL is disabled for  $I_{DD2N}$ , current changes by approximately -23%.
8. When CAL is enabled for  $I_{DD2N}$ , current changes by approximately -25%.
9. When gear-down is enabled for  $I_{DD2N}$ , current changes by approximately 0%.
10. When CA parity is enabled for  $I_{DD2N}$ , current changes by approximately +7%.
11.  $I_{PP3N}$  test and limit is applicable for all  $I_{DD2x}$ ,  $I_{DD3x}$ ,  $I_{DD4x}$ ,  $I_{DD6x}$ , and  $I_{DD8}$  conditions; that is, testing  $I_{PP3N}$  should satisfy the  $I_{PP5}$  for the noted  $I_{DD}$  tests.
12. When additive latency is enabled for  $I_{DD3N}$ , current changes by approximately +0.6%.
13. When additive latency is enabled for  $I_{DD4R}$ , current changes by approximately +5%.
14. When read DBI is enabled for  $I_{DD4R}$ , current changes by approximately 0%.
15. When additive latency is enabled for  $I_{DD4W}$ , current changes by approximately +4%.
16. When write DBI is enabled for  $I_{DD4W}$ , current changes by approximately 0%.
17. When write CRC is enabled for  $I_{DD4W}$ , current changes by approximately -3%.
18. When CA parity is enabled for  $I_{DD4W}$ , current changes by approximately +12%.
19. When 2X REF is enabled for  $I_{DD5R}$ , current changes by approximately -14%.
20. When 4X REF is enabled for  $I_{DD5R}$ , current changes by approximately -33%.
21. Applicable for MR2 settings  $A7 = 0$  and  $A6 = 0$ ; manual mode with normal temperature range of operation (0–85°C).
22. Applicable for MR2 settings  $A7 = 1$  and  $A6 = 0$ ; manual mode with extended temperature range of operation (0–95°C).
23. Applicable for MR2 settings  $A7 = 0$  and  $A6 = 1$ ; manual mode with reduced temperature range of operation (0–45°C).
24.  $I_{DD6R}$  and  $I_{DD6A}$  values are typical.

**Table 9: x16  $I_{DD}$ ,  $I_{PP}$ , and  $I_{DDQ}$  Current Limits – Rev. B**

Symbol	DDR4-2133 <sup>1</sup>	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit	Notes
$I_{DD0}$ : One bank ACTIVATE-to-PRE-CHARGE current	90	96	102	108	114	mA	2, 3, 4
$I_{PP0}$ : One bank ACTIVATE-to-PRE-CHARGE $I_{PP}$ current	6	6	6	6	6	mA	
$I_{DD1}$ : One bank ACTIVATE-to-READ-to-PRECHARGE current	114	120	126	132	138	mA	3, 4, 5
$I_{DD2N}$ : Precharge standby current	66	68	70	72	74	mA	4, 6, 7, 8, 9, 10, 11
$I_{DD2NT}$ : Precharge standby ODT current	90	100	100	110	120	mA	4, 11
$I_{DD2P}$ : Precharge power-down current	50	50	50	50	50	mA	4, 11
$I_{DD2Q}$ : Precharge quiet standby current	60	60	60	60	60	mA	4, 11
$I_{DD3N}$ : Active standby current	80	86	92	98	104	mA	4, 11



**Table 9: x16 I<sub>DD</sub>, I<sub>PP</sub>, and I<sub>DDQ</sub> Current Limits – Rev. B (Continued)**

Symbol	DDR4-2133 <sup>1</sup>	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit	Notes
I <sub>PP3N</sub> : Active standby I <sub>PP</sub> current	6	6	6	6	6	mA	
I <sub>DD3P</sub> : Active power-down current	70	74	78	82	86	mA	4, 11
I <sub>DD4R</sub> : Burst read current	250	270	292	314	336	mA	4, 14, 13, 11
I <sub>DD4W</sub> : Burst write current	230	246	264	282	300	mA	4, 11, 15, 16, 17, 18
I <sub>DD5R</sub> : Distributed refresh current (1X REF)	100	106	112	118	124	mA	4, 19, 20
I <sub>PP5R</sub> : Distributed refresh I <sub>PP</sub> current (1X REF)	10	10	10	10	10	mA	
I <sub>DD6N</sub> : Self refresh current; 0–85°C	60	60	60	60	60	mA	11, 21
I <sub>DD6E</sub> : Self refresh current; 0–95°C	70	70	70	70	70	mA	11, 22
I <sub>DD6R</sub> : Self refresh current; 0–45°C	40	40	40	40	40	mA	11, 23, 24
I <sub>DD6A</sub> : Auto self refresh current (25°C)	17.2	17.2	17.2	17.2	17.2	mA	11, 24
I <sub>DD6A</sub> : Auto self refresh current (45°C)	40	40	40	40	40	mA	11, 24
I <sub>DD6A</sub> : Auto self refresh current (75°C)	60	60	60	60	60	mA	11, 24
I <sub>PP6X</sub> : Auto self refresh current I <sub>PP</sub> current	10	10	10	10	10	mA	11, 24
I <sub>DD7</sub> : Bank interleave read current	340	350	360	370	380	mA	4
I <sub>PP7</sub> : Bank interleave read I <sub>PP</sub> current	30	30	30	30	30	mA	
I <sub>DD8</sub> : Maximum power-down current	50	50	50	50	50	mA	11

- Notes:
1. DDR4-1600 and DDR4-1866 use the same I<sub>DD</sub> limits as DDR4-2133.
  2. When additive latency is enabled for I<sub>DD0</sub>, current changes by approximately 0%.
  3. I<sub>PP0</sub> test and limit is applicable for I<sub>DD0</sub> and I<sub>DD1</sub> conditions.
  4. The I<sub>DD</sub> values must be derated (increased) when operated outside of the range 0°C ≤ T<sub>C</sub> ≤ 85°C:
 

When T<sub>C</sub> < 0°C: I<sub>DD2P</sub> and I<sub>DD3P</sub> must be derated by 6%; I<sub>DD4R</sub> and I<sub>DD4W</sub> must be derated by +4%; and I<sub>DD7</sub> must be derated by +11%.

When T<sub>C</sub> > 85°C: I<sub>DD0</sub>, I<sub>DD1</sub>, I<sub>DD2N</sub>, I<sub>DD2NT</sub>, I<sub>DD2Q</sub>, I<sub>DD3N</sub>, I<sub>DD3P</sub>, I<sub>DD4R</sub>, I<sub>DD4W</sub>, and I<sub>DD5R</sub> must be derated by +3%; I<sub>DD2P</sub> must be derated by +40%.
  5. When additive latency is enabled for I<sub>DD1</sub>, current changes by approximately +4%.
  6. When additive latency is enabled for I<sub>DD2N</sub>, current changes by approximately 0%.
  7. When DLL is disabled for I<sub>DD2N</sub>, current changes by approximately –23%.
  8. When CAL is enabled for I<sub>DD2N</sub>, current changes by approximately –25%.
  9. When gear-down is enabled for I<sub>DD2N</sub>, current changes by approximately 0%.



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10. When CA parity is enabled for  $I_{DD2N}$ , current changes by approximately +7%.
11.  $I_{PP3N}$  test and limit is applicable for all  $I_{DD2x}$ ,  $I_{DD3x}$ ,  $I_{DD4x}$ ,  $I_{DD6x}$ , and  $I_{DD8}$  conditions; that is, testing  $I_{PP3N}$  should satisfy the  $I_{PPS}$  for the noted  $I_{DD}$  tests.
12. When additive latency is enabled for  $I_{DD3N}$ , current changes by approximately +0.6%.
13. When additive latency is enabled for  $I_{DD4R}$ , current changes by approximately +5%.
14. When read DBI is enabled for  $I_{DD4R}$ , current changes by approximately 0%.
15. When additive latency is enabled for  $I_{DD4W}$ , current changes by approximately +4%.
16. When write DBI is enabled for  $I_{DD4W}$ , current changes by approximately 0%.
17. When write CRC is enabled for  $I_{DD4W}$ , current changes by approximately -3%.
18. When CA parity is enabled for  $I_{DD4W}$ , current changes by approximately +12%.
19. When 2X REF is enabled for  $I_{DD5R}$ , current changes by approximately -14%.
20. When 4X REF is enabled for  $I_{DD5R}$ , current changes by approximately -33%.
21. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).
22. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0–95°C).
23. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0–45°C).
24.  $I_{DD6R}$  and  $I_{DD6A}$  values are typical.

**Table 10: x16  $I_{DD}$ ,  $I_{PP}$ , and  $I_{DDQ}$  Current Limits – Rev. D**

Symbol	DDR4-2133 <sup>1</sup>	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit	Notes
$I_{DD0}$ : One bank ACTIVATE-to-PRECHARGE current	90	96	102	108	114	mA	2, 3, 4
$I_{PP0}$ : One bank ACTIVATE-to-PRECHARGE $I_{PP}$ current	6	6	6	6	6	mA	
$I_{DD1}$ : One bank ACTIVATE-to-READ-to-PRECHARGE current	114	120	126	132	138	mA	3, 4, 5
$I_{DD2N}$ : Precharge standby current	66	68	70	72	74	mA	4, 6, 7, 8, 9, 10, 11
$I_{DD2NT}$ : Precharge standby ODT current	90	100	100	110	120	mA	4, 11
$I_{DD2P}$ : Precharge power-down current	50	50	50	50	50	mA	4, 11
$I_{DD2Q}$ : Precharge quiet standby current	60	60	60	60	60	mA	4, 11
$I_{DD3N}$ : Active standby current	90	96	102	108	112	mA	4, 11
$I_{PP3N}$ : Active standby $I_{PP}$ current	6	6	6	6	6	mA	
$I_{DD3P}$ : Active power-down current	70	74	78	82	86	mA	4, 11
$I_{DD4R}$ : Burst read current	250	270	292	314	336	mA	4, 14, 13, 11
$I_{DD4W}$ : Burst write current	250	264	284	300	320	mA	4, 11, 15, 16, 17, 18





Table 10: x16 I<sub>DD</sub>, I<sub>PP</sub>, and I<sub>DDQ</sub> Current Limits – Rev. D (Continued)

Symbol	DDR4-2133 <sup>1</sup>	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit	Notes
I <sub>DD5R</sub> : Distributed refresh current (1X REF)	112	116	122	128	132	mA	4, 19, 20
I <sub>PP5R</sub> : Distributed refresh I <sub>PP</sub> current (1X REF)	10	10	10	10	10	mA	
I <sub>DD6N</sub> : Self refresh current; 0–85°C	62	62	62	62	62	mA	11, 21
I <sub>DD6E</sub> : Self refresh current; 0–95°C	72	72	72	72	72	mA	11, 22
I <sub>DD6R</sub> : Self refresh current; 0–45°C	42	42	42	42	42	mA	11, 23, 24
I <sub>DD6A</sub> : Auto self refresh current (25°C)	17.2	17.2	17.2	17.2	17.2	mA	11, 24
I <sub>DD6A</sub> : Auto self refresh current (45°C)	42	42	42	42	42	mA	11, 24
I <sub>DD6A</sub> : Auto self refresh current (75°C)	62	62	62	62	62	mA	11, 24
I <sub>PP6X</sub> : Auto self refresh current I <sub>PP</sub> current	10	10	10	10	10	mA	11, 24
I <sub>DD7</sub> : Bank interleave read current	340	350	360	370	380	mA	4
I <sub>PP7</sub> : Bank interleave read I <sub>PP</sub> current	30	30	30	30	30	mA	
I <sub>DD8</sub> : Maximum power-down current	50	50	50	50	50	mA	11

- Notes:
1. DDR4-1600 and DDR4-1866 use the same I<sub>DD</sub> limits as DDR4-2133.
  2. When additive latency is enabled for I<sub>DD0</sub>, current changes by approximately 0%.
  3. I<sub>PP0</sub> test and limit is applicable for I<sub>DD0</sub> and I<sub>DD1</sub> conditions.
  4. The I<sub>DD</sub> values must be derated (increased) when operated outside of the range 0°C ≤ T<sub>C</sub> ≤ 85°C:

When T<sub>C</sub> < 0°C: I<sub>DD2P</sub> and I<sub>DD3P</sub> must be derated by 6%; I<sub>DD4R</sub> and I<sub>DD4W</sub> must be derated by +4%; and I<sub>DD7</sub> must be derated by +11%.

When T<sub>C</sub> > 85°C: I<sub>DD0</sub>, I<sub>DD1</sub>, I<sub>DD2N</sub>, I<sub>DD2NT</sub>, I<sub>DD2Q</sub>, I<sub>DD3N</sub>, I<sub>DD3P</sub>, I<sub>DD4R</sub>, I<sub>DD4W</sub>, and I<sub>DD5R</sub> must be derated by +3%; I<sub>DD2P</sub> must be derated by +40%.

5. When additive latency is enabled for I<sub>DD1</sub>, current changes by approximately +4%.
6. When additive latency is enabled for I<sub>DD2N</sub>, current changes by approximately 0%.
7. When DLL is disabled for I<sub>DD2N</sub>, current changes by approximately –23%.
8. When CAL is enabled for I<sub>DD2N</sub>, current changes by approximately –25%.
9. When gear-down is enabled for I<sub>DD2N</sub>, current changes by approximately 0%.
10. When CA parity is enabled for I<sub>DD2N</sub>, current changes by approximately +7%.
11. I<sub>PP3N</sub> test and limit is applicable for all I<sub>DD2x</sub>, I<sub>DD3x</sub>, I<sub>DD4x</sub>, I<sub>DD6x</sub>, and I<sub>DD8</sub> conditions; that is, testing I<sub>PP3N</sub> should satisfy the I<sub>PPs</sub> for the noted I<sub>DD</sub> tests.
12. When additive latency is enabled for I<sub>DD3N</sub>, current changes by approximately +0.6%.
13. When additive latency is enabled for I<sub>DD4R</sub>, current changes by approximately +5%.



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14. When read DBI is enabled for  $I_{DD4R}$ , current changes by approximately 0%.
15. When additive latency is enabled for  $I_{DD4W}$ , current changes by approximately +4%.
16. When write DBI is enabled for  $I_{DD4W}$ , current changes by approximately 0%.
17. When write CRC is enabled for  $I_{DD4W}$ , current changes by approximately -3%.
18. When CA parity is enabled for  $I_{DD4W}$ , current changes by approximately +12%.
19. When 2X REF is enabled for  $I_{DD5R}$ , current changes by approximately -14%.
20. When 4X REF is enabled for  $I_{DD5R}$ , current changes by approximately -33%.
21. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).
22. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0–95°C).
23. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0–45°C).
24.  $I_{DD6R}$  and  $I_{DD6A}$  values are typical.

**Table 11: x16  $I_{DD}$ ,  $I_{PP}$ , and  $I_{DDQ}$  Current Limits – Rev. E**

Symbol	DDR4-2133 <sup>1</sup>	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit	Notes
$I_{DD0}$ : One bank ACTIVATE-to-PRECHARGE current	78	82	86	90	94	mA	2, 3, 4
$I_{PP0}$ : One bank ACTIVATE-to-PRECHARGE $I_{PP}$ current	6	6	6	6	6	mA	
$I_{DD1}$ : One bank ACTIVATE-to-READ-to-PRECHARGE current	110	114	118	122	126	mA	3, 4, 5
$I_{DD2N}$ : Precharge standby current	58	60	62	64	66	mA	4, 6, 7, 8, 9, 10, 11
$I_{DD2NT}$ : Precharge standby ODT current	72	76	80	84	88	mA	4, 11
$I_{DD2P}$ : Precharge power-down current	44	44	44	44	44	mA	4, 11
$I_{DD2Q}$ : Precharge quiet standby current	52	52	52	52	52	mA	4, 11
$I_{DD3N}$ : Active standby current	70	74	78	82	86	mA	4, 11
$I_{PP3N}$ : Active standby $I_{PP}$ current	6	6	6	6	6	mA	
$I_{DD3P}$ : Active power-down current	58	60	62	64	66	mA	4, 11
$I_{DD4R}$ : Burst read current	270	290	312	334	356	mA	4, 14, 13, 11
$I_{DD4W}$ : Burst write current	228	246	264	282	300	mA	4, 11, 15, 16, 17, 18
$I_{DD5R}$ : Distributed refresh current (1X REF)	92	94	96	98	100	mA	4, 19, 20
$I_{PP5R}$ : Distributed refresh $I_{PP}$ current (1X REF)	10	10	10	10	10	mA	
$I_{DD6N}$ : Self refresh current; 0–85°C	68	68	68	68	68	mA	11, 21



**Table 11: x16 I<sub>DD</sub>, I<sub>PP</sub>, and I<sub>DDQ</sub> Current Limits – Rev. E (Continued)**

Symbol	DDR4-2133 <sup>1</sup>	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit	Notes
I <sub>DD6E</sub> : Self refresh current; 0–95°C	116	116	116	116	116	mA	11, 22
I <sub>DD6R</sub> : Self refresh current; 0–45°C	42	42	42	42	42	mA	11, 23, 24
I <sub>DD6A</sub> : Auto self refresh current (25°C)	17.2	17.2	17.2	17.2	17.2	mA	11, 24
I <sub>DD6A</sub> : Auto self refresh current (45°C)	42	42	42	42	42	mA	11, 24
I <sub>DD6A</sub> : Auto self refresh current (75°C)	62	62	62	62	62	mA	11, 24
I <sub>PP6X</sub> : Auto self refresh current I <sub>PP</sub> current	10	10	10	10	10	mA	11, 24
I <sub>DD7</sub> : Bank interleave read current	340	350	360	370	380	mA	4
I <sub>PP7</sub> : Bank interleave read I <sub>PP</sub> current	26	26	26	26	26	mA	
I <sub>DD8</sub> : Maximum power-down current	36	36	36	36	36	mA	11

- Notes:
1. DDR4-1600 and DDR4-1866 use the same I<sub>DD</sub> limits as DDR4-2133.
  2. When additive latency is enabled for I<sub>DD0</sub>, current changes by approximately +1%.
  3. I<sub>PP0</sub> test and limit is applicable for I<sub>DD0</sub> and I<sub>DD1</sub> conditions.
  4. The I<sub>DD</sub> values must be derated (increased) when operated outside of the range 0°C ≤ T<sub>C</sub> ≤ 85°C:

When T<sub>C</sub> < 0°C: I<sub>DD2P</sub> and I<sub>DD3P</sub> must be derated by +6%; I<sub>DD4R</sub> and I<sub>DD4W</sub> must be derated by +4%; and I<sub>DD7</sub> must be derated by +11%.

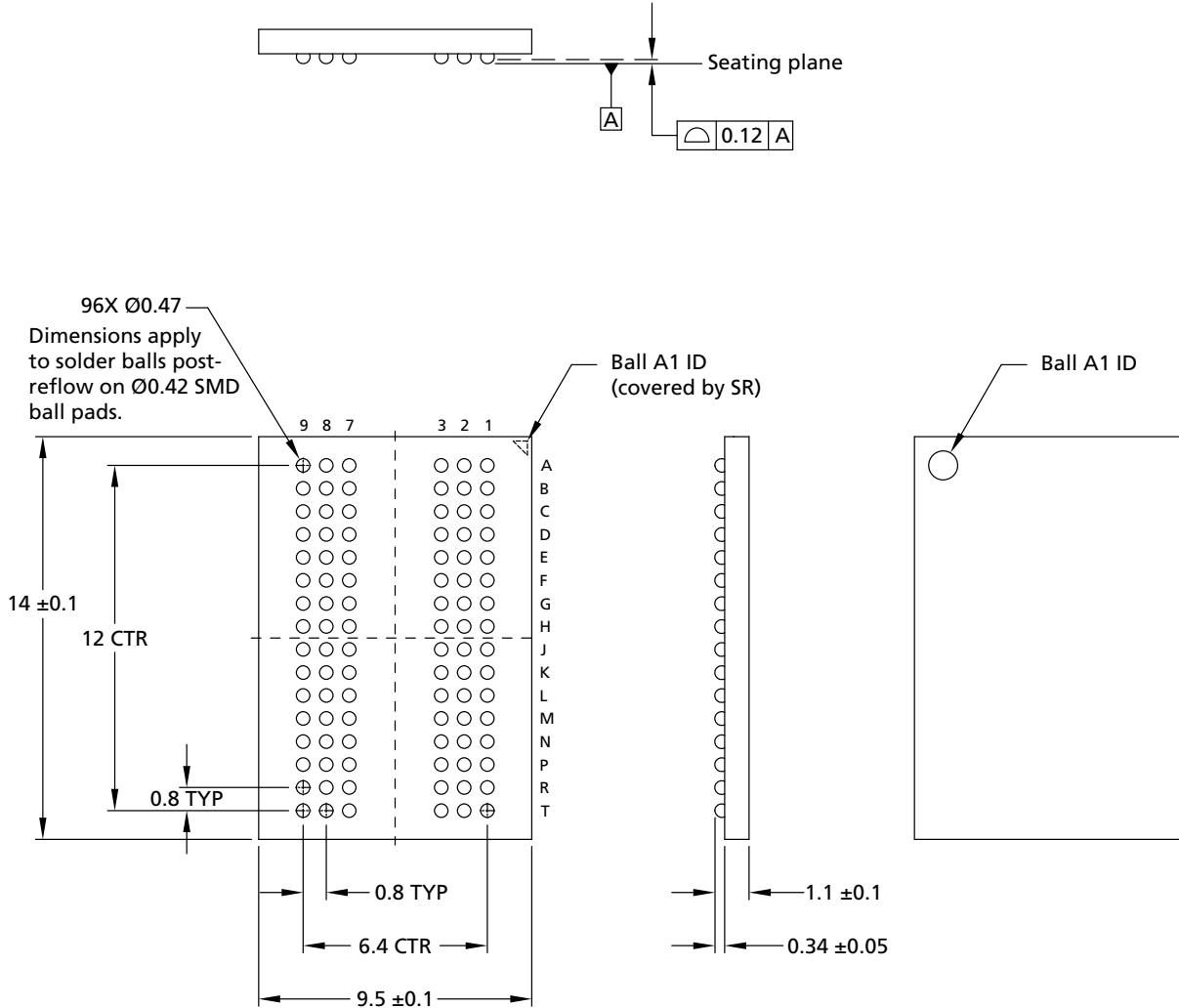
When T<sub>C</sub> > 85°C: I<sub>DD0</sub>, I<sub>DD1</sub>, I<sub>DD2N</sub>, I<sub>DD2NT</sub>, I<sub>DD2Q</sub>, I<sub>DD3N</sub>, I<sub>DD3P</sub>, I<sub>DD4R</sub>, I<sub>DD4W</sub>, and I<sub>DD5R</sub> must be derated by +3%; I<sub>DD2P</sub> must be derated by +10%.

5. When additive latency is enabled for I<sub>DD1</sub>, current changes by approximately +8%.
6. When additive latency is enabled for I<sub>DD2N</sub>, current changes by approximately +1%.
7. When DLL is disabled for I<sub>DD2N</sub>, current changes by approximately –6%.
8. When CAL is enabled for I<sub>DD2N</sub>, current changes by approximately –30%.
9. When gear-down is enabled for I<sub>DD2N</sub>, current changes by approximately 0%.
10. When CA parity is enabled for I<sub>DD2N</sub>, current changes by approximately +10%.
11. I<sub>PP3N</sub> test and limit is applicable for all I<sub>DD2X</sub>, I<sub>DD3X</sub>, I<sub>DD4X</sub>, I<sub>DD6X</sub>, and I<sub>DD8</sub> conditions; that is, testing I<sub>PP3N</sub> should satisfy the I<sub>PPS</sub> for the noted I<sub>DD</sub> tests.
12. When additive latency is enabled for I<sub>DD3N</sub>, current changes by approximately +1%.
13. When additive latency is enabled for I<sub>DD4R</sub>, current changes by approximately +4%.
14. When read DBI is enabled for I<sub>DD4R</sub>, current changes by approximately -14%.
15. When additive latency is enabled for I<sub>DD4W</sub>, current changes by approximately +3%.
16. When write DBI is enabled for I<sub>DD4W</sub>, current changes by approximately 0%.
17. When write CRC is enabled for I<sub>DD4W</sub>, current changes by approximately +5%.
18. When CA parity is enabled for I<sub>DD4W</sub>, current changes by approximately +12%.
19. When 2X REF is enabled for I<sub>DD5R</sub>, current changes by approximately –25%.

20. When 4X REF is enabled for  $I_{DD5R}$ , current changes by approximately –35%.
21. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).
22. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0–95°C).
23. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0–45°C).
24.  $I_{DD6R}$  and  $I_{DD6A}$  values are typical.

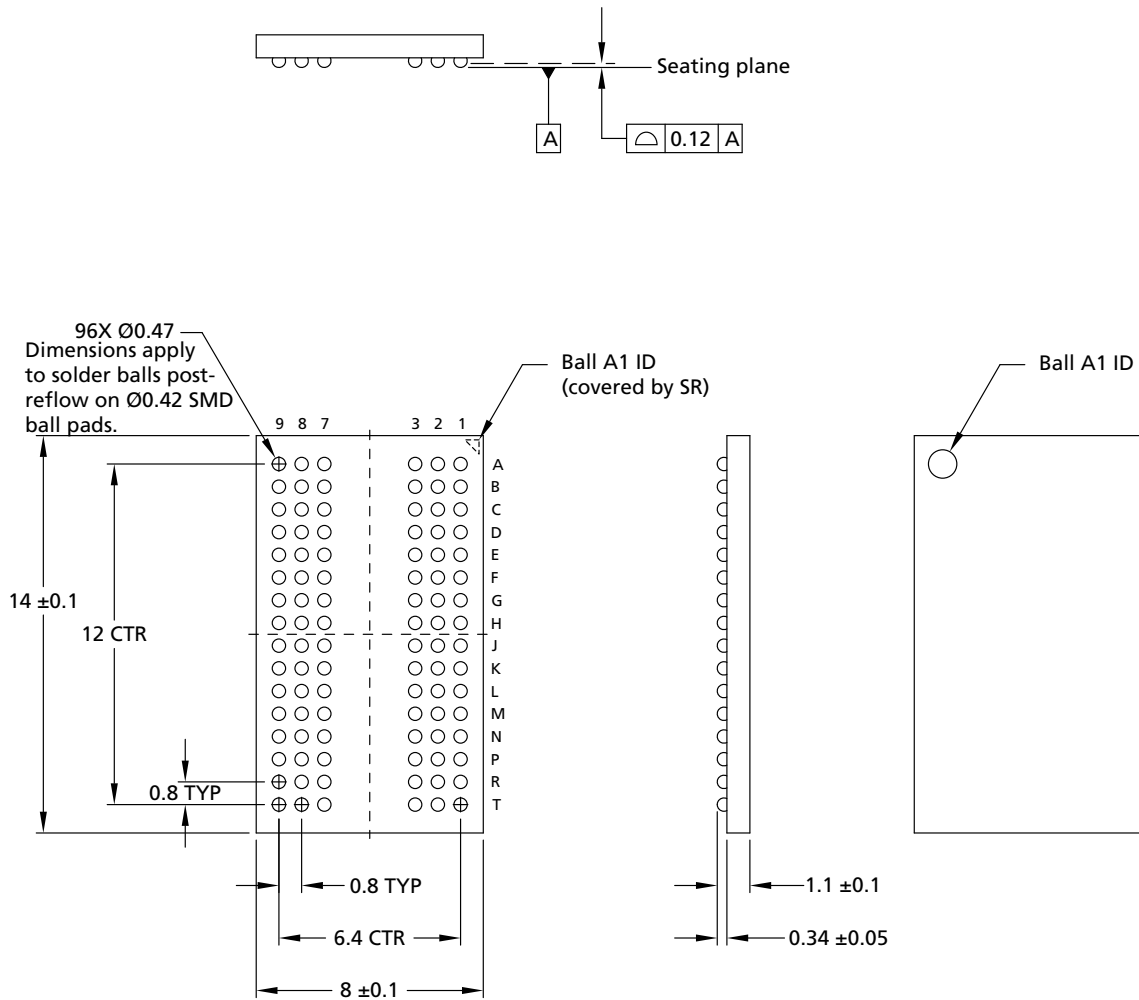
## Package Dimensions

Figure 5: 96-Ball FBGA Die Rev. A (package code HBA)



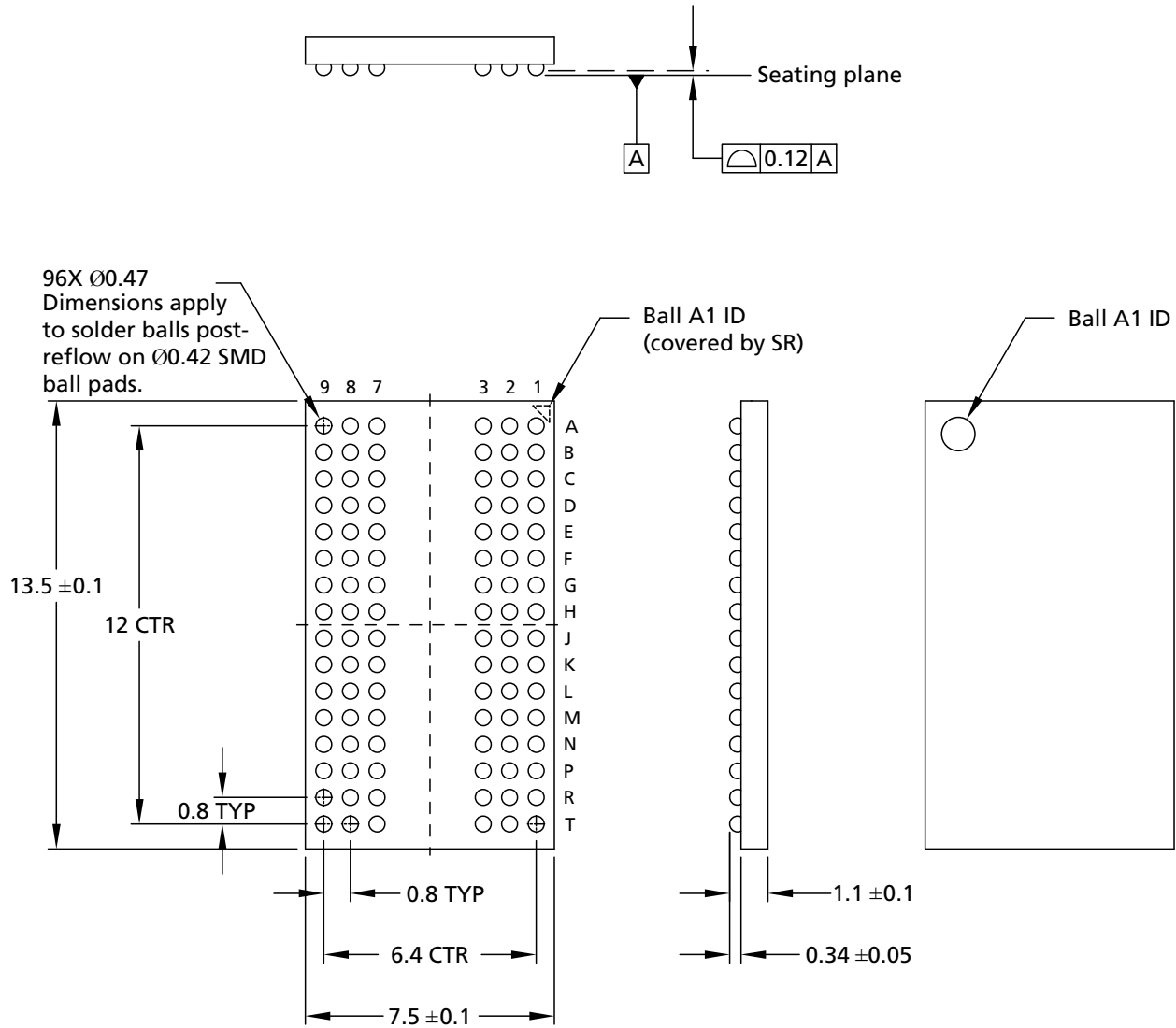
- Notes:
1. All dimensions are in millimeters.
  2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

**Figure 6: 96-Ball FBGA Die Rev. B (package code WBU)**



- Notes:
1. All dimensions are in millimeters.
  2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

**Figure 7: 96-Ball FBGA Die Rev. E (package code KNR)**



- Notes: 1. All dimensions are in millimeters.  
 2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-4000

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.



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**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331