

## 1. General description

Planar passivated sensitive gate four quadrant triac in a SOT54 (TO-92) plastic package intended for use in applications requiring direct interfacing to logic ICs and low power gate drivers.

## 2. Features and benefits

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate in four quadrants
- Triggering in all four quadrants

## 3. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

## 4. Quick reference data

Table 1. Quick reference data

| Symbol                        | Parameter                            | Conditions                                                                                                                            | Min | Typ | Max | Unit               |
|-------------------------------|--------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|--------------------|
| $V_{DRM}$                     | repetitive peak off-state voltage    |                                                                                                                                       | -   | -   | 800 | V                  |
| $I_{T(RMS)}$                  | RMS on-state current                 | full sine wave; $T_{lead} \leq 45\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a> | -   | -   | 1   | A                  |
| $I_{TSM}$                     | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>   | -   | -   | 8   | A                  |
|                               |                                      | full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 16.7\text{ ms}$                                                   | -   | -   | 8.5 | A                  |
| $T_j$                         | junction temperature                 |                                                                                                                                       | -   | -   | 125 | $^{\circ}\text{C}$ |
| <b>Static characteristics</b> |                                      |                                                                                                                                       |     |     |     |                    |
| $I_{GT}$                      | gate trigger current                 | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 7</a>                      | -   | -   | 10  | mA                 |
|                               |                                      | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 7</a>                      | -   | -   | 10  | mA                 |
|                               |                                      | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 7</a>                      | -   | -   | 10  | mA                 |

| Symbol                         | Parameter                             | Conditions                                                                                                                                                       | Min | Typ | Max | Unit             |
|--------------------------------|---------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------------------|
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                                                | -   | -   | 10  | mA               |
| $I_H$                          | holding current                       | $V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>                                                                                  | -   | -   | 10  | mA               |
| $V_T$                          | on-state voltage                      | $I_T = 1\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>                                                                                  | -   | 1.3 | 1.6 | V                |
| <b>Dynamic characteristics</b> |                                       |                                                                                                                                                                  |     |     |     |                  |
| $dV_D/dt$                      | rate of rise of off-state voltage     | $V_{DM} = 536\text{ V}$ ; $T_j = 110\text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit; <a href="#">Fig. 12</a> | 50  | -   | -   | V/ $\mu\text{s}$ |
| $dV_{com}/dt$                  | rate of change of commutating voltage | $V_D = 400\text{ V}$ ; $T_j = 110\text{ }^\circ\text{C}$ ; $dI_{com}/dt = 0.44\text{ A/ms}$ ; $I_T = 1\text{ A}$ ; gate open circuit                             | 2   | -   | -   | V/ $\mu\text{s}$ |

## 5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description     | Simplified outline                                                                                      | Graphic symbol                                                                       |
|-----|--------|-----------------|---------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| 1   | T2     | main terminal 2 |  <p>TO-92 (SOT54)</p> |  |
| 2   | G      | gate            |                                                                                                         |                                                                                      |
| 3   | T1     | main terminal 1 |                                                                                                         |                                                                                      |

## 6. Ordering information

Table 3. Ordering information

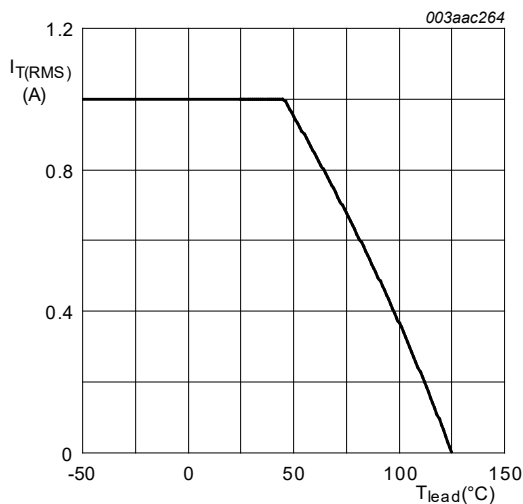
| Type number | Package |                                                             |         |
|-------------|---------|-------------------------------------------------------------|---------|
|             | Name    | Description                                                 | Version |
| Z0109NA     | TO-92   | plastic single-ended leaded (through hole) package; 3 leads | SOT54   |

## 7. Limiting values

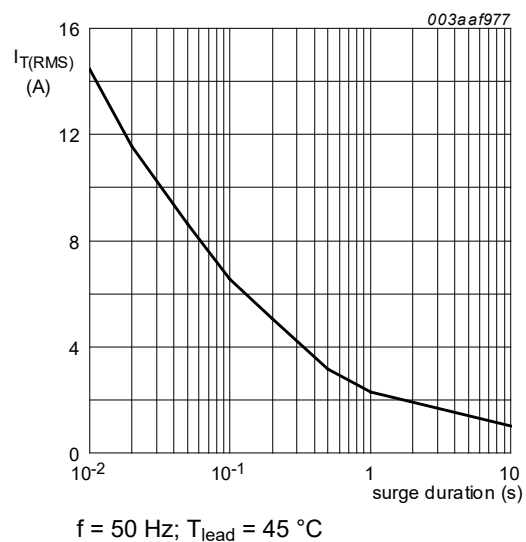
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

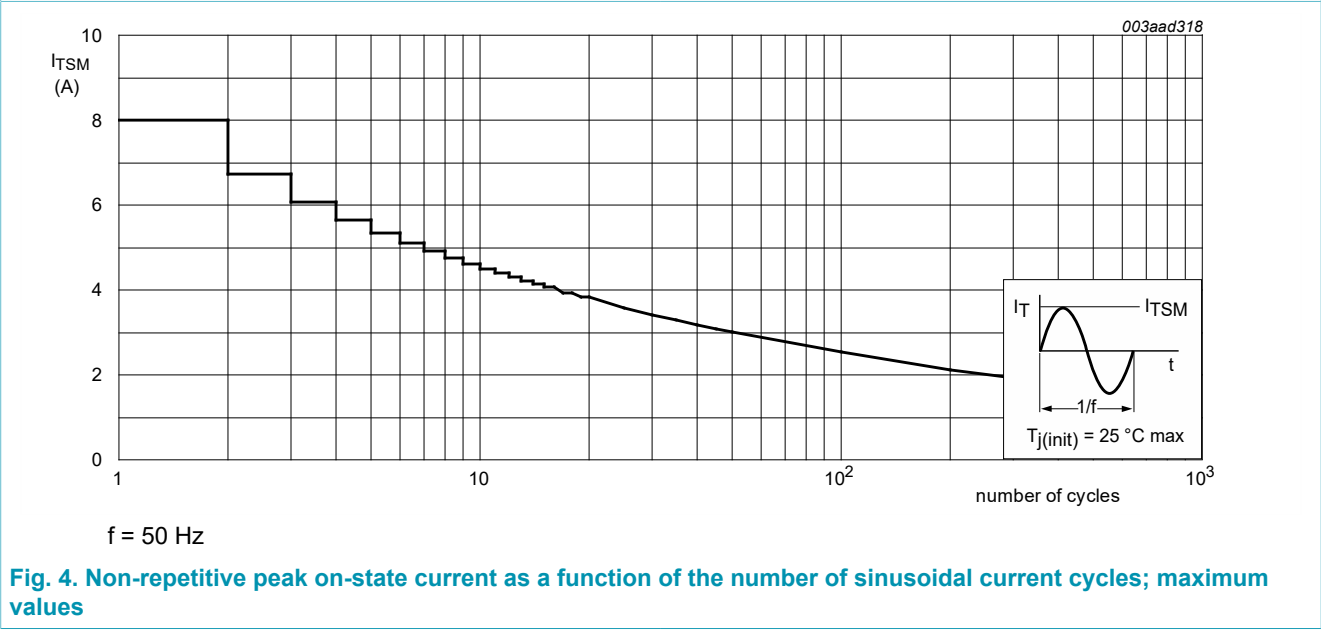
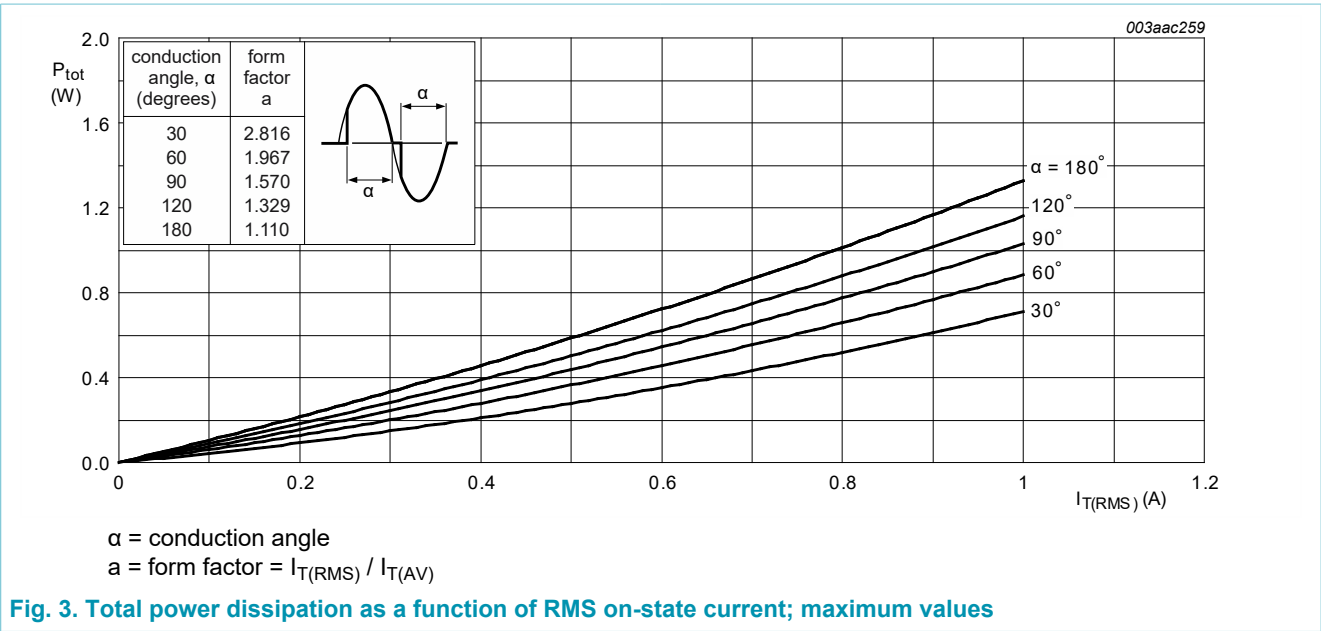
| Symbol              | Parameter                            | Conditions                                                                                                                            | Min | Max  | Unit             |
|---------------------|--------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|-----|------|------------------|
| $V_{\text{DRM}}$    | repetitive peak off-state voltage    |                                                                                                                                       | -   | 800  | V                |
| $I_{\text{T(RMS)}}$ | RMS on-state current                 | full sine wave; $T_{\text{lead}} \leq 45\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>        | -   | 1    | A                |
| $I_{\text{TSM}}$    | non-repetitive peak on-state current | full sine wave; $T_{\text{j(init)}} = 25\text{ °C}$ ; $t_{\text{p}} = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a> | -   | 8    | A                |
|                     |                                      | full sine wave; $T_{\text{j(init)}} = 25\text{ °C}$ ; $t_{\text{p}} = 16.7\text{ ms}$                                                 | -   | 8.5  | A                |
| $I^2t$              | $I^2t$ for fusing                    | $t_{\text{p}} = 10\text{ ms}$ ; SIN                                                                                                   | -   | 0.32 | A <sup>2</sup> s |
| $di_{\text{T}}/dt$  | rate of rise of on-state current     | $I_{\text{G}} = 20\text{ mA}$ ; T2+ G+                                                                                                | -   | 50   | A/ $\mu\text{s}$ |
|                     |                                      | $I_{\text{G}} = 20\text{ mA}$ ; T2+ G-                                                                                                | -   | 50   | A/ $\mu\text{s}$ |
|                     |                                      | $I_{\text{G}} = 20\text{ mA}$ ; T2- G-                                                                                                | -   | 50   | A/ $\mu\text{s}$ |
|                     |                                      | $I_{\text{G}} = 20\text{ mA}$ ; T2- G+                                                                                                | -   | 20   | A/ $\mu\text{s}$ |
| $I_{\text{GM}}$     | peak gate current                    |                                                                                                                                       | -   | 1    | A                |
| $P_{\text{GM}}$     | peak gate power                      |                                                                                                                                       | -   | 2    | W                |
| $P_{\text{G(AV)}}$  | average gate power                   | over any 20 ms period                                                                                                                 | -   | 0.1  | W                |
| $T_{\text{stg}}$    | storage temperature                  |                                                                                                                                       | -40 | 150  | °C               |
| $T_{\text{j}}$      | junction temperature                 |                                                                                                                                       | -   | 125  | °C               |

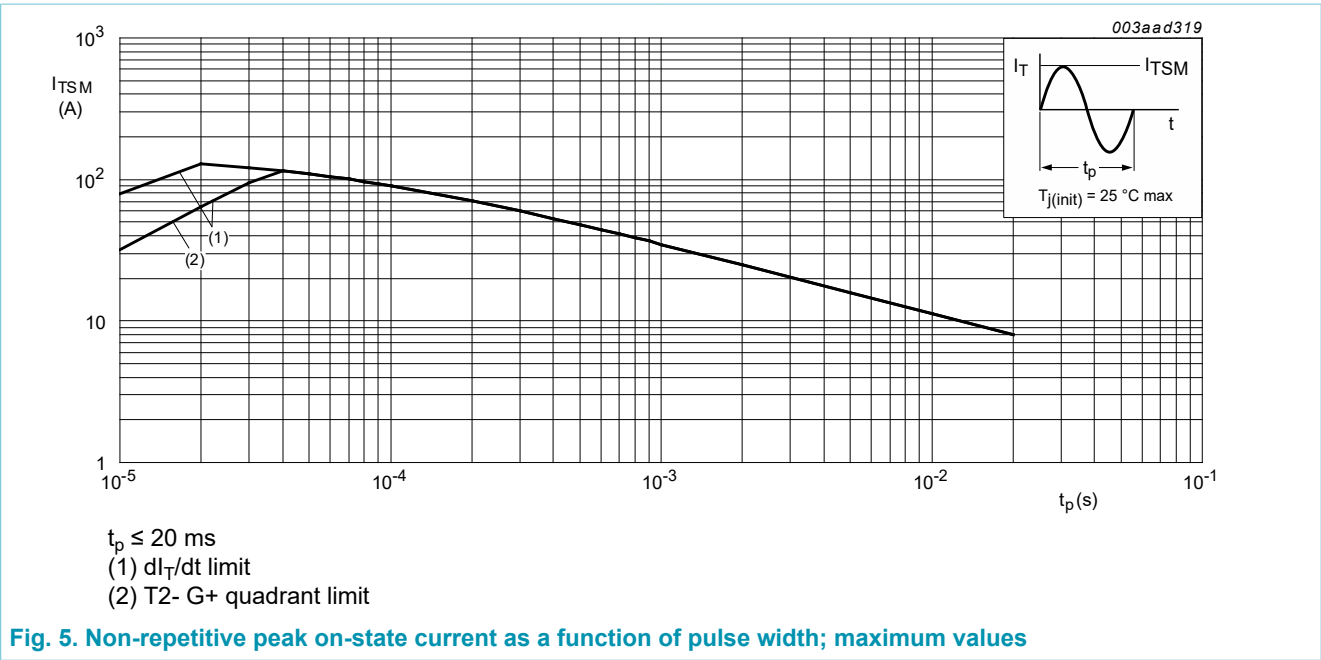


**Fig. 1. RMS on-state current as a function of lead temperature; maximum values**



**Fig. 2. RMS on-state current as a function of surge duration; maximum values**

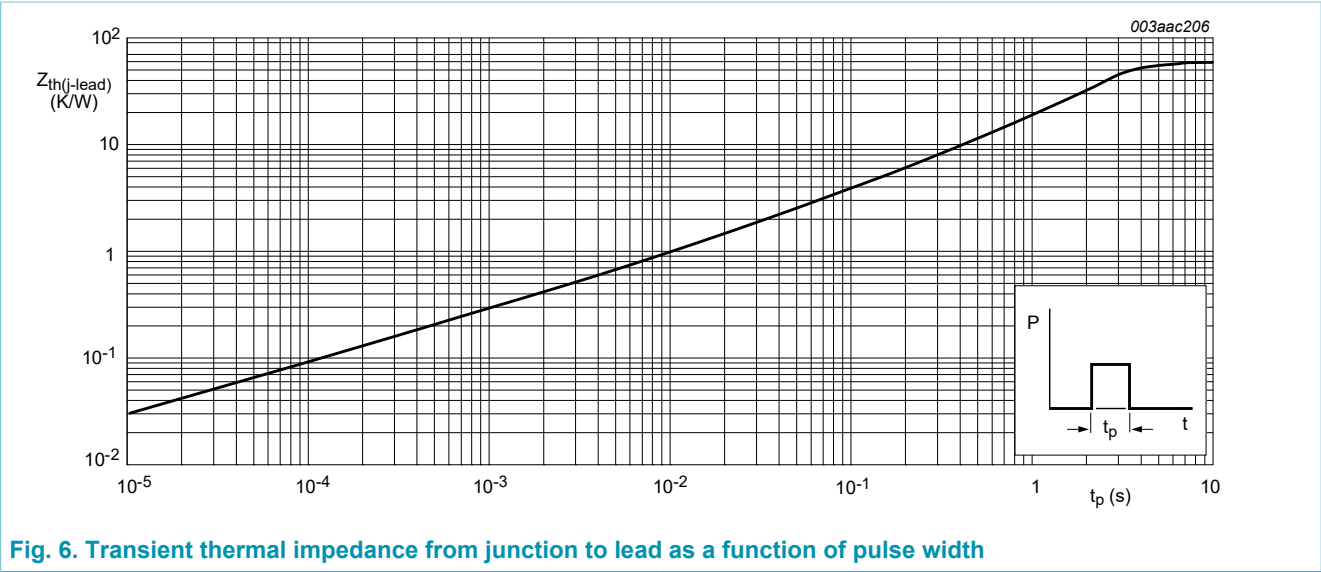




8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol           | Parameter                                            | Conditions                                                    | Min | Typ | Max | Unit |
|------------------|------------------------------------------------------|---------------------------------------------------------------|-----|-----|-----|------|
| $R_{th(j-lead)}$ | thermal resistance from junction to lead             | full cycle; Fig. 6                                            | -   | -   | 60  | K/W  |
| $R_{th(j-a)}$    | thermal resistance from junction to ambient free air | full cycle; printed circuit board mounted; lead length = 4 mm | -   | 150 | -   | K/W  |



## 9. Characteristics

Table 6. Characteristics

| Symbol                         | Parameter                             | Conditions                                                                                                                                                       |  | Min | Typ | Max | Unit             |
|--------------------------------|---------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|-----|-----|-----|------------------|
| <b>Static characteristics</b>  |                                       |                                                                                                                                                                  |  |     |     |     |                  |
| $I_{GT}$                       | gate trigger current                  | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                                                |  | -   | -   | 10  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                                                |  | -   | -   | 10  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                                                |  | -   | -   | 10  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                                                |  | -   | -   | 10  | mA               |
| $I_L$                          | latching current                      | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>                                                |  | -   | -   | 15  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>                                                |  | -   | -   | 25  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>                                                |  | -   | -   | 15  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>                                                |  | -   | -   | 15  | mA               |
| $I_H$                          | holding current                       | $V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>                                                                                  |  | -   | -   | 10  | mA               |
| $V_T$                          | on-state voltage                      | $I_T = 1\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>                                                                                  |  | -   | 1.3 | 1.6 | V                |
| $V_{GT}$                       | gate trigger voltage                  | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ;<br><a href="#">Fig. 11</a>                                                       |  | -   | -   | 1   | V                |
|                                |                                       | $V_D = 800\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 125\text{ }^\circ\text{C}$ ;<br><a href="#">Fig. 11</a>                                                     |  | 0.2 | -   | -   | V                |
| $I_D$                          | off-state current                     | $V_D = 800\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$                                                                                                         |  | -   | -   | 0.5 | mA               |
| <b>Dynamic characteristics</b> |                                       |                                                                                                                                                                  |  |     |     |     |                  |
| $dV_D/dt$                      | rate of rise of off-state voltage     | $V_{DM} = 536\text{ V}$ ; $T_j = 110\text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit; <a href="#">Fig. 12</a> |  | 50  | -   | -   | V/ $\mu\text{s}$ |
| $dV_{com}/dt$                  | rate of change of commutating voltage | $V_D = 400\text{ V}$ ; $T_j = 110\text{ }^\circ\text{C}$ ; $dI_{com}/dt = 0.44\text{ A/ms}$ ; $I_T = 1\text{ A}$ ; gate open circuit                             |  | 2   | -   | -   | V/ $\mu\text{s}$ |

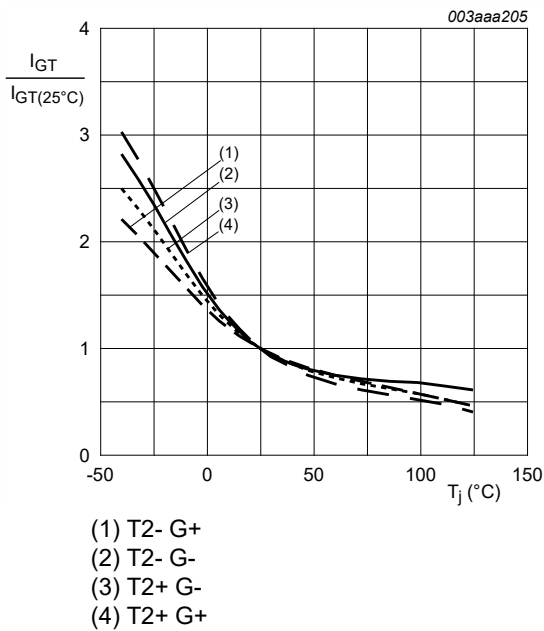


Fig. 7. Normalized gate trigger current as a function of junction temperature

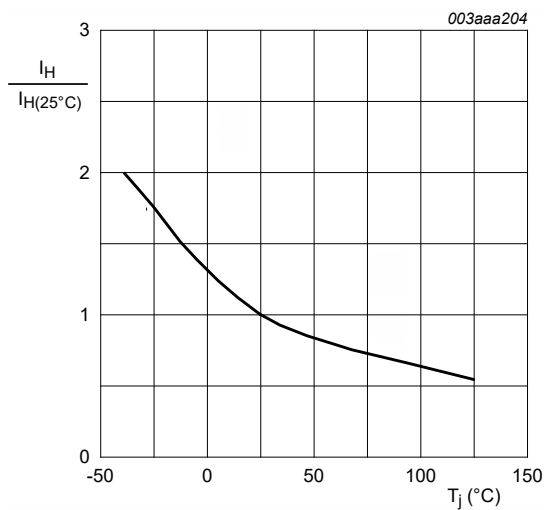


Fig. 9. Normalized holding current as a function of junction temperature

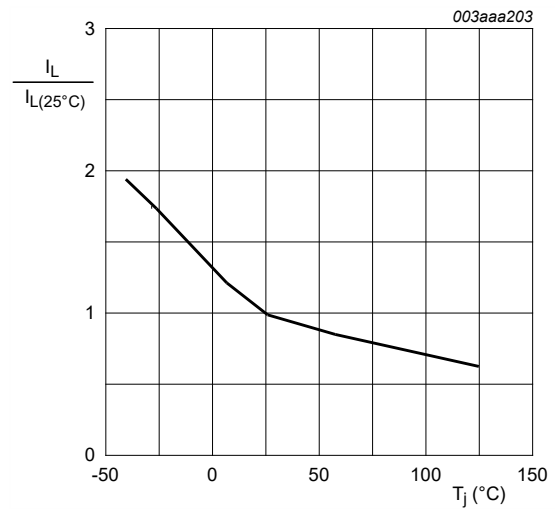
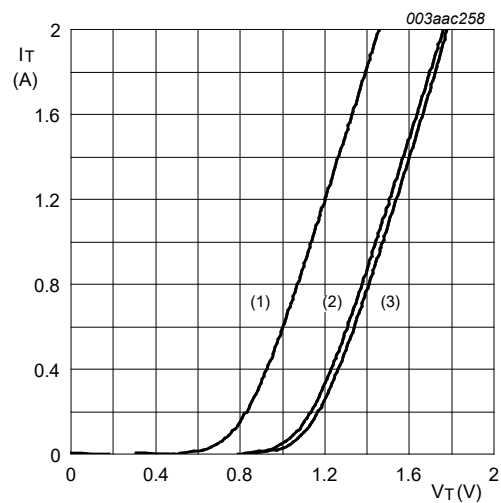


Fig. 8. Normalized latching current as a function of junction temperature



$V_o = 1.13 \text{ V}$

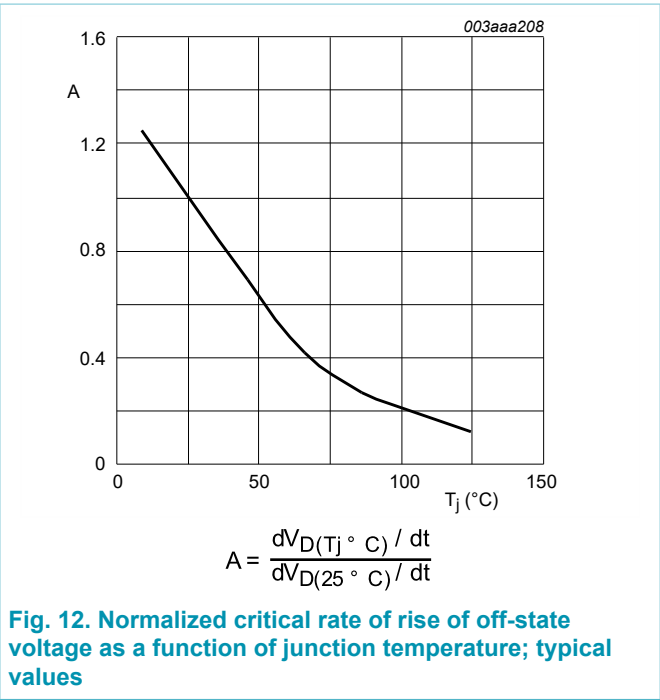
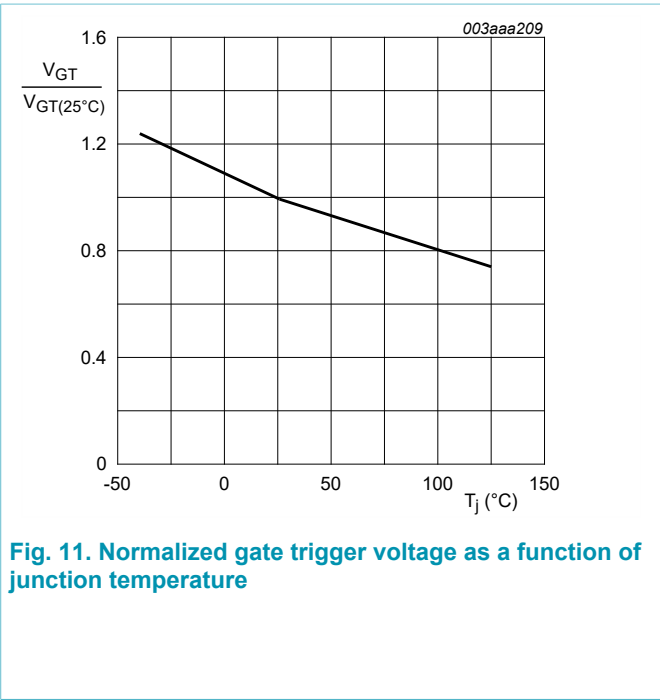
$R_s = 0.31 \Omega$

(1)  $T_J = 125^{\circ}\text{C}$ ; typical values

(2)  $T_J = 125^{\circ}\text{C}$ ; maximum values

(3)  $T_J = 25^{\circ}\text{C}$ ; maximum values

Fig. 10. On-state current as a function of on-state voltage



10. Package outline

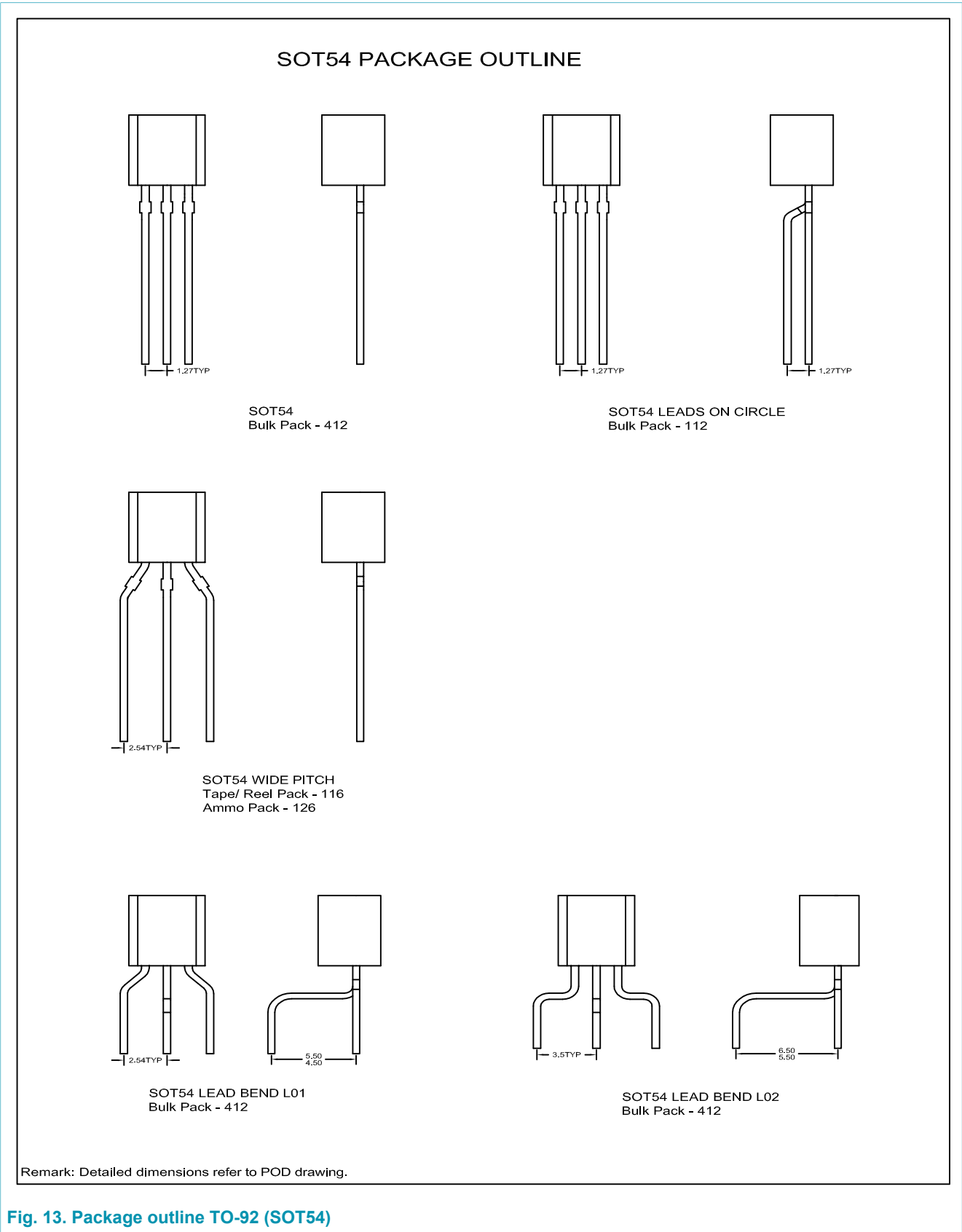


Fig. 13. Package outline TO-92 (SOT54)

## 11. Legal information

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| Document status [1][2]         | Product status [3] | Definition                                                                            |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
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- [1] Please consult the most recently issued document before initiating or completing a design.
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Date of release: 17 September 2018

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