

## Features

- **PEX 8604 General Features**
  - 4-lane PCI Express switch
    - Integrated 5.0 GT/s SerDes
  - Up to 4 configurable ports
  - 15 x 15mm<sup>2</sup>, 196-ball PBGA
  - Typical Power: 1.29 Watts
- **PEX 8604 Key Features**
  - **Standards Compliant**
    - PCI Express Base Specification r2.0 (Backwards compatible with PCIe r1.0a/1.1)
    - PCI Power Management Spec r1.2
    - Microsoft Vista Compliant
    - Supports Access Control Services
    - Dynamic link-width control
  - **High Performance**
    - Non-blocking internal architecture
    - Full line rate on all ports
    - Cut-Thru latency: 190ns
    - 2KB max payload size
    - Read Pacing (intelligent bandwidth allocation)
    - Dual Cast
  - **Dual-Host & Fail-Over Support**
    - Configurable Non-Transparent port (NTB)
    - Moveable upstream port
    - Crosslink port capability on all ports
  - **Flexible Configuration**
    - 4 flexible & configurable ports (x1 or x2)
    - Configurable with strapping pins, EEPROM, I<sup>2</sup>C, or Host software
    - Lane and polarity reversal
  - **PCI Express Power Management**
    - Link power management states: L0, L0s, L1, L2/L3 Ready, and L3
    - Device states: D0 and D3<sub>hot</sub>
  - **Spread Spectrum Clock Isolation**
    - Dual clock domain
  - **Quality of Service (QoS)**
    - Two Virtual Channels (VC) per port
    - Eight Traffic Classes per port
    - Weighted Round-Robin Port & VC Arbitration
  - **Reliability, Availability, Serviceability**
    - All ports Hot-Plug capable thru I<sup>2</sup>C (Hot-Plug Controller on every port)
    - ECRC & Poison bit support
    - Data path protection
    - Memory (RAM) error correction
    - Advanced Error Reporting support
    - Port Status bits and GPIO available
    - Per port error diagnostics
    - Performance monitoring (per port payload & header counters)
    - JTAG AC/DC boundary scan
    - Fatal Error (FATAL\_ERR#) output signal
    - INTA# output signal

# PEX 8604

## *Flexible & Versatile 4-lane 4-port PCI Express® Switch*

The *ExpressLane*™ PEX 8604 device offers PCI Express switching capability enabling users to add scalable high bandwidth non-blocking interconnection to a wide variety of applications including **control plane applications, consumer applications and embedded systems**. The PEX 8604 is well suited for **fan-out, peer-to-peer**, and **intelligent I/O module** applications.

### Low Packet Latency & High Performance

The PEX 8604 architecture supports packet **cut-thru with a maximum latency of 190ns in x1 to x1 configuration**. This, combined with low power consumption and non-blocking internal switch architecture, provides full line rate on all ports for low-power applications such as **consumer and embedded**. The low latency enables applications to achieve high throughput and performance. In addition to low latency, the device supports a **max payload size of 2048 bytes**, enabling the user to achieve even higher throughput.

### Data Integrity

The PEX 8604 provides **end-to-end CRC** protection (ECRC) and **Poison** bit support to enable designs that require **guaranteed error-free packets**. PLX also supports data path parity and memory (RAM) error correction as packets pass through the switch.

### Dual-Host and Fail-Over Support

The PEX 8604 supports full non-transparent bridging (NTB) functionality to allow implementation of **multi-host systems** and **intelligent I/O modules** in applications which require redundancy support such as select **embedded** applications.

Non-transparent bridges allow systems to isolate host memory domains by presenting the processor subsystem as an endpoint rather than another memory system. Base address registers are used to translate addresses, doorbell registers are used to send interrupts between the address domains, and scratchpad registers are accessible from both address domains to allow inter-processor communication.

### Interoperability

The PEX 8604 is designed to be fully compliant with the PCI Express Base Specification r2.0 and is backwards compatible to PCI Express Base Specification r1.1 and r1.0a. Additionally each port supports **auto-negotiation** and **polarity reversal**. Furthermore, the PEX 8604 is designed for Microsoft Vista compliance. All PLX switches undergo thorough interoperability testing in PLX's **Interoperability Lab** and **compliance testing at the PCI-SIG plug-fest** to ensure compatibility with PCI Express devices in the market.

### Device Operation Configuration Flexibility

The PEX 8604 provides several ways to configure its operations. The device can be configured through strapping pins, I<sup>2</sup>C interface, CPU configuration cycles and/or an optional serial EEPROM. This allows for easy debug during the development phase and functional monitoring during the operation phase.



## Flexible Port Configurations

The PEX 8604 flexible architecture supports a number of port configurations as required by the target applications as shown in figure 1 below.

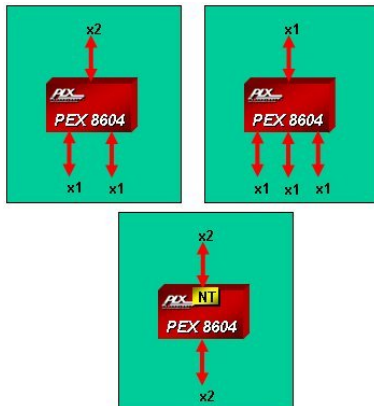


Figure 1. Port Configurations

## Hot-Plug for High Availability

Hot-Plug capability allows users to replace hardware modules and perform maintenance without powering down the system. The PEX 8604 Hot-Plug capability feature makes it suitable for **High Availability (HA) applications**. If the PEX 8604 is used in an application where one or more of its downstream ports connect to PCI Express slots, each port's Hot-Plug Controller can be used to manage the Hot-Plug event of its associated slot. Every port on the PEX 8604 is equipped with a Hot-Plug control/status register to support Hot-Plug capability through external logic via the I<sup>2</sup>C interface.

## Dual Cast

The PEX 8604 supports Dual Cast, a feature which allows for the copying of data (e.g. packets) from one ingress port to two egress ports allowing for higher performance in storage, security, and mirroring applications.

## Read Pacing

The Read Pacing feature allows users to throttle the amount of read requests being made by downstream devices. In the case where a downstream device requests several long reads back-to-back, the Root Complex gets tied up in serving this downstream port. If this port has a narrow link and is therefore slow in receiving these read packets from the Root Complex, then other downstream ports may become starved – thus, impacting performance. The Read Pacing feature enhances performances by allowing for the adequate servicing of all downstream devices by intelligent handling of read requests.

## SerDes Power and Signal Management

The PEX 8604 provides low power capability that is fully compliant with the PCI Express power management specification. In addition, the SerDes physical links can be turned off when unused for even lower power. The PEX 8604 supports **software control** of the **SerDes outputs** to allow optimization of power and signal strength in a system. The PLX SerDes implementation supports four levels of power –

off, low, typical, and high. The SerDes block also supports **loop-back modes** and **advanced reporting of error conditions**, which enables efficient debug and management of the entire system.

## Port and Virtual Channel (VC) Arbitration

The PEX 8604 switch supports hardware fixed and Weighted Round-Robin Ingress Port Arbitration. This allows fine tuning of Quality of Service and efficient use of packet buffers for better system performance. The PEX 8604 also supports WRR VC arbitration scheme between the two virtual channels.

## Applications

Suitable for **fan-out, control plane applications, embedded systems** as well as **intelligent I/O applications**, PEX 8604 can be configured for a wide variety of form factors and applications.

## Fan-Out

The PEX 8604 switch, with its flexible configurations, allows user specific tuning to a variety of **host-centric as well as peer-to-peer applications**.

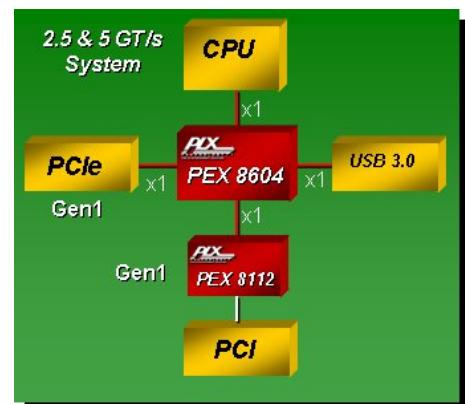


Figure 2. Fan-in/out Usage

Figure 2 shows a typical **fan-out** design, where the processor provides a PCI Express link that needs to be fanned into a larger number of smaller ports for a variety of I/O functions, each with different bandwidth requirements.

In this example, the PEX 8604 would typically have a 1-lane upstream port, and three downstream ports. The downstream ports provide x1 PCI Express connectivity to the endpoints. With its four ports, the PEX 8604 can provide fan-out connectivity to up to three PCI Express devices. The figure also shows how some of the ports can be bridged to provide **PCI slots** through the use of the **PEX 8112 PCIe bridging** devices.

## Consumer Applications

With its small footprint, the PEX 8604 is ideal for consumer applications. Figure 3 shows an example for a set top box. The PEX8604 connects to legacy devices using a PEX85112

The diagram illustrates a PC system architecture with the following components and connections:

- CODEC** and **CPU** are connected by a bidirectional bus.
- CPU** is connected to **LCD** and **RS232** by bidirectional buses.
- USB 3.0** is connected to the **PEX 8604** controller.
- LAN** is connected to the **PEX 8604** controller via a **PCI Bus**.
- The **PEX 8604** controller is connected to the **PEX 8112** controller via a **PCI Bus**.
- TV Tuner** is connected to the **PEX 8112** controller via a **PCI Bus**.
- The **Philips Hybrid Tuner** is connected to the **CVBS** input and the **TS** output.
- The **CVBS** input is connected to the **Conexant CX2382** chip.
- The **Conexant CX2382** chip is connected to the **Conexant Demod CX22702** chip via a **2IF** bus.
- The **Conexant Demod CX22702** chip is connected to the **TS** output.
- The **Conexant CX2382** chip is also connected to the **PEX 8112** controller via a **PCI Bus**.

## Mobile Wireless Adaptor

Diagram illustrating the PEX 8604 switch configuration. The switch is shown as a red box labeled **PEX 8604**. It has a single input on the left (labeled **X1**) and three outputs on the right (labeled **x1**, **x1**, and **x1**). The outputs are connected to **USB 3.0**, **Wireless**, and **Wireless** ports respectively.

## Embedded Mezzanine Module

The diagram illustrates the connection of the PEX 8604 PCI Express to Baseboard Controller to a Baseboard. It is divided into two main sections: Mezzanine and Baseboard.

**Mezzanine:** This section contains the PEX 8604 controller. It is connected to three I/O blocks (labeled I/O, I/O, and CPU) via x1 links. The controller is also connected to the Baseboard via an x1 link.

**Baseboard:** This section contains the PEX 8608 Root Complex. It is connected to an arbitrary mix of I/O Mezzanines (labeled I/O Mezz., I/O Mezz., and I/O Mezz.). The Root Complex is also connected to the Mezzanine via an x1 link.

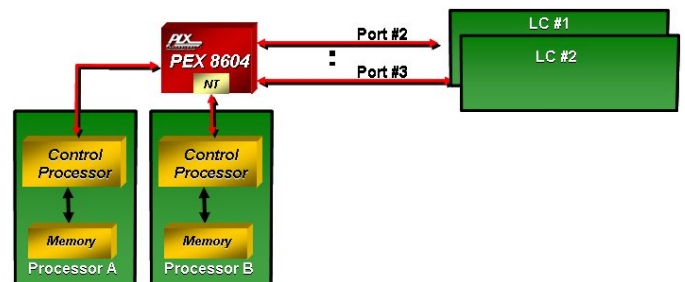
## Intelligent Adapter Card

The diagram illustrates the architecture of the PEX 8604 and PEX 8608 PCI Express switches. The PEX 8604 switch is shown as a red component with a 'Non-Transparent Port' (NT) and a 'Primary Host CPU Blade' connected to it. It is connected to an 'Intelligent I/O Adaptor' (green) which contains a 'CPU' and 'I/O' blocks. The PEX 8608 switch is shown as a red component with four 'I/O' blocks connected to it. The PEX 8604 switch is connected to the PEX 8608 switch via a red line. The PEX 8604 switch is also connected to the 'Primary Host CPU Blade' via a red line. The PEX 8608 switch is connected to the 'Primary Host CPU Blade' via a red line. The PEX 8604 switch is connected to the 'Intelligent I/O Adaptor' via a red line. The PEX 8604 switch is connected to the 'Non-Transparent Port' via a red line. The PEX 8604 switch is connected to the 'Primary Host CPU Blade' via a red line. The PEX 8608 switch is connected to the 'Primary Host CPU Blade' via a red line. The PEX 8604 switch is connected to the 'Intelligent I/O Adaptor' via a red line. The PEX 8604 switch is connected to the 'Non-Transparent Port' via a red line. The PEX 8604 switch is connected to the 'Primary Host CPU Blade' via a red line. The PEX 8608 switch is connected to the 'Primary Host CPU Blade' via a red line.

In this figure, the CPU on the adapter card is isolated from the host CPU. The PEX 8604 non-transparent port allows the two CPUs to be isolated but communicate with each other through various registers that are designed in the PEX 8604 for that purpose. The host CPU **can dynamically re-assign both the upstream port and the non-transparent port** of PEX 8604 allowing the system to be reconfigured.

## Active-Standby Failover Model

The redundancy of the host and the fabric can be achieved through many possible configurations using NTB function of PEX 8604. In the configuration shown below Processor A is the primary active host of the PCI Express system. Processor B acts as the backup Host. In the case of a failure on Processor A, application software is instructed to migrate the PCI Express system to Processor B. Consequently, Processor B becomes the active host and Processor A can be replaced as the backup Host.



### Figure 7. Active-Standby Control Plane

## Software Usage Model

From a system model viewpoint, each PCI Express port is a virtual PCI to PCI bridge device and has its own set of PCI Express configuration registers. It is through the upstream port that the BIOS or host can configure the other ports using standard PCI enumeration. The virtual PCI-to-PCI bridges within the PEX 8604 are compliant to the PCI and PCI Express system models. The Configuration Space Registers (CSRs) in a virtual primary/secondary PCI-to-PCI bridge are accessible by type 0 configuration cycles through the virtual primary bus interface (matching bus number, device number, and function number).

## Interrupt Sources/Events

The PEX 8604 supports the INTx interrupt message type (compatible with PCI 2.3 Interrupt signals) or Message Signaled Interrupts (MSI) when enabled. Interrupts/messages are generated by PEX 8604 for Hot-Plug events, doorbell interrupts, baseline error reporting, and advanced error reporting.

## Development Tools

PLX offers hardware and software tools to enable rapid customer design activity. These tools consist of a PEX 8604 Rapid Development Kit (RDK), hardware documentation, and a Software Development Kit (also available at [www.plxtech.com/sdk](http://www.plxtech.com/sdk)).

## RDK

The PEX 8604RDK is a hardware module containing the PEX 8604 which plugs right into your system (Figure 8). The PEX 8604RDK hardware module can be installed in a motherboard, used as a riser card, or configured as a bench-top board. The PEX 8604RDK can be used to test and validate customer software. Additionally, it can be used as an evaluation vehicle for PEX 8604 features and benefits.

## SDK

The SDK tool set includes:

- Linux & Windows drivers
- C/C++ Source code, Objects, libraries
- User's Guides & Application examples

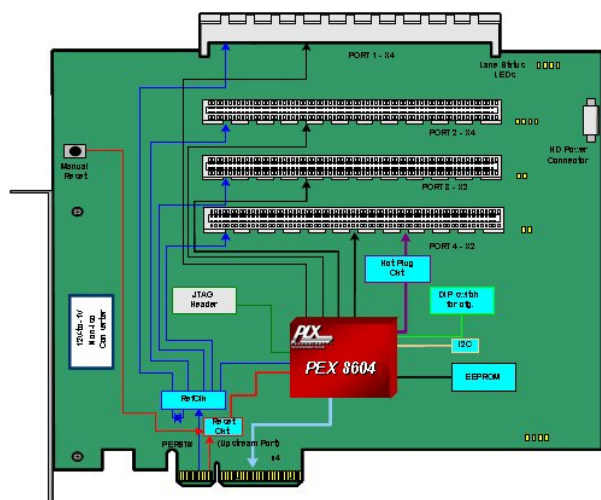
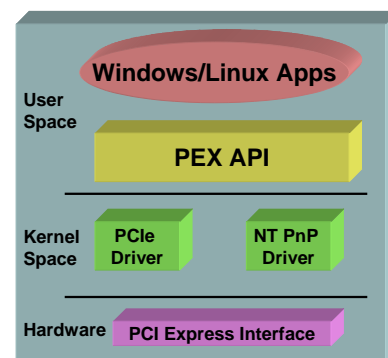


Figure 8. PEX 8604RDK



PLX Technology, Inc.  
870 W. Maude Ave.  
Sunnyvale, CA 94085 USA  
[www.plxtech.com](http://www.plxtech.com)

## Product Ordering Information

Part Number	Description
PEX8604-BA50BC	4 Lane, 4 Port PCIe Switch, 196-ball PBGA 15x15mm <sup>2</sup> pkg
PEX8604-BA50BC G	4 Lane, 4 Port PCIe Switch, 196-ball PBGA 15x15mm <sup>2</sup> pkg, Pb-free
PEX 8604BA-AIC1U1D RDK	PEX 8604 Rapid Development Kit with 4-ports

Please visit the PLX Web site at <http://www.plxtech.com> for sampling.

© 2009 by PLX Technology, Inc. All rights reserved. PLX and the PLX logo are registered trademarks of PLX Technology, Inc. ExpressLane is a trademark of PLX Technology, Inc., which may be registered in some jurisdiction. All other product names that appear in this material are for identification purposes only and are acknowledged to be trademarks or registered trademarks of their respective companies. Information supplied by PLX is believed to be accurate and reliable, but PLX Technology, Inc. assumes no responsibility for any errors that may appear in this material. PLX Technology, Inc. reserves the right, without notice, to make changes in product design or specification.





**Стандарт  
Электрон  
Связь**

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

**Наши контакты:**

**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331