

# 74HC240; 74HCT240

Octal buffer/line driver; 3-state; inverting

Rev. 5 — 15 July 2020

Product data sheet

## 1. General description

The 74HC240; 74HCT240 is an 8-bit inverting buffer/line driver with 3-state outputs. The device can be used as two 4-bit buffers or one 8-bit buffer. The device features two output enables ( $1\overline{OE}$  and  $2\overline{OE}$ ), each controlling four of the 3-state outputs. A HIGH on  $n\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Input levels:
  - For 74HC240: CMOS level
  - For 74HCT240: TTL level
- Inverting 3-state outputs
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC240D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HCT240D				
74HC240DB	-40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HCT240DB				
74HC240PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HCT240PW				
74HC240BQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
74HCT240BQ				

4. Functional diagram

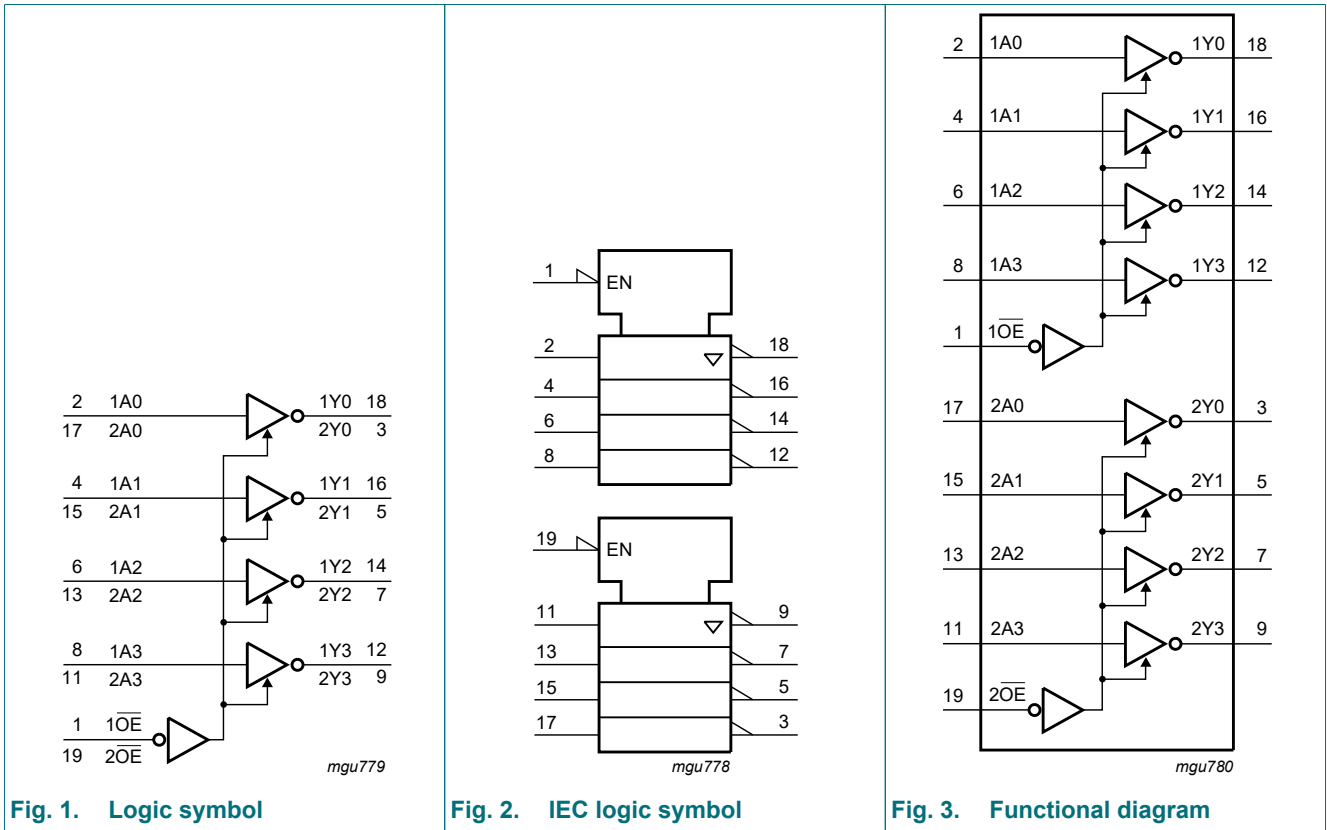


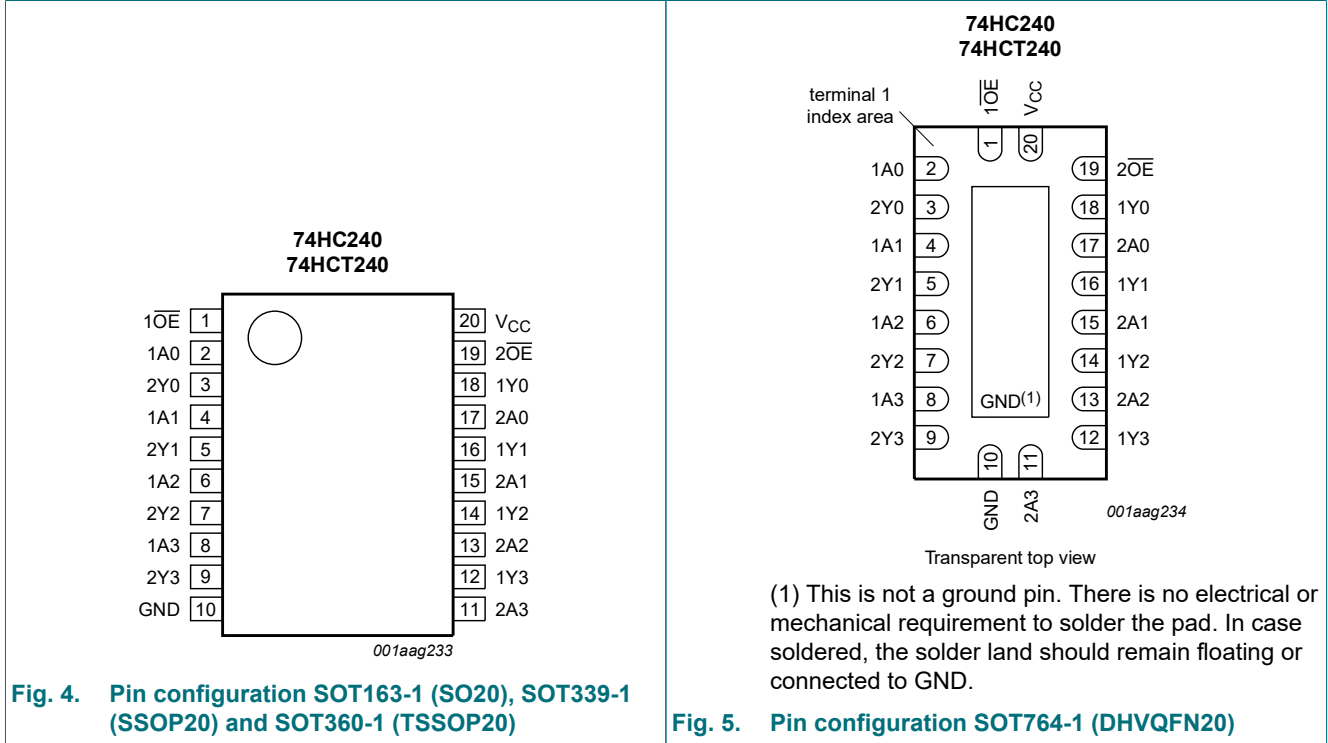
Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

Fig. 3. Functional diagram

## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 19	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	3, 5, 7, 9	bus output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	17, 15, 13, 11	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	bus output
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output
nOE	nAn	nYn
L	L	H
L	H	L
H	X	Z

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_O$	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	$\pm 35$	mA
$I_{CC}$	supply current		-	70	mA
$I_{GND}$	ground current		-70	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	[1]	-	500	mW

- [1] For SOT163-1 (SO20) package:  $P_{tot}$  derates linearly with 12.3 mW/K above 109 °C.  
 For SOT339-1 (SSOP20) package:  $P_{tot}$  derates linearly with 10.0 mW/K above 100 °C.  
 For SOT360-1 (TSSOP20) package:  $P_{tot}$  derates linearly with 10.0 mW/K above 100 °C.  
 For SOT764-1 (DHVQFN20) package:  $P_{tot}$  derates linearly with 12.9 mW/K above 111 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	74HC240			74HCT240			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC240</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -6.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I <sub>O</sub> = -7.8 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 6.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 7.8 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 6.0 V; V <sub>O</sub> = V <sub>CC</sub> or GND	-	-	±0.5	-	±5.0	-	±10	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-	160	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF
<b>74HCT240</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -6 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 6.0 mA	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = V <sub>CC</sub> or GND	-	-	±0.5	-	±5.0	-	±10	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 0 A	-	-	8.0	-	80	-	160	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V; I <sub>O</sub> = 0 A								
		nAn or inputs	-	150	540	-	675	-	735	µA
		nOE input	-	70	252	-	315	-	343	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

$GND = 0\text{ V}$ ; for test circuit see Fig. 8.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC240</b>										
$t_{pd}$	propagation delay	nAn to nYn; see Fig. 6 [1]								
		$V_{CC} = 2.0\text{ V}$	-	30	100	-	125	-	150	ns
		$V_{CC} = 4.5\text{ V}$	-	11	20	-	25	-	30	ns
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	9	-	-	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$	-	9	17	-	21	-	26	ns
$t_{en}$	enable time	n $\overline{OE}$ to nYn; see Fig. 7 [2]								
		$V_{CC} = 2.0\text{ V}$	-	39	150	-	190	-	225	ns
		$V_{CC} = 4.5\text{ V}$	-	14	30	-	38	-	45	ns
		$V_{CC} = 6.0\text{ V}$	-	11	26	-	33	-	38	ns
$t_{dis}$	disable time	n $\overline{OE}$ to nYn or see Fig. 7 [3]								
		$V_{CC} = 2.0\text{ V}$	-	41	150	-	190	-	225	ns
		$V_{CC} = 4.5\text{ V}$	-	15	30	-	38	-	45	ns
		$V_{CC} = 6.0\text{ V}$	-	12	26	-	33	-	38	ns
$t_t$	transition time	see Fig. 6 [4]								
		$V_{CC} = 2.0\text{ V}$	-	14	60	-	75	-	90	ns
		$V_{CC} = 4.5\text{ V}$	-	5	12	-	15	-	18	ns
		$V_{CC} = 6.0\text{ V}$	-	4	10	-	13	-	15	ns
$C_{PD}$	power dissipation capacitance	per buffer; $V_I = GND$ to $V_{CC}$ [5]	-	30	-	-	-	-	-	pF
<b>74HCT240</b>										
$t_{pd}$	propagation delay	nAn to nYn; see Fig. 6 [1]								
		$V_{CC} = 4.5\text{ V}$	-	11	20	-	25	-	30	ns
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	9	-	-	-	-	-	ns
$t_{en}$	enable time	n $\overline{OE}$ to nYn; $V_{CC} = 4.5\text{ V}$ ; see Fig. 7 [2]	-	13	30	-	38	-	45	ns
$t_{dis}$	disable time	n $\overline{OE}$ to nYn; $V_{CC} = 4.5\text{ V}$ ; see Fig. 7 [3]	-	13	25	-	31	-	38	ns
$t_t$	transition time	$V_{CC} = 4.5\text{ V}$ ; see Fig. 6 [4]	-	5	12	-	15	-	18	ns
$C_{PD}$	power dissipation capacitance	per buffer; $V_I = GND$ to $V_{CC} - 1.5\text{ V}$ [5]	-	30	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .

[2]  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .

[3]  $t_{dis}$  is the same as  $t_{PHZ}$  and  $t_{PLZ}$ .

[4]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

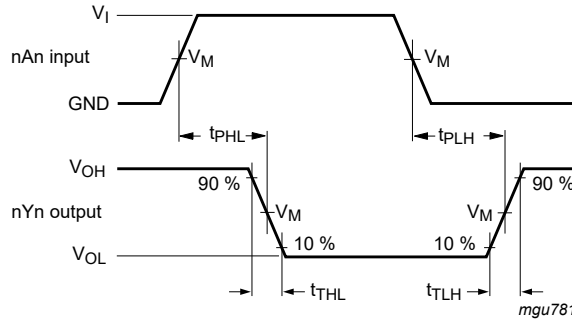
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

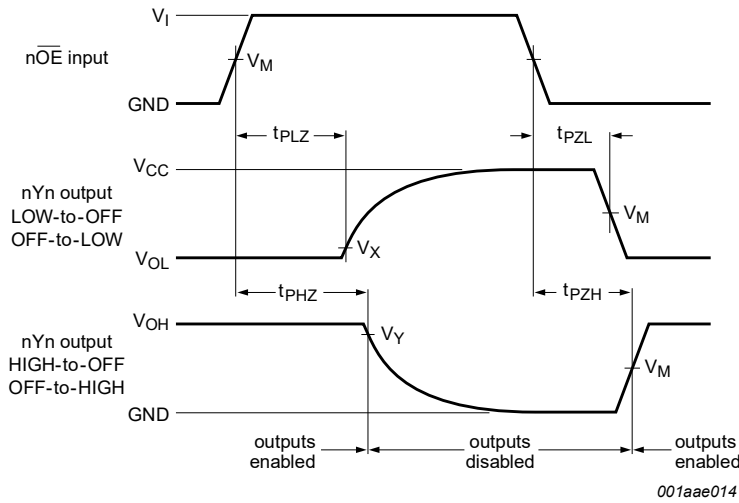
10.1. Waveforms



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 6. Input (nAn) to output (nYn) propagation delays and output transition times**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 7. 3-state enable and disable times**

**Table 8. Measurement points**

Type	Input	Output		
	$V_M$	$V_M$	$V_X$	$V_Y$
74HC240	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$
74HCT240	1.3 V	1.3 V	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$

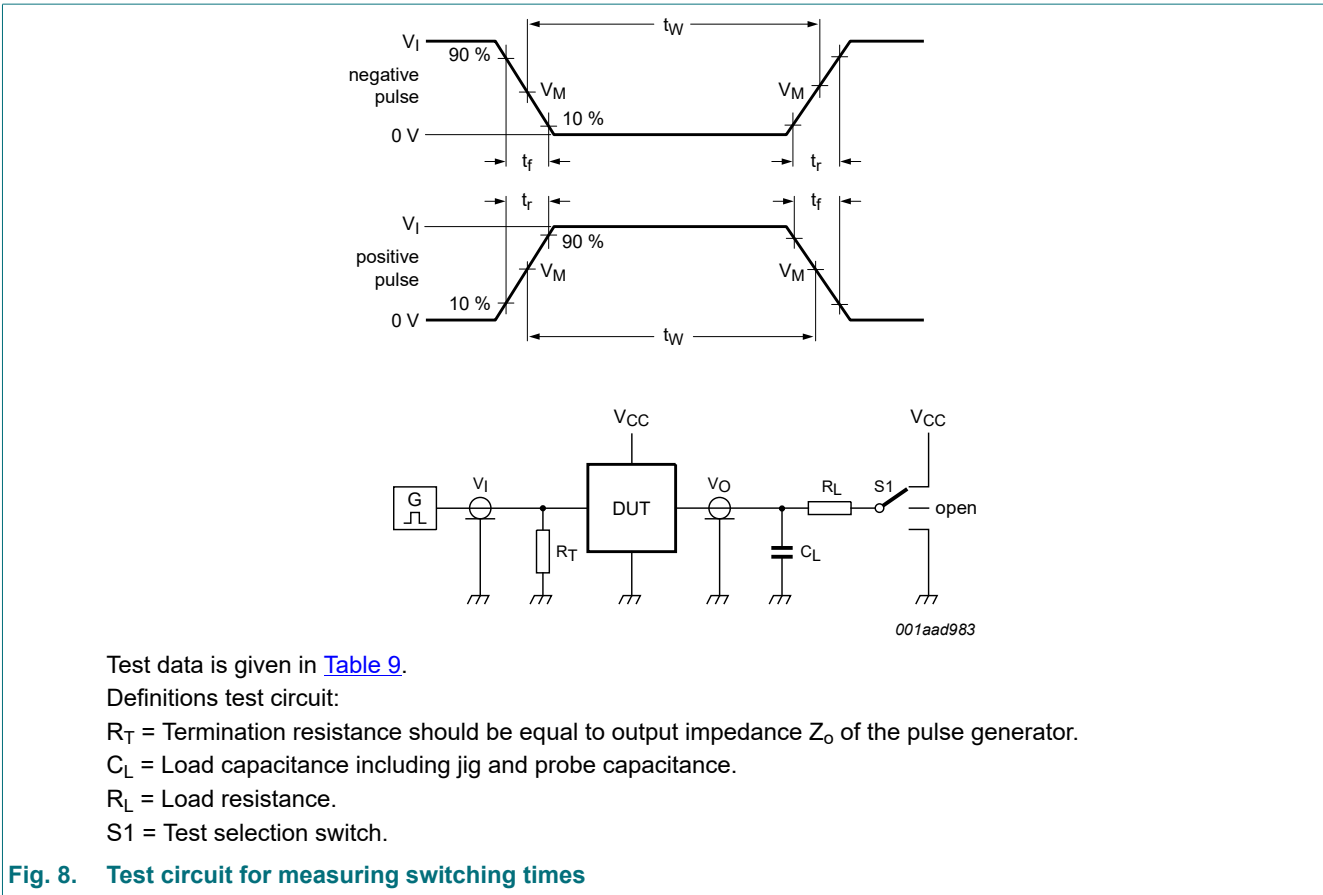


Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74HC240	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74HCT240	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$



11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Fig. 9. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

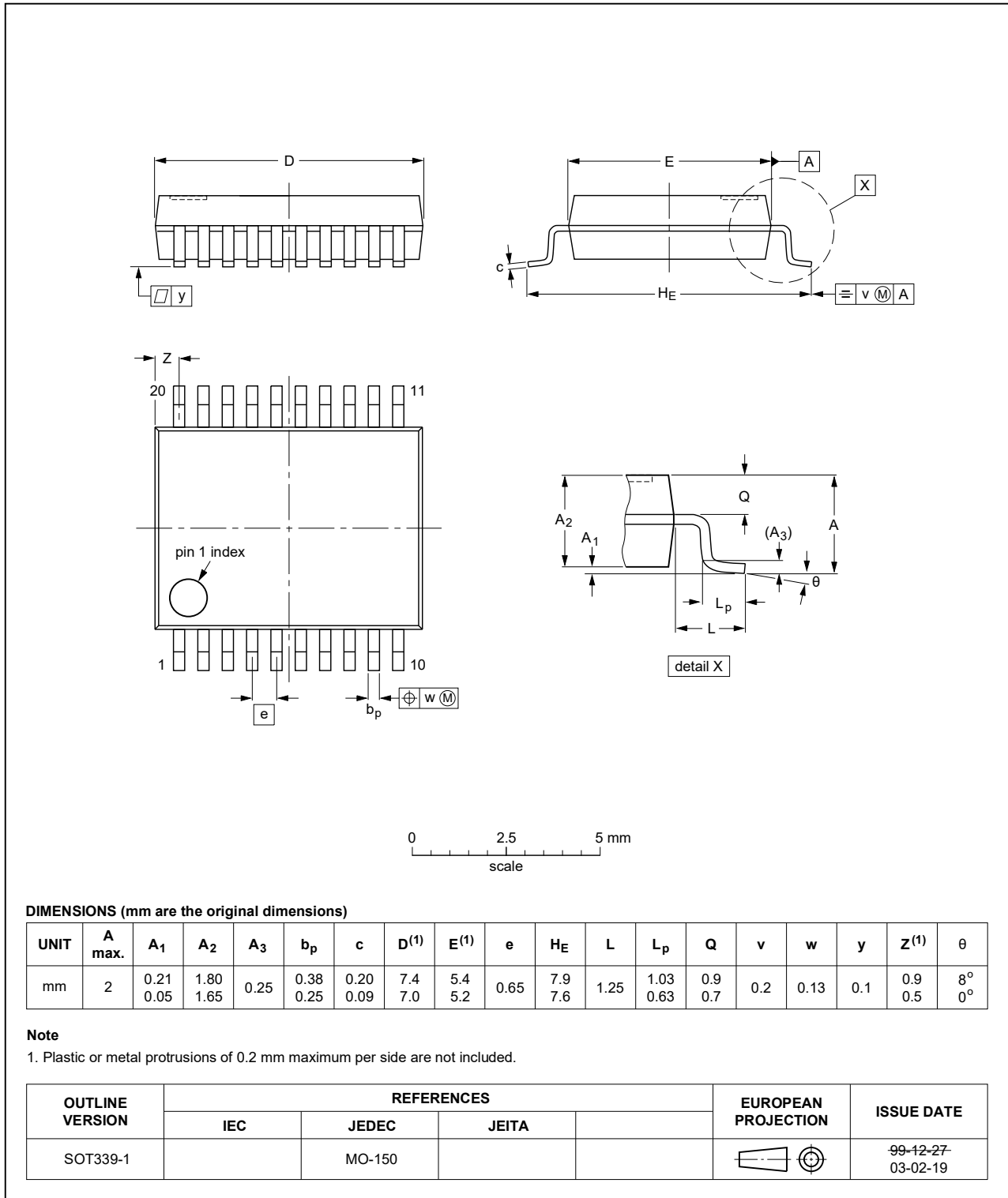


Fig. 10. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig. 11. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



Fig. 12. Package outline SOT764-1 (DHVQFN20)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT240 v.5	20200715	Product data sheet	-	74HC_HCT240 v.4
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 2</a> updated.</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74HC_HCT240 v.4	20160225	Product data sheet	-	74HC_HCT240 v.3
Modifications:	<ul style="list-style-type: none"> <li>Type numbers 74HC240N and 74HCT240N (SOT146-1) removed.</li> </ul>			
74HC_HCT240 v.3	20070802	Product data sheet	-	74HC_HCT240_CNV v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Added type number 74HC240BQ and 74HCT240BQ (DHVQFN20 package)</li> </ul>			
74HC_HCT240_CNV v.2	19970828	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 15 July 2020

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