

# 74AHC574; 74AHCT574

Octal D-type flip-flop; positive edge-trigger; 3-state

Rev. 02 — 24 January 2008

Product data sheet

## 1. General description

The 74AHC574; 74AHCT574 are high-speed Si-gate CMOS devices and are pin compatible with Low Power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74AHC574; 74AHCT574 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) and an output enable ( $\overline{OE}$ ) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When  $\overline{OE}$  is LOW the contents of the 8 flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

The 74AHC574; 74AHCT574 is functionally identical to the 74AHC564; 74AHCT564, but has non-inverting outputs. The 74AHC574; 74AHCT574 is functionally identical to the 74AHC374; 74AHCT374, but has a different pinning.

## 2. Features

- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- 3-state non-inverting outputs for bus orientated applications
- 8-bit positive, edge-triggered register
- Independent register and 3-state buffer operation
- Common 3-state output enable input
- For 74AHC574 only: operates with CMOS input levels
- For 74AHCT574 only: operates with TTL input levels
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
  - ◆ CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

## 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AHC574D 74AHCT574D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHC574PW 74AHCT574PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74AHC574BQ 74AHCT574BQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

## 4. Functional diagram

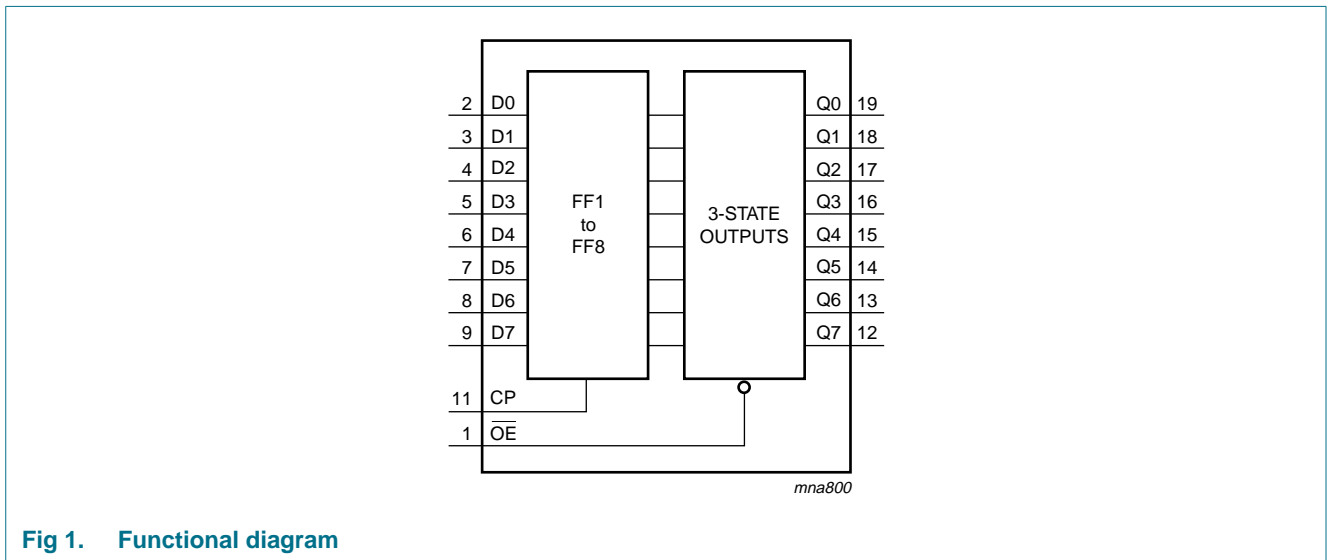


Fig 1. Functional diagram

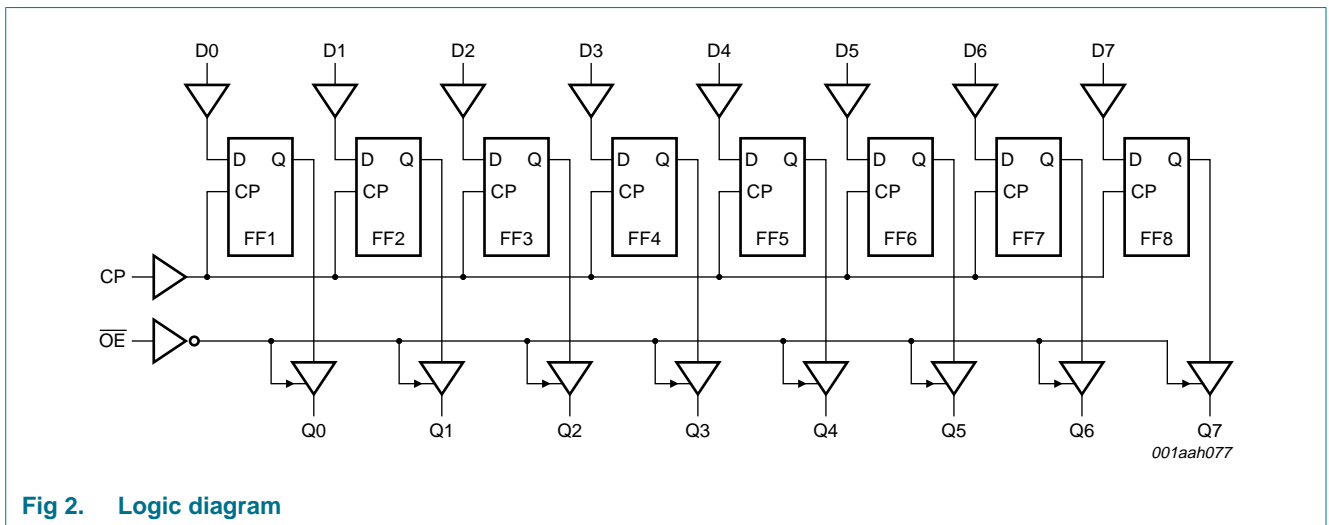


Fig 2. Logic diagram

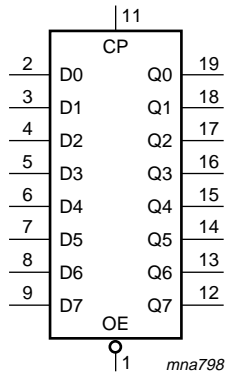


Fig 3. Logic symbol

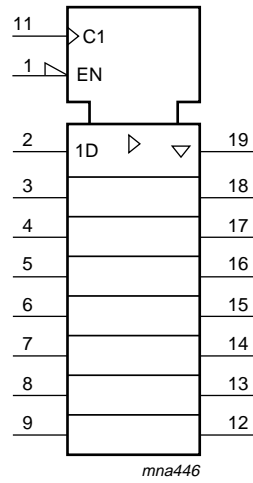
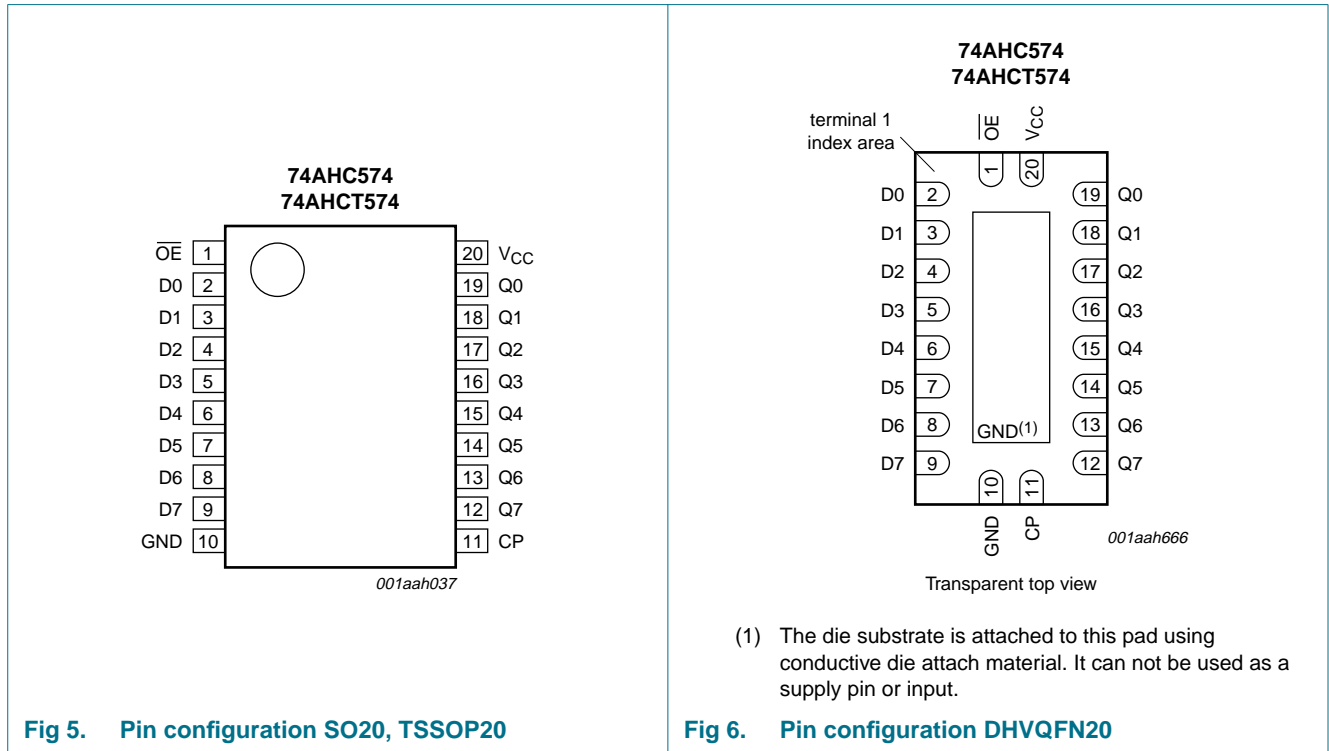


Fig 4. IEC logic symbol

## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	3-state output enable input (active LOW)
D[0:7]	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge triggered)
Q[0:7]	19, 18, 17, 16, 15, 14, 13, 12	3-state flip-flop output
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Operating mode	Input			Internal flip-flop	Output Qn
	$\overline{OE}$	CP	Dn		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable output	H	↑	l	L	Z
	H	↑	h	H	Z

- [1] H = HIGH voltage level;  
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW CP transition;  
 L = LOW voltage level;  
 l = LOW voltage level one setup time prior to the HIGH-to-LOW CP transition;  
 Z = high-impedance OFF-state;  
 ↑ = LOW-to-HIGH clock transition.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V	[1] -20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1] -	±20	mA
$I_O$	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-	±25	mA
$I_{CC}$	supply current		-	75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
	SO20 package		[2] -	500	mW
	TSSOP20 package		[3] -	500	mW
	DHVQFN20 package		[4] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2]  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.  
 [3]  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.  
 [4]  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC574			74AHCT574			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	5.5	0	-	5.5	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V <sub>CC</sub> = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>For type 74AHC574</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I <sub>O</sub> = -8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.25	-	±2.5	-	±10.0	μA
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	4.0	-	40	-	80	μA

**Table 6. Static characteristics ...continued**  
*Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C <sub>I</sub>	input capacitance		-	3.0	10	-	10	-	10	pF
C <sub>O</sub>	output capacitance		-	4.0	-	-	-	-	-	pF
<b>For type 74AHCT574</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I <sub>OZ</sub>	OFF-state output current	per input pin; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 0 A; V <sub>O</sub> = V <sub>CC</sub> or GND; other pins at V <sub>CC</sub> or GND	-	-	±0.25	-	±2.5	-	±10.0	µA
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	4.0	-	40	-	80	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; I <sub>O</sub> = 0 A; other pins at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C <sub>I</sub>	input capacitance		-	3	10	-	10	-	10	pF
C <sub>O</sub>	output capacitance		-	4.0	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**  
*GND = 0 V. For test circuit see Figure 10.*

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
<b>For type 74AHC574</b>										
$t_{pd}$	propagation delay	CP to Qn; see Figure 7 <sup>[2]</sup>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$								
		$C_L = 15\text{ pF}$	-	6.5	13.2	1.0	15.5	1.0	16.5	ns
		$C_L = 50\text{ pF}$	-	9.3	16.7	1.0	19.0	1.0	21.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	4.4	8.6	1.0	10.0	1.0	11.0	ns
$t_{en}$	enable time	$\overline{OE}$ to Qn; see Figure 9 <sup>[1]</sup>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$								
		$C_L = 15\text{ pF}$	-	5.7	12.8	1.0	15.0	1.0	16.0	ns
		$C_L = 50\text{ pF}$	-	8.2	16.3	1.0	18.5	1.0	20.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	4.2	9.0	1.0	10.5	1.0	11.5	ns
$t_{dis}$	disable time	$\overline{OE}$ to Qn; see Figure 9 <sup>[2]</sup>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$								
		$C_L = 15\text{ pF}$	-	6.3	13.0	1.0	15.0	1.0	16.5	ns
		$C_L = 50\text{ pF}$	-	9.1	15.0	1.0	17.0	1.0	19.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	4.3	9.0	1.0	10.5	1.0	11.5	ns
$f_{max}$	maximum frequency	CP; see Figure 7								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$								
		$C_L = 15\text{ pF}$	80	125	-	65	-	65	-	MHz
		$C_L = 50\text{ pF}$	50	75	-	45	-	45	-	MHz
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	130	180	-	110	-	110	-	MHz
$t_W$	pulse width	CP; HIGH or LOW; see Figure 7								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 50\text{ pF}$	5.0	-	-	5.0	-	5.0	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$	5.0	-	-	5.0	-	5.0	-	ns



**Table 7. Dynamic characteristics ...continued**  
*GND = 0 V. For test circuit see Figure 10.*

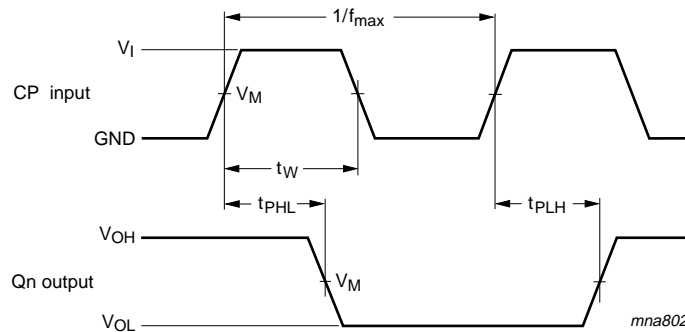
Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
t <sub>su</sub>	set-up time	Dn to CP; see <a href="#">Figure 8</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 50 pF	3.5	-	-	3.5	-	3.5	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V; C <sub>L</sub> = 50 pF	3.0	-	-	3.0	-	3.0	-	ns
t <sub>h</sub>	hold time	Dn to CP; see <a href="#">Figure 8</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 50 pF	1.5	-	-	1.5	-	1.5	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V; C <sub>L</sub> = 50 pF	1.5	-	-	1.5	-	1.5	-	ns
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub>	<sup>[3]</sup>	-	10	-	-	-	-	pF
<b>For type 74AHCT574</b>										
t <sub>pd</sub>	propagation delay	CP to Qn; see <a href="#">Figure 7</a>		<sup>[2]</sup>						
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	4.4	8.6	1.0	10.0	1.0	11.0	ns
		C <sub>L</sub> = 50 pF	-	6.3	10.6	1.0	12.0	1.0	13.5	ns
t <sub>en</sub>	enable time	$\overline{\text{OE}}$ to Qn; see <a href="#">Figure 9</a>								
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	4.3	9.0	1.0	10.5	1.0	11.5	ns
		C <sub>L</sub> = 50 pF	-	6.1	11.0	1.0	12.5	1.0	14.0	ns
t <sub>dis</sub>	disable time	$\overline{\text{OE}}$ to Qn; see <a href="#">Figure 9</a>		<sup>[2]</sup>						
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	4.3	9.0	1.0	10.5	1.0	11.5	ns
		C <sub>L</sub> = 50 pF	-	6.2	10.1	1.0	11.5	1.0	13.0	ns
f <sub>max</sub>	maximum frequency	CP; see <a href="#">Figure 7</a>								
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	130	180	-	110	-	110	-	MHz
		C <sub>L</sub> = 50 pF	85	115	-	75	-	75	-	MHz
t <sub>w</sub>	pulse width	CP; HIGH or LOW; see <a href="#">Figure 7</a>								
		V <sub>CC</sub> = 4.5 V to 5.5 V; C <sub>L</sub> = 50 pF	5.0	-	-	5.5	-	5.5	-	ns
t <sub>su</sub>	set-up time	Dn to CP; see <a href="#">Figure 8</a>								
		V <sub>CC</sub> = 4.5 V to 5.5 V; C <sub>L</sub> = 50 pF	3.0	-	-	3.5	-	3.5	-	ns

**Table 7. Dynamic characteristics ...continued**  
*GND = 0 V. For test circuit see Figure 10.*

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
$t_h$	hold time	Dn to CP; see Figure 8 $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V};$ $C_L = 50 \text{ pF}$	1.5	-	-	1.5	-	1.5	-	ns
$C_{PD}$	power dissipation capacitance	per buffer; $C_L = 50 \text{ pF}; f = 1 \text{ MHz};$ $V_I = \text{GND to } V_{CC}$	[3]	-	12	-	-	-	-	pF

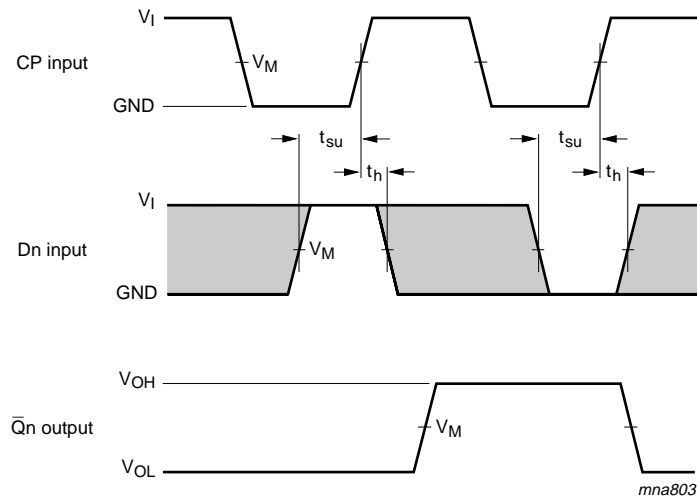
- [1] Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3 \text{ V}$  and  $V_{CC} = 5.0 \text{ V}$ ).
- [2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .  
 $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .  
 $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .
- [3]  $C_{PD}$  is used to determine the dynamic power dissipation  $P_D$  ( $\mu\text{W}$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in V.

**10.1 Waveforms**



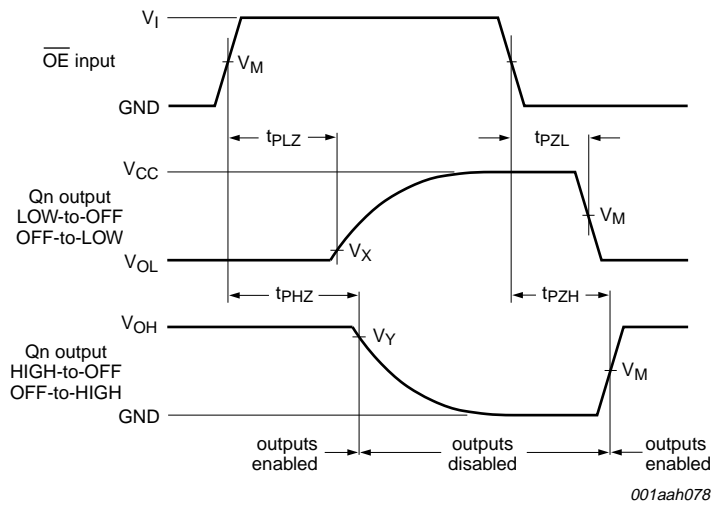
Measurement points are given in Table 8.  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. Propagation delay input (CP) to output (Qn), clock input (CP) pulse width and the maximum frequency (CP)**



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.  
 The shaded areas indicate when the input is permitted to change for predicable output performance.

**Fig 8. The data input (D) to clock input (CP) set-up times and clock input (CP) to data input (D) hold times**

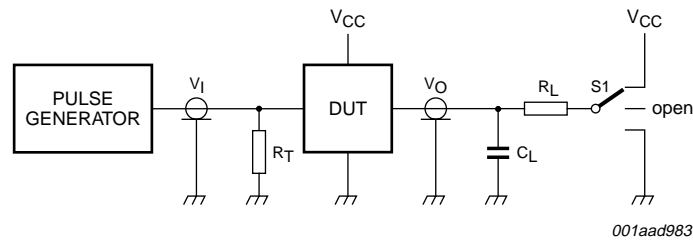
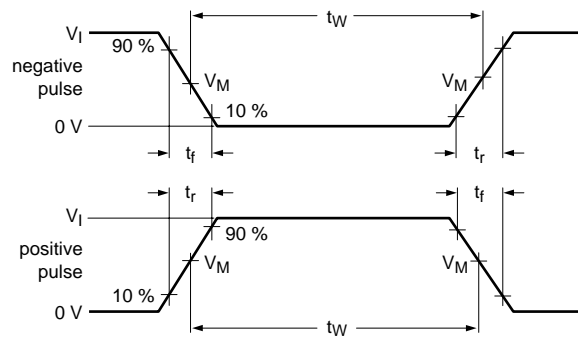


Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 9. Enable and disable times**

**Table 8. Measurement points**

Type	Input	Output		
	$V_M$	$V_M$	$V_X$	$V_Y$
74AHC574	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
74AHCT574	1.5 V	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



001aad983

Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

S1 = Test selection switch.

**Fig 10. Load circuitry for switching times**

**Table 9. Test data**

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74AHC574	$V_{CC}$	3.0 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74AHCT574	3.0 V	3.0 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

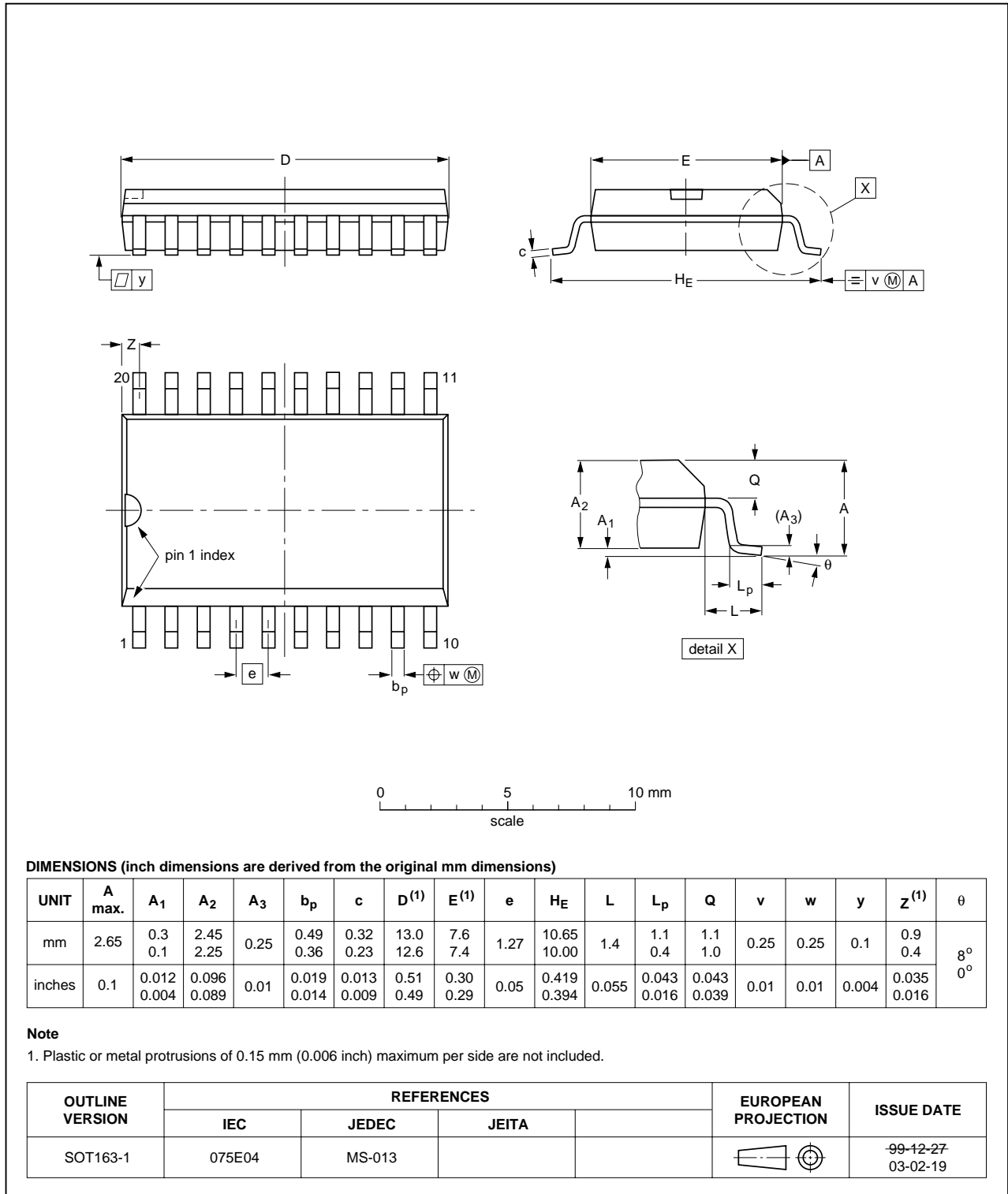


Fig 11. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig 12. Package outline SOT360-1 (TSSOP20)

**DHVQFN20:** plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

**SOT764-1**



**Fig 13. Package outline SOT764-1 (DHVQFN20)**

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT574_2	20080124	Product data sheet	-	74AHC_AHCT574_1
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Section 3</a>: DHVQFN20 package added.</li> <li>• <a href="#">Section 7</a>: derating values added for DHVQFN20 package.</li> <li>• <a href="#">Section 11</a>: outline drawing added for DHVQFN20 package.</li> </ul>			
74AHC_AHCT574_1	19990616	Product specification	-	-



## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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