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Kind regards,

Team Nexperia

# PEMB17; PUMB17

PNP/PNP resistor-equipped transistors;  
R1 = 47 k $\Omega$ , R2 = 22 k $\Omega$

Rev. 03 — 1 September 2009

Product data sheet

## 1. Product profile

### 1.1 General description

PNP/PNP resistor-equipped transistors

Table 1. Product overview

Type number	Package		NPN/PNP complement	NPN/PNP complement
	NXP	JEITA		
PEMB17	SOT666	-	PEMD17	PEMH17
PUMB17	SOT363	SC-88	PUMD17	PUMH17

### 1.2 Features

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place cost

### 1.3 Applications

- Low current peripheral driver
- Control of IC inputs
- Replacement of general-purpose transistors in digital applications

### 1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	-50	V
I <sub>O</sub>	output current (DC)		-	-	-100	mA
R1	bias resistor 1 (input)		33	47	61	k $\Omega$
R2/R1	bias resistor ratio		0.37	0.47	0.57	

## 2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Symbol
1	GND (emitter) TR1		
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		

## 3. Ordering information

Table 4. Ordering information

Type number	Package		Version
	Name	Description	
PEMB17	-	plastic surface mounted package; 6 leads	SOT666
PUMB17	SC-88	plastic surface mounted package; 6 leads	SOT363

## 4. Marking

Table 5. Marking codes

Type number	Marking code <sup>[1]</sup>
PEMB17	5M
PUMB17	B*8

[1] \* = -: made in Hong Kong  
 \* = p: made in Hong Kong  
 \* = t: made in Malaysia  
 \* = W: made in China

## 5. Limiting values

**Table 6. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Per transistor</b>						
V <sub>CBO</sub>	collector-base voltage	open emitter	-	-50	V	
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-50	V	
V <sub>EBO</sub>	emitter-base voltage	open collector	-	-10	V	
V <sub>I</sub>	input voltage					
	positive		-	+10	V	
	negative		-	-40	V	
I <sub>O</sub>	output current (DC)		-	-100	mA	
I <sub>CM</sub>	peak collector current		-	-100	mA	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C				
	SOT363		[1]	-	200	mW
	SOT666		[1] [2]	-	200	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C	
T <sub>j</sub>	junction temperature		-	150	°C	
T <sub>amb</sub>	ambient temperature		-65	+150	°C	
<b>Per device</b>						
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C				
	SOT363		[1]	-	300	mW
	SOT666		[1] [2]	-	300	mW

[1] Device mounted on a FR4 printed-circuit board, single-sided copper, standard footprint.

[2] Reflow soldering is the only recommended soldering method.

## 6. Thermal characteristics

**Table 7. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	T <sub>amb</sub> ≤ 25 °C				
	SOT363		[1]	-	625	K/W
	SOT666		[1] [2]	-	625	K/W
<b>Per device</b>						
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	T <sub>amb</sub> ≤ 25 °C				
	SOT363		[1]	-	416	K/W
	SOT666		[1] [2]	-	416	K/W

[1] Device mounted on a FR4 printed-circuit board, single-sided copper, standard footprint.

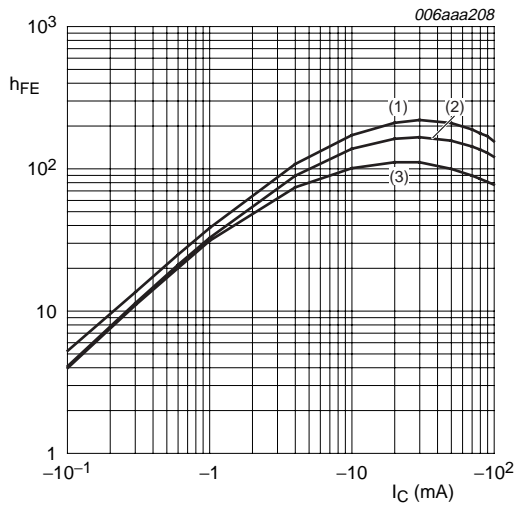
[2] Reflow soldering is the only recommended soldering method.

## 7. Characteristics

**Table 8. Characteristics**

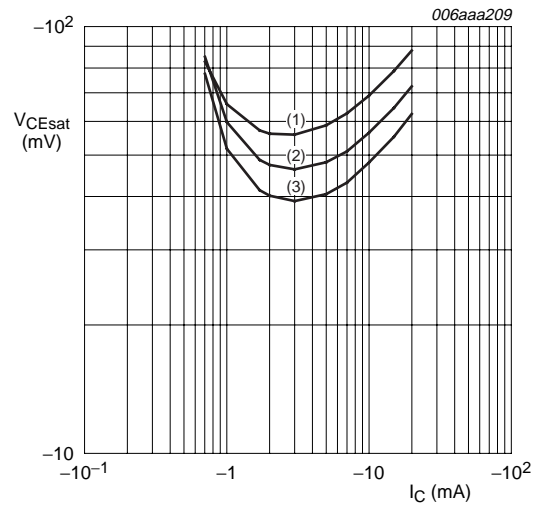
$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$I_{CBO}$	collector-base cut-off current	$V_{CB} = -50\text{ V}; I_E = 0\text{ A}$	-	-	-100	nA
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = -30\text{ V}; I_B = 0\text{ A}$	-	-	-1	$\mu\text{A}$
		$V_{CE} = -30\text{ V}; I_B = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	-50	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0\text{ A}$	-	-	-110	$\mu\text{A}$
$h_{FE}$	DC current gain	$V_{CE} = -5\text{ V}; I_C = -5\text{ mA}$	60	-	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -10\text{ mA}; I_B = -0.5\text{ mA}$	-	-	-150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5\text{ V}; I_C = -100\text{ }\mu\text{A}$	-	-1.7	-1.2	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = -0.3\text{ V}; I_C = -2\text{ mA}$	-4	-2.7	-	V
R1	bias resistor 1 (input)		33	47	61	k $\Omega$
R2/R1	bias resistor ratio		0.37	0.47	0.57	
$C_c$	collector capacitance	$V_{CB} = -10\text{ V}; I_E = i_e = 0\text{ A}; f = 1\text{ MHz}$	-	-	3	pF



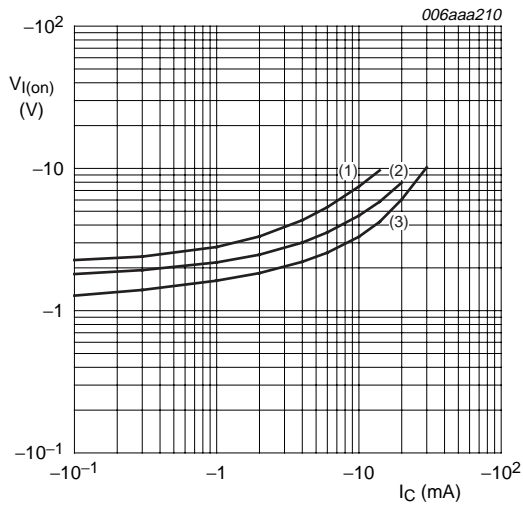
$V_{CE} = -5\text{ V}$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -40\text{ °C}$

**Fig 1. DC current gain as a function of collector current; typical values**



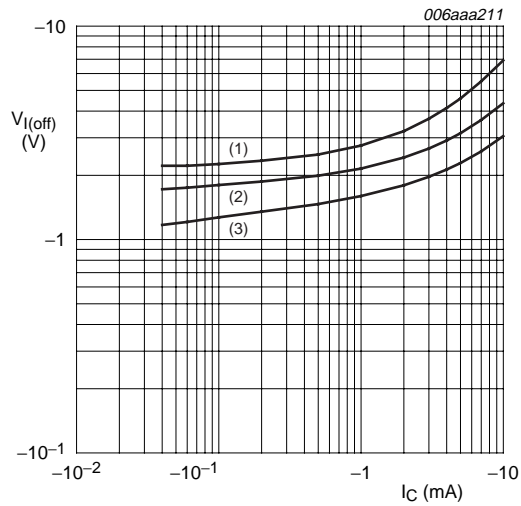
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -40\text{ °C}$

**Fig 2. Collector-emitter saturation voltage as a function of collector current; typical values**



$V_{CE} = -0.3\text{ V}$   
 (1)  $T_{amb} = -40\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = 100\text{ °C}$

**Fig 3. On-state input voltage as a function of collector current; typical values**



$V_{CE} = -5\text{ V}$   
 (1)  $T_{amb} = -40\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = 100\text{ °C}$

**Fig 4. Off-state input voltage as a function of collector current; typical values**

**8. Package outline**

Plastic surface-mounted package; 6 leads

SOT363

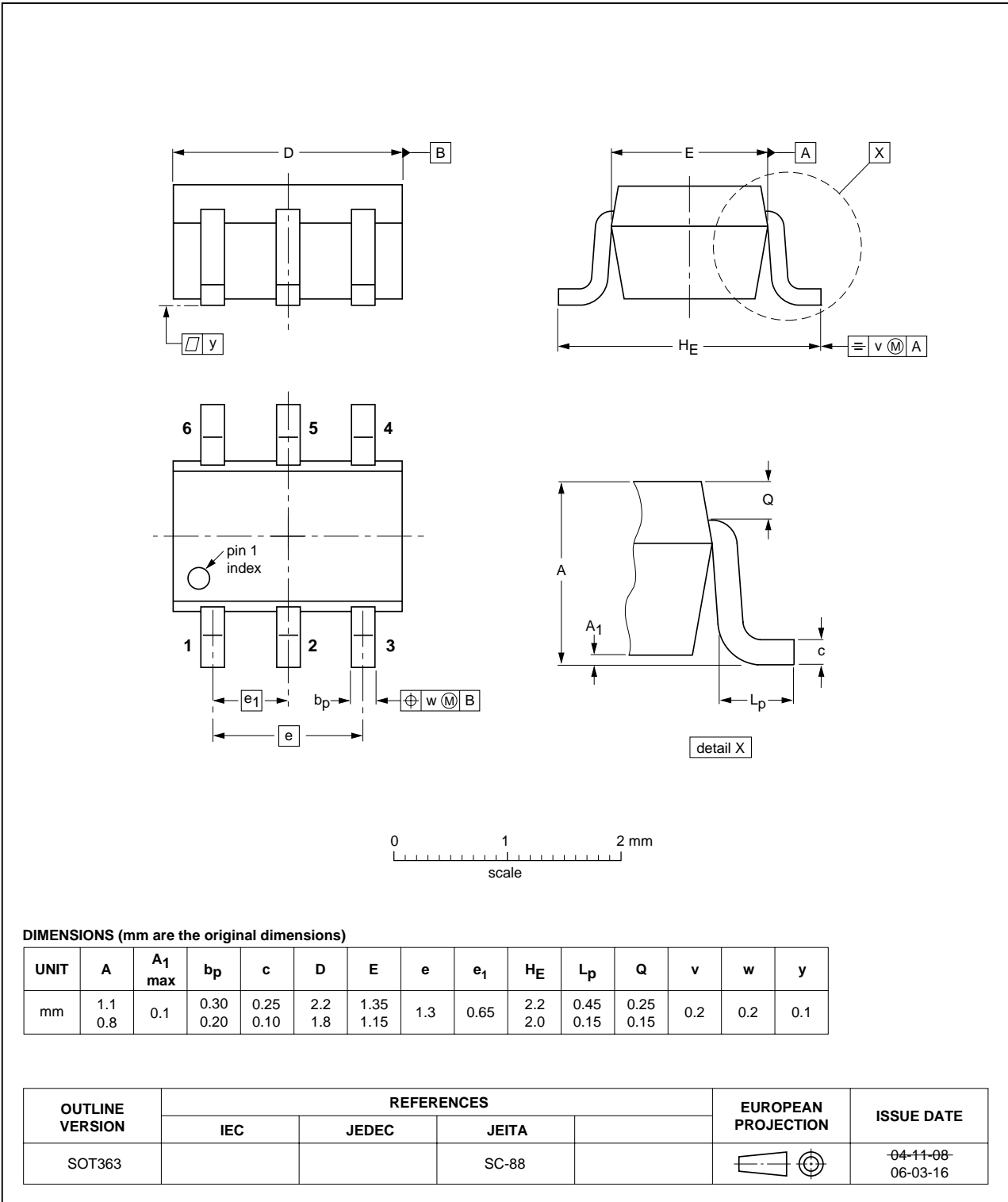


Fig 5. Package outline SOT363 (SC-88)

Plastic surface-mounted package; 6 leads

SOT666

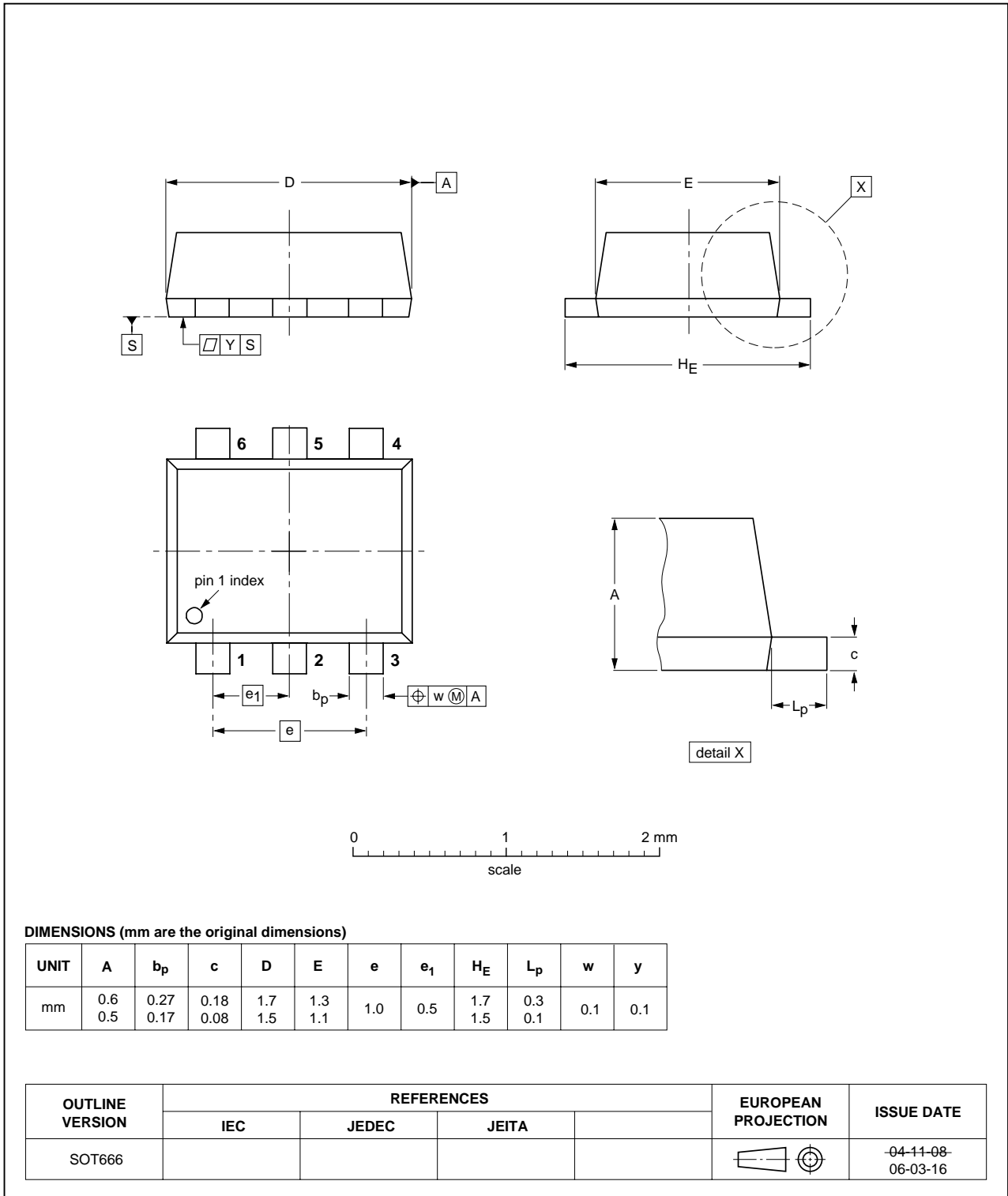


Fig 6. Package outline SOT666



## 9. Packing information

**Table 9. Packing methods**

The indicated -xxx are the last three digits of the 12NC ordering code. [\[1\]](#)

Type number	Package	Description	Packing quantity		
			3000	4000	10000
PEMB17	SOT666	4 mm pitch, 8 mm tape and reel;	-	-115	-
PUMB17	SOT363	4 mm pitch, 8 mm tape and reel; T1 <a href="#">[2]</a>	-115	-	-135
PUMB17	SOT363	4 mm pitch, 8 mm tape and reel; T2 <a href="#">[3]</a>	-125	-	-165

[1] For further information and the availability of packing methods, see [Section 12](#).

[2] T1: normal taping

[3] T2: reverse taping

## 10. Revision history

**Table 10. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PEMB17_PUMB17_3	20090901	Product data sheet	-	PEMB17_PUMB17_2
Modifications:	<ul style="list-style-type: none"> <li>• This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content.</li> <li>• <a href="#">Figure 5 “Package outline SOT363 (SC-88)”</a>: updated</li> <li>• <a href="#">Figure 6 “Package outline SOT666”</a>: updated</li> </ul>			
PEMB17_PUMB17_2	20050203	Product data sheet	-	PUMB17_1
PUMB17_1	20031103	Product specification	-	-

## 11. Legal information

### 11.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.





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