



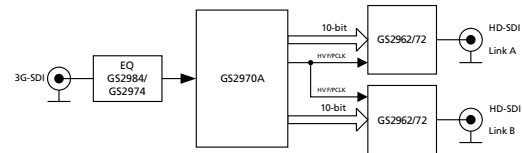
3Gb/s, HD, SD SDI Receiver Complete with SMPTE Audio and Video Processing

Key Features

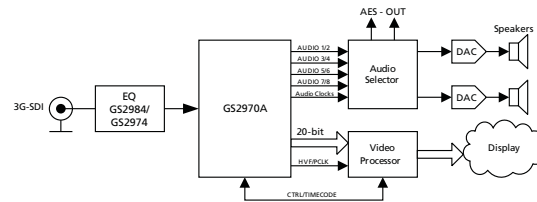
- Operation at 2.970Gb/s, 2.970/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s
- Supports SMPTE ST 425 (Level A and Level B), SMPTE ST 424, SMPTE ST 292, SMPTE ST 259-C and DVB-ASI
- Integrated Reclocker
- Integrated low phase noise VCO
- Serial digital reclocked, or non-reclocked loop-through output
- Integrated audio de-embedder for 8 channels of 48kHz audio
- Integrated audio clock generator
- Ancillary data extraction
- Optional conversion from SMPTE ST 425 Level B to Level A for 1080p 50/59.94/60 4:2:2 10-bit inputs
- Parallel data bus selectable as either 20-bit or 10-bit
- Comprehensive error detection and correction features
- Output H, V, F or CEA 861 timing signals
- 1.2V digital core power supply, 1.2V and 3.3V analog power supplies, and selectable 1.8V or 3.3V I/O power supply
- GSPI host interface
- -20°C to +85°C operating temperature range
- Low power operation (typically 350mW)
- Small 11mm x 11mm 100-ball BGA package
- Pb-free and RoHS compliant

Applications

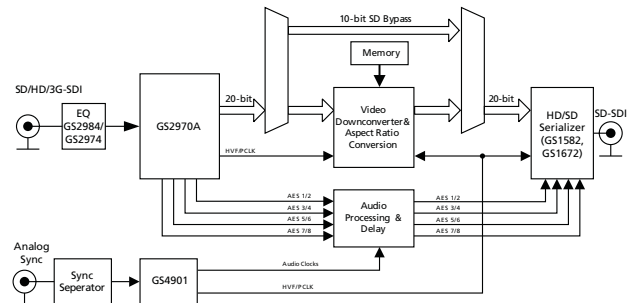
Application: Single Link (3G-SDI) to Dual Link (HD-SDI) Converter



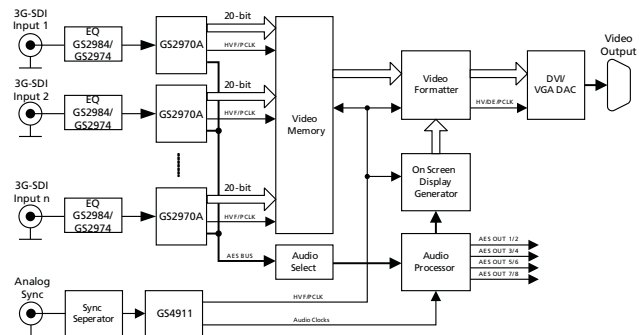
Application: 1080p50/60 Monitor



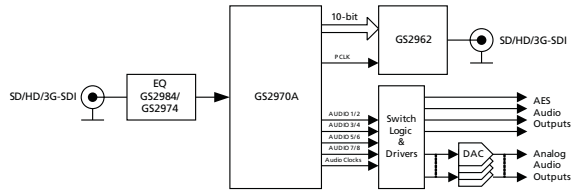
Application: Multi-format Downconverter



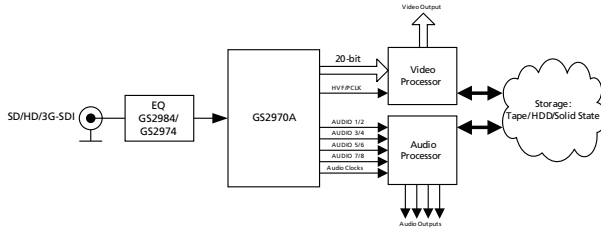
Application: Multi-input Video Monitoring System



Application: Multi-format Audio De-embedder Module



Application: Multi-format Digital VTR/Video Server



Description

The GS2970A is a multi-rate SDI Receiver which includes complete SMPTE processing, as per SMPTE ST 425, SMPTE ST 292 and SMPTE ST 259-C. The SMPTE processing features can be bypassed to support signals with other coding schemes.

The device features an Integrated Reclocker with an internal VCO and a wide Input Jitter Tolerance (IJT) of 0.7UI.

A serial digital loop-through output is provided, which can be configured to output either reclocked or non-reclocked serial digital data. The serial digital output can be connected to an external cable driver.

The device operates in one of four basic modes: SMPTE mode, DVB-ASI mode, Data-Through mode or Standby mode.

In SMPTE mode (the default operating mode), the GS2970A performs full SMPTE processing, and features a number of data integrity checks and measurement capabilities.

The device also supports ancillary data extraction, and can provide entire ancillary data packets through host-accessible registers. It also provides a variety of other packet detection and error handling features. All of these processing features are optional, and may be individually enabled or disabled through register programming.

Both SMPTE ST 425 Level A and Level B inputs are supported with optional conversion from Level B to Level A for 1080p 50/59.94/60 4:2:2 10-bit inputs.

In DVB-ASI mode, sync word detection, alignment and 8b/10b decoding is applied to the received data stream.

In Data-Through mode all forms of SMPTE and DVB-ASI processing are disabled, and the device can be used as a simple serial to parallel converter.

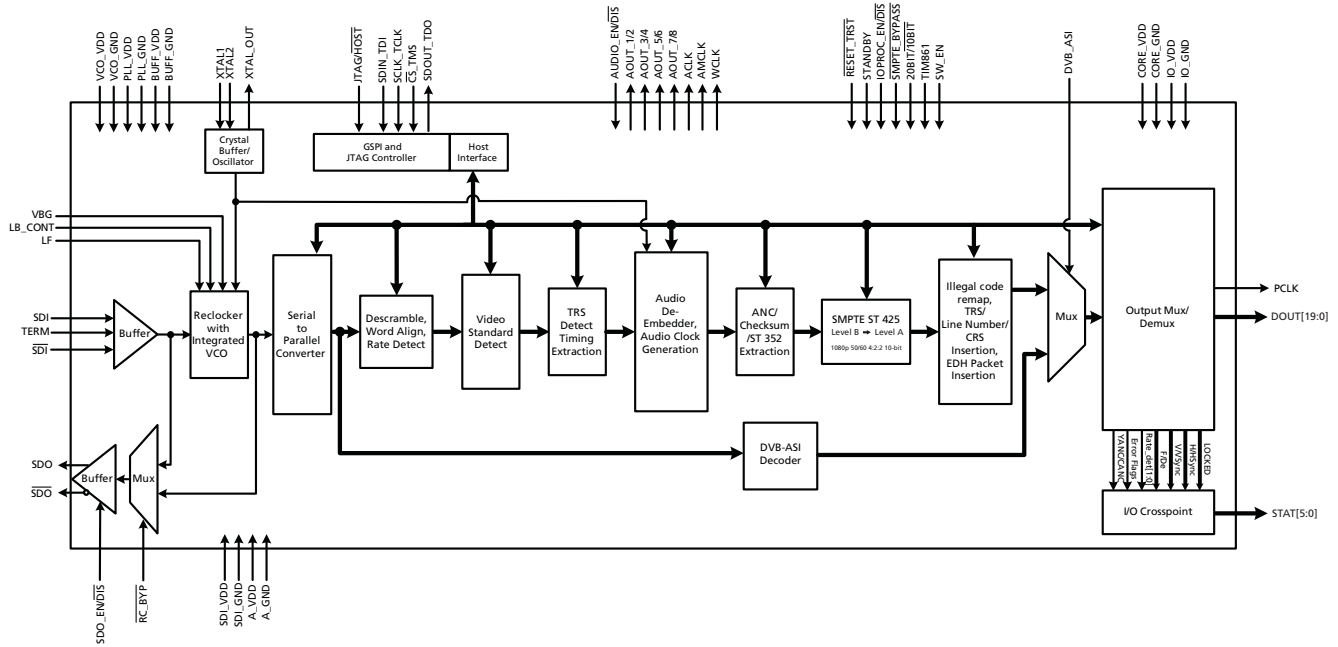
The device can also operate in a lower power Standby mode. In this mode, no signal processing is carried out and the parallel output is held static.

Parallel data outputs are provided in 20-bit or 10-bit format for 3Gb/s, HD and SD video rates, with a variety of mapping options. As such, this parallel bus can interface directly with video processor ICs, and output data can be multiplexed onto 10 bits for a low pin count interface.

Up to eight channels (two audio groups) of serial digital audio may be extracted from the video data stream, in accordance with SMPTE ST 272-C and SMPTE ST 299.

The output audio formats supported by the device include AES/EBU and I²S, and two other industry standard serial digital formats. A variety of audio processing features are provided to ease implementation. Audio clocks are internally generated and provided by the device.

Functional Block Diagram



GS2970A Functional Block Diagram

Revision History

| Version | ECO | PCN | Date | Changes and/or Modifications |
|---------|--------|-----|----------------|--|
| 3 | 014961 | - | August 2013 | Clarified IOPROC_EN/DIS register configuration throughout Section 4. Added note to Section 4.20. Updated SMPTE format throughout document. |
| 2 | 158084 | - | September 2012 | Changes throughout the document. |
| 1 | 154875 | - | September 2010 | Removed three duplicated pages from Table 4.21.1 Video Core Registers. |
| 0 | 154391 | - | July 2010 | New Document. |

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1. Pin Out

1.1 Pin Assignment

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|-------------------------|------------|-----------------------------|---------|----------|----------|-----------------------------------|---------------|--------|--------|
| A | VBG | LF | LB_CONT | VCO_VDD | STAT0 | STAT1 | IO_VDD | PCLK | DOUT18 | DOUT17 |
| B | A_VDD | PLL_VDD | RSV | VCO_GND | STAT2 | STAT3 | IO_GND | DOUT19 | DOUT16 | DOUT15 |
| C | SDI | A_GND | PLL_VDD | PLL_VDD | STAT4 | STAT5 | $\overline{\text{RESET_TRST}}$ | DOUT12 | DOUT14 | DOUT13 |
| D | $\overline{\text{SDI}}$ | A_GND | A_GND | PLL_GND | CORE_GND | CORE_VDD | SW_EN | JTAG/HOST | IO_GND | IO_VDD |
| E | SDI_VDD | SDI_GND | A_GND | PLL_GND | CORE_GND | CORE_VDD | SDOUT_TDO | SDIN_TDI | DOUT10 | DOUT11 |
| F | TERM | RSV | A_GND | PLL_GND | CORE_GND | CORE_VDD | $\overline{\text{CS_TMS}}$ | SCLK_TCK | DOUT8 | DOUT9 |
| G | RSV | RSV | $\overline{\text{RC_BYP}}$ | RSV | CORE_GND | CORE_VDD | $\overline{\text{SMPTE_BYPASS}}$ | DVB_ASI | IO_GND | IO_VDD |
| H | BUFF_VDD | BUFF_GND | AUDIO_EN/DIS | WCLK | TIM_861 | XTAL_OUT | 20bit/10bit | IOPROC_EN/DIS | DOUT6 | DOUT7 |
| J | SDO | SDO_EN/DIS | AOUT_1/2 | ACLK | AOUT_5/6 | XTAL2 | IO_GND | DOUT1 | DOUT4 | DOUT5 |
| K | $\overline{\text{SDO}}$ | STANDBY | AOUT_3/4 | AMCLK | AOUT_7/8 | XTAL1 | IO_VDD | DOUT0 | DOUT2 | DOUT3 |

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

| Pin Number | Name | Type | Description |
|------------|---------|--------------|---|
| A1 | VBG | Analog Input | Band Gap voltage filter connection. |
| A2 | LF | Analog Input | Loop Filter component connection. |
| A3 | LB_CONT | Analog Input | Connection for loop bandwidth control resistor. |
| A4 | VCO_VDD | Input Power | POWER pin for the VCO. Connect to a 1.2V±5% analog supply followed by a RC filter (see 5.1 Typical Application Circuit). A 105Ω 1% resistor must be used in the RC filter circuit. VCO_VDD is nominally 0.7V. |

Table 1-1: Pin Descriptions (Continued)

| Pin Number | Name | Type | Description | |
|---------------------------|-----------|-------------|---|--------------------------------|
| A5, A6, B5, B6, C5, C6 | STAT[0:5] | Output | MULTI-FUNCTIONAL OUTPUT PORT. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Each of the STAT[0:5] pins can be configured individually to output one of the following signals: | |
| | | | Signal | Default |
| | | | H/HSYNC | STAT0 |
| | | | V/VSYNC | STAT1 |
| | | | F/DE | STAT2 |
| | | | LOCKED | STAT3 |
| | | | Y/1ANC | STAT4 |
| | | | C/2ANC | – |
| | | | <u>DATA ERROR</u> | STAT5 |
| | | | <u>VIDEO ERROR</u> | – |
| | | | <u>AUDIO ERROR</u> | – |
| | | | EDH DETECTED | – |
| CARRIER DETECT | – | | | |
| RATE_DET0 | – | | | |
| RATE_DET1 | – | | | |
| A7, D10, G10, K7 | IO_VDD | Input Power | POWER connection for digital I/O. Connect to 3.3V or 1.8V DC digital. | |
| A8 | PCLK | Output | PARALLEL DATA BUS CLOCK Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. | |
| | | | 3G 10-bit or 20-bit mode | PCLK @ 148.5 or 148.5/1.001MHz |
| | | | HD 10-bit mode | PCLK @ 148.5 or 148.5/1.001MHz |
| | | | HD 20-bit mode | PCLK @ 74.25 or 74.25/1.001MHz |
| | | | SD 10-bit mode | PCLK @ 27MHz |
| | | | SD 20-bit mode | PCLK @ 13.5MHz |

Table 1-1: Pin Descriptions (Continued)

| Pin Number | Name | Type | Description |
|--|--|--------------|---|
| | | | PARALLEL DATA BUS Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. |
| A9, A10, B8, B9, B10, C8, C9, C10, E9, E10 | DOUT18, 17, 19, 16, 15, 12, 14, 13, 10, 11 | Output | <p>20-bit mode 20bit/10bit = HIGH</p> <p>SMPTE mode ($\overline{\text{SMPTE_BYPASS}} = \text{HIGH}$ and $\text{DVB_ASI} = \text{LOW}$): Luma data output for SD and HD data rates; Data Stream 1 for 3G data rate</p> <p>DVB-ASI mode ($\overline{\text{SMPTE_BYPASS}} = \text{LOW}$ and $\text{DVB_ASI} = \text{HIGH}$): Not defined</p> <p>Data-Through mode ($\overline{\text{SMPTE_BYPASS}} = \text{LOW}$ and $\text{DVB_ASI} = \text{LOW}$): Data output</p> <hr/> <p>10-bit mode 20bit/10bit = LOW</p> <p>SMPTE mode ($\overline{\text{SMPTE_BYPASS}} = \text{HIGH}$ and $\text{DVB_ASI} = \text{LOW}$): Multiplexed Luma/Chroma data output for SD and HD data rates; Multiplexed Data Stream 1&2 for 3G data rate</p> <p>DVB-ASI mode ($\overline{\text{SMPTE_BYPASS}} = \text{LOW}$ and $\text{DVB_ASI} = \text{HIGH}$): 8b/10b decoded DVB-ASI data</p> <p>Data-Through mode ($\overline{\text{SMPTE_BYPASS}} = \text{LOW}$ and $\text{DVB_ASI} = \text{LOW}$): Data output</p> |
| B1 | A_VDD | Input Power | POWER pin for analog circuitry. Connect to 3.3V DC analog. |
| B2, C3, C4 | PLL_VDD | Input Power | POWER pins for the Reclocker PLL. Connect to 1.2V DC analog. |
| B3, F2, G1, G2, G4 | RSV | | These pins must be left unconnected. |
| B4 | VCO_GND | Input Power | GND pin for the VCO. Connect to analog GND. |
| B7, D9, G9, J7 | IO_GND | Input Power | GND connection for digital I/O. Connect to digital GND. |
| C1, D1 | SDI, $\overline{\text{SDI}}$ | Analog Input | Serial Digital Differential Input. |
| C2, D2, D3, E3, F3 | A_GND | Input Power | GND pins for sensitive analog circuitry. Connect to analog GND. |

Table 1-1: Pin Descriptions (Continued)

| Pin Number | Name | Type | Description |
|----------------|--------------------------------------|-------------|--|
| C7 | $\overline{\text{RESET_TRST}}$ | Input | <p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to reset the internal operating conditions to default settings and to reset the JTAG sequence.</p> <p>Normal mode ($\text{JTAG}/\overline{\text{HOST}} = \text{LOW}$):</p> <p>When LOW, all functional blocks are set to default conditions and all digital output signals become high impedance.</p> <p>When HIGH, normal operation of the device resumes.</p> <p>JTAG test mode ($\text{JTAG}/\overline{\text{HOST}} = \text{HIGH}$):</p> <p>When LOW, all functional blocks are set to default and the JTAG test sequence is reset.</p> <p>When HIGH, normal operation of the JTAG test sequence resumes after $\overline{\text{RESET_TRST}}$ is de-asserted.</p> |
| D4, E4, F4 | PLL_GND | Input Power | GND pins for the Reclocker PLL. Connect to analog GND. |
| D5, E5, F5, G5 | CORE_GND | Input Power | GND connection for device core. Connect to digital GND. |
| D6, E6, F6, G6 | CORE_VDD | Input Power | POWER connection for device core. Connect to 1.2V DC digital. |
| D7 | SW_EN | Input | <p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to enable switch-line locking, as described in Section 4.10.1.</p> |
| D8 | $\text{JTAG}/\overline{\text{HOST}}$ | Input | <p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to select JTAG test mode or host interface mode.</p> <p>When $\text{JTAG}/\overline{\text{HOST}}$ is HIGH, the host interface port is configured for JTAG test.</p> <p>When $\text{JTAG}/\overline{\text{HOST}}$ is LOW, normal operation of the host interface port resumes.</p> |
| E1 | SDI_VDD | Input Power | POWER pin for SDI buffer. Connect to 3.3V DC analog. |
| E2 | SDI_GND | Input Power | GND pin for SDI buffer. Connect to analog GND. |
| E7 | SDOUT_TDO | Output | <p>COMMUNICATION SIGNAL OUTPUT</p> <p>Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>GSPI serial data output/test data out.</p> <p>In JTAG mode ($\text{JTAG}/\overline{\text{HOST}} = \text{HIGH}$), this pin is used to shift test results from the device.</p> <p>In host interface mode, this pin is used to read status and configuration data from the device.</p> |

Table 1-1: Pin Descriptions (Continued)

| Pin Number | Name | Type | Description |
|--|----------------------------------|--------------|--|
| E8 | SDIN_TDI | Input | <p>COMMUNICATION SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>GSPI serial data in/test data in.</p> <p>In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is used to shift test data into the device.</p> <p>In host interface mode, this pin is used to write address and configuration data words into the device.</p> |
| F1 | TERM | Analog Input | Decoupling for internal SDI termination resistors. |
| F7 | $\overline{\text{CS}}$ _TMS | Input | <p>COMMUNICATION SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Chip select / test mode start.</p> <p>In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is Test Mode Start, used to control the operation of the JTAG test.</p> <p>In host interface mode (JTAG/$\overline{\text{HOST}}$ = LOW), this pin operates as the host interface chip select and is active LOW.</p> |
| F8 | SCLK_TCK | Input | <p>COMMUNICATION SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Serial data clock signal.</p> <p>In JTAG mode (JTAG/$\overline{\text{HOST}}$ = HIGH), this pin is the JTAG clock.</p> <p>In host interface mode (JTAG/$\overline{\text{HOST}}$ = LOW), this pin is the host interface serial bit clock.</p> <p>All JTAG/host interface addresses and data are shifted into/out of the device synchronously with this clock.</p> |
| F9, F10, H9, H10, J8, J9, J10, K8, K9, K10 | DOUT8, 9, 6, 7, 1, 4, 5, 0, 2, 3 | Output | <p>PARALLEL DATA BUS</p> <p>Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <hr/> <p>SMPTE mode ($\overline{\text{SMPTE_BYPASS}}$ = HIGH and DVB_ASI = LOW): Chroma data output for SD and HD data rates; Data Stream 2 for 3G data rate</p> <p>DVB-ASI mode ($\overline{\text{SMPTE_BYPASS}}$ = LOW and DVB_ASI = HIGH): Not defined</p> <p>Data-Through mode ($\overline{\text{SMPTE_BYPASS}}$ = LOW and DVB_ASI = LOW): Data output</p> <hr/> <p>10-bit mode 20bit/$\overline{10\text{bit}}$ = LOW</p> <p>Forced LOW</p> |
| G3 | $\overline{\text{RC_BYP}}$ | Input | <p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>When this pin is LOW, the serial digital output is the buffered version of the input serial data. When this pin is HIGH, the serial digital output is the reclocked version of the input serial data.</p> |

Table 1-1: Pin Descriptions (Continued)

| Pin Number | Name | Type | Description |
|------------|-----------------------------------|----------------|--|
| G7 | $\overline{\text{SMPTE_BYPASS}}$ | Input/Output | <p>CONTROL SIGNAL INPUT/OUTPUT</p> <p>Please refer to the Input/Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Indicates the presence of valid SMPTE data.</p> <p>When the $\overline{\text{AUTO/MAN}}$ bit in the host interface register is HIGH (Default), this pin is an OUTPUT. $\overline{\text{SMPTE_BYPASS}}$ is HIGH when the device locks to a SMPTE compliant input. $\overline{\text{SMPTE_BYPASS}}$ is LOW under all other conditions.</p> <p>When the $\overline{\text{AUTO/MAN}}$ bit in the host interface register is LOW, this pin is an INPUT:</p> <p>No SMPTE scrambling takes place, and none of the I/O processing features of the device are available when $\overline{\text{SMPTE_BYPASS}}$ is set LOW.</p> <p>When $\overline{\text{SMPTE_BYPASS}}$ is set HIGH, the device carries out SMPTE scrambling and I/O processing.</p> <p>When $\overline{\text{SMPTE_BYPASS}}$ and $\overline{\text{DVB_ASI}}$ are both set LOW, the device operates in Data-Through mode.</p> |
| G8 | DVB_ASI | Input/Output | <p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input/Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to enable/disable DVB-ASI data extraction in manual mode.</p> <p>When the $\overline{\text{AUTO/MAN}}$ bit in the host interface is LOW, this pin is an input and when the DVB_ASI pin is set HIGH the device will carry out DVB_ASI data extraction and processing. The $\overline{\text{SMPTE_BYPASS}}$ pin must be set LOW. When $\overline{\text{SMPTE_BYPASS}}$ and DVB_ASI are both set LOW, the device operates in Data-Through mode.</p> <p>When the $\overline{\text{AUTO/MAN}}$ bit in the host interface is HIGH (default), DVB-ASI is configured as a status output (set LOW), and DVB-ASI input streams are not supported or recognized.</p> |
| H1 | BUFF_VDD | Input Power | POWER pin for the serial digital output 50Ω buffer. Connect to 3.3V DC analog. |
| H2 | BUFF_GND | Input Power | GND pin for the cable driver buffer. Connect to analog GND. |
| H3 | AUDIO_EN/ $\overline{\text{DIS}}$ | Input | <p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Enables or disables audio extraction.</p> |
| H4 | WCLK | Output | <p>48kHz word clock for Audio.</p> <p>Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> |
| H5 | TIM_861 | Input | <p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to select CEA-861 timing mode.</p> <p>When TIM_861 is HIGH, the device outputs CEA 861 timing signals (HSYNC/VSYNC/DE) instead of H:V:F digital timing signals.</p> |
| H6 | XTAL_OUT | Digital Output | Buffered 27MHz crystal output. Can be used to cascade the crystal signal. |

Table 1-1: Pin Descriptions (Continued)

| Pin Number | Name | Type | Description |
|------------|-----------------------------|--------------|---|
| H7 | 20bit/ $\overline{10bit}$ | Input | CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to select the output bus width. HIGH = 20-bit, LOW = 10-bit. |
| H8 | IOPROC_EN/ \overline{DIS} | Input | CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable or disable audio and video processing features. When IOPROC_EN is HIGH, the audio and video processing features of the device are enabled. When IOPROC_EN is LOW, the processing features of the device are disabled, and the device is in a low-latency operating mode. |
| J1, K1 | SDO, \overline{SDO} | Output | Serial Data Output Signal. 50Ω CML buffer for interfacing to an external cable driver. Serial digital output signal operating at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s. |
| J2 | SDO_EN/ \overline{DIS} | Input | CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable/disable the serial digital output stage. When SDO_EN/ \overline{DIS} is LOW, the serial digital output signals, SDO and \overline{SDO} , are both pulled HIGH. When SDO_EN/ \overline{DIS} is HIGH, the serial digital output signals, SDO and \overline{SDO} , are enabled. |
| J3 | AOUT_1/2 | Output | Serial Audio Output; Channels 1 and 2. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. |
| J4 | ACLK | Output | 64fs sample clock for audio. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. |
| J5 | AOUT_5/6 | Output | Serial Audio Output; Channels 5 and 6. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. |
| J6, K6 | XTAL2, XTAL1 | Analog Input | Input connection for 27MHz crystal. |
| K2 | STANDBY | Input | CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. When this pin is set HIGH, the device is placed in a power-saving mode. No data processing occurs, and the digital I/Os are powered down. In this mode, the serial digital output signals, SDO and \overline{SDO} , are both pulled HIGH. |
| K3 | AOUT_3/4 | Output | Serial Audio Output; Channels 3 and 4. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. |

Table 1-1: Pin Descriptions (Continued)

| Pin Number | Name | Type | Description |
|------------|----------|--------|--|
| K4 | AMCLK | Output | Oversampled master clock for audio (128fs, 256fs, 512fs selectable). Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. |
| K5 | AOUT_7/8 | Output | Serial Audio Output; Channels 7 and 8. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. |

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

| Parameter | Value/Units |
|--|-----------------|
| Supply Voltage, Digital Core (CORE_VDD) | -0.3V to +1.5V |
| Supply Voltage, Digital I/O (IO_VDD) | -0.3V to +4.0V |
| Supply Voltage, Analog 1.2V (PD_VDD, VCO_VDD) | -0.3V to +1.5V |
| Supply Voltage, Analog 3.3V (SDI_VDD, BUFF_VDD, A_VDD) | -0.3V to +4.0V |
| Input Voltage Range (digital inputs) | -2.0V to +5.25V |
| Operating Temperature Range | -20°C to +85°C |
| Functional Temperature Range | -40°C to +85°C |
| Storage Temperature Range | -50°C to +125°C |
| Peak Reflow Temperature (JEDEC J-STD-020C) | 260°C |
| ESD Sensitivity, HBM (JESD22-A114) | 2kV |

Note:

Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

T_A = -20°C to + 85°C, unless otherwise shown.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|--------------------------------------|----------|------------|------|-----|------|-------|-------|
| Supply Voltage, Digital Core | CORE_VDD | – | 1.14 | 1.2 | 1.26 | V | – |
| Supply Voltage, Digital I/O | IO_VDD | 1.8V mode | 1.71 | 1.8 | 1.89 | V | – |
| | | 3.3V mode | 3.13 | 3.3 | 3.47 | V | – |
| Supply Voltage, PLL | PLL_VDD | – | 1.14 | 1.2 | 1.26 | V | – |
| Supply Voltage, Analog | A_VDD | – | 3.13 | 3.3 | 3.47 | V | 1 |
| Supply Voltage, Serial Digital Input | SDI_VDD | – | 3.13 | 3.3 | 3.47 | V | 1 |
| Supply Voltage, CD Buffer | BUFF_VDD | – | 3.13 | 3.3 | 3.47 | V | 1 |

Note:

1. The 3.3V supplies must track the 3.3V supply of an external EQ and external CD.

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|------------------------------------|-----------|------------------------|-----------------|-----|-----------------|-------|
| System | | | | | | |
| +1.2V Supply Current | I_{1V2} | 10bit 3G | – | 220 | 265 | mA |
| | | 20bit 3G | – | 215 | 265 | mA |
| | | 10/20bit HD | – | 175 | 215 | mA |
| | | 10/20bit SD | – | 145 | 180 | mA |
| | | DVB_ASI | – | 135 | 165 | mA |
| +1.8V Supply Current | I_{1V8} | 10bit 3G | – | 32 | 34 | mA |
| | | 20bit 3G | – | 32 | 34 | mA |
| | | 10/20bit HD | – | 20 | 21 | mA |
| | | 10/20bit SD | – | 6 | 7 | mA |
| | | DVB_ASI | – | 6 | 7 | mA |
| +3.3V Supply Current | I_{3V3} | 10bit 3G | – | 95 | 105 | mA |
| | | 20bit 3G | – | 95 | 105 | mA |
| | | 10/20bit HD | – | 65 | 75 | mA |
| | | 10/20bit SD | – | 35 | 45 | mA |
| | | DVB_ASI | – | 35 | 45 | mA |
| Total Device Power (IO_VDD = 1.8V) | P_{1D8} | 10bit 3G | – | 380 | 470 | mW |
| | | 20bit 3G | – | 350 | 435 | mW |
| | | 10/20bit HD | – | 300 | 360 | mW |
| | | 10/20bit SD | – | 235 | 305 | mW |
| | | DVB_ASI | – | 235 | 305 | mW |
| | | Reset | – | 200 | – | mW |
| | | Standby | – | 16 | 44 | mW |
| Total Device Power (IO_VDD = 3.3V) | P_{3D3} | 10bit 3G | – | 580 | 700 | mW |
| | | 20bit 3G | – | 580 | 695 | mW |
| | | 10/20bit HD | – | 430 | 530 | mW |
| | | 10/20bit SD | – | 290 | 370 | mW |
| | | DVB_ASI | – | 290 | 370 | mW |
| | | Reset | – | 220 | – | mW |
| | | Standby | – | 16 | 44 | mW |
| Digital I/O | | | | | | |
| Input Logic LOW | V_{IL} | 3.3V or 1.8V operation | IO_VSS -0.3 | – | 0.3 x IO_VDD | V |
| Input Logic HIGH | V_{IH} | 3.3V or 1.8V operation | 0.7 x IO_VDD | – | IO_VDD +0.3 | V |

Table 2-3: DC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|-----------------------------------|----------|---------------------------|--------------------------|-----------------------|---------------------------|-------|
| Output Logic LOW | V_{OL} | IOL = 5mA, 1.8V operation | – | – | 0.2 | V |
| | | IOL = 8mA, 3.3V operation | – | – | 0.4 | V |
| Output Logic HIGH | V_{OH} | IOH = 5mA, 1.8V operation | 1.4 | – | – | V |
| | | IOH = 8mA, 3.3V operation | 2.4 | – | – | V |
| Serial Input | | | | | | |
| Serial Input Common Mode Voltage | – | 50Ω load | 2.5 | SDI_VDD -(0.75/2) | SDI_VDD -(0.55/2) | V |
| Serial Output | | | | | | |
| Serial Output Common Mode Voltage | – | 50Ω load | BUFF_VD D -(0.6/2) | BUFF_VDD -(0.45/2) | BUFF_VD D -(0.35/2) | V |

Note:

The output drive strength of the digital outputs can be programmed through the host interface. Please see [Table 4-29: Video Core Configuration and Status Registers](#), register 06Dh for details.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|--|--------------------|--------------|------|-----|-------|-------|-------|
| System | | | | | | | |
| Device Latency: AUDIO_EN = 1, SMPTE mode, IOPROC_EN = 1 | - | 3G (Level A) | 80 | - | 83 | PCLK | - |
| | | 3G (Level B) | 143 | - | 151 | PCLK | - |
| | | HD | 80 | - | 83 | PCLK | - |
| | | SD | 50 | - | 55 | PCLK | - |
| Device Latency: AUDIO_EN = 0, SMPTE mode, IOPROC_EN = 1 | - | 3G (Level A) | 44 | - | 48 | PCLK | - |
| | | 3G (Level B) | 108 | - | 116 | PCLK | - |
| | | HD | 44 | - | 48 | PCLK | - |
| | | SD | 44 | - | 48 | PCLK | - |
| Device Latency: AUDIO_EN = 0, SMPTE mode, IOPROC_EN = 0 | - | 3G (Level A) | 33 | - | 36 | PCLK | - |
| | | HD | 33 | - | 36 | PCLK | - |
| | | SD | 32 | - | 35 | PCLK | - |
| Device Latency: AUDIO_EN = 0, SMPTE bypass, IOPROC_EN = 0 | - | 3G (Level A) | 6 | - | 9 | PCLK | - |
| | | HD | 6 | - | 9 | PCLK | - |
| | | SD | 5 | - | 9 | PCLK | - |
| Device Latency: DVB-ASI | - | SD | 12 | - | 16 | PCLK | - |
| Reset Pulse Width | t_{reset} | - | 1 | - | - | ms | - |
| Parallel Output | | | | | | | |
| Parallel Clock Frequency | f_{PCLK} | - | 13.5 | - | 148.5 | MHz | - |
| Parallel Clock Duty Cycle | DC_{PCLK} | - | 40 | - | 60 | % | - |

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes | |
|------------------------------|----------|------------------------------|----------|------|-----|-------|-------|----|
| Output Data Hold Time (1.8V) | t_{oh} | SPI | 1.5 | – | – | ns | 1 | |
| | | 3G 10-bit 6pF C_{LOAD} | AUDIO | 1.5 | – | – | ns | 1 |
| | | | DBUS | 0.3 | – | – | ns | 1 |
| | | | STAT | 0.3 | – | – | ns | 1 |
| | | | DBUS | 1.0 | – | – | ns | 1 |
| | | 3G 20-bit 6pF C_{LOAD} | STAT | 1.0 | – | – | ns | 1 |
| | | | DBUS | 1.0 | – | – | ns | 1 |
| | | HD 10-bit 6pF C_{LOAD} | STAT | 1.0 | – | – | ns | 1 |
| | | | DBUS | 1.0 | – | – | ns | 1 |
| | | HD 20-bit 6pF C_{LOAD} | STAT | 1.0 | – | – | ns | 1 |
| | | | DBUS | 1.0 | – | – | ns | 1 |
| | | SD 10-bit 6pF C_{LOAD} | STAT | 19.4 | – | – | ns | 1 |
| | | | DBUS | 19.4 | – | – | ns | 1 |
| | | SD 20-bit 6pF C_{LOAD} | STAT | 38.0 | – | – | ns | 1 |
| | | | DBUS | 38.0 | – | – | ns | 1 |
| | | Output Data Hold Time (3.3V) | t_{oh} | SPI | 1.5 | – | – | ns |
| 3G 10-bit 6pF C_{LOAD} | AUDIO | | | 1.5 | – | – | ns | 2 |
| | DBUS | | | 0.3 | – | – | ns | 2 |
| | STAT | | | 0.3 | – | – | ns | 2 |
| | DBUS | | | 1.0 | – | – | ns | 2 |
| 3G 20-bit 6pF C_{LOAD} | STAT | | | 1.0 | – | – | ns | 2 |
| | DBUS | | | 1.0 | – | – | ns | 2 |
| HD 10-bit 6pF C_{LOAD} | STAT | | | 1.0 | – | – | ns | 2 |
| | DBUS | | | 1.0 | – | – | ns | 2 |
| HD 20-bit 6pF C_{LOAD} | STAT | | | 1.0 | – | – | ns | 2 |
| | DBUS | | | 1.0 | – | – | ns | 2 |
| SD 10-bit 6pF C_{LOAD} | STAT | | | 19.4 | – | – | ns | 2 |
| | DBUS | | | 19.4 | – | – | ns | 2 |
| SD 20-bit 6pF C_{LOAD} | STAT | | | 38.0 | – | – | ns | 2 |
| | DBUS | | | 38.0 | – | – | ns | 2 |

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes | |
|-------------------------------|----------|------------------------------|-------|-----|------|-------|-------|---|
| Output Data Delay Time (1.8V) | t_{od} | SPI | – | – | 14.0 | ns | 3 | |
| | | 3G 10-bit 15pF C_{LOAD} | AUDIO | – | – | 7.0 | ns | 3 |
| | | | DBUS | – | – | 1.8 | ns | 3 |
| | | | STAT | – | – | 2.5 | ns | 3 |
| | | 3G 20-bit 15pF C_{LOAD} | DBUS | – | – | 3.7 | ns | 3 |
| | | | STAT | – | – | 4.4 | ns | 3 |
| | | HD 10-bit 15pF C_{LOAD} | DBUS | – | – | 3.7 | ns | 3 |
| | | | STAT | – | – | 4.4 | ns | 3 |
| | | HD 20-bit 15pF C_{LOAD} | DBUS | – | – | 3.7 | ns | 3 |
| | | | STAT | – | – | 4.4 | ns | 3 |
| | | SD 10-bit 15pF C_{LOAD} | DBUS | – | – | 22.2 | ns | 3 |
| | | | STAT | – | – | 22.2 | ns | 3 |
| | | SD 20-bit 15pF C_{LOAD} | DBUS | – | – | 41.0 | ns | 3 |
| | | | STAT | – | – | 41.0 | ns | 3 |
| Output Data Delay Time (3.3V) | t_{od} | SPI | – | – | 14.0 | ns | 4 | |
| | | 3G 10-bit 15pF C_{LOAD} | AUDIO | – | – | 7.0 | ns | 4 |
| | | | DBUS | – | – | 1.9 | ns | 4 |
| | | | STAT | – | – | 2.2 | ns | 4 |
| | | 3G 20-bit 15pF C_{LOAD} | DBUS | – | – | 3.7 | ns | 4 |
| | | | STAT | – | – | 4.1 | ns | 4 |
| | | HD 10-bit 15pF C_{LOAD} | DBUS | – | – | 3.7 | ns | 4 |
| | | | STAT | – | – | 4.1 | ns | 4 |
| | | HD 20-bit 15pF C_{LOAD} | DBUS | – | – | 3.7 | ns | 4 |
| | | | STAT | – | – | 4.1 | ns | 4 |
| | | SD 10-bit 15pF C_{LOAD} | DBUS | – | – | 22.2 | ns | 4 |
| | | | STAT | – | – | 22.2 | ns | 4 |
| | | SD 20-bit 15pF C_{LOAD} | DBUS | – | – | 41.0 | ns | 4 |
| | | | STAT | – | – | 41.0 | ns | 4 |

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes | | |
|-----------------------------------|------------------|--|---------------------------------------|-------|------|-------------------|-------|----|---|
| Output Data Rise/Fall Time (1.8V) | t_r/t_f | 3G 10-bit 6pF C_{LOAD} | STAT | – | – | 0.4 | ns | 1 | |
| | | | DBUS | – | – | 0.3 | ns | 1 | |
| | | | AUDIO | – | – | 0.6 | ns | 1 | |
| | | All other modes 6pF C_{LOAD} | STAT | – | – | 0.4 | ns | 1 | |
| | | | DBUS | – | – | 0.4 | ns | 1 | |
| | | | AUDIO | – | – | 0.6 | ns | 1 | |
| | | 3G 10-bit 15pF C_{LOAD} | STAT | – | – | 1.5 | ns | 3 | |
| | | | DBUS | – | – | 1.1 | ns | 3 | |
| | | | AUDIO | – | – | 2.3 | ns | 3 | |
| | | | All other modes 15pF C_{LOAD} | STAT | – | – | 1.5 | ns | 3 |
| | | | | DBUS | – | – | 1.4 | ns | 3 |
| | | | | AUDIO | – | – | 2.3 | ns | 3 |
| Output Data Rise/Fall Time (3.3V) | t_r/t_f | 3G 10-bit 6pF C_{LOAD} | STAT | – | – | 0.5 | ns | 2 | |
| | | | DBUS | – | – | 0.4 | ns | 2 | |
| | | | AUDIO | – | – | 0.6 | ns | 2 | |
| | | All other modes 6pF C_{LOAD} | STAT | – | – | 0.5 | ns | 2 | |
| | | | DBUS | – | – | 0.4 | ns | 2 | |
| | | | AUDIO | – | – | 0.6 | ns | 2 | |
| Output Data Rise/Fall Time (3.3V) | t_r/t_f | 3G 10-bit 15pF C_{LOAD} | STAT | – | – | 1.6 | ns | 4 | |
| | | | DBUS | – | – | 1.5 | ns | 4 | |
| | | | AUDIO | – | – | 2.2 | ns | 4 | |
| | | All other modes 15pF C_{LOAD} | STAT | – | – | 1.6 | ns | 4 | |
| | | | DBUS | – | – | 1.4 | ns | 4 | |
| | | | AUDIO | – | – | 2.2 | ns | 4 | |
| Serial Digital Input | | | | | | | | | |
| Serial Input Data Rate | DR_{SDI} | – | 0.27 | – | 2.97 | Gb/s | – | | |
| Serial Input Swing | ΔV_{SDI} | Differential with 100 Ω load | 500 | 800 | 1100 | mV _{p-p} | – | | |
| Serial Input Jitter Tolerance | IJT | Nominal loop bandwidth | Square wave mod. | 0.7 | 0.8 | – | UI | – | |

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|------------------|--------------------------------------|------|-----|------|-------------------|-------|
| Serial Digital Output | | | | | | | |
| Serial Output Data Rate | DR_{SDO} | – | 0.27 | – | 2.97 | Gb/s | – |
| Serial Output Swing | ΔV_{SDO} | Differential with 100 Ω load | 350 | – | 600 | mV _{p-p} | – |
| Serial Output Rise Time 20% ~ 80% | tr_{SDO} | – | – | – | 180 | ps | – |
| Serial Output Fall Time 20% ~ 80% | tf_{SDO} | – | – | – | 180 | ps | – |
| Serial Output Intrinsic Jitter | t_{OJ} | SMPTE colour bar 3G signal | – | – | 100 | ps | – |
| | | SMPTE colour bar HD signal | – | – | 100 | ps | – |
| | | SMPTE colour bar SD signal | – | – | 400 | ps | – |
| Serial Output Duty Cycle Distortion | DCD_{SDD} | 3G | – | 10 | – | ps | – |
| | | HD | – | 10 | – | ps | – |
| | | SD | – | 20 | – | ps | – |
| Synchronous lock time | – | – | – | – | 25 | μ s | – |
| Asynchronous lock time | – | Manual mode, noise immunity disabled | 100 | – | 350 | μ s | – |
| | | Auto mode, noise immunity disabled | 100 | – | 600 | μ s | 5 |
| | | Noise immunity enabled | 100 | – | 1200 | μ s | 5 |
| Lock time from power-up | – | After 20 minutes at -20°C | – | 325 | – | ms | – |
| GSPI | | | | | | | |
| GSPI Input Clock Frequency | f_{SCLK} | | – | – | 60 | MHz | 5 |
| GSPI Input Clock Duty Cycle | DC_{SCLK} | | 40 | 50 | 60 | % | 5 |
| GSPI Input Data Setup Time | – | | 1.5 | – | – | ns | 5 |
| GSPI Input Data Hold Time | – | | 1.5 | – | – | ns | 5 |
| GSPI Output Data Hold Time | – | 50% levels 3.3V or 1.8V operation | 1.5 | – | – | ns | 5 |
| \overline{CS} low before SCLK rising edge | – | | 1.5 | – | – | ns | 5 |
| Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle | – | | 37.1 | – | – | ns | 5 |

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|--|--------|--------------------------------------|-------|-----|-----|-------|-------|
| Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle | – | 50% levels 3.3V or 1.8V operation | 148.4 | – | – | ns | 5 |
| \overline{CS} high after SCLK falling edge | – | | 37.1 | – | – | ns | 5 |

Notes:

1. 1.89V and 0°C.
2. 3.47V and 0°C.
3. 1.71V and 85°C
4. 3.13V and 85°C
5. Timing parameters defined in [Section 4.20.3](#)

3. Input/Output Circuits

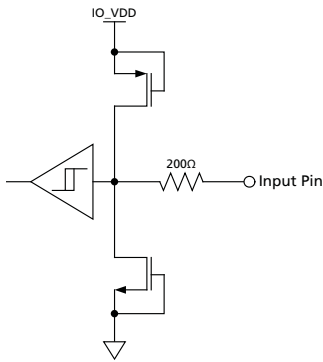


Figure 3-1: Digital Input Pin with Schmitt Trigger (20bit/10bit, $\overline{\text{AUDIO_EN/DIS}}$, $\overline{\text{CS_TMS}}$, $\overline{\text{SW_EN}}$, $\overline{\text{IOPROC_EN/DIS}}$, $\overline{\text{JTAG/HOST}}$, $\overline{\text{RC_BYP}}$, $\overline{\text{RESET_TRST}}$, $\overline{\text{SCLK_TCK}}$, $\overline{\text{SDIN_TDI}}$, $\overline{\text{SDO_EN/DIS}}$, $\overline{\text{STANDBY}}$, TIM_861)

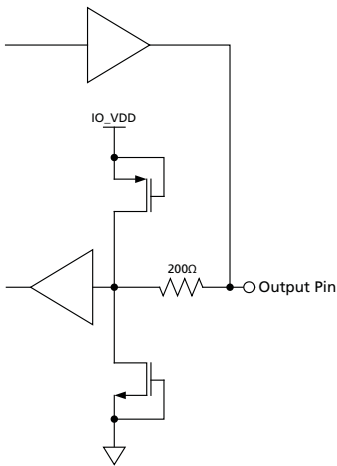


Figure 3-2: Bidirectional Digital Input/Output Pin - Configured to Output unless in Reset Mode. (ACLK, AMCLK, AOUT_1/2, AOUT_3/4, AOUT_5/6, AOUT_7/8, DVB_ASI, $\overline{\text{SMPTE_BYPASS}}$, WCLK)

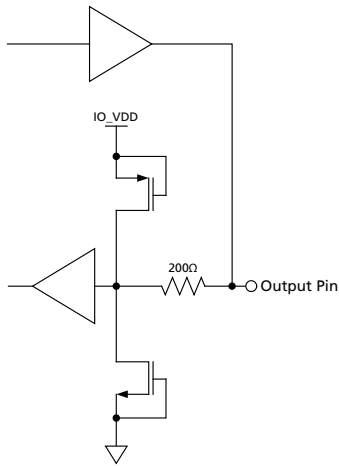


Figure 3-3: Bidirectional Digital Input/Output Pin with programmable drive strength. These pins are configured to output unless in Reset Mode; in which case they are high-impedance. The drive strength can be set by writing to address 06Dh in the host interface register. (DOUT0, DOUT1, DOUT2, DOUT3, DOUT4, DOUT5, DOUT6, DOUT7, DOUT8, DOUT9, SDOUT_TDO, STAT0, STAT1, STAT2, STAT3, STAT4, STAT5, XTAL_OUT, DOUT10, DOUT11, DOUT12, DOUT13, DOUT14, DOUT15, DOUT16, DOUT17, DOUT18, DOUT19, PCLK)

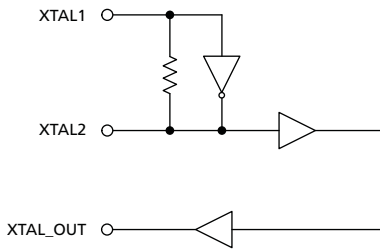


Figure 3-4: XTAL1/XTAL2/XTAL_OUT

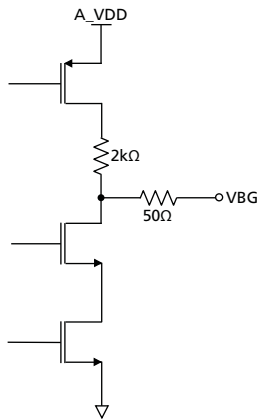


Figure 3-5: VBG

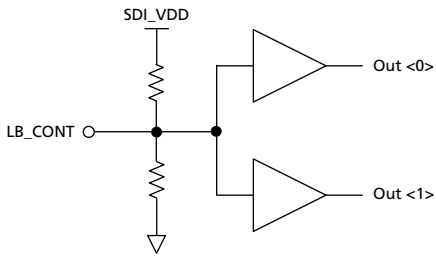


Figure 3-6: LB_CONT

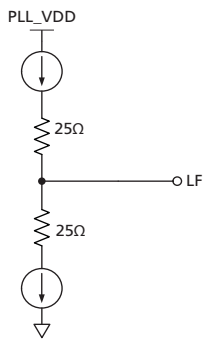


Figure 3-7: Loop Filter

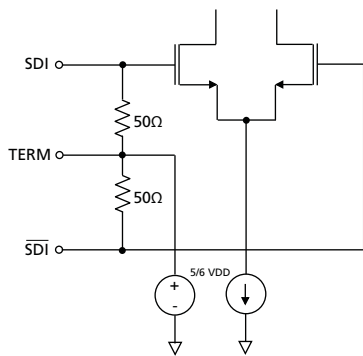


Figure 3-8: SDI/ $\overline{\text{SDI}}$ and TERM

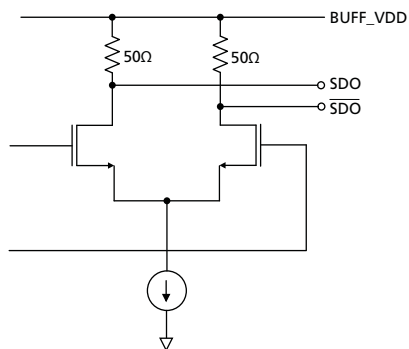


Figure 3-9: SDO/ $\overline{\text{SDO}}$

4.2.2 Level B Mapping

The 2 x 292 HD SDI interface - this can be two distinct links running at 1.5Gb/s or one 3Gb/s link formatted according to SMPTE ST 292 on two 10-bit links (Y/C interleaved). For 1080p/50/59.94/60 4:2:2 video formats, each link should be line-interleaved as per SMPTE ST 372. See [Figure 4-2](#):

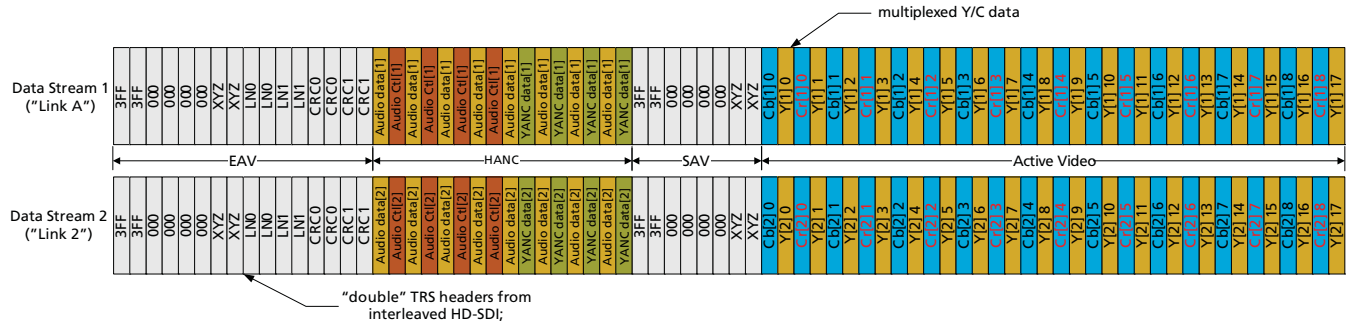


Figure 4-2: Level B Mapping

The GS2970A distinguishes between Level A and Level B mappings at 3Gb/s. When Level B data is detected, each 10-bit link is demultiplexed into its individual component streams, and most video processing features, including error detection and correction are enabled separately for Data Stream 1 and Data Stream 2 (Link A and Link B, respectively). Note that audio demultiplexing and ancillary data extraction can only be enabled for one link for 3Gb/s Level B data. Data Stream 1 or Data Stream 2 can be selected via the host interface.

4.3 Serial Digital Input

The GS2970A can accept serial digital inputs compliant with SMPTE ST 424, SMPTE ST 292 and SMPTE ST 259-C. The serial digital input buffer features 50Ω input termination and can be DC-coupled to Semtech's 3Gb/s-capable equalizers.

4.4 Serial Digital Loop-Through Output

The GS2970A contains a 100Ω differential serial output buffer which can be configured to output either a retimed or a buffered version of the serial digital input. The SDO and $\overline{\text{SDO}}$ outputs of this buffer can interface directly to a 3Gb/s-capable, SMPTE compliant Semtech cable driver. See [5.1 Typical Application Circuit](#) on page 144.

When the $\overline{\text{RC_BYP}}$ pin is set HIGH, the serial digital output is the re-timed version of the serial input.

When the $\overline{\text{RC_BYP}}$ pin is set LOW, the serial digital output is simply the buffered version of the serial input, bypassing the internal reclocker.

The output can be disabled by setting the SDO_EN/ $\overline{\text{DIS}}$ pin LOW. The output is also disabled when the STANDBY pin is asserted HIGH. When the output is disabled, both SDO and $\overline{\text{SDO}}$ pins are set to VDD and remain static.

The SDO output is muted when the $\overline{\text{RC_BYP}}$ pin is set HIGH and the PLL is unlocked (LOCKED pin is LOW). When muted, the output is held static at logic '0' or logic '1'.

Table 4-1: Serial Digital Output

| SDO_EN/ $\overline{\text{DIS}}$ | $\overline{\text{RC_BYP}}$ | SDO/ $\overline{\text{SDO}}$ |
|---------------------------------|-----------------------------|------------------------------|
| 0 | X | Disabled |
| 1 | 1 | Re-timed |
| 1 | 0 | Buffered (not re-timed) |

Note: the serial digital output is muted when the GS2970A is unlocked.

4.5 Serial Digital Reclocker

The GS2970A includes both a PLL stage and a sampling stage.

The PLL is comprised of two distinct loops:

- A coarse frequency acquisition loop sets the centre frequency of the integrated Voltage Controlled Oscillator (VCO) using an external 27MHz reference clock
- A fine frequency and phase locked loop aligns the VCO's phase and frequency to the input serial digital stream

The frequency lock loop results in a very fast lock time.

The sampling stage re-times the serial digital input with the locked VCO clock. This generates a clean serial digital stream, which may be output on the SDO/ $\overline{\text{SDO}}$ output pins and converted to parallel data for further processing. Parallel data is not affected by $\overline{\text{RC_BYP}}$. Only the SDO is affected by this pin.

4.5.1 PLL Loop Bandwidth

The fine frequency and phase lock loop in the GS2970A reclocker is non-linear. The PLL loop bandwidth scales with the jitter amplitude of the input data stream; automatically reduces bandwidth in response to higher jitter. This allows the PLL to reject more of the jitter in the input data stream and produce a very clean reclocked output.

The loop bandwidth of the GS2970A PLL is defined with 0.2UI input jitter. The bandwidth is controlled by the LB_CONT pin. Under nominal conditions, with the LB_CONT pin floating and 0.2UI input jitter applied, the loop bandwidth is set to 1/1000 of the frequency of the input data stream. Connecting the LB_CONT pin to 3.3V reduces the bandwidth to half of the nominal setting. Connecting the LB_CONT pin to GND increases the bandwidth to double the nominal setting. [Table 4-2](#) below summarizes this information.

Table 4-2: PLL Loop Bandwidth

| Input Data Rate | LB_CONT Pin Connection | Loop Bandwidth (MHz) ¹ |
|-----------------|------------------------|-----------------------------------|
| SD | 3.3V | 0.135 |
| | Floating | 0.27 |
| | 0V | 0.54 |
| HD | 3.3V | 0.75 |
| | Floating | 1.5 |
| | 0V | 3.0 |
| 3G | 3.3V | 1.5 |
| | Floating | 3.0 |
| | 0V | 6.0 |

¹Measured with 0.2UI input jitter applied

4.6 External Crystal/Reference Clock

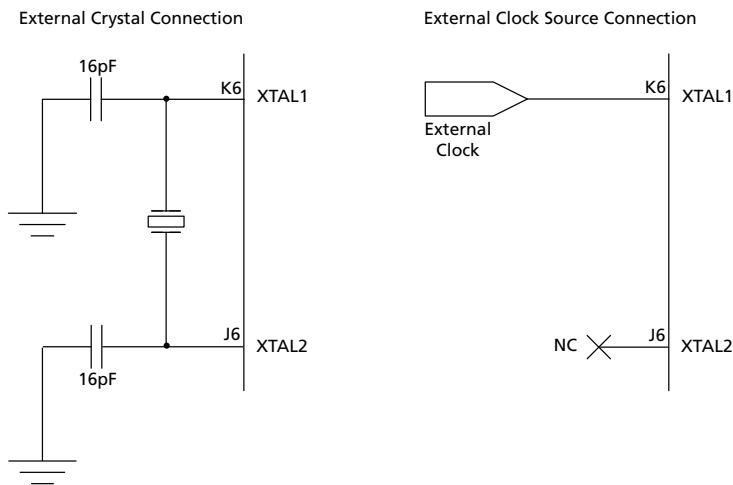
The GS2970A requires an external 27MHz reference clock for correct operation. This reference clock is generated by connecting a crystal to the XTAL1 and XTAL2 pins of the device. See [Application Reference Design on page 144](#). Table 4-3 shows XTAL characteristics.

Alternately, a 27MHz external clock source can be connected to the XTAL1 pin of the device, as shown in [Figure 4-3](#).

The frequency variation of the crystal including aging, supply and temperature variation, should be less than +/-100ppm.

The equivalent series resistance (or motional resistance) should be a maximum of 50Ω.

The external crystal is used in the frequency acquisition process. It has no impact on the output jitter performance of the part when the part is locked to incoming data. Because of this, the only key parameter is the frequency variation of the crystal that is stated above.



Notes:

1. Capacitor values listed represent the total capacitance, including discrete capacitance and parasitic board capacitance.
2. XTAL1 serves as an input, which may alternatively accept a 27MHz clock source.

Figure 4-3: 27MHz Clock Sources

Table 4-3: Input Clock Requirements

| Parameter | Min | Typ | Max | Units |
|---|--------------|-----|---------------|-------|
| XTAL1 Low Level Input Voltage (V_{il}) | – | – | 20% of VDD_IO | V |
| XTAL1 High Level Input Voltage (V_{ih}) | 80% of VDDIO | – | – | V |
| XTAL1 Input Slew Rate | 2 | – | – | V/ns |
| XTAL1 to XOUT Prop. Delay (High to Low) | 1.3 | 1.5 | 2.3 | ns |
| XTAL1 to XOUT Prop. Delay (Low to High) | 1.3 | 1.6 | 2.3 | ns |

Note:

Valid when the cell is used to buffer an external clock source which is connected to the XTAL1 pin, then nothing should be connected to the XTAL2 pin.

4.7 Lock Detect

The LOCKED output signal is available by default on the STAT3 output pin, but may be programmed to be output through any one of the six programmable multi-functional pins of the device: STAT[5:0].

The LOCKED output signal is set HIGH by the Lock Detect block under the following conditions:

Table 4-4: Lock Detect Conditions

| Mode of Operation | Mode Setting | Condition for Locked |
|---|--|---|
| Data-Through Mode | $\overline{\text{SMPTE_BYPASS}} = \text{LOW}$ $\text{DVB_ASI} = \text{LOW}$ | Reclocker PLL is locked. |
| SMPTE Mode | $\overline{\text{SMPTE_BYPASS}} = \text{HIGH}$ $\text{DVB_ASI} = \text{LOW}$ | Reclocker PLL is locked. Two consecutive TRS words are detected in a two-line window. |
| SMPTE Mode with Lock Noise-Immunity Enabled | $\overline{\text{SMPTE_BYPASS}} = \text{HIGH}$ $\text{DVB_ASI} = \text{LOW}$ Bit 0x085[10] set to 1 $\text{AUTO}/\overline{\text{MAN}} = \text{HIGH}$ | Reclocker PLL is locked. Two consecutive TRS words are detected in a two-line window. The last two detected TRS words must have the same alignment. Note: Auto mode only. Not supported in Manual mode. |
| DVB_ASI Mode | $\overline{\text{SMPTE_BYPASS}} = \text{LOW}$ $\text{DVB_ASI} = \text{HIGH}$ Bit $\text{AUTO}/\overline{\text{MAN}} = \text{LOW}$ | Reclocker PLL is locked. 32 consecutive DVB_ASI words with no errors are detected within a 128-word window. |

Note 1: The part will lock into ASI in Auto mode, but could falsely unlock for some ASI input patterns.

Note 2: In Standby mode, the reclocker PLL unlocks. However, the LOCKED signal retains whatever state it previously held. So, if before Standby assertion, the LOCKED signal is HIGH, then during standby, it remains HIGH regardless of the status of the PLL.

4.7.1 Asynchronous Lock

The lock detection algorithm is a continuous process, beginning at device power-up or after a system reset. It continues until the device is powered down or held in reset.

The device first determines if a valid serial digital input signal has been presented to the device. If no valid serial data stream has been detected, the serial data into the device is considered invalid, and the LOCKED signal is LOW.

Once a valid input signal has been detected, the asynchronous lock algorithm enters a “hunt” phase, in which the device attempts to detect the presence of either TRS words or DVB-ASI sync words.

By default, the device powers up in auto mode (the $\text{AUTO}/\overline{\text{MAN}}$ bit in the host interface is set HIGH). In this mode, the device operating frequency toggles between 3G, HD and SD rates as it attempts to lock to the incoming data rate. The PCLK output continues to operate, and the frequency may switch between 148.5MHz, 74.25MHz, 27MHz and 13.5MHz.

When the device is operating in manual mode (AUTO/ $\overline{\text{MAN}}$ bit in the host interface is LOW), the operating frequency needs to be set through the host interface using the RATE_DET[1:0] bits. In this mode, the asynchronous lock algorithm does not toggle the operating rate of the device and attempts to lock within a single standard. Lock is achieved within three lines of the selected standard.

4.7.2 Signal Interruption

The device tolerates a signal interruption of up to 10 μ s without unlocking, as long as no TRS words are deleted by this interruption. If a signal interruption of greater than 10 μ s is detected, the lock detection algorithm may lose the current data rate, and LOCKED will de-assert until the data rate is re-acquired by the lock detection block.

4.8 SMPTE Functionality

4.8.1 Descrambling and Word Alignment

The GS2970A performs NRZI to NRZ decoding and data descrambling according to SMPTE ST 424/SMPTE ST 292/SMPTE ST 259-C and word aligns the data to TRS sync words.

When operating in manual mode (AUTO/ $\overline{\text{MAN}}$ = LOW), the device only carries out SMPTE decoding, descrambling and word alignment when the $\overline{\text{SMPTE_BYPASS}}$ pin is set HIGH and the DVB_ASI pin is set LOW.

When operating in Auto mode (AUTO/ $\overline{\text{MAN}}$ = HIGH), the GS2970A carries out descrambling and word alignment to enable the detection of TRS sync words. When two consecutive valid TRS words (SAV and EAV), with the same bit alignment have been detected, the device word-aligns the data to the TRS ID words.

TRS ID word detection is a continuous process. The device remains in SMPTE mode until TRS ID words fail to be detected.

Note 1: Both 8-bit and 10-bit TRS headers are identified by the device.

Note 2: In 3G Level B mode, the device only supports Data Stream 1 and Data Stream 2 having the same bit width (i.e. both data streams contain 8-bit data, or both data streams contain 10-bit data). If the bit widths between the two data streams are different, the GS2970A cannot word align the input stream, and switches in Data-Through mode.

4.9 Parallel Data Outputs

The parallel data outputs are aligned to the rising edge of the PCLK.

4.9.1 Parallel Data Bus Buffers

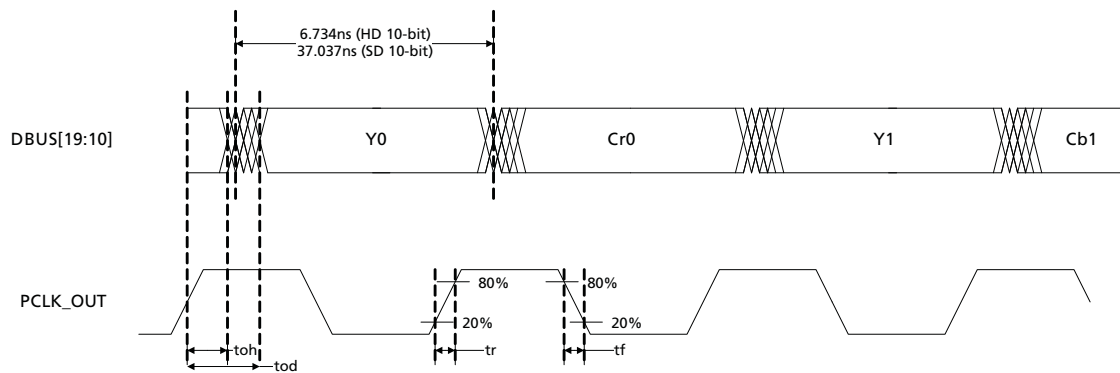
The parallel data bus, status signal outputs and control signal input pins are all connected to high-impedance buffers.

The device supports 1.8 or 3.3V (LVTTTL and LVCMOS levels) supplied at the IO_VDD and IO_GND pins.

All output buffers (including the PCLK output), are set to high-impedance in Reset mode ($\overline{\text{RESET_TRST}} = \text{LOW}$).

I/O Timing Specs:

10-bit SDR Mode:



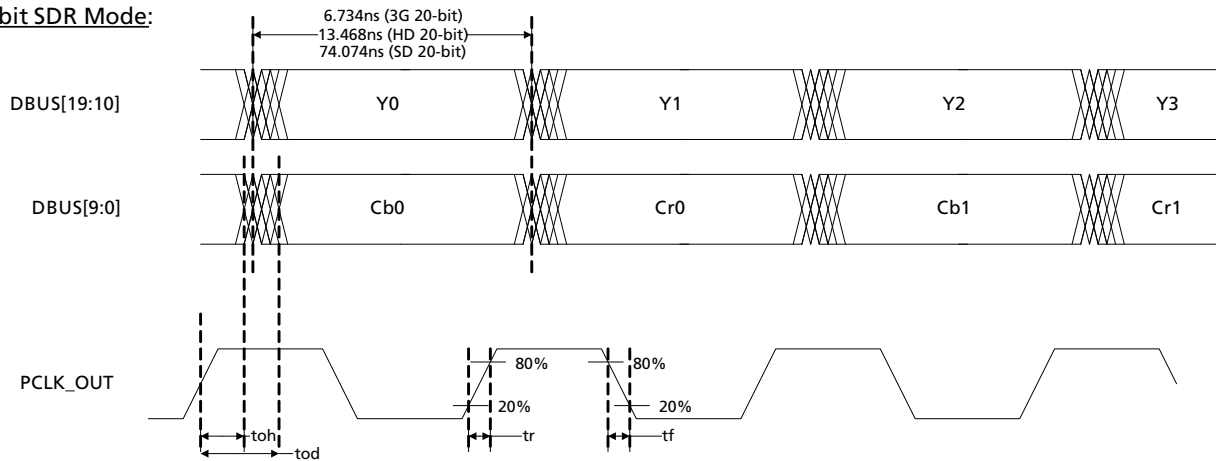
| 10bHD Mode | | | | | | | | | | | | |
|------------|---------|-------------|-------------------|---------|-------------|-------------------|---------|-------------|-------------------|---------|-------------|-------------------|
| | 3.3V | | | | | | 1.8V | | | | | |
| | toh | tr/tf (min) | C _{load} | tod | tr/tf (max) | C _{load} | toh | tr/tf (min) | C _{load} | tod | tr/tf (max) | C _{load} |
| dbus | 1.000ns | 0.400ns | 6 pF | 3.700ns | 1.400ns | 15 pF | 1.000ns | 0.400ns | 6 pF | 3.700ns | 1.400ns | 15 pF |
| stat | 1.000ns | 0.500ns | | 4.100ns | 1.600ns | | 1.000ns | 0.400ns | | 4.400ns | 1.500ns | |

| 10bSD Mode | | | | | | | | | | | | |
|------------|----------|-------------|-------------------|----------|-------------|-------------------|----------|-------------|-------------------|----------|-------------|-------------------|
| | 3.3V | | | | | | 1.8V | | | | | |
| | toh | tr/tf (min) | C _{load} | tod | tr/tf (max) | C _{load} | toh | tr/tf (min) | C _{load} | tod | tr/tf (max) | C _{load} |
| dbus | 19.400ns | 0.400ns | 6 pF | 22.200ns | 1.400ns | 15 pF | 19.400ns | 0.400ns | 6 pF | 22.200ns | 1.400ns | 15 pF |
| stat | 19.400ns | 0.500ns | | 22.200ns | 1.600ns | | 19.400ns | 0.400ns | | 22.200ns | 1.500ns | |

Figure 4-4: PCLK to Data and Control Signal Output Timing - SDR Mode 1

I/O Timing Specs:

20-bit SDR Mode:



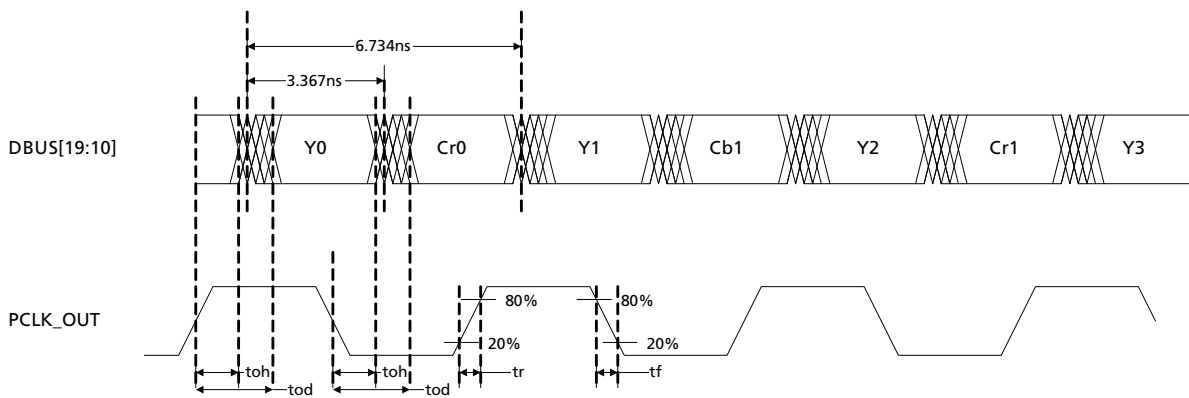
| 20b3G and 20bHD Modes | | | | | | | | | | | | |
|-----------------------|---------|-------------|-------------------|---------|-------------|-------------------|---------|-------------|-------------------|---------|-------------|-------------------|
| | 3.3V | | | | | | 1.8V | | | | | |
| | toh | tr/tf (min) | C _{load} | tod | tr/tf (max) | C _{load} | toh | tr/tf (min) | C _{load} | tod | tr/tf (max) | C _{load} |
| dbus | 1.000ns | 0.400ns | 6 pF | 3.700ns | 1.400ns | 15 pF | 1.000ns | 0.400ns | 6 pF | 3.700ns | 1.400ns | 15 pF |
| stat | 1.000ns | 0.500ns | | 4.100ns | 1.600ns | | 1.000ns | 0.400ns | | 4.400ns | 1.500ns | |

| 20bSD Mode | | | | | | | | | | | | |
|------------|----------|-------------|-------------------|----------|-------------|-------------------|----------|-------------|-------------------|----------|-------------|-------------------|
| | 3.3V | | | | | | 1.8V | | | | | |
| | toh | tr/tf (min) | C _{load} | tod | tr/tf (max) | C _{load} | toh | tr/tf (min) | C _{load} | tod | tr/tf (max) | C _{load} |
| dbus | 38.000ns | 0.400ns | 6 pF | 41.000ns | 1.400ns | 15 pF | 38.000ns | 0.400ns | 6 pF | 41.000ns | 1.400ns | 15 pF |
| stat | 38.000ns | 0.500ns | | 41.000ns | 1.600ns | | 38.000ns | 0.400ns | | 41.000ns | 1.500ns | |

Figure 4-5: PCLK to Data and Control Signal Output Timing - SDR Mode 2

I/O Timing Specs:

DDR Mode:



| 10b3G Mode | | | | | | | | | | | | |
|------------|---------|-------------|-------------------|---------|-------------|-------------------|---------|-------------|-------------------|---------|-------------|-------------------|
| | 3.3V | | | | | | 1.8V | | | | | |
| | toh | tr/tf (min) | C _{load} | tod | tr/tf (max) | C _{load} | toh | tr/tf (min) | C _{load} | tod | tr/tf (max) | C _{load} |
| dbus | 0.450ns | 0.400ns | 6 pF | 1.900ns | 1.500ns | 15 pF | 0.400ns | 0.300ns | 6 pF | 1.800ns | 1.100ns | 15 pF |
| stat | 0.450ns | 0.500ns | | 2.200ns | 1.600ns | | 0.450ns | 0.400ns | | 2.500ns | 1.500ns | |

Figure 4-6: PCLK to Data and Control Signal Output Timing - DDR Mode

The GS2970A has a 20-bit output parallel bus, which can be configured for different output formats as shown in Table 4-5.

Table 4-5: GS2970A Output Video Data Format Selections

| Output Data Format | Pin/Register Bit Settings | | | | | DOUT[9:0] | DOUT[19:10] |
|----------------------------------|---------------------------|-----------|-----------|--------------|---------|--|--------------------------------------|
| | 20BIT /10BIT | RATE_SELO | RATE_SEL1 | SMPTE_BYPASS | DVB-ASI | | |
| 20-bit demultiplexed HD format | HIGH | LOW | LOW | HIGH | LOW | Chroma | Luma |
| 20-bit data output HD format | HIGH | LOW | LOW | LOW | LOW | DATA | DATA |
| 20-bit demultiplexed SD format | HIGH | HIGH | X | HIGH | LOW | Chroma | Luma |
| 20-bit data output SD format | HIGH | HIGH | X | LOW | LOW | DATA | DATA |
| 10-bit multiplexed 3G DDR format | LOW | LOW | HIGH | HIGH | LOW | Driven LOW | Data Stream One/ Data Stream Two* |
| 10-bit multiplexed HD format | LOW | LOW | LOW | HIGH | LOW | Driven LOW | Luma/Chroma |
| 10-bit data output HD format | LOW | LOW | LOW | LOW | LOW | Driven LOW | DATA |
| 10-bit multiplexed SD format | LOW | HIGH | X | HIGH | LOW | Driven LOW | Luma/Chroma |
| 10-bit data output SD format | LOW | HIGH | X | LOW | LOW | Driven LOW | DATA |
| 20-bit demultiplexed 3G format | HIGH | LOW | HIGH | HIGH | LOW | Data Stream Two* | Data Stream One* |
| DVB-ASI format | LOW | HIGH | X | – | HIGH | DOUT19 = WORD_ERR DOUT18 = SYNC_OUT DOUT17 = H_OUT DOUT16 = G_OUT DOUT15 = F_OUT DOUT14 = E_OUT DOUT13 = D_OUT DOUT12 = C_OUT DOUT11 = B_OUT DOUT10 = A_OUT | |

*In 3G Mode, the data streams can be swapped at the output through the host interface.

Note: When in Auto Mode, swap RATE_SEL with RATE_DET.

4.9.2 Parallel Output in SMPTE Mode

When the device is operating in SMPTE mode ($\overline{\text{SMPTE_BYPASS}} = \text{HIGH}$ and $\text{DVB_ASI} = \text{LOW}$), data is output in either Multiplexed or Demultiplexed form depending on the setting of the $20\text{bit}/\overline{10\text{bit}}$ pin.

When operating in 20-bit mode ($20\text{bit}/\overline{10\text{bit}} = \text{HIGH}$), the output data is demultiplexed Luma and Chroma data for SD and HD data rates, and Data Stream 1 and Data Stream 2 for the 3G data.

When operating in 10-bit mode ($20\text{bit}/\overline{10\text{bit}} = \text{LOW}$), the output data is multiplexed Luma and Chroma data for SD and HD data rates, and multiplexed Data Stream 1 and Data Stream 2 for the 3G data. In this mode, the data is presented on the $\text{DOUT}[19:10]$ pins, with $\text{DOUT}[9:0]$ being forced LOW.

4.9.3 Parallel Output in DVB-ASI Mode

In DVB-ASI mode, the $20\text{bit}/\overline{10\text{bit}}$ pin must be set LOW to configure the output parallel bus for 10-bit operation.

DVB-ASI mode is enabled when the $\text{AUTO}/\overline{\text{MAN}}$ bit is LOW, $\overline{\text{SMPTE_BYPASS}}$ pin is LOW and the DVB_ASI pin is HIGH.

The extracted 8-bit data is presented on $\text{DOUT}[17:10]$ such that $\text{DOUT}[17:10] = \text{HOUT} \sim \text{AOUT}$, where AOUT is the least significant bit of the decoded transport stream data.

In addition, the $\text{DOUT}19$ and $\text{DOUT}18$ pins are configured as DVB-ASI status signals WORDERR and SYNCOUT respectively.

SYNCOUT is HIGH whenever a K28.5 sync character is output from the device.

WORDERR is HIGH whenever the device has detected a running disparity error or illegal code word.

4.9.4 Parallel Output in Data-Through Mode

This mode is enabled when the $\overline{\text{SMPTE_BYPASS}}$ and DVB_ASI pins are LOW.

In this mode, data is passed to the output bus without any decoding, descrambling or word-alignment.

The output data width (10-bit or 20-bit) is controlled by the setting of the $20\text{bit}/\overline{10\text{bit}}$ pin.

Note: In order to use Data-Through Mode, a 3G-B input signal must not be connected at the input of the device when the switch is made from Auto Mode to Data-Through Mode.

4.9.5 Parallel Output Clock (PCLK)

The frequency of the PCLK output signal of the GS2970A is determined by the output data rate and the $20\text{bit}/\overline{10\text{bit}}$ pin setting. Table 4-6 lists the output signal formats according to the data format selected in Manual mode ($\text{AUTO}/\overline{\text{MAN}}$ bit in the host interface is set LOW), or detected in Auto mode ($\text{AUTO}/\overline{\text{MAN}}$ bit in the host interface is set HIGH).

Table 4-6: GS2970A PCLK Output Rates

| Output Data Format | Pin/Control Bit Settings | | | | | PCLK Rate |
|----------------------------------|--------------------------|-----------|-----------|------------------------|---------|-------------------------|
| | 20bit/ 10bit | RATE_DET0 | RATE_DET1 | <u>SMPTE</u> BYPASS | DVB-ASI | |
| 20-bit demultiplexed HD format | HIGH | LOW | LOW | HIGH | LOW | 74.25 or 74.25/1.001MHz |
| 20-bit data output HD format | HIGH | LOW | LOW | LOW | LOW | 74.25 or 74.25/1.001MHz |
| 20-bit demultiplexed SD format | HIGH | HIGH | X | HIGH | LOW | 13.5MHz |
| 20-bit data output SD format | HIGH | HIGH | X | LOW | LOW | 13.5MHz |
| 20-bit demultiplexed 3G format | HIGH | LOW | HIGH | HIGH | LOW | 148.5 or 148.5/1.001MHz |
| 10-bit multiplexed 3G DDR format | LOW | LOW | HIGH | HIGH | LOW | 148.5 or 148.5/1.001MHz |
| 10-bit multiplexed HD format | LOW | LOW | LOW | HIGH | LOW | 148.5 or 148.5/1.001MHz |
| 10-bit data output HD format | LOW | LOW | LOW | LOW | LOW | 148.5 or 148.5/1.001MHz |
| 10-bit multiplexed SD format | LOW | HIGH | X | HIGH | LOW | 27MHz |
| 10-bit data output SD format | LOW | HIGH | X | LOW | LOW | 27MHz |
| 10-bit ASI output SD format | LOW | HIGH | X | LOW | HIGH | 27MHz |

4.9.6 DDR Parallel Clock Timing

The GS2970A has the ability to transmit 10-bit parallel video data with a DDR (Dual Data Rate) pixel clock over a single-ended interface. DDR Mode can be enabled when the SDI data bandwidth is 3Gb/s. In this case, the 10-bit parallel data rate is 297Mb/s, and the frequency of the DDR clock is 148.5MHz (10-bit output in 3G mode).

The DDR pixel clock avoids the need to operate a high-drive pixel clock at 297MHz. This reduces power consumption, clock drive strength, and noise generation, and precludes from generating excessive EMI had PCLK on the board have to run at 297MHz. It also enables easier board routing and avoids the need to use the higher-speed I/Os on FPGAs, which may require more expensive speed grades.

Figure 4-7 and Figure 4-8 show how the DDR interface operates. The pixel clock is transmitted at half the data rate, and the interleaved data is sampled at the receiver on both clock edges.

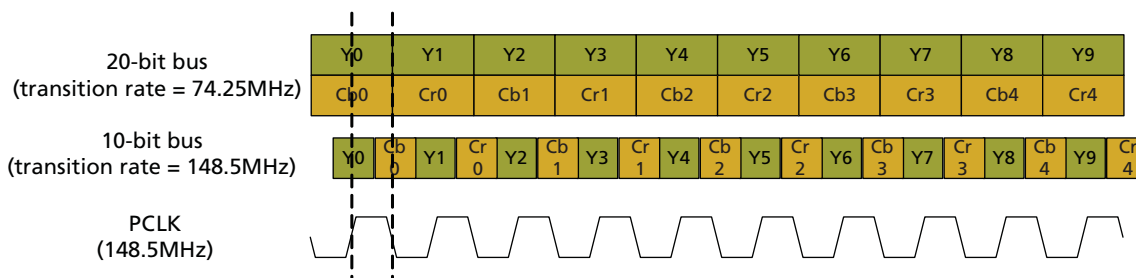


Figure 4-7: DDR Video Interface - 3G Level A

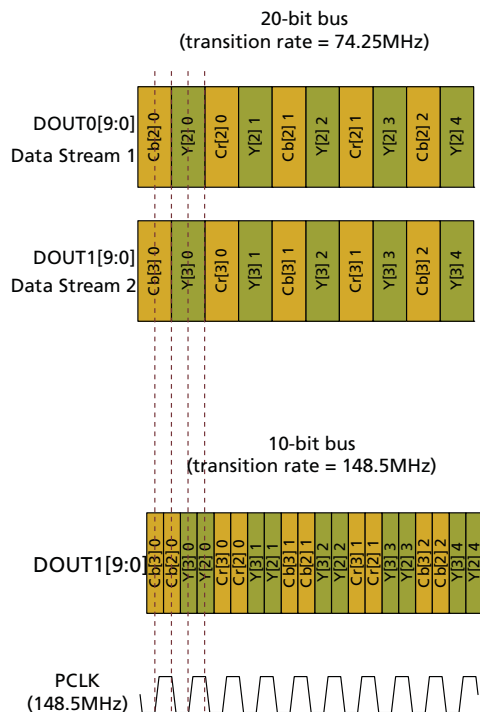


Figure 4-8: DDR Video Interface - 3G Level B

The GS2970A has the ability to shift the Setup/Hold window on the receive interface, by using an on-chip delay line to shift the phase of PCLK with respect to the data bus.

The timing of the PCLK output, relative to the data, can be adjusted through the host interface registers. Address 06Ch contains the delay line controls:

Bit[5] (DEL_LINE_CLK_SEL) is a coarse delay adjustment that selects between the default (nominal) PCLK phase and a quadrature phase, for a 90° phase shift.

Bits[4:0] (DEL_LINE_OFFSET) comprise a fine delay adjustment to shift the PCLK in 40ps increments (typical conditions). The maximum fine delay adjustment is approximately 1.2ns under nominal conditions.

An example delay adjustment over min/typ/max conditions is illustrated in Figure 4-9. The target delay is 0.84ns under typical conditions (approximately 45° PCLK phase shift), and requires a control word setting of 0x0014 for address 0x006C.

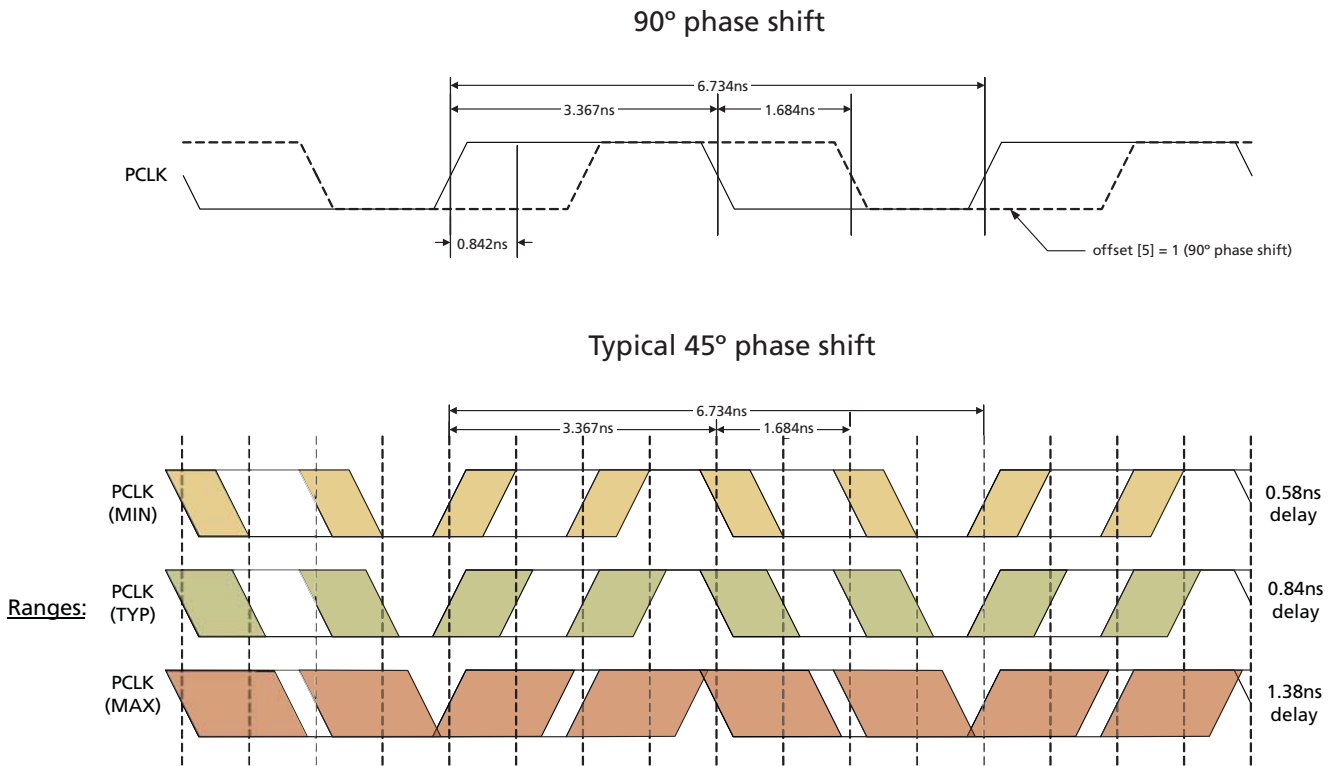


Figure 4-9: Delay Adjustment Ranges

4.10 Timing Signal Generator

The GS2970A has an internal timing signal generator which is used to generate digital FVH timing reference signals, to detect and correct certain error conditions and automatic video standard detection.

The timing signal generator is only operational in SMPTE mode ($\overline{\text{SMPTE_BYPASS}} = \text{HIGH}$).

The timing signal generator consists of a number of counters and comparators operating at video pixel and video line rates. These counters maintain information about the total line length, active line length, total number of lines per field/frame and total active lines per field/frame for the received video standard.

It takes one video frame to obtain full synchronization to the received video standard.

Note: Both 8-bit and 10-bit TRS words are identified by the device. Once synchronization has been achieved, the timing signal generator continues to monitor the received TRS timing information to maintain synchronization.

The timing signal generator re-synchronizes all pixel and line based counters on every received TRS ID. Note that for correct operation of the timing signal generator, the SW_EN input pin must be set LOW, unless manual synchronous switching is enabled (Section 4.10.1).

4.10.1 Manual Switch Line Lock Handling

The principle of switch line lock handling is that the switching of synchronous video sources will only disturb the horizontal timing and alignment, whereas the vertical timing remains in synchronization - i.e. switching between video sources of the same format.

To account for the horizontal disturbance caused by a synchronous switch, the word alignment block and timing signal generator automatically re-synchronizes to the new timing immediately if the synchronous switch happens during the designated switch line, as defined in SMPTE recommended practice RP168-2002.

The device samples the SW_EN pin on every PCLK cycle. When a Logic LOW to HIGH transition on this pin is detected anywhere within the active line, the word alignment block and timing signal generator re-synchronize immediately to the next TRS word.

This allows the system to force immediate lock on any line, if the switch point is non-standard.

To ensure proper switch line lock handling, the SW_EN signal should be asserted HIGH anywhere within the active portion of the line on which the switch has taken place, and should be held HIGH for approximately one video line. After this time period, SW_EN should be de-asserted. SW_EN should be held LOW during normal device operation.

Note: It is the rising edge of the SW_EN signal, which generates the switch line lock re-synchronization. This edge must be in the active portion of the line containing the video switch point.

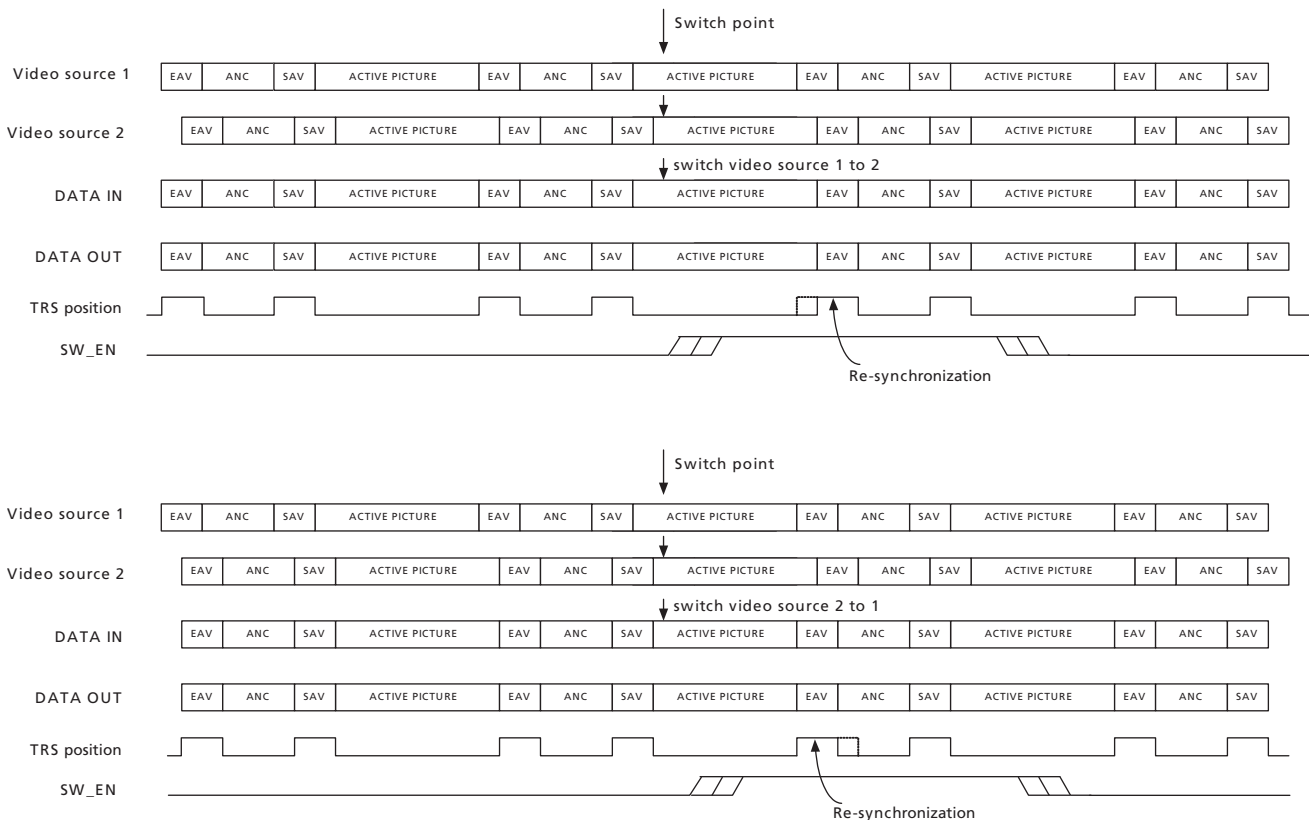


Figure 4-10: Switch Line Locking on a Non-Standard Switch Line

4.10.2 Automatic Switch Line Lock Handling

The synchronous switch point is defined for all major video standards in SMPTE RP168-2002. The device automatically re-synchronizes the word alignment block and timing signal generator at the switch point, based on the detected video standard.

The device, as described in [Section 4.10.1](#) and [Figure 4-10](#) above, implements the re-synchronization process automatically, every field/frame. The switch line is defined as follows:

- For 525 line interlaced systems: resynchronization takes place at then end of lines 10 & 273
- For 525 line progressive systems: resynchronization takes place at then end of line 10
- For 625 line interlaced systems: resynchronization takes place at then end of lines 6 & 319
- For 625 line progressive systems: resynchronization takes place at then end of line 6
- For 750 line progressive systems: resynchronization takes place at then end of line 7
- For 1125 line interlaced systems: resynchronization takes place at then end of lines 7 & 568
- For 1125 line progressive systems: resynchronization takes place at then end of line 7

Note: Unless indicated by SMPTE ST 352 payload identifier packets, the GS2970A does not distinguish between 1125-line progressive segmented-frame (PsF) video and 1125-line interlaced video operating at 25 or 30fps. However, PsF video operating at 24fps is detected by the device.

A full list of all major video standards and switching lines is shown in [Table 4-7](#).

4.10.3 Switch Line Lock Handling During Level B to Level A Conversion

When 3G data is detected by the GS2970A, and Level B to Level A conversion is enabled, the device only supports a limited phase offset between two synchronous video sources if a synchronous switch is implemented.

If the synchronous switch point results in an “extended” active video period, the GS2970A only re-synchronizes to the following TRS ID if the phase difference between the two sources is less than or equal to 10 μ s. If the phase difference is greater than 10 μ s, the GS2970A takes one additional line to re-synchronize. In this case, the user may observe a missing H pulse on the line following the switch line, on the H timing output.

Note that this 10 μ s constraint is only valid when Level B to Level A conversion is enabled, and only when the synchronous switch point results in an extended active video area.

Table 4-7: Switch Line Position for Digital Systems

| System | Frame Rate & Structure | Pixel Structure | | Signal Standard | Parallel Interface | Serial Interface | Line No. |
|--------|------------------------|-----------------|---------|-----------------|--------------------|------------------|----------|
| 1125 | 60/P | 1920x1080 | 4:2:2 | ST 274 + RP211 | | ST 292 | 7 |
| | 50/P | | | ST 274 + RP211 | | | |
| | 60/I | | | ST 274 + RP211 | | | 7/569 |
| | 50/I | | | ST 274 + RP211 | | | |
| | 30/P | | | ST 274 + RP211 | | | 7 |
| | 25/P | | | ST 274 + RP211 | | | |
| | 24/P | | | ST 274 + RP211 | | | |
| | 30/PsF | | | ST 274 + RP211 | | | |
| | 25/PsF | | | ST 274 + RP211 | | | |
| | 24/PsF | | | ST 274 + RP211 | | | |
| 750 | 60/P | 1280x720 | 4:2:2 | ST 296 | | ST 292 | 7 |
| | 50/P | | | ST 296 | | | |
| | 30/P | | | ST 296 | | | |
| | 25/P | | | ST 296 | | | |
| | 24/P | | | ST 296 | | | |
| 625 | 50/P | 720x576 | 4:2:2 | BT.1358 | ST 349 | ST 292 | 6 |
| | | | | BT.1358 | ST 347 | ST 344 | |
| | | | | BT.1358 | BT.1358 | BT.1362 | |
| | | | 4:2:0 | BT.1358 | ST 349 | ST 292 | |
| | | | | BT.1358 | BT.1358 | BT.1362 | |
| | 50/I | 960x576 | 4:2:2 | BT.601 | ST 349 | ST 292 | 6/319 |
| | | | | BT.601 | BT.656 | ST 259 | |
| | | 720x576 | 4:4:4:4 | BT.799 | ST 349 | ST 292 | |
| | | | | BT.799 | ST 347 | ST 344 | |
| | | | | BT.799 | BT.799 | ST 344 | |
| | | | BT.799 | BT.799 | – | | |
| | | | 4:2:2 | BT.601 | ST 349 | ST 292 | |
| BT.601 | ST 125 | ST 259 | | | | | |

Table 4-7: Switch Line Position for Digital Systems (Continued)

| System | Frame Rate & Structure | Pixel Structure | | Signal Standard | Parallel Interface | Serial Interface | Line No. |
|---------|------------------------|-----------------|---------|-----------------|--------------------|------------------|----------|
| 525 | 59.94/P | 720x483 | 4:2:2 | ST 293 | ST 349 | ST 292 | 10 |
| | | | | ST 293 | ST 347 | ST 344 | |
| | | | | ST 293 | ST 293 | ST 294 | |
| | | 4:2:0 | ST 293 | ST 349 | ST 292 | | |
| | | | ST 293 | ST 293 | ST 294 | | |
| | | | 960x483 | 4:2:2 | ST 267 | ST 349 | |
| | ST 267 | ST 267 | | | ST 259 | | |
| | 4:4:4 | ST 267 | | ST 349 | ST 292 | | |
| | | ST 267 | | ST 347 | ST 344 | | |
| | | ST 267 | | RP174 | ST 344 | | |
| | | ST 267 | | RP175 | RP175 | | |
| | 4:2:2 | ST 125 | ST 349 | ST 292 | | | |
| ST 125 | | ST 125 | ST 259 | | | | |
| HD-SDTI | P or PsF structure | 1920x1080 | 4:2:2 | ST 274 | ST 274 + ST 348 | ST 292 | 7 |
| | I structure | | | ST 274 | | | 7/569 |
| | P structure | 1280x720 | | ST 296 | ST 296 + ST 348 | | 7 |
| SDTI | 50/I | 720x576 | 4:2:2 | BT.656 | BT.656 + ST 305 | ST 259 | 6/319 |
| | 59.94/I | 720x483 | | ST 125 | ST 125 + ST 305 | | 10/273 |

4.11 Programmable Multi-function Outputs

The GS2970A has six multi-function output pins, STAT[5:0], which are programmable via the host interface to output one of the following signals:

Table 4-8: Output Signals Available on Programmable Multi-Function Pins

| Status Signal | Selection Code | Default Output Pin |
|---|----------------|--------------------|
| H/HSYNC (according to TIM_861 Pin) Section 4.12 | 0000 | STAT 0 |
| V/VSNC (according to TIM_861 Pin) Section 4.12 | 0001 | STAT 1 |
| F/DE (according to TIM_861 Pin) Section 4.12 | 0010 | STAT 2 |
| LOCKED Section 4.7 | 0011 | STAT 3 |
| Y/1ANC Section 4.17 | 0100 | STAT 4 |
| C/2ANC Section 4.17 | 0101 | - |

Table 4-8: Output Signals Available on Programmable Multi-Function Pins (Continued)

| Status Signal | Selection Code | Default Output Pin |
|---|----------------|--------------------|
| DATA ERROR Section 4.16 | 0110 | STAT 5 |
| VIDEO ERROR | 0111 | – |
| AUDIO ERROR | 1000 | – |
| EDH DETECTED | 1001 | – |
| CARRIER DETECT | 1010 | – |
| RATE_DET0 | 1011 | – |
| RATE_DET1 | 1100 | – |

Note:

Each of the STAT[5:0] pins are configurable individually using the register bits in the host interface; STAT[5:0]_CONFIG (008h/009h).

4.12 H:V:F Timing Signal Generation

The GS2970A extracts critical timing parameters from the received TRS words.

Horizontal blanking (H), Vertical blanking (V), and Field odd/even (F) timing are output on the STAT[2:0] pins by default.

Using the H_CONFIG bit in the host interface, the H signal timing can be selected as one of the following:

1. Active line blanking (H_CONFIG = LOW) - the H output is HIGH for the horizontal blanking period, including the EAV TRS words.
2. TRS based blanking (H_CONFIG = HIGH) - the H output is set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS signals.

The timing of these signals is shown in the figures below.

Note: Both 8-bit and 10-bit TRS words are identified by the device.

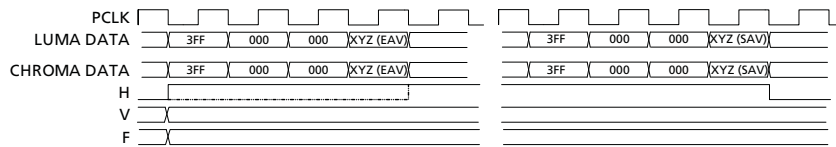


Figure 4-11: H:V:F Output Timing - 3G Level A and HDTV 20-bit Mode

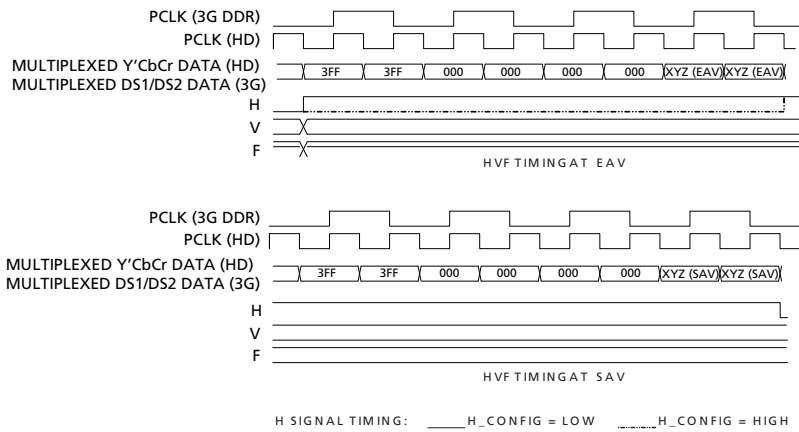


Figure 4-12: H:V:F Output Timing - 3G Level A and HDTV 10-bit Mode
3G Level B 20-bit Mode, each 10-bit stream

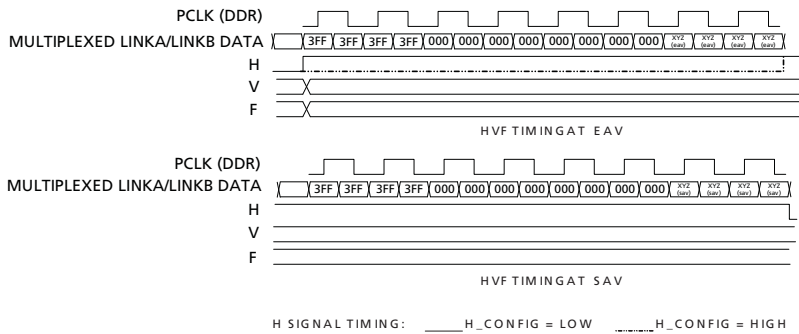


Figure 4-13: H:V:F Output Timing - 3G Level B 10-bit Mode

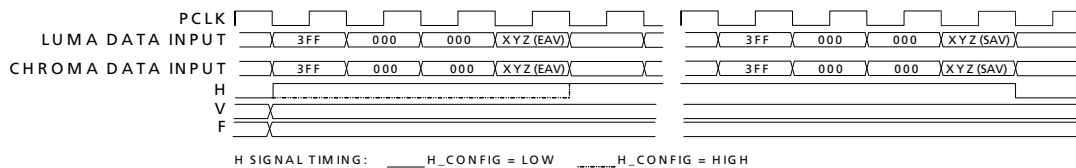


Figure 4-14: H:V:F Output Timing - HD 20-bit Output Mode

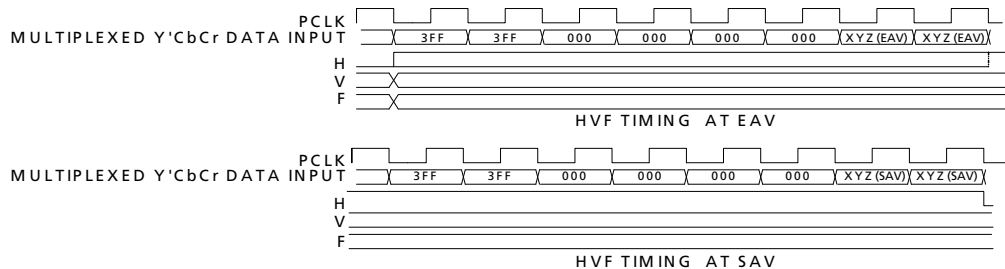


Figure 4-15: H:V:F Output Timing - HD 10-bit Output Mode

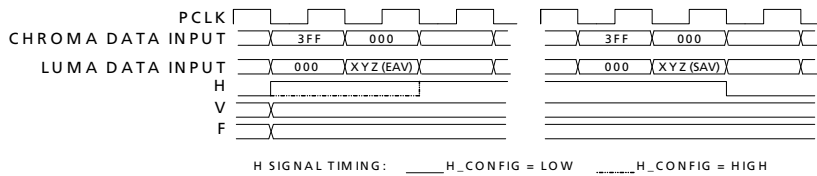


Figure 4-16: H:V:F Output Timing - SD 20-bit Output Mode

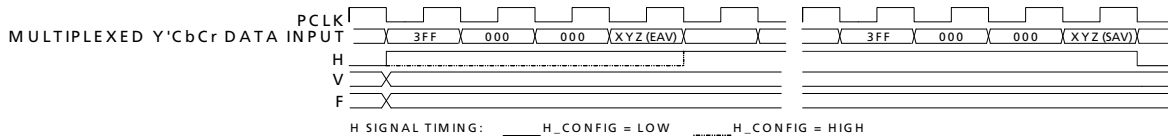


Figure 4-17: H:V:F Output Timing - SD 10-bit Output Mode

4.12.1 CEA-861 Timing Generation

The GS2970A is capable of generating CEA 861 timing instead of SMPTE HVF timing for all of the supported video formats.

This mode is selected when the TIM_861 pin is HIGH.

Horizontal sync (HSYNC), Vertical sync (VSYNC), and Data Enable (DE) timing are output on the STAT[2:0] pins by default.

Table 4-9 shows the CEA-861 formats supported by the GS2970A:

Table 4-9: Supported CEA-861 Formats

| Format | CEA-861 Format | VD_STD[5:0] |
|-------------------------------|-----------------|--------------------|
| 720(1440) x 480i @ 59.94/60Hz | 6 & 7 | 16h, 17h, 19h, 1Bh |
| 720(1440) x 576i @ 50Hz | 21 & 22 | 18h, 1Ah |
| 1280 x 720p @ 59.94/60Hz | 4 | 20h, 00h |
| 1280 x 720p @ 50Hz | 19 | 24h, 04h |
| 1920 x 1080i @ 59.94/60Hz | 5 | 2Ah, 0Ah |
| 1920 x 1080i @ 50Hz | 20 | 2Ch, 0Ch |
| 1920 x 1080p @ 29.97/30Hz | 34 ¹ | 2Bh, 0Bh |
| 1920 x 1080p @ 25Hz | 33 ² | 2Dh, 0Dh |
| 1920 x 1080p @ 23.98/24Hz | 32 | 30h, 10h |
| 1920 x 1080p @ 59.94/60Hz | 16 ¹ | 2Bh |
| 1920 x 1080p @ 50Hz | 31 ² | 2Dh |

Notes:

1,2: Timing is identical for the corresponding formats.

4.12.1.1 Vertical Timing

When CEA861 timing is selected, the device outputs standards compliant CEA861 timing signals as shown in the figures below; for example 240 active lines per field for SMPTE ST 125.

The register bit TRS_861 is used to select DFP timing generator mode which follows the vertical blanking timing as defined by the embedded TRS code words.

The timing of the CEA 861 timing reference signals can be found in the CEA 861 specifications. For information, they are included in the following diagrams. These diagrams may not be comprehensive.

Table 4-10: CEA861 Timing Formats

| Format | Parameters |
|--------|--|
| 4 | H:V:DE Input Timing 1280 x 720p @ 59.94/60Hz |
| 5 | H:V:DE Input Timing 1920 x 1080i @ 59.94/60Hz |
| 6&7 | H:V:DE Input Timing 720 (1440) x 480i @ 59.94/60Hz |
| 19 | H:V:DE Input Timing 1280 x 720p @ 50Hz |
| 20 | H:V:DE Input Timing 1920 x 1080i @ 50Hz |
| 21&22 | H:V:DE Input Timing 720 (1440) x 576 @ 50Hz |
| 16 | H:V:DE Input Timing 1920 x 1080p @ 59.94/60Hz |
| 31 | H:V:DE Input Timing 1920 x 1080p @ 50Hz |
| 32 | H:V:DE Input Timing 1920 x 1080p @ 23.94/24Hz |
| 33 | H:V:DE Input Timing 1920 x 1080p @ 25Hz |
| 34 | H:V:DE Input Timing 1920 x 1080p @ 29.97/30Hz |

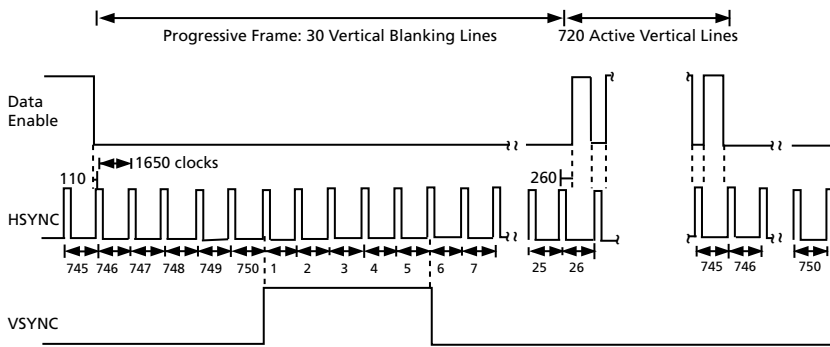
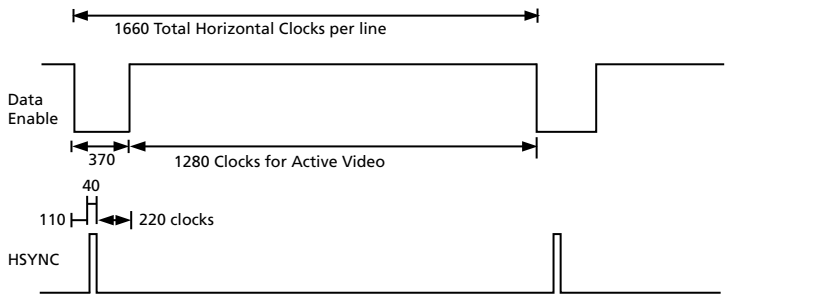


Figure 4-18: H:V:DE Output Timing 1280 x 720p @ 59.94/60 (Format 4)

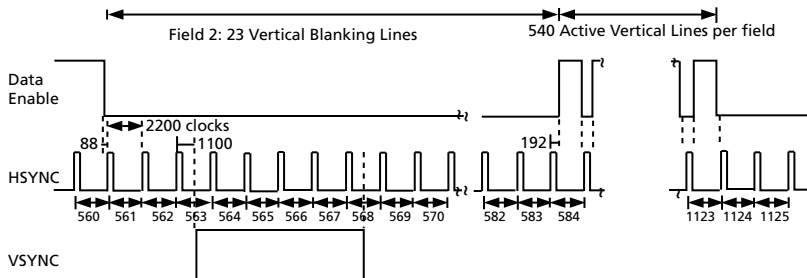
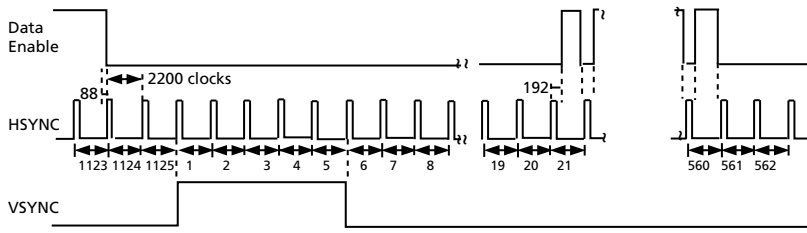
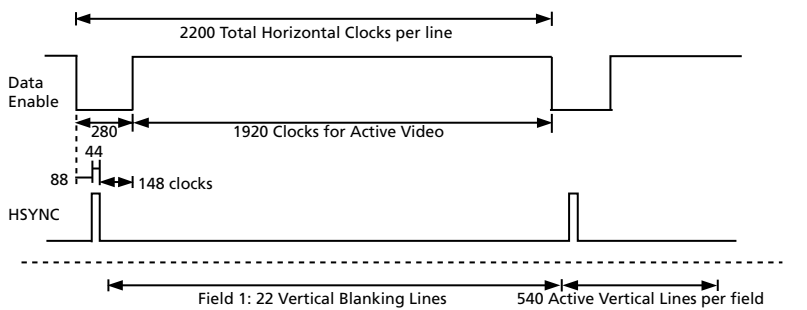


Figure 4-19: H:V:DE Output Timing 1920 x 1080i @ 59.94/60 (Format 5)

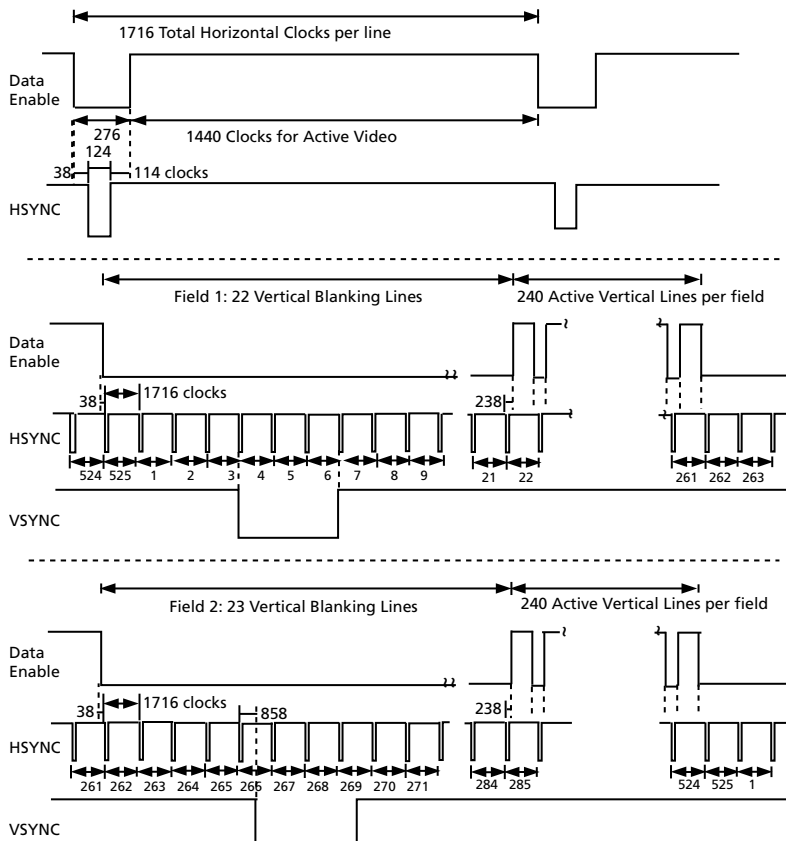


Figure 4-20: H:V:DE Output Timing 720 (1440) x 480i @ 59.94/60 (Format 6&7)

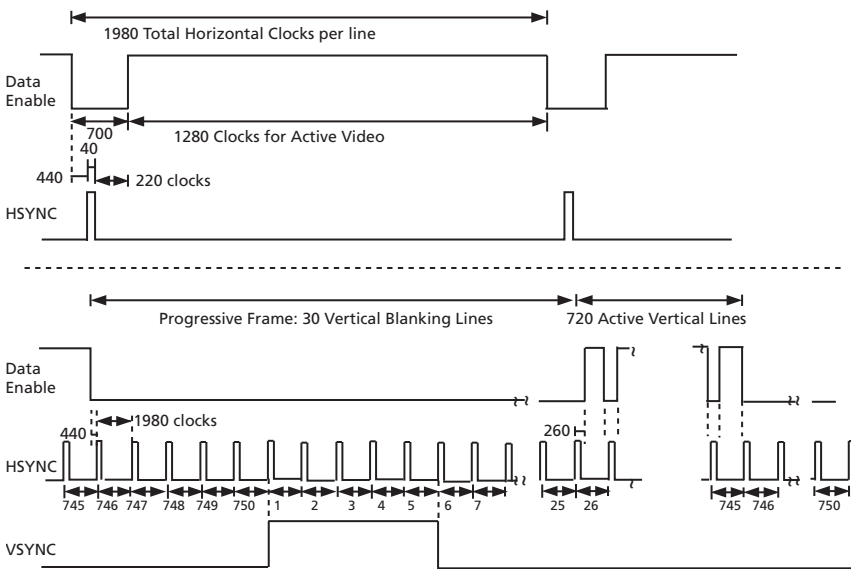


Figure 4-21: H:V:DE Output Timing 1280 x 720p @ 50 (Format 19)

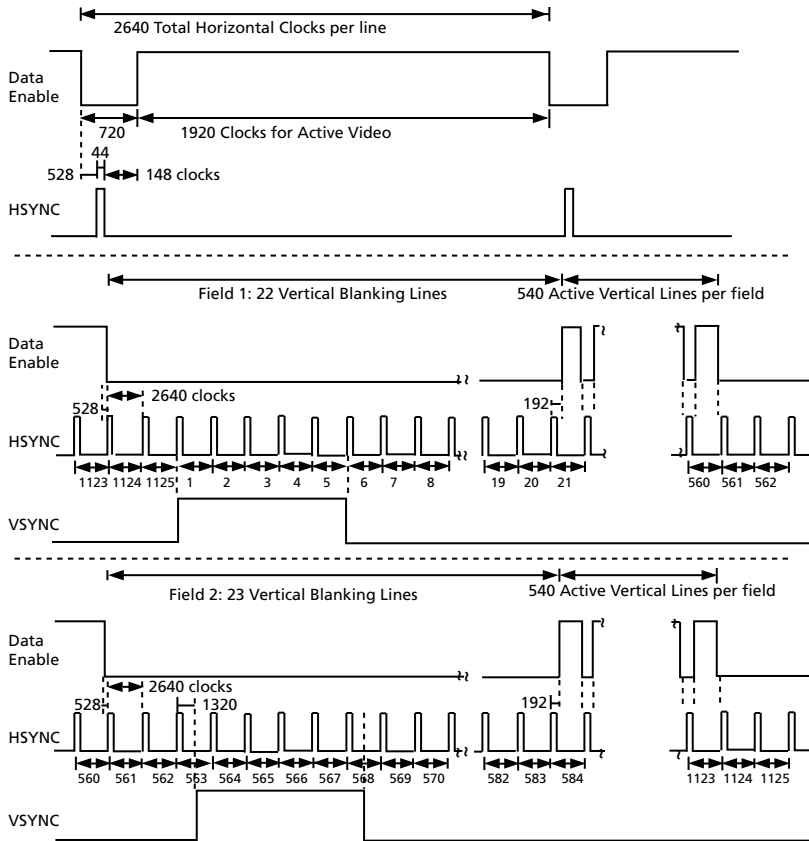


Figure 4-22: H:V:DE Output Timing 1920 x 1080i @ 50 (Format 20)

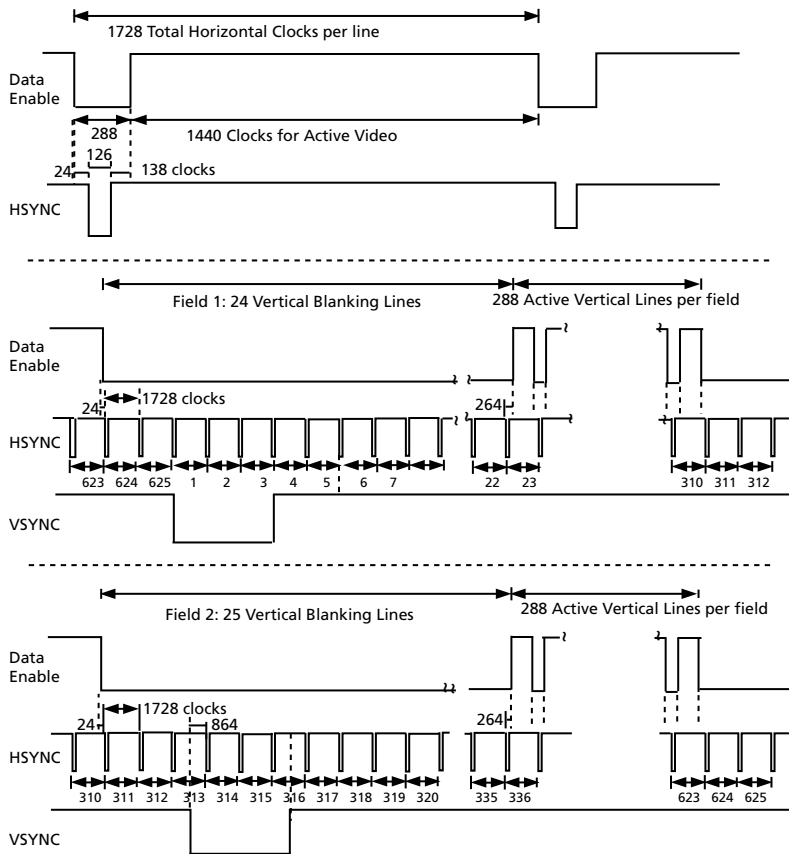


Figure 4-23: H:V:DE Output Timing 720 (1440) x 576 @ 50 (Format 21 & 22)

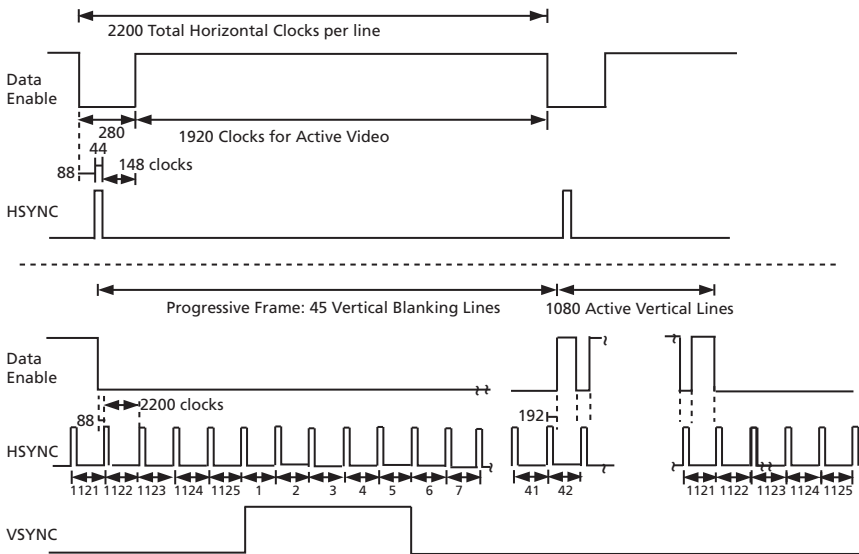


Figure 4-24: H:V:DE Output Timing 1920 x 1080p @ 59.94/60 (Format 16)



Figure 4-25: H:V:DE Output Timing 1920 x 1080p @ 50 (Format 31)

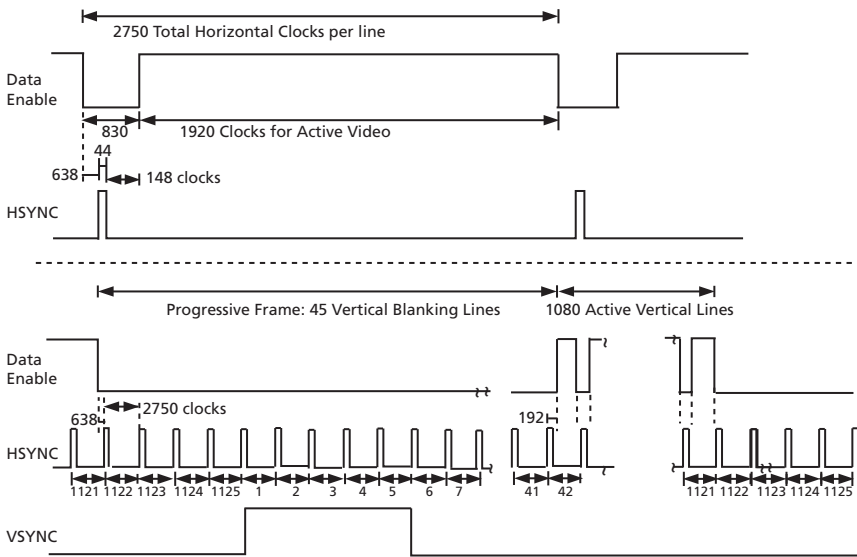


Figure 4-26: H:V:DE Output Timing 1920 x 1080p @ 23.94/24 (Format 32)

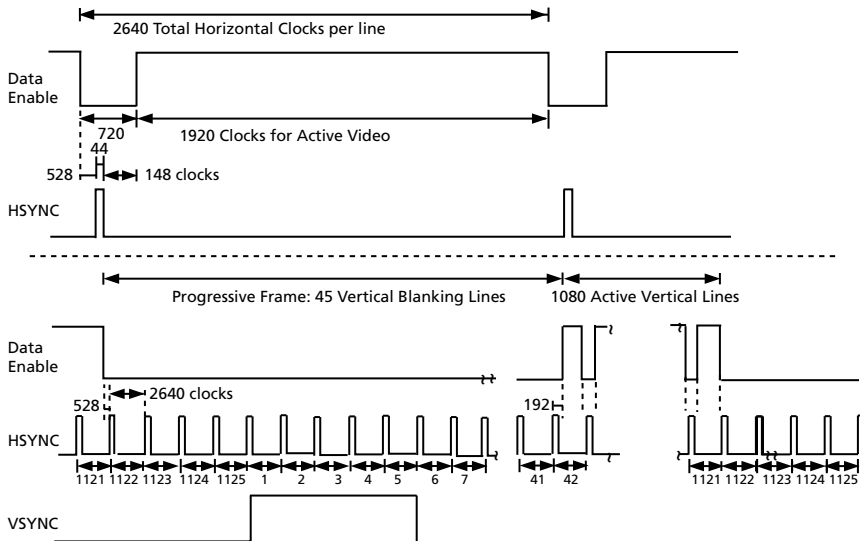


Figure 4-27: H:V:DE Output Timing 1920 x 1080p @ 25 (Format 33)

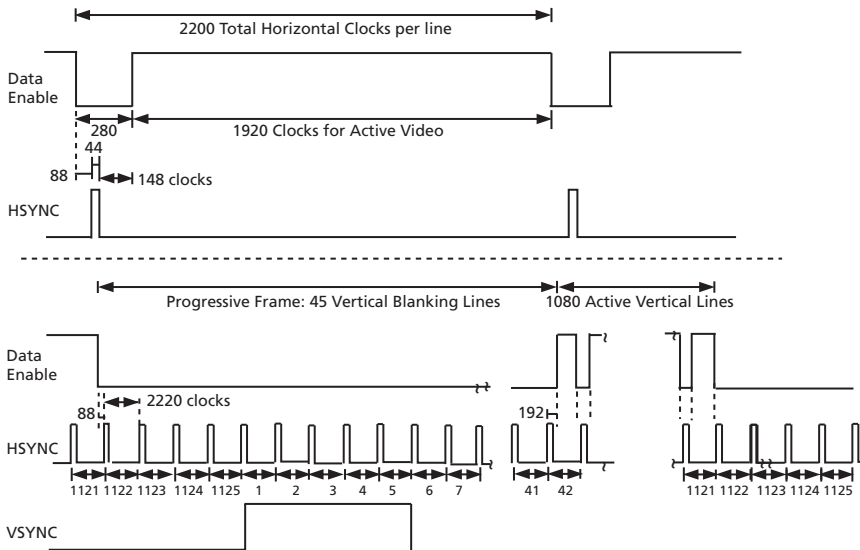


Figure 4-28: H:V:DE Output Timing 1920 x 1080p @ 29.97/30 (Format 34)

4.13 Automatic Video Standards Detection

Using the timing extracted from the received TRS signals, the GS2970A is able to identify the received video standard.

In 3G input mode, the GS2970A measures the timing parameters of one of the two identical data streams. The Rate Selection/Indication bits and the VD_STD code may be used in combination to determine the video standard.

The total samples per line, active samples per line, total lines per field/frame and active lines per field/frame are all measured.

Four registers are provided to allow the system to read the video standard information from the device. These raster structure registers are provided in addition to the

VIDEO_FORMAT_352_A_X and VIDEO_FORMAT_352_B_X registers, and are updated once per frame at the end of line 12.

The raster structure registers also contain three status bits: STD_LOCK, INT/ $\overline{\text{PROG}}$ and M. The STD_LOCK bit is set HIGH whenever the timing signal generator is fully synchronized to the incoming standard, and detects it as one of the supported formats. The INT/ $\overline{\text{PROG}}$ bit is set HIGH if the detected video standard is interlaced and LOW if the detected video standard is progressive. M is set HIGH if the clock frequency includes the “1000/1001” factor denoting a 23.98, 29.97 or 59.94Hz frame rate.

The video standard code is reported in the VD_STD bits of the host interface register. Table 4-11 describes the 5-bit codes for the recognized video standards.

Table 4-11: Supported Video Standard Codes

| SMPTE Standard | Active Video Area | RATE_DET[1] HD/3G | RATE_DET[0] SD/HD | Lines per Frame | Active Lines per Frame | Words per Active Line | Words per Line | VD_STD [5:0] |
|---------------------------------------|--|----------------------|----------------------|-----------------|------------------------|-----------------------|----------------|--------------|
| ST 425 (3G Level A) 4:2:2 | 1920x1080/60 (1:1) | 1 | 0 | 1125 | 1080 | 1920 | 2200 | 28h |
| | 1920x1080/50 (1:1) | 1 | 0 | 1125 | 1080 | 1920 | 2640 | 2Dh |
| ST 425 (3G Level B DS1 and DS2) 4:2:2 | 1920x1080/60 (2:1) | 1 | 0 | 1125 | 540 | 1920 | 2200 | 0Ah |
| | 1920x1080/50 (2:1) | 1 | 0 | 1125 | 540 | 1920 | 2640 | 0Ch |
| ST 425 (3G) 4:4:4 | 1920x1080/60 (2:1) or 1920x1080/30 (PsF) | 1 | 0 | 1125 | 1080 | 3840 | 4400 | 2Ah |
| | 1920x1080/50 (2:1) or 1920x1080/25 (PsF) | 1 | 0 | 1125 | 1080 | 3840 | 5280 | 2Ch |
| | 1280x720/60 (1:1) | 1 | 0 | 750 | 720 | 2560 | 3300 | 20h |
| | 1280x720/50 (1:1) | 1 | 0 | 750 | 720 | 2560 | 3960 | 24h |
| | 1920x1080/30 (1:1) | 1 | 0 | 1125 | 1080 | 3840 | 4400 | 28h |
| | 1920x1080/25 (1:1) | 1 | 0 | 1125 | 1080 | 3840 | 5280 | 2Dh |
| | 1280x720/25 (1:1) | 1 | 0 | 750 | 720 | 2560 | 7920 | 26h |
| | 1920x1080/24 (1:1) | 1 | 0 | 1125 | 1080 | 3840 | 5500 | 30h |
| 1280x720/24 (1:1) | 1 | 0 | 750 | 720 | 2560 | 8250 | 28h | |
| ST 260 (HD) | 1920x1035/60 (2:1) | 0 | 0 | 1125 | 1035 | 1920 | 2200 | 15h |
| ST 295 (HD) | 1920x1080/50 (2:1) | 0 | 0 | 1250 | 1080 | 1920 | 2376 | 14h |

Table 4-11: Supported Video Standard Codes (Continued)

| SMPTE Standard | Active Video Area | RATE_DET[1] HD/3G | RATE_DET[0] SD/HD | Lines per Frame | Active Lines per Frame | Words per Active Line | Words per Line | VD_STD [5:0] |
|----------------|--|----------------------|----------------------|-----------------|------------------------|-----------------------|----------------|--------------|
| ST 274 (HD) | 1920x1080/60 (2:1) or 1920x1080/30 (PsF) | 0 | 0 | 1125 | 1080 | 1920 | 2200 | 0Ah |
| | 1920x1080/50 (2:1) or 1920x1080/25 (PsF) | 0 | 0 | 1125 | 1080 | 1920 | 2640 | 0Ch |
| | 1920x1080/30 (1:1) | 0 | 0 | 1125 | 1080 | 1920 | 2200 | 0Bh |
| | 1920x1080/25 (1:1) | 0 | 0 | 1125 | 1080 | 1920 | 2640 | 0Dh |
| | 1920x1080/24 (1:1) | 0 | 0 | 1125 | 1080 | 1920 | 2750 | 10h |
| | 1920x1080/24 (PsF) | 0 | 0 | 1125 | 1080 | 1920 | 2750 | 11h |
| | 1920x1080/25 (1:1) – EM | 0 | 0 | 1125 | 1080 | 2304 | 2640 | 0Eh |
| | 1920x1080/25 (PsF) – EM | 0 | 0 | 1125 | 1080 | 2304 | 2640 | 0Fh |
| | 1920x1080/24 (1:1) – EM | 0 | 0 | 1125 | 1080 | 2400 | 2750 | 12h |
| | 1920x1080/24 (PsF) – EM | 0 | 0 | 1125 | 1080 | 2400 | 2750 | 13h |
| ST 296 (HD) | 1280x720/30 (1:1) –EM | 0 | 0 | 750 | 720 | 1280 | 3300 | 02h |
| | 1280x720/30 (1:1) – EM | 0 | 0 | 750 | 720 | 2880 | 3300 | 03h |
| | 1280x720/50 (1:1) | 0 | 0 | 750 | 720 | 1280 | 1980 | 04h |
| ST 296 (HD) | 1280x720/50 (1:1) – EM | 0 | 0 | 750 | 720 | 1728 | 1980 | 05h |
| | 1280x720/25 (1:1) | 0 | 0 | 750 | 720 | 1280 | 3960 | 06h |
| | 1280x720/25 (1:1) – EM | 0 | 0 | 750 | 720 | 3456 | 3960 | 07h |
| | 1280x720/24 (1:1) | 0 | 0 | 750 | 720 | 1280 | 4125 | 08h |
| | 1280x720/24 (1:1) – EM | 0 | 0 | 750 | 720 | 3600 | 4125 | 09h |
| | 1280x720/60 (1:1) | 0 | 0 | 750 | 720 | 1280 | 1650 | 00h |
| | 1280x720/60 (1:1) – EM | 0 | 0 | 750 | 720 | 1440 | 1650 | 01h |
| ST 125 (SD) | 1440x487/60 (2:1) | x | 1 | 525 | 244 or 243 | 1440 | 1716 | 16h |
| | 1440x507/60 | x | 1 | 525 | 254 or 253 | 1440 | 1716 | 17h |
| | 525-line 487 generic | x | 1 | 525 | – | – | 1716 | 19h |
| | 525-line 507 generic | x | 1 | 525 | – | – | 1716 | 18h |

Table 4-11: Supported Video Standard Codes (Continued)

| SMPTE Standard | Active Video Area | RATE_ DET[1] HD/3G | RATE_ DET[0] SD/HD | Lines per Frame | Active Lines per Frame | Words per Active Line | Words per Line | VD_STD [5:0] |
|---|--|--------------------------|--------------------------|-----------------------|------------------------------|--------------------------------|-------------------|-----------------|
| ITU-R BT.656 (SD) | 1440x576/50 (2:1) Or dual link progressive) | x | 1 | 625 | – | 1440 | 1728 | 18h |
| | 625-line generic | x | 1 | 625 | – | – | 1728 | 1Ah |
| Unknown HD | $SD/\overline{HD} = 0$ | 0 | 0 | – | – | – | – | 1Dh |
| Unknown SD | $SD/\overline{HD} = 1$ | x | 1 | – | – | – | – | 1Eh |
| Unknown 3G | $SD/\overline{HD} = 0$ | 1 | 0 | – | – | – | – | 3Ch |
| 2K Standards (see 4.13.1 2K Support) | | | | | | | | |
| 2048-2- 200xX (4:2:2) | 2048x1080/30 (1:1) | 0 | 0 | 1125 | 1080 | 2048 | 2200 | 31h |
| | 2048x1080/25 (1:1) | 0 | 0 | 1125 | 1080 | 2048 | 2640 | 32h |
| | 2048x1080/24 (1:1) | 0 | 0 | 1125 | 1080 | 2048 | 2750 | 33h |
| | 2048x1080/60 (1:1) | 1 | 0 | 1125 | 1080 | 2048 | 2200 | 37h |
| | 2048x1080/50 (1:1) | 1 | 0 | 1125 | 1080 | 2048 | 2640 | 38h |
| | 2048x1080/48 (1:1) | 1 | 0 | 1125 | 1080 | 2048 | 2750 | 39h |
| 2048-2- 200X (4:4:4) | 2048x1080/30 (1:1) | 1 | 0 | 1125 | 1080 | 2048 | 2200 | 34h |
| | 2048x1080/25 (1:1) | 1 | 0 | 1125 | 1080 | 2048 | 2640 | 35h |
| | 2048x1080/24 (1:1) | 1 | 0 | 1125 | 1080 | 2048 | 2750 | 36h |
| Non SMPTE or 2048-2- 200xX (4:2:2) Level B DS1 and DS2 | 2048x1080/60 (2:1) | 0 (1) | 0 | 1125 | 540 | 2048 | 2200 | 3Dh |
| | 2048x1080/50 (2:1) | 0 (1) | 0 | 1125 | 540 | 2048 | 2640 | 3Eh |
| | 2048x1080/48 (2:1) | 0 (1) | 0 | 1125 | 540 | 2048 | 2750 | 3Fh |
| Non SMPTE | Unknown 2K | x | 0 | – | – | 2048 | – | 3Ah |

Notes:

1. The Line Numbers in brackets refer to version zero SMPTE ST 352 packet locations, if they are different from version 1.
2. The part may provide full or limited functionality with standards that are not included in this table. Please consult a Semtech technical representative.
3. For SD-SDI streams, the device can report an incorrect M value when SMPTE ST 352 packets are present.

Note: In certain systems, due to greater ppm offsets in the crystal, the ‘M’ bit may not assert properly. In such cases, bits 3:0 in Register 06Fh can be increased to a maximum value of 4.

By default (after power up or after systems reset), the four RASTER_STRUCTURE, VD_STD, STD_LOCK and INT/PROG registers are set to zero. These registers are also cleared when the $\overline{\text{SMPTE_BYPASS}}$ pin is LOW.

4.13.1 2K Support

In order to fully support 2K standards without customer intervention, Semtech provides FPGA code for enhancing the GS2970A's 2K capability.

The features of the 2K FPGA enhancement are:

- Automatic video standard detection for 2K standards
- 1/1.001 rate detection for 2K standards
- CEA-861 timing generation for 2K standards
- Automatic enabling of audio extraction

This enhancement is an interface between the GS2970A and the customer system. The behaviour of the GS2970A with or without the additional 2K enhancement FPGA code is identical from a user-perspective.

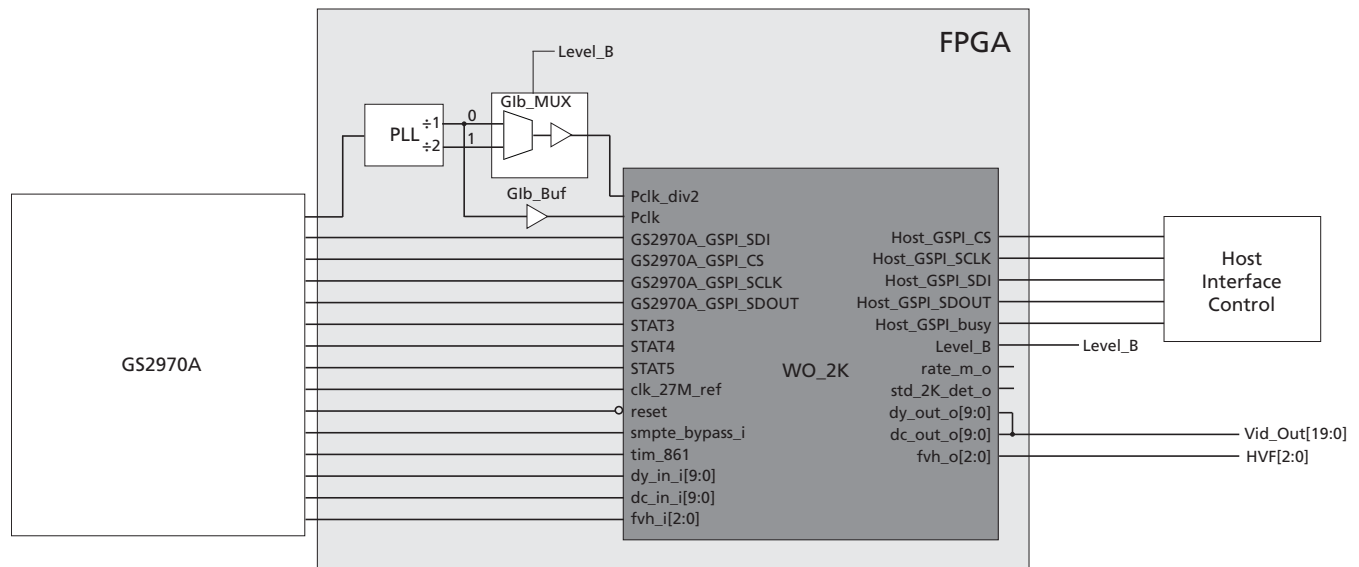


Figure 4-29: 2K Feature Enhancement

4.14 Data Format Detection & Indication

In addition to detecting the video standard, the GS2970A detects the data format, i.e. SDTI, SDI, TDM data (SMPTE ST 346), etc.

This information is represented by bits in the DATA_FORMAT_DSX register accessible through the host interface.

Data format detection is only carried out when the LOCKED signal is HIGH.

By default (at power up or after system reset), the DATA_FORMAT_DSX register is set to Fh (undefined). This register is also set as undefined when the LOCKED signal is LOW and/or the $\overline{\text{SMPTE_BYPASS}}$ pin is LOW.

Table 4-12: Data Format Register Codes

| YDATA_FORMAT[3:0] or CDATA_FORMAT[3:0] | Data Format | Remarks |
|--|-----------------------|---|
| 0h ~ 05h | SDTI | SMPTE ST 321, SMPTE ST 322, SMPTE ST 326 |
| 6h | SDI | – |
| 7h | Reserved | – |
| 8h | TDM | SMPTE ST 346 |
| 9h | HD-SDTI | – |
| Ah ~ Eh | Reserved | – |
| Fh | Non-SMPTE data format | Detected data format is not SMPTE. LOCKED = LOW. Note: This Data Format register is invalid in SMPTE_BYPASS mode. |

The data format is determined using the following criteria:

- If TRS ID words are detected but no SDTI header or TDM header is detected, then the data format is SDI
- If TRS ID words are detected and the SDTI header is available then the format is SDTI
- If TRS ID words are detected and the TDM data header is detected then the format is TDM video
- No TRS words are detected, but the PLL is locked, then the data format is unknown

Note: Two data format sets are provided for HD video rates. This is because the Y and Cr/Cb channels can be used separately to carry SDTI data streams of different data formats. In SD video mode, only the Y data format register contains the data, and the C register is set to Fh (undefined format).

4.15 EDH Detection

4.15.1 EDH Packet Detection

The GS2970A determines if EDH packets are present in the incoming video data and asserts the EDH_DETECT status according to the SMPTE standard.

EDH_DETECT is set HIGH when EDH packets have been detected and remains HIGH until EDH packets are no longer present. It is set LOW at the end of the vertical blanking (falling edge of V) if an EDH packet has not been detected during vertical blanking.

EDH_DETECT can be programmed to be output on the multi-function output port pins. The EDH_DETECT bit is also available in the host interface.

4.15.2 EDH Flag Detection

The EDH flags for ancillary data, active picture, and full field regions are extracted from the detected EDH packets and placed in the EDH_FLAG_IN register.

When the EDH_FLAG_UPDATE_MASK bit in the host interface is set HIGH, the GS2970A updates the Ancillary Data, Full Field, and Active Picture EDH flags according to SMPTE RP165. The updated EDH flags are available in the EDH_FLAG_OUT register. The EDH packet output from the device contains these updated flags.

One set of flags is provided for both fields 1 and 2. The field 1 flag data is overwritten by the field 2 flag data.

When EDH packets are not detected, the UES flags in the EDH_FLAG_OUT register are set HIGH to signify that the received signal does not support Error Detection and Handling. In addition, the EDH_DETECT bit is set LOW. These flags are set regardless of the setting of the EDH_FLAG_UPDATE_MASK bit.

EDH_FLAG_OUT and EDH_FLAG_IN may be read via the host interface at any time during the received frame except on the lines defined in SMPTE RP165, when these flags are updated.

The GS2970A indicates the CRC validity for both active picture and full field CRCs. The AP_CRC_V bit in the host interface indicates the active picture CRC validity, and the FF_CRC_V bit indicates the full field CRC validity. When EDH_DETECT = LOW, these bits are cleared.

The EDH_FLAG_OUT and EDH_FLAG_IN register values remain set until overwritten by the decoded flags in the next received EDH packet. When an EDH packet is not detected during vertical blanking, the flag registers are cleared at the end of the vertical blanking period.

4.16 Video Signal Error Detection & Indication

The GS2970A includes a number of video signal error detection functions. These are provided to enhance operation of the device when operating in SMPTE mode ($\overline{\text{SMPTE_BYPASS}} = \text{HIGH}$). These features are not available in the other operating modes of the device (i.e. when $\overline{\text{SMPTE_BYPASS}} = \text{LOW}$).

Signal errors that can be detected include:

1. TRS errors.
2. HD line based CRC errors.
3. EDH errors.
4. HD line number errors.
5. Video standard errors.

The device maintains an ERROR_STAT_X register. Each error condition has a specific flag in the ERROR_STAT_X register, which is set HIGH whenever an error condition is detected.

An ERROR_MASK register is also provided, allowing the user to select which error conditions are reported. Each bit of the ERROR_MASK register corresponds to a unique error type.

Separate $\text{SD_AUDIO_ERROR_MASK}$ and $\text{HD_AUDIO_ERROR_MASK}$ registers for SD and HD audio cores are also provided, allowing select error conditions to be reported. Each bit of each ERROR_MASK register corresponds to a unique error type.

By default (at power up or after system reset), all bits of the ERROR_MASK registers are zero, enabling all errors to be reported. Individual error detection may be disabled by setting the corresponding bit HIGH in the mask registers.

Error conditions are indicated by a $\overline{\text{VIDEO_ERROR}}$ signal and an $\overline{\text{AUDIO_ERROR}}$ signal, which are available for output on the multifunction I/O output pins. The two signals are also combined into a summary $\overline{\text{DATA_ERROR}}$ signal, which is also available on the multifunction I/O pins. These signals are normally HIGH, but are set LOW by the device when an error condition has been detected.

These signals are a logical 'NOR' of the appropriate error status flags stored in the ERROR_STAT_X register, which are gated by the bit settings in the ERROR_MASK registers. When an error status bit is HIGH and the corresponding error mask bit is LOW, the corresponding $\overline{\text{DATA_ERROR}}$ signal is set LOW by the device.

The ERROR_STAT_X registers, and correspondingly the $\overline{\text{DATA_ERROR}}$, $\overline{\text{VIDEO_ERROR}}$, and $\overline{\text{AUDIO_ERROR}}$ signals, are cleared at the start of the next video field or when read via the host interface, whichever condition occurs first. Note that any $\overline{\text{AUDIO_ERROR}}$ condition will cause $\overline{\text{DATA_ERROR}}$ to assert. Use the $\text{SD_AUDIO_ERROR_MASK}$ and $\text{HD_AUDIO_ERROR_MASK}$ registers if masking these events is desired.

All bits of the ERROR_STAT_X registers are also cleared under any of the following conditions:

1. $\overline{\text{LOCKED}}$ signal = LOW.
2. $\overline{\text{SMPTE_BYPASS}} = \text{LOW}$.
3. When a change in video standard has been detected.
4. $\overline{\text{RESET_TRST}} = \text{LOW}$

Table 4-13 shows the ERROR_STAT_X register and ERROR_MASK_X register.

Note: Since the error indication registers are cleared once per field, if an external host micro is polling the error registers periodically, an error flag may be missed if it is intermittent, and the polling frequency is less than the field rate.

Table 4-13: Error Status Register and Error Mask Register

| Video Error Status Register | Video Error Mask Register |
|-----------------------------|----------------------------|
| SAV_ERR (02h, 03h) | SAV_ERR_MASK (037h, 038h) |
| EAV_ERR (02h, 03h) | EAV_ERR_MASK (037h, 038h) |
| YCRC_ERR (02h, 03h) | YCRC_ERR_MASK (037h, 038h) |
| CCRC_ERR (02h, 03h) | CCRC_ERR_MASK (037h, 038h) |
| LNUM_ERR (02h, 03h) | LNUM_ERR_MASK (037h, 038h) |
| YCS_ERR (02h, 03h) | YCS_ERR_MASK (037h, 038h) |
| CCS_ERR (02h, 03h) | CCS_ERR_MASK (037h, 038h) |
| AP_CRC_ERR (02h) | AP_CRC_ERR_MASK (037h) |
| FF_CRC_ERR (02h) | FF_CRC_ERR_MASK (037h) |
| VD_STD_ERR (02h, 03h) | VD_STD_ERR_MASK (037h) |

Note 1: See Section 4.19 for Audio Error Status.

Note 2: In 3G Level B mode, separate Video Error Mask registers exist for Link A and Link B. The GS2970A distinguishes between Level A and Level B mappings at 3Gb/s. When Level B data is detected, error detection is enabled separately for Data Stream 1 and Data Stream 2 (Link A and Link B, respectively). Therefore, a second set of error status and mask registers is available for Data Stream 2, and is only valid when 3Gb/s Level B data is detected by the device.

4.16.1 TRS Error Detection

TRS error flags are generated by the GS2970A under the following two conditions:

1. A phase shift in received TRS timing is observed on a non-switching line.
2. The received TRS Hamming codes are incorrect.

Both SAV and EAV TRS words are checked for timing and data integrity errors.

For HD mode, only the Y channel TRS codes are checked for errors.

For 3G mode Level A signals, only data stream one TRS codes are checked for errors. For 3G Level B signals, the Y channel TRS codes of both Link A and Link B are checked for errors.

Both 8-bit and 10-bit TRS code words are checked for errors.

The SAV_ERR bit of the ERROR_STAT_X register is set HIGH when an SAV TRS error is detected.

The EAV_ERR bit of the ERROR_STAT_X register is set HIGH when an EAV TRS error is detected.

4.16.2 Line Based CRC Error Detection

The GS2970A calculates line based CRCs for HD and 3G video signals. CRC calculations are done for each 10-bit channel (Y and C for HD video, DS1 and DS2 for 3G video).

These calculated CRC values are compared with the received CRC values.

If a mismatch in the calculated and received CRC values is detected for Y channel data (Data Stream 1 for 3G video), the YCRC_ERR bit in the ERROR_STAT_X register is set HIGH.

If a mismatch in the calculated and received CRC values is detected for C channel data (Data Stream 2 for 3G video), the CCRC_ERR bit in the ERROR_STAT_X register is set HIGH.

Y or C CRC errors are also generated if CRC values are not embedded.

Line based CRC errors are only generated when the device is operating in HD and 3G modes.

Note: By default, 8-bit to 10-bit TRS remapping is enabled. If an 8-bit input is used, the HD CRC check is based on the 10-bit remapped value, not the 8-bit value, so the CRC Error Flag is incorrectly asserted and should be ignored. If 8-bit to 10-bit remapping is enabled, then CRC correction and insertion should be enabled by setting the CRC_INS_MASK bit LOW in the IOPROC_1 or IOPROC_2 register. This ensures that the CRC values are updated.

4.16.3 EDH CRC Error Detection

The GS2970A also calculates Full Field (FF) and Active Picture (AP) CRC's according to SMPTE RP165 in support of Error Detection and Handling packets in SD signals.

These calculated CRC values are compared with the received CRC values.

Error flags for AP and FF CRC errors are provided and each error flag is a logical OR of field 1 and field 2 error conditions.

The AP_CRC_ERR bit in the VIDEO_ERROR_STAT_X register is set HIGH when an Active Picture CRC mismatch has been detected in field 1 or 2.

The FF_CRC_ERR bit in the VIDEO_ERROR_STAT_X register is set HIGH when a Full Field CRC mismatch has been detected in field 1 or 2.

EDH CRC errors are only indicated when the device is operating in SD mode and when the device has correctly received EDH packets.

4.16.4 HD & 3G Line Number Error Detection

If a mismatch in the calculated and received line numbers is detected, the LNUM_ERR bit in the VIDEO_ERROR_STAT_X register is set HIGH.

4.17 Ancillary Data Detection & Indication

The GS2970A detects ancillary data in both the vertical and horizontal ancillary data spaces. Status signal outputs Y/1ANC and C/2ANC are provided to indicate the position of ancillary data in the output data streams. These signals may be selected for output on the multi-function I/O port pins (STAT[5:0]).

The GS2970A indicates the presence of all types of ancillary data by detecting the 000h, 3FFh, 3FFh (00h, FFh, FFh for 8-bit video) ancillary data preamble.

Note 1: Both 8 and 10-bit ancillary data preambles are detected by the device.

By default (at power up or after system reset) the GS2970A indicates all types of ancillary data. Up to 5 types of ancillary data can be specifically programmed for recognition.

For HD video signals, ancillary data may be placed in both the Y and Cb/Cr video data streams separately. For SD video signals, the ancillary data is multiplexed and combined into the YCbCr data space.

For 3G signals, ancillary data may be placed in either or both of the virtual interface data streams. Both data streams are examined for ancillary data.

For a 3G data stream formatted as per Level A mapping:

- The ancillary data is placed in Data Stream 1 first, with overflow into Data Stream 2
- SMPTE ST 352 packets are duplicated in both data streams

For a 3G data stream formatted as per Level B mapping:

- Each multiplexed data stream forming the 3G signal contains ancillary data embedded according to SMPTE ST 291
- Each multiplexed data stream forming the 3G signal contains SMPTE ST 352 packets embedded according to SMPTE ST 425

When operating in HD mode, the Y/1ANC signal is HIGH whenever ancillary data is detected in the Luma data stream, and C/2ANC is HIGH whenever ancillary data is detected in the Chroma data stream. The signals are asserted HIGH at the start of the ancillary data preamble, and remain HIGH until after the ancillary data checksum.

When detecting ancillary data in 3G Level A data, the Y/1ANC status output is HIGH whenever Data Stream 1 ancillary data is detected and the C/2ANC status output is HIGH whenever Data Stream 2 ancillary data is detected.

When detecting ancillary data in 3G Level B data, the Y/1ANC status output is HIGH whenever Data Stream 1 ancillary data is detected on either Y or C channels and the C/2ANC status output is HIGH whenever Data Stream 2 ancillary data is detected on either Y or C channels.

When operating in SD mode, the Y/1ANC and C/2ANC signals depend on the output data format. For 20-bit demultiplexed data, the Y/1ANC and C/2ANC signals operate independently to indicate the first and last ancillary Data Word position in the Luma and/or Chroma data streams. For 10-bit multiplexed data, the Y/1ANC signal is HIGH whenever ancillary data is detected, and the C/2ANC signal is always LOW.

When operating in 3G modes, the Y/1ANC and C/2ANC flags are both zero if the 10-bit multiplexed output format is selected.

These status signal outputs are synchronous with PCLK and may be used as clock-enables for external logic, or as write-enables for an external FIFO or other memory devices.

The operation of the Y/1ANC and C/2ANC signals is shown below in Figure 4-30.

Note 2: When I/O processing is disabled, the Y/1ANC and C/2ANC flags may toggle, but they are invalid and should be ignored.

Note 3: In 3G Level B mode, if the ANC_EXT_SEL_DS2_DS1 bit is HIGH and the ANC_DATA_DELETE bit is HIGH, the Y/1ANC and C/2ANC flags are not valid.

Note 4: For 3G Level B data, the Y/1ANC flag identifies all ANC data on Data Stream 1 (Link A), whether it is embedded in the Y or C component – ANC data is not identified separately for each component. Similarly, the C/2ANC flag identifies all ANC data on Data Stream 2 (Link B), whether it is embedded in the Y or C component.

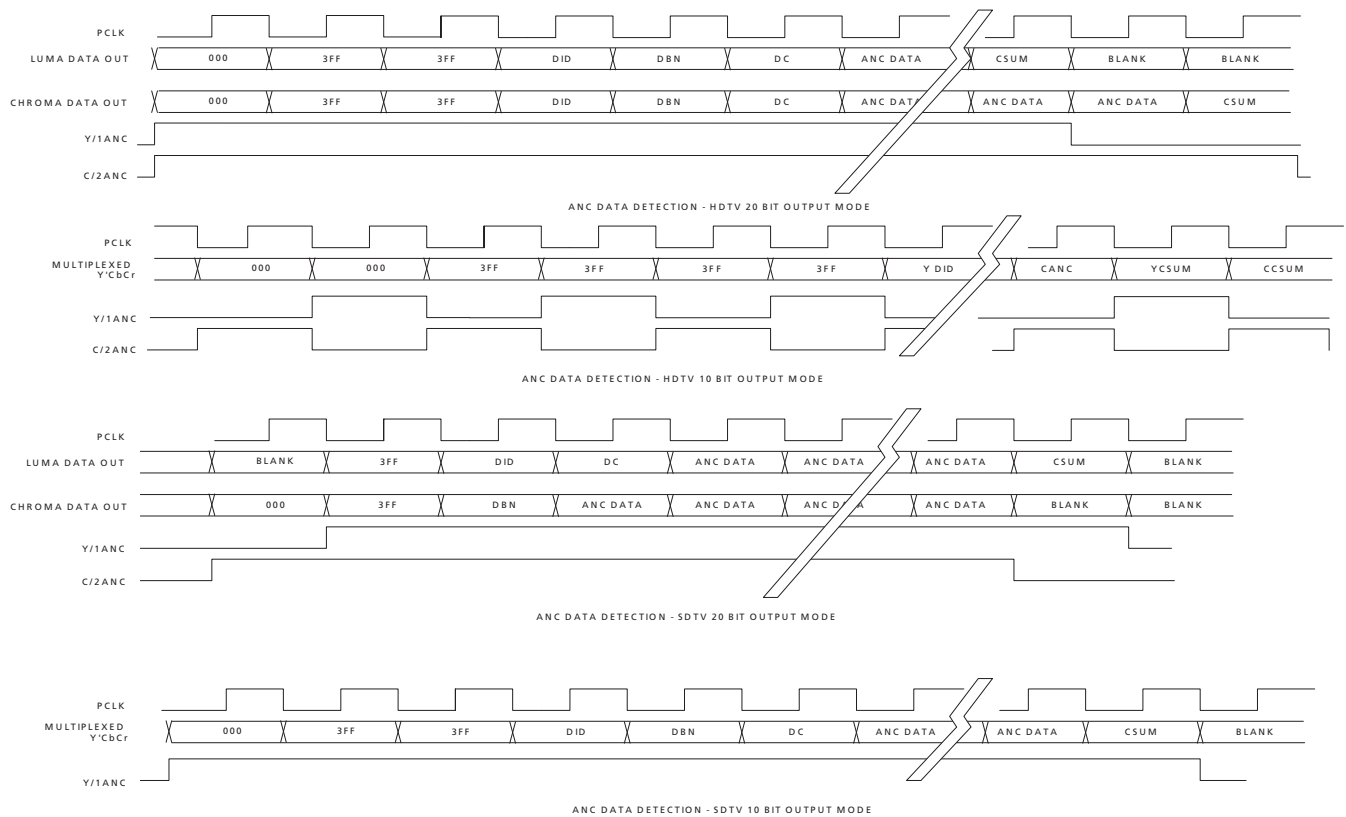


Figure 4-30: Y/1ANC and C/2ANC Signal Timing

4.17.1 Programmable Ancillary Data Detection

As described above in Section 4.17, the GS2970A detects and indicates all ancillary data types by default.

It is possible to program which ancillary data types are to be detected and indicated. Up to five different ancillary data types may be programmed for detection by the GS2970A in the ANC_TYPE_DS1 registers for SD, HD and 3G Level A data.

When so programmed, the GS2970A only indicates the presence of the specified ancillary data types, ignoring all other ancillary data. For each data type to be detected, the user must program the DID and/or SDID of that ancillary data type. In the case where no DID or SDID values are programmed, the GS2970A indicates the presence of all ancillary data. In the case where one or more, DID and/or SDID values have been programmed, then only those matching data types are detected and indicated.

The timing of the Y/1ANC and C/2ANC signals in this case is as shown in [Figure 4-30](#).

The GS2970A compares the received DID and/or SDID with the programmed values. If a match is found, ancillary data is indicated.

For any DID or SDID value set to zero, no comparison or match is made. For example, if the DID is programmed and the SDID is not programmed, the GS2970A only detects a match to the DID value.

If both DID and SDID values are non-zero, then the received ancillary data type must match both the DID and SDID before Y/1ANC and/or C/2ANC is set HIGH.

Note 1: For 3G Level B data, the ANC_TYPE_DS1 registers are valid for Data Stream 1, and a second set of five ANC_TYPE registers (ANC_TYPE_DS2) is provided for detection of specific ancillary data in Data Stream 2.

Note 2: SMPTE ST 352 Payload Identifier packets and Error Detection and Handling (EDH) Packets are always detected by the GS2970A, irrespective of the settings of the ANC_TYPE registers.

4.17.2 SMPTE ST 352 Payload Identifier

The GS2970A automatically extracts the SMPTE ST 352 payload identifier present in the input data stream for SD, HD, and 3G Level A signals. The four word payload identifier packets are written to VIDEO_FORMAT_X_DS1 and VIDEO_FORMAT_X_DS2 bits accessible through the host interface.

The device also indicates the version of the payload packet in the VERSION_352M bit of the DATA_FORMAT_DSX register. When the SMPTE ST 352 packet is formatted as a “version 1” packet, the VERSION_352M bit is set HIGH, when the packet is formatted as a “version 2” packet, this bit is set LOW.

The VIDEO_FORMAT_352_A_X and VIDEO_FORMAT_352_B_X registers are only updated if there are no checksum errors in the received SMPTE ST 352 packets.

By default (at power up or after system reset), the VIDEO_FORMAT_X_DS1 and VIDEO_FORMAT_X_DS2 bits are set to 0, indicating an undefined format.

Note 1: When 3G Level B data is detected by the device, the user needs to extract the SMPTE ST 352 Payload Identifier packets by using the ANC packet extraction block - they are not detected and extracted automatically. In this case:

- The VD_STD_ERR bit is not valid
- ST 352 extraction is only done on one data stream or the other, not both simultaneously (Link A or Link B selected via the host interface)
- Previously embedded ST 352 packets can be deleted on one data stream only (using the ANC_DATA_DELETE bit, see [Section 4.18.8](#)), but these packets are replaced with 10-bit Y/C blanking values only

- It is necessary to manually extract the SMPTE ST 352 data by programming the DID, SDID and line number information into the ANC data extraction block

Note 2: SMPTE ST 352 packet regeneration is enabled by default for 3G Level B inputs, and should be disabled through the host interface if Level B to Level A conversion is not enabled.

4.17.2.1 SMPTE ST 352 Payload Identifier Usage

The SMPTE ST 352 Payload Identifier is used to confirm the video format identified by the Automatic Video Standards Detection block (see [Section 4.17.4](#)).

Table 4-14: SMPTE ST 352 Packet Data

| Bit Name | Bit | Name | Description | R/W | Default |
|-------------------------------------|------|------------------------|---|-----|---------|
| VIDEO_FORMAT_4_DS1 Address: 01Ah | 15-8 | SMPTE ST 352 Byte 4 | | R | 0 |
| VIDEO_FORMAT_3_DS1 Address: 01Ah | 7-0 | SMPTE ST 352 Byte 3 | Data is available in this register when Video Payload Identification Packets are detected in the data stream. | R | 0 |
| VIDEO_FORMAT_2_DS1 Address: 019h | 15-8 | SMPTE ST 352 Byte 2 | | R | 0 |
| VIDEO_FORMAT_2_DS1 Address: 019h | 7-0 | SMPTE ST 352 Byte 1 | | R | 0 |

4.17.2.2 3G SMPTE ST 352 Packets Following Level B to Level A Conversion

After Level B to Level A conversion, modified payload data must be programmed via the host interface into the VIDEO_FORMAT_352_X_X registers and automatically inserted by the GS2970A on the correct SMPTE ST 352 Line Number.

SMPTE ST 352 Packets are embedded in both data streams.

Previously embedded ST 352 packets may be deleted from one data stream only (using the ANC_DATA_DELETE bit, see [Section 4.18.8](#)), but these packets are replaced with 10-bit Y/C blanking values.

Note: Pre-existing SMPTE ST 352 Packets that are not deleted are re-mapped to different line numbers during conversion to Level A formatting. These packets should be ignored by the system, since they are on non-standard SMPTE ST 352 lines.

4.17.3 Ancillary Data Checksum Error

The GS2970A calculates checksums for all received ancillary data.

These calculated checksums are compared with the received ancillary data checksum words.

If a mismatch in the calculated and received checksums is detected, then a checksum error is indicated.

When operating in HD mode, the device makes comparisons on both the Y and C channels separately. If an error condition in the Y channel is detected, the YCS_ERR bit

in the VIDEO_ERROR_STAT_X register is set HIGH. If an error condition in the C channel is detected, the CCS_ERR bit in the VIDEO_ERROR_STAT_X register is set HIGH.

When operating in 3G Level A mode, the device makes comparisons on both the Y (Data Stream 1) and C (Data Stream 2) channels separately. If an error condition in the Y channel is detected, the YCS_ERR bit in the VIDEO_ERROR_STAT_X register is set HIGH. If an error condition in the C channel is detected, the CCS_ERR bit in the VIDEO_ERROR_STAT_X register is set HIGH.

When operating in 3G Level B mode, the device makes comparisons on both the Y channel and the C channel of both Link A and Link B.

When operating in SD mode, only the YCS_ERR bit is set HIGH when checksum errors are detected.

4.17.3.1 Programmable Ancillary Data Checksum Calculation

As described above, the GS2970A calculates and compares checksum values for all ancillary data types by default. It is possible to program which ancillary data types are checked as described in [Section 4.17.1](#).

When so programmed, the GS2970A only checks ancillary data checksums for the specified data types, ignoring all other ancillary data.

The YCS_ERR and/or CCS_ERR bits in the VIDEO_ERROR_STAT_X register are only set HIGH if an error condition is detected for the programmed ancillary data types.

4.17.4 Video Standard Error

If a mismatch between the received SMPTE ST 352 packets and the calculated video standard occurs, the GS2970A indicates a video standard error by setting the VD_STD_ERR bit of the VIDEO_ERROR_STAT_X register HIGH.

The device detects the SMPTE ST 352 Packet version as defined in the SMPTE ST 352 standard. If the incoming packet is Version Zero, then no comparison is made with the internally generated payload information and the VD_STD_ERR bit is not set HIGH.

Note 1: If the received SMPTE ST 352 packet indicates 25, 30 or 29.97PsF formats, the device only indicates an error when the video format is actually progressive. The device detects 24 and 23.98PsF video standards and perform error checking at these rates.

Note 2: The VD_STD_ERR bit should be ignored in all 3G modes.

Note 3: VD_STD_ERR_DS1 is set incorrectly for a 1920x1080/PsF/24 payload ID. To resolve this issue, choose one of the two methods.

- Set the VD_STD_ERR_DS1 mask bit high in the ERROR_MASK_1 register to avoid having incorrect assertion of the DATA_ERROR pin.
- Monitor the received SMPTE ST 352 packet in the VIDEO_FORMAT_352_A_1 and VIDEO_FORMAT_352_B_1 registers and compare that to the video format identified in the VD_STD_DS1 bits in the DATA_FORMAT_DS1 register. Then, make the determination of whether or not there is a mismatch on their own.

4.18 Signal Processing

In addition to error detection and indication, the GS2970A can also correct errors, inserting corrected code words, checksums and CRC values into the data stream.

The following processing can be performed by the GS2970A:

1. TRS error correction and insertion.
2. HD line based CRC correction and insertion.
3. EDH CRC error correction and insertion.
4. HD line number error correction and insertion.
5. Illegal code re-mapping.
6. Ancillary data checksum error correction and insertion.
7. Audio extraction.
8. SMPTE ST 372 (Level B to Level A) Conversion.

All of the above features are only available in SMPTE mode ($\overline{\text{SMPTE_BYPASS}} = \text{HIGH}$).

To enable these features, the IOPROC_EN/ $\overline{\text{DIS}}$ pin must be set HIGH, and the individual feature must be enabled via bits in the IOPROC_1 and/or IOPROC_2 (depending on the data stream) register(s).

The IOPROC_1 and IOPROC_2 registers contains one bit for each processing feature allowing each one to be enabled/disabled individually.

By default (at power up or after device reset), all of the IOPROC_1 and IOPROC_2 register bits described in Table 4-15 below are set to zero (0), which enables all of the processing features.

To disable an individual processing feature, set the corresponding bit to one (1) in the IOPROC_1 and/or IOPROC_2 register(s).

Table 4-15: IOPROC_1 and IOPROC_2 Register Bits

| Processing Feature | IOPROC_1 Register Bit | IOPROC_2 Register Bit |
|---|---------------------------------|---------------------------------|
| TRS error correction and insertion | TRS_INS_DS1_MASK | TRS_INS_DS2_MASK |
| Y and C line based CRC error correction | CRC_INS_DS1_MASK | CRC_INS_DS2_MASK |
| Y and C line number error correction | LNUM_INS_DS1_MASK | LNUM_INS_DS2_MASK |
| Ancillary data check sum correction | ANC_CHECKSUM_INSERTION_DS1_MASK | ANC_CHECKSUM_INSERTION_DS2_MASK |
| EDH CRC error correction | EDH_CRC_INS_MASK | N/A |
| Illegal code re-mapping | ILLEGAL_WORD_REMAP_DS1_MASK | ILLEGAL_WORD_REMAP_DS2_MASK |
| H timing signal configuration | H_CONFIG | N/A |
| Update EDH Flags | EDH_FLAG_UPDATE_MASK | N/A |
| Audio Data Extraction | N/A | AUDIO_SEL_DS2_DS1 |
| Ancillary Data Extraction | ANC_DATA_EXT_MASK | ANC_EXT_SEL_DS2_DS1 |

Table 4-15: IOPROC_1 and IOPROC_2 Register Bits (Continued)

| Processing Feature | IOPROC_1 Register Bit | IOPROC_2 Register Bit |
|--------------------------------|-----------------------|-----------------------|
| Audio Extraction | AUD_EXT_MASK | N/A |
| Regeneration of ST 352 packets | N/A | REGEN_352M_MASK |

4.18.1 TRS Correction & Insertion

When TRS Error Correction and Insertion is enabled, the GS2970A generates and overwrites TRS code words as required.

TRS Word Generation and Insertion is performed using the timing generated by the Timing Signal Generator, providing an element of noise immunity over using just the received TRS information.

This feature is enabled when the IOPROC_EN/ $\overline{\text{DIS}}$ pin is HIGH and the TRS_INS_DS1_MASK or TRS_INS_DS2_MASK bits in the IOPROC_1 or IOPROC_2 registers are set LOW. The TRS_INS_DS1_MASK bit is in the IOPROC_1 register and is used to enable/disable TRS correction and insertion for SD, HD, and 3G-A data streams. The TRS_INS_DS2_MASK bit is in the IOPROC_2 register and is used to enable/disable TRS correction and insertion for 3G-B data streams only.

Note: Inserted TRS code words are always 10-bit compliant, irrespective of the bit depth of the incoming video stream.

4.18.2 Line Based CRC Correction & Insertion

When CRC Error Correction and Insertion is enabled, the GS2970A generates and inserts line based CRC words into both the Y and C channels of the data stream.

Line based CRC word generation and insertion only occurs in HD and 3G modes, and is enabled in when the IOPROC_EN/ $\overline{\text{DIS}}$ pin is HIGH and the CRC_INS_DSX_MASK bit in the IOPROC_X register is set LOW.

4.18.3 Line Number Error Correction & Insertion

When Line Number Error Correction and Insertion is enabled, the GS2970A calculates and inserts line numbers into the output data stream. Re-calculated line numbers are inserted into both the Y and C channels.

Line number generation is in accordance with the relevant HD or 3G video standard as determined by the Automatic Standards Detection block.

This feature is enabled when the device is operating in HD or 3G modes, the IOPROC_EN/ $\overline{\text{DIS}}$ pin is HIGH and the LNUM_INS_DSX_MASK bit in the IOPROC_X register is set LOW.

4.18.4 ANC Data Checksum Error Correction & Insertion

When ANC data Checksum Error Correction and Insertion is enabled, the GS2970A generates and inserts ancillary data checksums for all ancillary data words by default.

Where user specified ancillary data has been programmed (see [Section 4.17.1](#)), only the checksums for the programmed ancillary data are corrected.

This feature is enabled when the IOPROC_EN/ $\overline{\text{DIS}}$ pin is HIGH and the ANC_CHECKSUM_INSERTION_DSX_MASK bit in the IOPROC_X register is set LOW.

4.18.5 EDH CRC Correction & Insertion

When EDH CRC Error Correction and Insertion is enabled, the GS2970A generates and overwrites full field and active picture CRC check-words.

Additionally, the device sets the active picture and full field CRC 'V' bits HIGH in the EDH packet. The AP_CRC_V and FF_CRC_V register bits only report the received EDH validity flags.

EDH FF and AP CRC's are only inserted when the device is operating in SD mode, and if the EDH data packet is detected in the received video data.

Although the GS2970A modifies and inserts EDH CRC's and EDH packet checksums, EDH error flags are only updated when the EDH_FLAG_UPDATE_MASK bit is LOW.

This feature is enabled in SD mode, when the IOPROC_EN/ $\overline{\text{DIS}}$ pin is HIGH and the EDH_CRC_INS_MASK bit in the IOPROC_1 register is set LOW.

4.18.6 Illegal Word Re-mapping

All words within the active picture (outside the horizontal and vertical blanking periods), between the values of 3FCh and 3FFh are re-mapped to 3FBh. All words within the active picture area between the values of 000h and 003h are remapped to 004h.

This feature is enabled when the IOPROC_EN/ $\overline{\text{DIS}}$ pin is HIGH and the ILLEGAL_WORD_REMAP_DSX_MASK bit in the IOPROC_X register is set LOW.

4.18.7 TRS and Ancillary Data Preamble Remapping

8-bit TRS and ancillary data preambles are re-mapped to 10-bit values. 8-bit to 10-bit mapping of TRS headers is only supported if the TRS values are 3FC 000 000. Other values such as 3FD, 3FE, 3FF, 001, 002 and 003 are not supported. This feature is enabled by default, and can be disabled via the IOPROC_X register.

4.18.8 Ancillary Data Extraction

Ancillary data may be extracted externally from the GS2970A output stream using the Y/1ANC and C/2ANC signals, and external logic.

As an alternative, the GS2970A includes a FIFO, which extracts ancillary data using read access via the host interface to ease system implementation. The FIFO stores up to 2048 x 16 bit words of ancillary data in two separate 1024 word memory banks.

Data is accessed from both memory banks using the same host interface addresses, 800h to BFFh (see [Table 4-32: ANC Extraction FIFO Access Registers](#)).

The device writes the contents of ANC packets into the FIFO, starting with the first Ancillary Data Flag (ADF), followed by up to 1024 words.

All Data Identification (DID), Secondary Data Identification (SDID), Data Count (DC), user data, and checksum words are written into the device memory.

The device detects ancillary data packet DID's placed anywhere in the video data stream, including the active picture area.

In HD and 3G mode, ancillary data from the Y channel or Data Stream One is placed in the Least Significant Word (LSW) of the FIFO, allocated to the lower 8 bits of each FIFO address.

Ancillary data from the C channel or Data Stream Two is placed in the Most Significant Word (MSW) (upper 8 bits) of each FIFO address.

Note: Please refer to the ANC insertion and Extraction Application Note (Doc ID: GENDOC-053410), for discrete steps and example of Ancillary data extraction using the GS2970A.

In SD mode, ancillary data is placed in the LSW of the FIFO. The MSW is set to zero.

If the ANC_TYPE registers are all set to zero, the device extracts all types of ancillary data. If programmable ancillary data extraction is required, then up to five types of ancillary data to be extracted can be programmed in the ANC_TYPE registers (see [Section 4.17.1](#)).

Additionally, the lines from which the packets are to be extracted can be programmed into the ANC_LINEA[10:0] and ANC_LINEB[10:0] registers, allowing ancillary data from a maximum of two lines per frame to be extracted. If only one line number register is programmed (with the other set to zero), ancillary data packets are extracted from one line per frame only. When both registers are set to zero, the device extracts packets from all lines.

To start Ancillary Data Extraction, the ANC_DATA_EXT_MASK bit of the host interface must be set LOW. Ancillary data packet extraction begins in the following frame (see [Figure 4-31: Ancillary Data Extraction - Step A](#)).

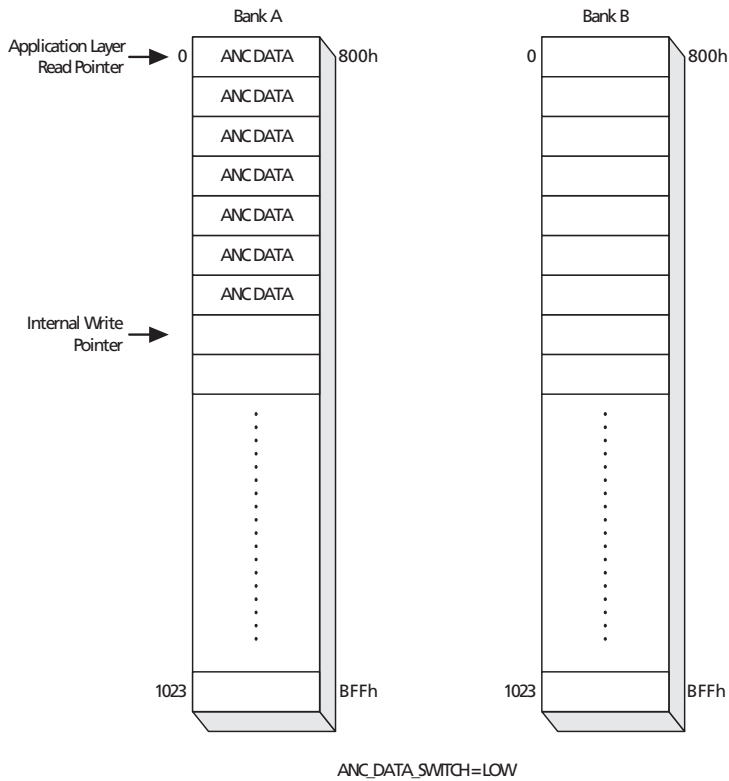


Figure 4-31: Ancillary Data Extraction - Step A

Ancillary data is written into Bank A until full. The Y/1ANC and C/2ANC output flags can be used to determine the length of the ancillary data extracted and when to begin reading the extracted data from memory.

While the `ANC_DATA_EXT_MASK` bit is set LOW, the `ANC_DATA_SWITCH` bit can be set HIGH during or after reading the extracted data. New data is then written into Bank B (up to 1024 x 16-bit words), at the corresponding host interface addresses (see [Figure 4-32: Ancillary Data Extraction - Step B](#)).

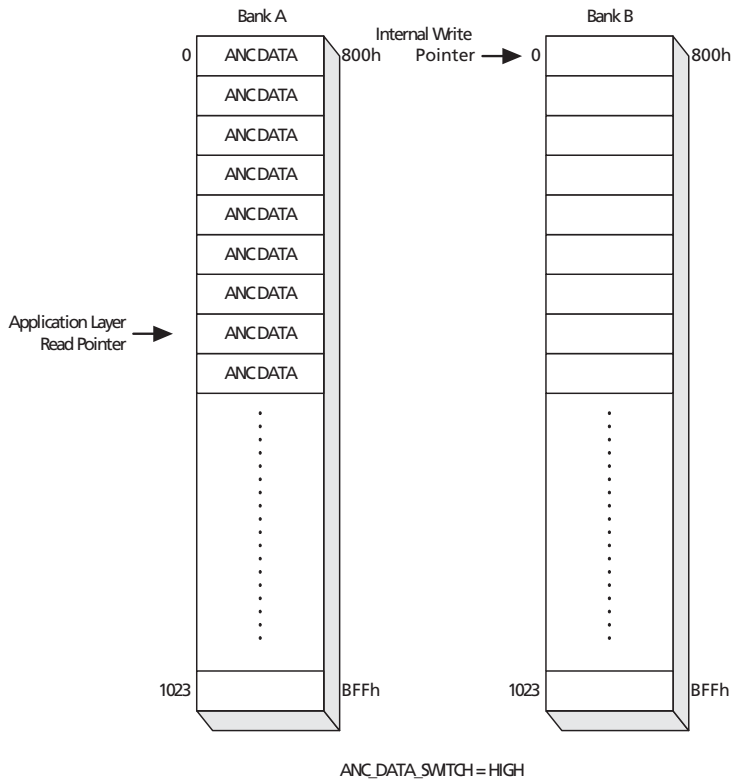


Figure 4-32: Ancillary Data Extraction - Step B

To read the new data, toggle the ANC_DATA_SWITCH bit LOW. The old data in Bank A is cleared to zero and extraction continues in Bank B (see [Figure 4-33: Ancillary Data Extraction - Step C](#)).

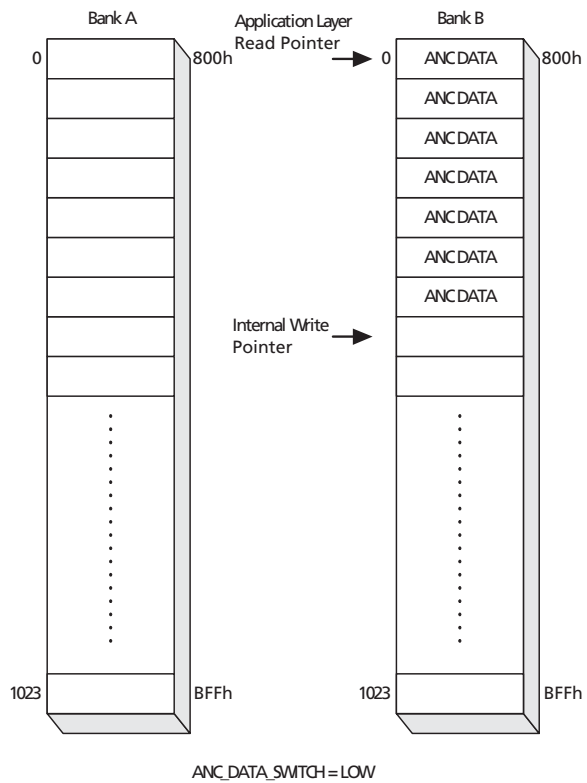


Figure 4-33: Ancillary Data Extraction - Step C

If the ANC_DATA_SWITCH bit is not toggled, extracted data is written into Bank B until full. To continue extraction in Bank A, the ANC_DATA_SWITCH bit must be toggled HIGH (see [Figure 4-34: Ancillary Data Extraction - Step D](#)).

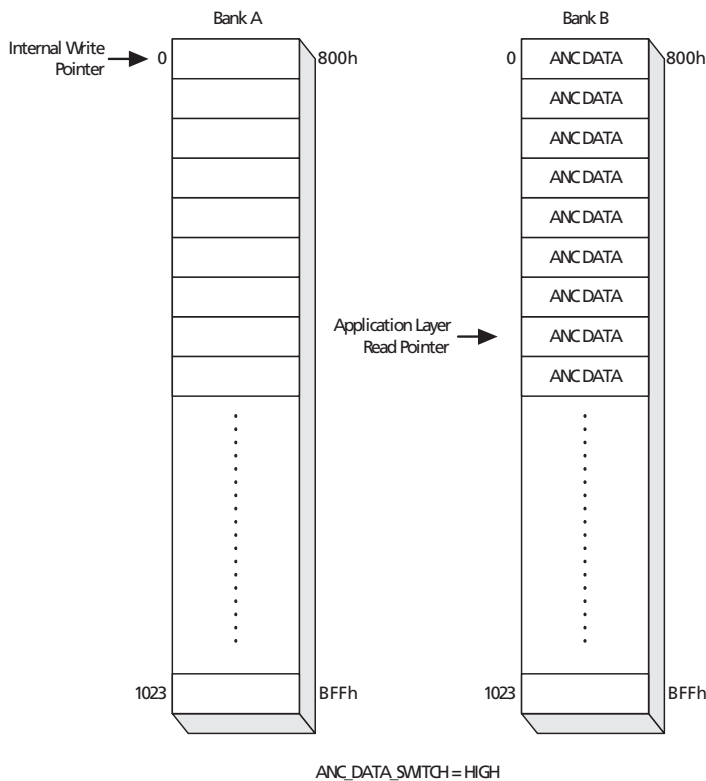


Figure 4-34: Ancillary Data Extraction - Step D

Toggling the ANC_DATA_SWITCH bit LOW returns the process to step A (Figure 4-31).

Note 1: Toggling the ANC_DATA_SWITCH must occur at a time when no extraction is taking place, i.e. when the both the Y/1ANC and C/2ANC signals are LOW.

To turn extraction off, the ANC_DATA_EXT_MASK bit must be set HIGH.

In HD mode, the device can detect ancillary data packets in the Luma video data only, Chroma video data only, or both. By default (at power-up or after a system reset) the device extracts ancillary data packets from the luma channel only.

In 3G mode Level A, the device can detect ancillary data packets in Luma video (Data Stream One) only, Chroma video (Data Stream Two) only, or both. By default (at power-up or after a system reset) the device extracts ancillary data packets from Data Stream One only.

In 3G mode Level B mode, the device can detect ancillary data packets in Luma video only, Chroma video only, or both from either Link A or Link B. Selection of Link A or Link B for ANC data extraction is done via the host interface. By default (at power-up or after a system reset) the device extracts ancillary data packets from Link A Luma only.

To extract packets from the Chroma/Data Stream Two channel only, the HD_ANC_C2 bit of the host interface must be set HIGH. To extract packets from both Luma/Data Stream One and Chroma/Data Stream Two video data, the HD_ANC_Y1_C2 bit must be set HIGH (the setting of the HD_ANC_C2 bit is ignored).

The default setting of both the HD_ANC_C2 and HD_ANC_Y1_C2 is LOW. The setting of these bits is ignored when the device is configured for SD video standards.

Ancillary data packet extraction and deletion is disabled when the IOPROC_EN/ $\overline{\text{DIS}}$ pin is set LOW.

After extraction, the ancillary data may be deleted from the video stream by setting the ANC_DATA_DEL bit of the host interface HIGH. When set HIGH, all existing ancillary data is removed and replaced with blanking values. If any of the ANC_TYPE registers are programmed with a DID and/or DID and SDID, only the ancillary data packets with the matching IDs are deleted from the video stream.

Note 2: After the ancillary data determined by the ANC_TYPE_X_APX registers has been deleted, other existing ancillary data may not be contiguous. The device does not concatenate the remaining ancillary data.

Note 3: Reading extracted ancillary data from the host interface must be performed while there is a valid video signal present at the serial input and the device is locked (LOCKED signal is HIGH).

4.18.9 Level B to Level A Conversion

When IOPROC_2 register bit LEVEL_B2A_CONV_DISABLE_MASK is HIGH (default), the GS2970A does not convert 3G LEVEL B streams between Level A and Level B mapping formats.

When LEVEL_B2A_CONV_DISABLE_MASK is LOW, the GS2970A converts a 3G 1080p Level B stream to the Level A mapping format, as per SMPTE ST 425.

The device assumes that Link A and Link B are phase-aligned at the transmitter.

The output data are line multiplexed such that the data content from Link A and Link B are assembled in a continuous fashion, at twice the input data rate. Extracted timing reference information is used to trigger a line counter which embeds the correct line number according to SMPTE ST 425.

The Level B/A conversion acts only on the active picture, ANC data can become corrupt outside of this region. In order to ensure that the embedded ANC data remains valid, we recommend extracting the ANC data with the receiver prior to the Level B/A conversion taking place.

Note 1: If Level B/A conversion is enabled, previous ST 352 Payload ID packets are not deleted from the data stream.

Note 2: When Level B/A conversion is enabled, timing reference information (FVH) present on the STAT outputs is not phase-aligned with the output video data, and should not be used for line or frame synchronization activities. Being that CEA 861 timing is derived from (FVH) timing reference information, it too should not be used. During Level B to Level A conversion, it is advised that the user generates the H and V timing signals from the embedded TRS words.

Note 3: If the GS2970A sees a synchronous switch where the difference in phases between two Level B inputs is greater than $\sim 10.7\mu\text{s}$, the user may observe a missing H pulse on the line following the switch line, when Level B/A conversion is enabled.

Note 4: Discontinuities in the line of video at the input of the Level B to A converter can cause erroneous mapping to the Level A format. Therefore, when enabling B to A conversion or enabling/disabling audio, it is recommended to reset the Level B to A converter with the following sequence:

1. Assert the B to A converter reset by writing '1' to bit 3 of register 05Eh.
2. Monitor H-pulse for a high-to-low transition.
3. De-assert the B to A converter reset by writing '0' to bit 3 of register 05Eh. This must be completed at the beginning of SAV and should be completed in 1920 PCLK periods.

4.19 Audio De-embedder

The GS2970A includes an integrated audio de-embedder which is enabled by default in SMPTE mode. It can be disabled by setting the AUDIO_EN/ $\overline{\text{DIS}}$ pin LOW, or by setting the host interface AUD_EXT_MASK bit to HIGH, or by keeping IOPROC_EN/ $\overline{\text{DIS}}$ pin LOW. In non-SMPTE modes, the audio de-embedder is not active.

Up to eight channels of audio may be extracted from the received serial digital video stream. The output signal formats supported by the device include AES/EBU, I²S (default) and industry standard serial digital formats.

16, 20 and 24-bit audio bit depths are supported for 48kHz synchronous audio for SD data rates. For HD and 3G data rates, 16, 20 and 24-bit audio bit depths are supported for 48kHz audio. The audio may be synchronous or asynchronous to the video.

In 3G mode:

- In Level A mode, all Audio Control Packets are extracted from Data Stream One and all Audio Data Packets are extracted from Data Stream Two, in accordance with SMPTE ST 425. This is similar to HD, in which Audio Control Packets are embedded in the Luma channel and audio data packets in the Chroma channel
- In Level B mode, extraction of audio packets from Link A (default) or Link B is selectable via the AUDIO_SEL_DS2_ $\overline{\text{DS1}}$ bit in the host interface

Additional audio processing features include audio mute on loss of lock, de-embed and delete, group selection, audio output re-mapping, ECC error detection and correction (HD/3G modes only), and audio channel status extraction.

4.19.1 Serial Audio Data I/O Signals

The Serial Audio Data I/O pins are listed in [Table 4-16: Serial Audio Pin Descriptions](#).

Table 4-16: Serial Audio Pin Descriptions

| Pin Name | Description |
|-----------------------------------|---------------------------------------|
| AUDIO_EN/ $\overline{\text{DIS}}$ | Enable Input for Audio Processing |
| AOUT_1/2 | Serial Audio output; Channels 1 and 2 |
| AOUT_3/4 | Serial Audio output; Channels 3 and 4 |
| AOUT_5/6 | Serial Audio Output; Channels 5 and 6 |
| AOUT_7/8 | Serial Audio Output; Channels 7 and 8 |
| ACLK | 64fs clock |

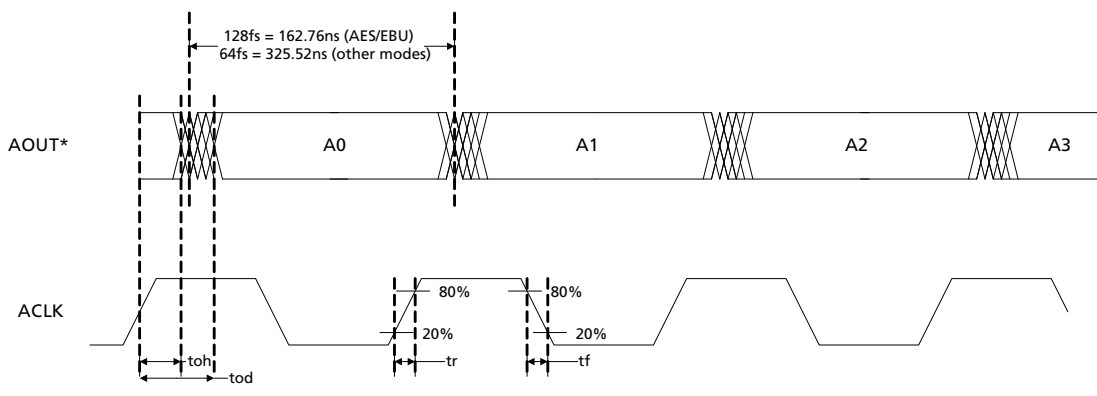
Table 4-16: Serial Audio Pin Descriptions (Continued)

| Pin Name | Description |
|----------|---|
| WCLK | Word clock |
| AMCLK | Audio Master Clock, selectable 128fs, 256fs, or 512fs |

The timing of the serial audio output signals and the ACLK output signal is shown in Figure 4-35: ACLK to Data Signal Output Timing.

I/O Timing Specs:

Audio Outputs:



| | Audio Outputs | | | | | | | | | | | |
|------|---------------|-------------|-------------------|---------|-------------|-------------------|---------|-------------|-------------------|---------|-------------|-------------------|
| | 3.3V | | | | | | 1.8V | | | | | |
| AOUT | toh | tr/tf (min) | C _{LOAD} | tod | tr/tf (max) | C _{LOAD} | toh | tr/tf (min) | C _{LOAD} | tod | tr/tf (max) | C _{LOAD} |
| | 1.500ns | 0.600ns | 6 pF | 7.000ns | 2.200ns | 15 pF | 1.500ns | 0.600ns | 6 pF | 7.000ns | 2.300ns | 15 pF |

Figure 4-35: ACLK to Data Signal Output Timing

When AUDIO_EN/ $\overline{\text{DIS}}$ is set HIGH, audio extraction is enabled and the audio output signals are extracted from the video data stream. When set LOW, the serial audio outputs, ACLK and WCLK outputs are set LOW.

In addition, all functional logic associated with audio extraction is disabled to reduce power consumption.

4.19.2 Serial Audio Data Format Support

The GS2970A supports the following serial audio data formats:

- I²S (default)
- AES/EBU
- Serial Audio Left Justified, MSB First
- Serial Audio Left Justified, LSB First
- Serial Audio Right Justified, MSB First
- Serial Audio Right Justified, LSB First (this mode is not supported in SD)

By default (at power up or after system reset) I²S is selected. The other data formats are selectable via the host interface using the AMA/AMB[1:0] bits.

Table 4-17: Audio Output Formats

| AMA/AMB[1:0] | Audio Output Format |
|--------------|---|
| 00 | AES/EBU audio output |
| 01 | Serial audio output: Left Justified; MSB first |
| 10 | Serial audio output: Right Justified; MSB first |
| 11 | I ² S (Default) |

The serial audio output formats may use LSB first according to the settings of the control bits LSB_FIRSTA, LSB_FIRSTB, LSB_FIRSTC, and LSB_FIRSTD. When in I²S mode, these control bits must all be set LOW (default).

When I²S format is desired, both groups must be set to I²S (i.e. AMA = AMB = 11). This is because they share the same WCLK.

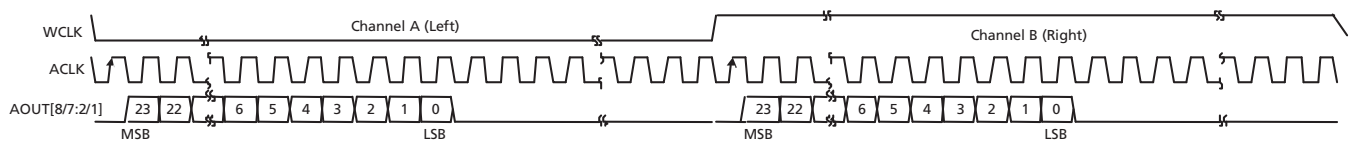


Figure 4-36: I²S Audio Output Format

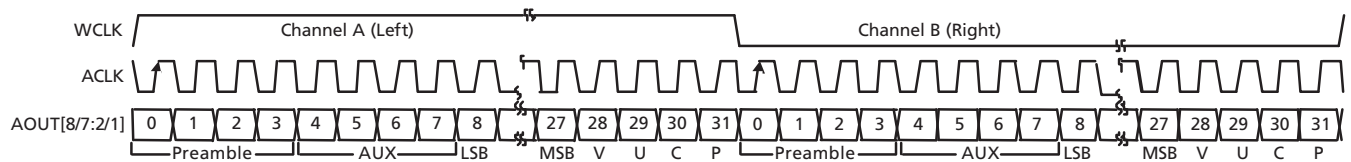


Figure 4-37: AES/EBU Audio Output Format

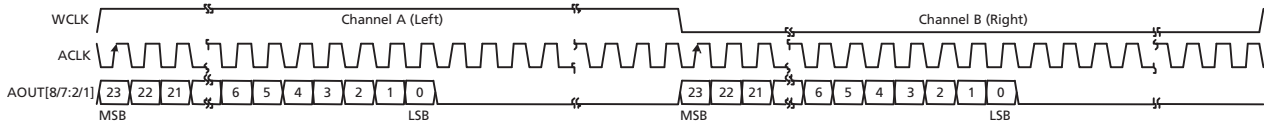


Figure 4-38: Serial Audio, Left Justified, MSB First

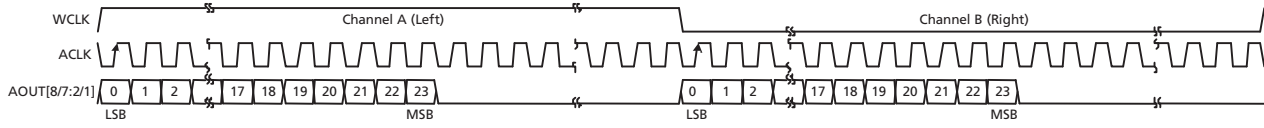


Figure 4-39: Serial Audio, Left Justified, LSB First

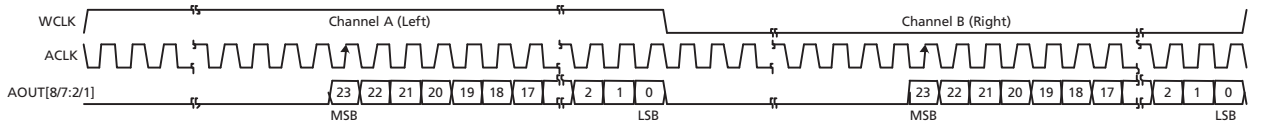


Figure 4-40: Serial Audio, Right Justified, MSB First

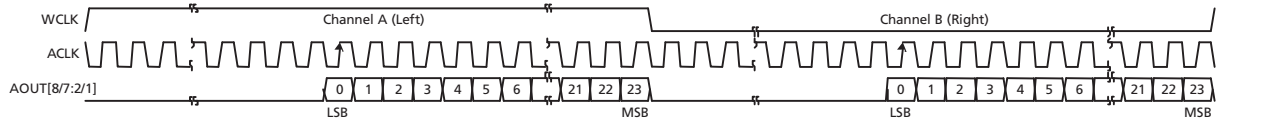


Figure 4-41: Serial Audio, Right Justified, LSB First

4.19.2.1 AES/EBU Mode

In AES/EBU output mode, the audio de-embedder uses a 128fs (6.144MHz audio bit clock) clock as shown in Figure 4-42.

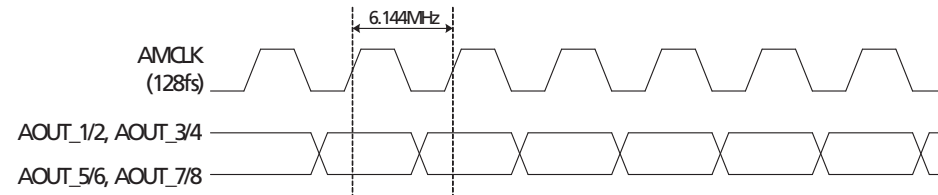


Figure 4-42: AES/EBU Audio Output to Bit Clock Timing

4.19.2.2 Audio Data Packet Extraction Block

The audio de-embedder looks for audio data packets on every line of the incoming video.

The audio data must be embedded according to SMPTE ST 272 (SD) or SMPTE ST 299 (HD or 3G).

In 3G Level A signals, the audio data packets must be embedded only in Data Stream Two.

In 3G Level B signals, the audio data packets must be embedded in the Chroma streams of either Link A or Link B.

The Audio Group Detect registers are set HIGH when audio data packets with a corresponding group DID are detected in the input video stream. The host interface reports the individual audio groups detected.

Table 4-18: Audio Data Packet Detect Register

| Name | Description | Default |
|-----------|---|---------|
| ADPG4_DET | Audio Group Four Data Packet Detection (1: Detected) | 0 |
| ADPG3_DET | Audio Group Three Data Packet Detection (1: Detected) | 0 |
| ADPG2_DET | Audio Group Two Data Packet Detection (1: Detected) | 0 |
| ADPG1_DET | Audio Group One Data Packet Detection (1: Detected) | 0 |

When an audio data packet with a DID set in IDA[1:0] and IDB[1:0] is detected, the audio sample information is extracted and written into the audio FIFO.

The embedded audio group selected by IDA[1:0] is described henceforth in this document as Group A or Primary Group. The embedded audio group selected by IDB[1:0] is described henceforth in this document as Group B or Secondary Group.

Due to the large size of the horizontal ancillary data space in 720p/24, 720p/25 and 720p/30 video standards, the maximum number of ancillary data words the audio de-embedder can process is limited to 1024 when configured for these standards.

4.19.2.3 Audio Control Packets

The audio de-embedder automatically detects the presence of audio control packets in the video stream. When audio control packets for audio Group A are detected, the CTRA_DET bit of the host interface is set HIGH. When audio control packets for audio Group B are detected, the CTRB_DET bit of the host interface is set HIGH.

The audio control packet data is accessible via the host interface.

The audio control packets must be embedded according to SMPTE ST 272 (SD) or SMPTE ST 299 (HD and 3G). In 3G Level A signals, the audio control packets must be embedded only in Data Stream One. In 3G Level B signals the audio control packets must be embedded in the Luma streams of each link that carries audio.

Note 1: In SD, the control packet host interface registers are updated with new control packet values, after the CTRA_DET/CTRB_DET flags are cleared. In HD, the update happens automatically.

Note 2: If there is an HD audio packet checksum error, no audio is extracted. The audio packet is not recognized, and the audio stays in the video stream. If nothing but the CLK phase parity bit is wrong, the audio will extract fine.

4.19.2.4 Setting Packet DID

Table 4-19 below, shows the 2-bit host interface setting for the audio group DID's.

For 24-bit audio support in SD mode, extended audio packets for Group A must have the same group DID set in IDA[1:0] of the host interface. Extended audio packets for Group B must have the same group DID set in IDB[1:0] of the host interface.

The audio de-embedder automatically detects the presence of extended audio packets. When detected, the audio output format is set to 24-bit audio sample word length.

The audio de-embedder defaults to audio Groups One and Two, where Group A is extracted from packets with audio Group One DID, and Group B from packets with audio Group Two DID.

Table 4-19: Audio Group DID Host Interface Settings

| Audio Group | SD Data DID | SD Extended DID | HD Data DID | SD Control DID | HD Control DID | Host Interface Register Setting (2-bit) |
|-------------|-------------|-----------------|-------------|----------------|----------------|---|
| 1 | 2FFh | 1FEh | 2E7h | 1EFh | 1E3h | 00b |
| 2 | 1FDh | 2FCh | 1E6h | 2EEh | 2E2h | 01b |
| 3 | 1FBh | 2FAh | 1E5h | 2EDh | 2E1h | 10b |
| 4 | 2F9h | 1F8h | 2E4h | 1ECh | 1E0h | 11b |

Table 4-20: Audio Data and Control Packet DID Setting Register

| Name | Description | Default |
|----------|---|---------|
| IDA[1-0] | Group A Audio data and control packet DID setting | 00b |
| IDB[1-0] | Group B Audio data and control packet DID setting | 01b |

Note: To keep sample delays between audio channels the same after changing the value of IDA or IDB in the SD audio core, the audio FIFOs must be cleared. This is accomplished by asserting CLEAR_AUDIO and de-asserting at least one frame later. When the FIFOs are in the clear state, audio will be muted, but audio clocks will continue to run.

4.19.2.5 Audio Packet Delete Block

To delete all ancillary data with a group DID shown in Table 4-19, the ALL_DEL bit in the host interface must be set HIGH.

4.19.2.6 ECC Error Detection & Correction Block (HD Mode Only)

The audio de-embedder performs BCH(31,25) forward error detection and correction, as described in SMPTE ST 299. The error correction for all embedded audio data packets is activated when the host interface ECC_OFF bit is set LOW (default LOW). The audio de-embedder corrects any errors in both the audio output and the embedded packet.

When a one-bit error is detected in a bit array of the ECC protected region of the audio data packet with audio group DID set in IDA[1:0], the ECCA_ERROR flag is set HIGH. When a one-bit error is detected in the ECC protected region of the audio data packet with audio group DID set in IDB[1:0], the ECCB_ERROR flag is set HIGH.

Figure 4-43 shows examples of error correction and detection. Up to 8 bits in error can be corrected, providing each bit error is in a different bit array (shown below). When there are two or more bits in error in the same 24-bit array, the errors are detected, but not corrected.

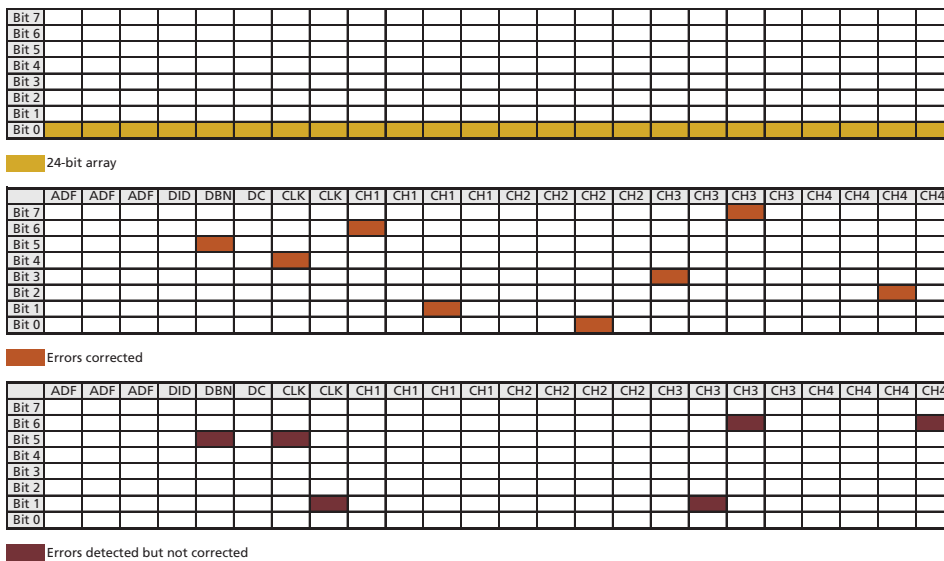


Figure 4-43: ECC 24-bit Array and Examples

4.19.3 Audio Processing

4.19.3.1 Audio Clock Generation

For SD and HD/3G audio, a single set of audio frequencies is generated for all audio channels, using a Direct Digital Period Synthesizer (DDPS) to minimize jitter.

- For Mapping structure one signals (1080p 50, 59.94 or 60), the pixel clock is $148.5/(M)$ MHz, and the phase data are based on this rate. An Audio Master Clock (AMCLK) is also generated. The frequency is selectable via the host interface as:
 - ♦ $f_s \times 128$

- ◆ fs x 256
- ◆ fs x 512

In SD mode, audio clocks are derived from the PCLK.

In HD/3G modes, the input control for the DDPS is derived from the two embedded audio clock phase words in the audio data packet corresponding to Group A. The audio clock phase information used is taken from the first embedded audio packet in the HANC space. With no embedded audio present, the device will not generate ACLK or WCLK. The IGNORE_PHASE bit should be asserted in this case to ensure the proper AMCLK frequency is generated.

The audio de-embedder also includes a Flywheel block to overcome any inconsistencies in the embedded audio clock phase information.

If the audio phase data is not present in the audio data packets, or is incorrect, the NO_PHASEA_DATA bit in the host interface is set and the clock will free-run based on the detected video format, the PCLK and the M value. IGNORE_PHASE should be set HIGH when NO_PHASEA_DATA is set. This does not occur automatically.

When the IGNORE_PHASE bit in the host interface is set HIGH, it is recommended that the M value be programmed via the host interface. This can be done by setting the FORCE_M bit HIGH, and programming the desired value into FORCE_MEQ1001. The correct value can be obtained by reading the M bit from the Video Core Registers.

If the DDPS is locked to phase data and audio data packets are lost or corrupted, the Clock Generator will flywheel for up to four audio data packets. If no valid audio data packet with valid phase data is provided within this time, the Clock Generator will free-run based on the video format, the PCLK and the M value.

If the IGNORE_PHASE bit in the host interface is HIGH, the clock will free-run based on the video format, the PCLK and the M value, independent of the NO_PHASEA_DATA bit.

In the 720p/24 video format, the total line length is 4125 pixels, which requires a resolution of 13 bits for the audio clock phase words in the embedded audio data packets. SMPTE ST 299 only specifies a maximum of 12 bits resolution. Proposed changes to SMPTE ST 299 suggest using bit 5 of UDW1 (currently reserved and set to zero) in the audio data packet as the MSB (ck13) for the audio clock phase data, providing 13 bits resolution.

Some audio encoders may hold the clock phase value at a maximum value when reached, until reset at the end of the line. This produces a small amount of audio phase jitter for the period of one sample.

To overcome this issue, the audio de-embedder checks for all cases. On detection of the maximum value, a comparison is made between previous clock phases and the correct position interpolated. If the clock phase data value starts to decrease, the de-embedder checks to see if bit 5 (ck13) of UDW1 in the audio data packet is set. If ck13 is set, the correct value is used. If ck13 is not set, the correct position is interpolated.

4.19.3.2 Detect Five-Frame Sequence Block

Five-frame sequence detection is required for 525-line based video formats only. The audio de-embedder checks the Audio Frame Number sequence in the audio control packets, when present. If the audio frame sequence is running (repeated 1 to 5 count), the audio de-embedder uses this information to determine the five-frame sequence. If

the audio control packet is not present, or the Audio Frame Number words are set to 200h, the audio de-embedder detects the five-frame sequence by counting the number of samples per frame. Figure 4-44 shows the number of samples per frame over a five-frame sequence.

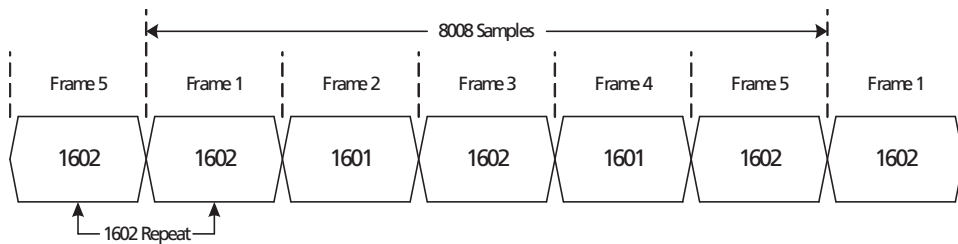


Figure 4-44: Sample Distribution over 5 Video Frames (525-line Systems)

When the audio inputs are asynchronously switched or disrupted, the audio de-embedder continues to write audio samples into the audio buffer, based on the current five-frame sequence. The de-embedder then re-locks to the new 5-frame sequence, at which point a sample may be lost.

Note: In SD, all four channel pairs must follow the same five-frame sequence.

4.19.3.3 Audio FIFO Block

The function of the FIFO block is to change the audio data word rate from the ANC rate multiplexed with the video signal to the 48kHz audio output rate.

The audio FIFO block contains the audio sample buffers; one per audio channel. Each buffer is 36 audio samples deep. At power up or reset, the read pointer is held at the zero position until 26 samples have been written into the FIFO (allows for 6 lines per frame with no audio samples; a maximum of 4 samples per line in SD Mode). See Figure 4-45.

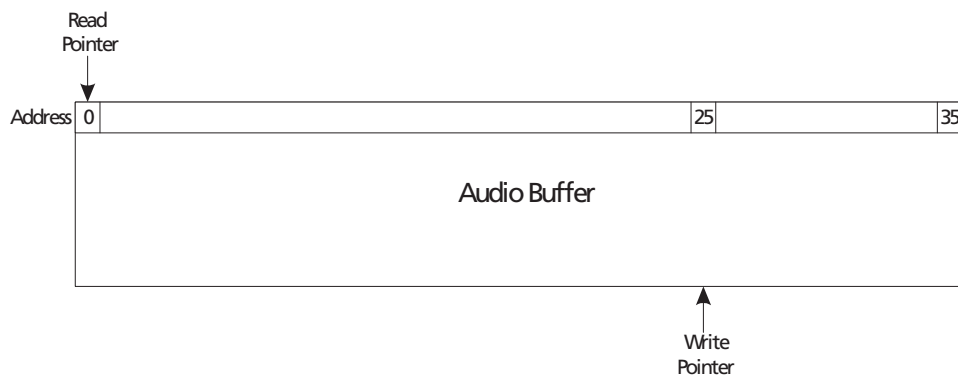


Figure 4-45: Audio Buffer After Initial 26 Sample Write

The position of the write pointer with respect to the read pointer is monitored continuously. If the write pointer is less than 6 samples ahead of the read pointer (point A in Figure 4-46), a sample is repeated from the read-side of the FIFO. If the write pointer is less than 6 samples behind the read pointer (point B in Figure 4-46), a sample is dropped. This avoids buffer underflow/overflow conditions.

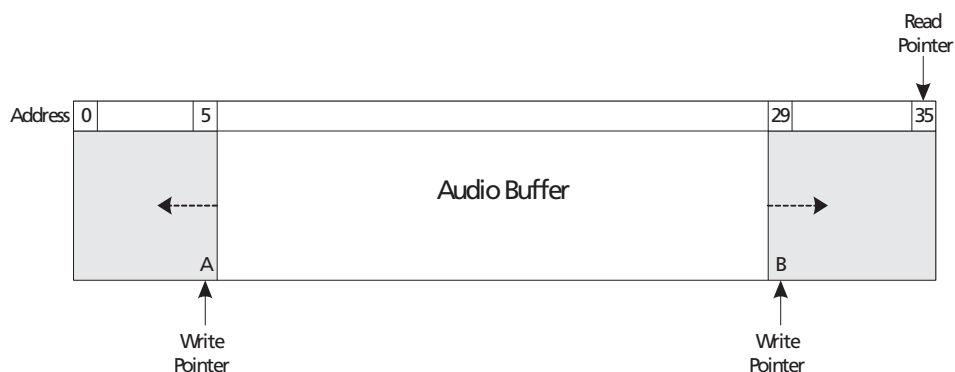


Figure 4-46: Audio Buffer Pointer Boundary Checking

The repeat or drop sample operation is performed a maximum of 28 consecutive times, after which the audio outputs are muted (all sample data set to zero). In SD Mode, 26 samples are required to be written into the FIFO prior to starting the read operation again.

The audio buffer pointer offset may be reduced from 26 samples to 12 or 6 samples using the OS_SEL[1:0] bits in the host interface. The default setting is 26 samples (see Table 4-21).

When the OS_SEL[1:0] bits are set for 6-sample pointer offset, no boundary-checking is performed.

In HD mode the audio FIFO is a maximum of 10 samples deep. According to SMPTE ST 299, audio samples are multiplexed immediately in the next HANC region after the audio sample occurs.

Table 4-21: Audio Buffer Pointer Offset Settings

| OS_SEL[1:0] | Buffer Pointer Offset |
|-------------|-----------------------|
| 00 | 26 samples (default) |
| 01 | 12 samples |
| 10 | 6 samples |

Sample Delay

When extracting SD audio, certain conditions can cause the sample delay through the audio FIFOs to be 1-4 samples different between channels.

If delays through the audio FIFOs must be the same, it is recommended that the FIFO size gets set to 22 or 16 with OS_SEL[1:0]. Additionally, the audio FIFO must be cleared when either of the following occurs:

1. Loss of lock. The FIFO should be cleared when the part has relocked.
2. When one of the groups of audio disappears and re-appears. Poll the audio data packet detected registers ADPG1_DET, ADPG2_DET, ADPG3_DET, and ADPG4_DET once every frame. If one of the groups currently de-embedded disappears and re-appears, clear the audio FIFO after the group re-appears.

Clear the audio FIFO by asserting CLEAR_AUDIO and de-asserting at least one frame later. When the FIFOs are in the clear state, audio will be muted but audio clocks will continue to run.

When switching between 525 and 625 formats, it is recommended that the device be reset to keep the delays through the audio FIFO the same between channels.

4.19.3.4 Audio Crosspoint Block

The Audio Crosspoint is used for audio output channel re-mapping. This feature allows any of the selected audio channels in Group A or Group B to be output on any of the eight output channels. The default setting is for one to one mapping, where AOUT_1/2 is extracted from Group A CH1 and CH2, AOUT_3/4 is extracted from Group A CH3 and CH4, and so on.

Note: If audio samples from embedded audio packets with the group set in IDA[1:0] are to be paired with samples from the group set in IDB[1:0], all of the channels must have been derived from the same Word Clock and must be synchronous.

The output channel is set in the OPn_SRC[2:0] host interface registers. [Table 4-22](#) lists the 3-bit address for audio channel mapping.

Table 4-22: Audio Channel Mapping Codes

| Audio Output Channel | 3-bit Host Interface Source Address |
|----------------------|-------------------------------------|
| 1 | 000 |
| 2 | 001 |
| 3 | 010 |
| 4 | 011 |
| 5 | 100 |
| 6 | 101 |
| 7 | 110 |
| 8 | 111 |

4.19.3.5 Serial Audio Output Word Length

The audio output, in serial modes, has a selectable 24, 20 or 16-bit sample word length. The ASWL[1:0] host interface register is used to configure the audio output sample word length. [Figure 4-23](#) shows the host interface 2-bit code for setting the audio sample word length. When the presence of extended audio packets is detected in SD modes, the audio de-embedder defaults to 24-bit audio sample word length.

Table 4-23: Audio Sample Word Lengths

| ASWL[1:0] | Audio Sample Word Length (SD) | Audio Sample Word Length (HD) |
|-----------|-------------------------------|-------------------------------|
| 00 | 24-bit | 24-bit |
| 01 | 20-bit | 20-bit |
| 10 | 16-bit | 16-bit |
| 11 | Auto 24/20-bit (Default) | Reserved (Default) |

Note: By default, at power-up, the word length is set to 12 bits. The desired word length should be programmed through the host interface.

4.19.3.6 Audio Channel Status

The GS2970A detects the AES/EBU Audio Channel Status (ACS) block information for each of the selected channel pairs.

ACS data detection is indicated by corresponding ACS_DET flag bits in the host interface. The flag is cleared by writing to the same location.

4.19.3.7 Audio Channel Status Read

AES/EBU ACS data is available separately for each of the channels in a stereo pair. The GS2970A defaults to reading the first channel of each pair. There are 184 bits in each ACS packet, which are written to twelve 16-bit right-justified registers in the host interface.

The ACS_USE_SECOND bit (default LOW) selects the second channel in each audio pair when set HIGH.

Once all of the ACS data for a channel has been acquired, the corresponding ACS_DET bit is set, and acquisition stops. The ACS data is overwritten with new data when the ACS_DET bit is cleared in the system.

4.19.3.8 Audio Channel Status Regeneration

When the ACS_REGEN bit in the host interface is set HIGH, the audio de-embedder embeds the 24 bytes of the Audio Channel Status information programmed in the ACSR[183:0] registers into the 'C' bit of the AES/EBU outputs. The same Audio Channel Status information is used for all output channels.

In order to apply ACSR data;

- Set the ACS_REGEN bit to logic HIGH
- Write the desired ACSR data to the ACSR registers
- Set the ACS_APPLY bit to HIGH

At the next status boundary, the device outputs the contents of the ACSR registers as ACS data. This event may occur at a different time for each of the output channels. While waiting for the status boundary, the device sets the appropriate ACS_APPLY_WAIT[A:D] flag.

Table 4-24 shows the host interface default settings for the Audio Channel Status block. The audio de-embedder automatically generates the CRC word.

Table 4-24: Audio Channel Status Information Registers

| Name | Description | Default |
|-------------------------------|--|-------------------|
| ACSR[7-0] | Audio channel status block byte 0 set. Used when ACS_REGEN is set HIGH | 85h |
| ACSR[15-8] | Audio channel status block byte 1 set. Used when ACS_REGEN is set HIGH | 08h |
| ACSR[23-16] | Audio channel status block byte 2 set. Used when ACS_REGEN is set HIGH | 28h (SD) 2Ch (HD) |
| ACSR[31-24]: ACSR[183-176] | Audio channel status block data for bytes 3 to 22. Used when ACS_REGEN is set HIGH | 00h |
| ACS_REGEN | Audio channel status regenerate | 0 |
| ACS_APPLY | Apply new ACSR data | 0 |
| ACS_APPLY_W AIT[A:D] | Waiting to apply new ACSR data | 0 |
| ACS[7-0]: ACS[183-176] | Audio channel status block data for bytes 0 to 22 | 00h: 00h |

Table 4-25: Audio Channel Status Block for Regenerate Mode Default Settings

| Name | Byte | Bit | Default | Mode |
|----------------------------|------|-----|---------|--|
| PRO | 0 | 0 | 1b | Professional use of channel status block |
| Emphasis | 0 | 2-4 | 100b | 100b None. Rec. manual override disabled |
| Sample Frequency | 0 | 6-7 | 01b | 48kHz. Manual override or auto disabled |
| Channel Mode | 1 | 0-3 | 0001b | Two channels. Manual override disabled |
| AUX | 2 | 0-2 | 000b | SD Modes: Maximum audio word length is 20 bits |
| | | | 001b | HD Mode: Maximum audio word length is 24 bits |
| Source Word Length | 2 | 3-5 | 101b | Maximum word length (based on AUX setting). 24-bit for HD Mode; 20-bit for SD Modes |
| All other bits set to zero | | | | |

4.19.3.9 Audio Mute

When the MUTE bits in the host interface are set HIGH, the audio outputs are muted (all audio sample bits are set to zero). To set all the audio output channels to mute, set the host interface MUTE_ALL bit HIGH.

Table 4-26: Audio Mute Control Bits

| Name | Description | Default |
|----------|--------------------------------------|---------|
| MUTE_ALL | Ch1-8 audio mute enable (1: Enabled) | 0 |
| MUTE8 | Ch8 audio mute enable (1: Enabled) | 0 |
| MUTE7 | Ch7 audio mute enable (1: Enabled) | 0 |
| MUTE6 | Ch6 audio mute enable (1: Enabled) | 0 |
| MUTE5 | Ch5 audio mute enable (1: Enabled) | 0 |
| MUTE4 | Ch4 audio mute enable (1: Enabled) | 0 |
| MUTE3 | Ch3 audio mute enable (1: Enabled) | 0 |
| MUTE2 | Ch2 audio mute enable (1: Enabled) | 0 |
| MUTE1 | Ch1 audio mute enable (1: Enabled) | 0 |

Mute On Loss Of Lock

When the GS2970A loses lock (LOCKED signal is LOW), the audio de-embedder sets all audio outputs LOW (no audio formatting is performed). The ACLK, WCLK and AMCLK outputs are also forced LOW.

4.19.4 Error Reporting

4.19.4.1 Data Block Number Error

When the 1-255 count sequence in the Data Block Number (DBN) word of Group A audio data packets is discontinuous, the DBNA_ERR bit in the host interface AUDIO_ERROR_STAT_X register is set HIGH. When the 1-255 count sequence in the DBN word of Group B audio data packets is discontinuous, the DBNB_ERR bit in the AUDIO_ERROR_STAT_X register is set HIGH.

The DBNA_ERR and DBNB_ERR flags also have associated SD_AUDIO_ERROR_MASK and HD_AUDIO_ERROR_MASK register flags for configuration of error reporting in the Receiver. The DBNA_ERR and DBNB_ERR flags remains set until cleared by writing to these locations.

4.19.4.2 ECC Error

The GS2970A monitors the ECC error status of the two selected audio groups, as described in [Section 4.19.2.6 on page 86](#).

The ECC[N]_ERROR flags also have associated SD_AUDIO_ERROR_MASK and HD_AUDIO_ERROR_MASK register flags for configuration of error reporting in the Receiver. The ECC[N]_ERROR flags remain set until read via the host interface.

4.20 GSPI - HOST Interface

The GSPI, or Gennum Serial Peripheral Interface, is a 4-wire interface provided to allow the system to access additional status and control information through configuration registers in the GS2970A.

The GSPI is comprised of a Serial Data Input signal (SDIN), Serial Data Output signal (SDOUT), an active low Chip Select (\overline{CS}), and a Burst Clock (SCLK).

Because these pins are shared with the JTAG interface port, an additional control signal pin JTAG/ \overline{HOST} is provided.

When JTAG/ \overline{HOST} is LOW, the GSPI interface is enabled. When JTAG/ \overline{HOST} is HIGH, the JTAG interface is enabled.

When operating in GSPI mode, the SCLK, SDIN, and \overline{CS} signals must be provided by the system. The SDOUT pin is a non-clocked loop-through of SDIN and may be connected to the SDIN of another device, allowing multiple devices to be connected to the GSPI chain. See Section 4.20.2 for details. The interface is illustrated in the Figure 4-47 below.

Note: When using more than one Semtech serializer or deserializer (SerDes) in the same design, the SDOUT pins of multiple SerDes ICs must not be bussed together as was done with older generations of Semtech SerDes ICs

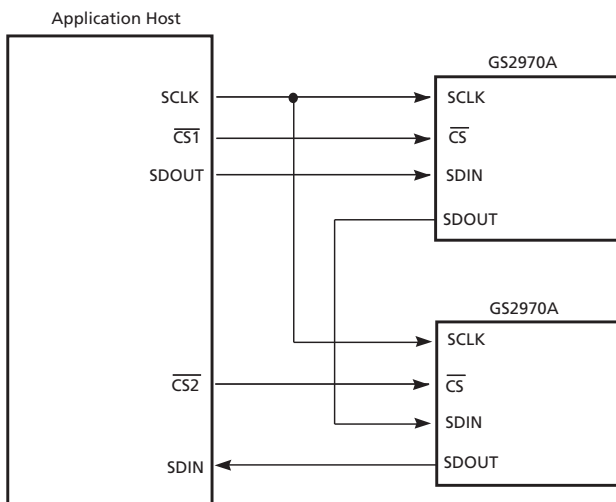


Figure 4-47: GSPI Application Interface Connection

All read or write access to the GS2970A is initiated and terminated by the system host processor. Each access always begins with a Command/Address Word, followed by a data write to, or data read from, the GS2970A.

4.20.1 Command Word Description

The Command Word consists of a 16-bit word transmitted MSB first and contains a read/write bit, an Auto-Increment bit and a 12-bit address.

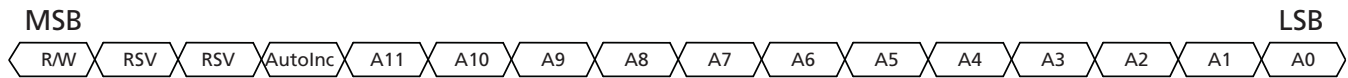


Figure 4-48: Command Word Format

Command Words are clocked into the GS2970A on the rising edge of the Serial Clock SCLK, which operates in a burst fashion. The chip select (\overline{CS}) signal must be set low a minimum of 1.5ns (t_0 in Figure 4-50) before the first clock edge to ensure proper operation.

When the Auto-Increment bit is set LOW, each Command Word must be followed by only one Data Word to ensure proper operation.

If the Auto-Increment bit is set HIGH, the following Data Word is written into the address specified in the Command Word, and subsequent Data Words are written into incremental addresses from the first Data Word. This facilitates multiple address writes without sending a Command Word for each Data Word.

Note: The RSV bits in the GSPI command word can be set to zero as placeholder, though these bits are not used.

4.20.2 Data Read or Write Access

During a read sequence (Command Word R/W bit set HIGH) serial data is transmitted or received MSB first, synchronous with the rising edge of the serial clock SCLK. The Chip Select (\overline{CS}) signal must be set low a minimum of 1.5ns (t_0 in Figure 4-50) before the first clock edge to ensure proper operation. The first bit (MSB) of the Serial Output (SDOUT) is available (t_5 in Figure 4-51) following the last falling SCLK edge of the read Command Word, the remaining bits are clocked out on the negative edges of SCLK.

Note: When several devices are connected to the GSPI chain, only one \overline{CS} may be asserted during a read sequence.

During a write sequence (Command Word R/W bit set LOW), a wait state of 37.1ns (t_4 in Figure 4-50) is required between the Command Word and the following Data Word. This wait state must also be maintained between successive Command Word/Data Word write sequences. When Auto Increment mode is selected (AutoInc = 1), the wait state must be maintained between successive Data Words after the initial Command Word/Data Word sequence.

During the write sequence, all Command and following Data Words input at the SDIN pin are output at the SDOUT pin unchanged. When several devices are connected to the GSPI chain, data can be written simultaneously to all the devices which have \overline{CS} set LOW.

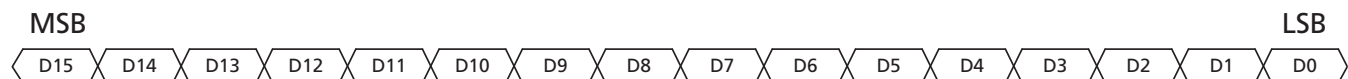


Figure 4-49: Data Word Format

4.20.3 GSPI Timing

Write and Read Mode timing for the GSPI interface;

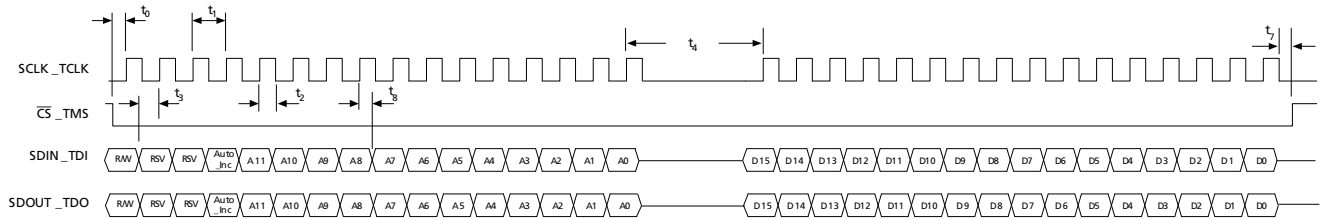


Figure 4-50: Write Mode

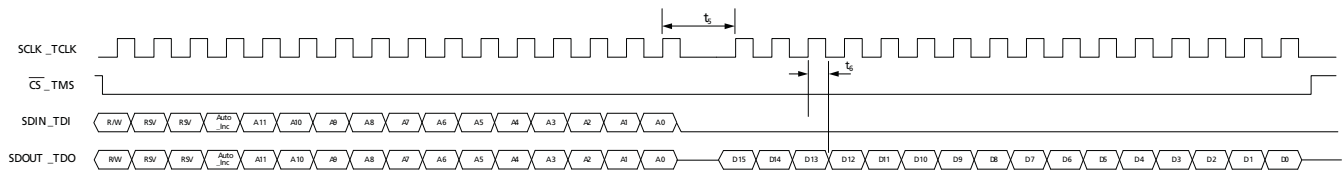


Figure 4-51: Read Mode

SDIN_TDI to SDOUT_TDO combinational path for daisy chain connection of multiple GS2970A devices.

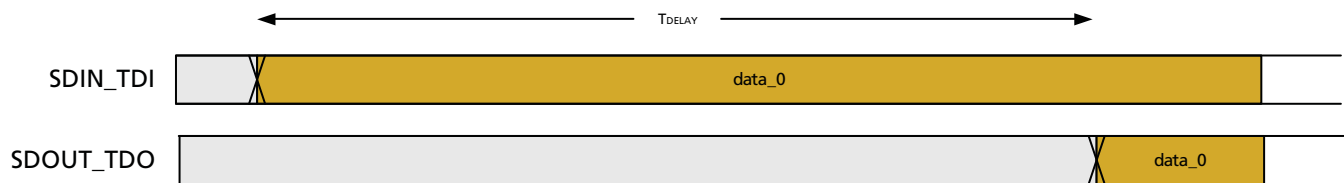


Figure 4-52: GSPI Time Delay

Table 4-27: GSPI Time Delay

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|------------|-------------|----------------------------|-----|-----|------|-------|
| Delay Time | t_{DELAY} | 50% levels; 1.8V operation | - | - | 13.1 | ns |
| Delay Time | t_{DELAY} | 50% levels; 3.3V operation | - | - | 9.7 | ns |

Table 4-28: GSPI Timing Parameters (50% levels; 3.3V or 1.8V operation)

| Parameter | Symbol | Min | Typ | Max | Units | |
|--|--------|------------|--------|-----|-------|----|
| \overline{CS} low before SCLK rising edge | t_0 | 1.5 | – | – | ns | |
| SCLK period | t_1 | 16.67 | – | – | ns | |
| SCLK duty cycle | t_2 | 40 | 50 | 60 | % | |
| Input data setup time | t_3 | 1.5 | – | – | ns | |
| Time between end of Command Word (or data in Auto-Increment mode) and the first SCLK of the following Data Word – write cycle | t_4 | PCLK (MHz) | ns | | | |
| | | unlocked | 100 | | | |
| | | 27.0 | 37.1 | – | – | ns |
| | | 74.25 | 13.5 | | | |
| | | 148.5 | 6.7 | | | |
| Time between end of Command Word (or data in Auto-Increment mode) and the first SCLK of the following Data Word – read cycle. | t_5 | PCLK (MHz) | ns | | | |
| | | unlocked | – | | | |
| | | 27.0 | 148.4* | – | – | ns |
| | | 74.25 | 53.9* | | | |
| | | 148.5 | 27* | | | |
| Time between end of Command Word (or data in Auto-Increment mode) and the first SCLK of the following Data Word – read cycle - ANC FIFO Read | t_5 | 222.6 | – | – | ns | |
| Output hold time (15pF load) | t_6 | 1.5 | – | – | ns | |
| \overline{CS} high after last SCLK rising edge | t_7 | PCLK (MHz) | ns | | | |
| | | unlocked | 445 | | | |
| | | 27.0 | 37.1 | – | – | ns |
| | | 74.25 | 13.5 | | | |
| | | 148.5 | 6.7 | | | |
| Input data hold time | t_8 | 1.5 | – | – | ns | |

*when the device is locked to these data rates

This timing must be satisfied across all ambient temperature and power supply operating conditions, as described in the [Electrical Characteristics](#) on page 17.

4.21 Host Interface Register Maps

Note: The GS2970A only accepts write/read commands to/from the Audio Register Maps when the audio core is locked to the incoming video data rate. The Video Register Map is always active, whether valid serial input data is present or not.

4.21.1 Video Core Registers

Table 4-29: Video Core Configuration and Status Registers

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|-----------------------------|-----|---|-----|---------|
| 000h | IOPROC_1 | RSVD | 15 | Reserved. | R | 0 |
| | | TRS_WORD_REMAP_DS1_DISABLE | 14 | Disables 8-bit TRS word remapping for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs. | R/W | 0 |
| | | RSVD | 13 | Reserved. | R/W | 0 |
| | | EDH_FLAG_UPDATE_MASK | 12 | Disables updating of EDH error flags. | R/W | 0 |
| | | EDH_CRC_INS_MASK | 11 | Disables EDH_CRC error correction and insertion. | R/W | 0 |
| | | H_CONFIG | 10 | Selects the H blanking indication: 0: Active line blanking - the H output is HIGH for all the horizontal blanking period, including the EAV and SAV TRS words. 1: TRS based blanking - the H output is set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS signals. This signal is only valid when TIM_861 is set to '0' (via pin or host interface). | R/W | 0 |
| | | ANC_DATA_EXT_MASK | 9 | Disables ancillary data extraction FIFO. | R/W | 0 |
| | | AUD_EXT_MASK | 8 | Disables audio extraction block. | R/W | 0 |
| | | TIM_861_PIN_DISABLE | 7 | Disable TIM_861 pin control when set to '1', and use TIMING_861 bit instead. | R/W | 0 |
| | | TIMING_861 | 6 | Selects the output timing reference format: 0 = Digital FVH timing output; 1 = CEA-861 timing output. | R/W | 0 |
| | | RSVD | 5 | Reserved. | R/W | 0 |
| | | ILLEGAL_WORD_REMAP_DS1_MASK | 4 | Disables illegal word remapping for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs. | R/W | 0 |

Table 4-29: Video Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|---------------------------------|-----|--|-----|---------|
| 000h | IOPROC_1 | ANC_CHECKSUM_INSERTION_DS1_MASK | 3 | Disables insertion of ancillary data checksums for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs. | R/W | 0 |
| | | CRC_INS_DS1_MASK | 2 | Disables insertion of HD/3G CRC words for 3G Level B Data Stream 1, 3G Level A, and HD inputs. | R/W | 0 |
| | | LNUM_INS_DS1_MASK | 1 | Disables insertion of line numbers for 3G Level B Data Stream 1, 3G Level A, and HD inputs. | R/W | 0 |
| | | TRS_INS_DS1_MASK | 0 | Disables insertion of TRS words for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs. | R/W | 0 |
| 001h | IOPROC_2 | RSVD | 15 | Reserved. | R/W | N/A |
| | | NONINV | 14 | With DISB_AUTDET set HIGH, if this bit is asserted (HIGH), forces non-inverted MPEG-2 decoding. If deasserted (LOW), forces inverted MPEG-2 decoding. Applicable in DVB-ASI mode only. | R/W | 0 |
| | | DISB_AUTDET | 13 | Disables auto detection of inverted DVB ASI MPEG-2 data when HIGH. When LOW, NONINV is ignored and the DVB decoder auto detects for inverted MPEG-2 data. Applicable in DVB-ASI mode only. | R/W | 0 |
| | | TRS_WORD_REMAP_DS2_DISABLE | 12 | Disables 8-bit TRS word remapping in Data Stream 2 (3G Level B only). | R/W | 0 |
| | | RSVD | 11 | Reserved. | R/W | 0 |
| | | REGEN_352M_MASK | 10 | Disables regeneration of the SMPTE ST 352 packet for 3G Level B data. Note: this bit needs to be enabled via the host interface to disable SMPTE ST 352 packet generation. It is strongly recommended to set this bit LOW only when Level B to Level A conversion is enabled. | R/W | 0 |

Table 4-29: Video Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|---------------------------------|-----|---|-----|---------|
| 001h | IOPROC_2 | DS_SWAP_3G | 9 | Swaps Data Stream 1 (DS1) and Data Stream 2 (DS2) at the output in 3G mode. In 20-bit output mode, DS1 shall be present on DOUT pins [19:10] and DS2 shall be present on DOUT pins [9:0] by default. When DS_SWAP_3G is set to '1', DS2 shall be present on DOUT pins [19:10] and DS1 shall be present on DOUT pins [9:0]. In 10-bit (DDR) output mode, DS2 shall precede DS1 by default. When DS_SWAP_3G is set to '1', DS1 shall precede DS2. | R/W | 0 |
| | | LEVEL_B2A_CONV_DISABLE_MASK | 8 | Disable conversion of a 3G Level B input to a 3G Level A format. Only effective if in 3G Level B mode. Default is active HIGH (disabled), so Level B inputs are formatted as Level B outputs. | R/W | 1 |
| | | ANC_EXT_SEL_DS2_DS1 | 7 | Selects data stream to extract ANC data from (valid for 3G Level B data). | R/W | 0 |
| | | AUDIO_SEL_DS2_DS1 | 6 | Selects data stream to be sent to audio core (valid for 3G Level B data). | R/W | 0 |
| | | RSVD | 5 | Reserved. | R/W | 0 |
| | | ILLEGAL_WORD_REMAP_DS2_MASK | 4 | Disables illegal word remapping in Data Stream 2 (3G Level B only). | R/W | 0 |
| | | ANC_CHECKSUM_INSERTION_DS2_MASK | 3 | Disables insertion of ancillary data checksums in Data Stream 2 (3G Level B only). | R/W | 0 |
| | | CRC_INS_DS2_MASK | 2 | Disables insertion of CRC words in Data Stream 2 (3G Level B only). | R/W | 0 |
| | | LNUM_INS_DS2_MASK | 1 | Disables insertion of line numbers in Data Stream 2 (3G Level B only). | R/W | 0 |
| | | TRS_INS_DS2_MASK | 0 | Disable insertion of TRS words in Data Stream 2 (3G Level B only). | R/W | 0 |

Table 4-29: Video Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|----------------|-------|---|------|---------|
| | | RSVD | 15-11 | Reserved. | ROCW | 0 |
| | | VD_STD_ERR_DS1 | 10 | Video Standard Error indication for HD and SD inputs. | ROCW | 0 |
| | | FF_CRC_ERR | 9 | EDH Full Frame CRC error indication. | ROCW | 0 |
| | | AP_CRC_ERR | 8 | EDH Active Picture CRC error indication. | ROCW | 0 |
| | | RSVD | 7 | Reserved. | ROCW | 0 |
| | | CCS_ERR_DS1 | 6 | Chroma ancillary data checksum error indication for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs. | ROCW | 0 |
| 002h | ERROR_STAT_1 | YCS_ERR_DS1 | 5 | Luma ancillary data checksum error indication for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs. | ROCW | 0 |
| | | CCRC_ERR_DS1 | 4 | Chroma CRC error indication for 3G Level B Data Stream 1, 3G Level A, and HD inputs. | ROCW | 0 |
| | | YCRC_ERR_DS1 | 3 | Luma CRC error indication for 3G Level B Data Stream 1, 3G Level A, and HD inputs. | ROCW | 0 |
| | | LNUM_ERR_DS1 | 2 | Line number error indication for 3G Level B Data Stream 1, 3G Level A, and HD inputs. | ROCW | 0 |
| | | SAV_ERR_DS1 | 1 | SAV error indication for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs. | ROCW | 0 |
| | | EAV_ERR_DS1 | 0 | EAV error indication for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs. | ROCW | 0 |

Table 4-29: Video Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|-----------|---------------|---|------|--|------|---------|
| | | RSVD | 15-7 | Reserved. | ROCW | 0 |
| 003h | ERROR_STAT_2 | CCS_ERR_DS2 | 6 | Chroma ancillary data checksum error indication for Data Stream 2 (3G Level B only). | ROCW | 0 |
| | | YCS_ERR_DS2 | 5 | Luma ancillary data checksum error indication for Data Stream 2 (3G Level B only). | ROCW | 0 |
| | | CCRC_ERR_DS2 | 4 | Chroma CRC error indication for Data Stream 2 (3G Level B only). | ROCW | 0 |
| | | YCRC_ERR_DS2 | 3 | Luma CRC error indication for Data Stream 2 (3G Level B only). | ROCW | 0 |
| | | LNUM_ERR_DS2 | 2 | Line number error indication for Data Stream 2 (3G Level B only). | ROCW | 0 |
| | | SAV_ERR_DS2 | 1 | SAV error indication for Data Stream 2 (3G Level B only). | ROCW | 0 |
| | | EAV_ERR_DS2 | 0 | EAV error indication for Data Stream 2 (3G Level B only). | ROCW | 0 |
| 004h | EDH_FLAG_IN | EDH_DETECT | 15 | Embedded EDH packet detected. | R | 0 |
| | | ANC_UES_IN | 14 | Ancillary data – unknown error status flag. | R | 0 |
| | | ANC_IDA_IN | 13 | Ancillary data – internal error detected already flag. | R | 0 |
| | | ANC_IDH_IN | 12 | Ancillary data – internal error detected here flag | R | 0 |
| | | ANC_EDA_IN | 11 | Ancillary data – error detected already flag. | R | 0 |
| | | ANC_EDH_IN | 10 | Ancillary data – error detected here flag. | R | 0 |
| | | FF_UES_IN | 9 | EDH Full Field – unknown error status flag. | R | 0 |
| | | FF_IDA_IN | 8 | EDH Full Field – internal error detected already flag. | R | 0 |
| | | FF_IDH_IN | 7 | EDH Full Field – internal error detected here flag. | R | 0 |
| FF_EDA_IN | 6 | EDH Full Field – error detected already flag. | R | 0 | | |

Table 4-29: Video Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|---|-----|--|-----|---------|
| 004h | EDH_FLAG_IN | FF_EDH_IN | 5 | EDH Full Field – error detected here flag. | R | 0 |
| | | AP_UES_IN | 4 | EDH Active Picture – unknown error status flag. | R | 0 |
| | | AP_IDA_IN | 3 | EDH Active Picture – internal error detected already flag. | R | 0 |
| | | AP_IDH_IN | 2 | EDH Active Picture – internal error detected here flag. | R | 0 |
| | | AP_EDA_IN | 1 | EDH Active Picture – error detected already flag. | R | 0 |
| | | AP_EDH_IN | 0 | EDH Active Picture – error detected here flag. | R | 0 |
| 005h | EDH_FLAG_OUT | RSVD | 15 | Reserved. | R | 0 |
| | | ANC_UES | 14 | Ancillary data – Unknown Error Status flag. | R | 1 |
| | | ANC_IDA | 13 | Ancillary data – Internal error Detected Already flag. | R | 0 |
| | | ANC_IDH | 12 | Ancillary data – Internal error Detected Here flag. | R | 0 |
| | | ANC_EDA | 11 | Ancillary data – Error Detected Already flag. | R | 0 |
| | | ANC_EDH | 10 | Ancillary data – Error Detected Here flag. | R | 0 |
| | | FF_UES | 9 | EDH Full Field – Unknown Error Status flag. | R | 1 |
| | | FF_IDA | 8 | EDH Full Field – Internal error Detected Already flag. | R | 0 |
| | | FF_IDH | 7 | EDH Full Field – Internal error Detected Here flag. | R | 0 |
| | | FF_EDA | 6 | EDH Full Field – Error Detected Already flag. | R | 0 |
| | | FF_EDH | 5 | EDH Full Field – Error Detected Here flag. | R | 0 |
| | | AP_UES | 4 | EDH Active Picture – Unknown Error Status flag. | R | 1 |
| | | AP_IDA | 3 | EDH Active Picture – Internal error Detected Already flag. | R | 0 |
| | | AP_IDH | 2 | EDH Active Picture – Internal error Detected Here flag. | R | 0 |
| AP_EDA | 1 | EDH Active Picture – Error Detected Already flag. | R | 0 | | |
| 005h | EDH_FLAG_OUT | AP_EDH | 0 | EDH Active Picture – Error Detected Here flag. | R | 0 |

Table 4-29: Video Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|-----------------|------------------|-------|--|-----|---------|
| 006h | DATA_FORMAT_DS1 | FF_CRC_V | 15 | EDH Full Field CRC Validity bit. | R | 0 |
| | | AP_CRC_V | 14 | EDH Active Picture CRC Validity bit. | R | 0 |
| | | VD_STD_DS1 | 13-8 | Detected Video Standard for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs. | R | 29 |
| | | CDATA_FORMAT_DS1 | 7-4 | Data format as indicated in Chroma channel for 3G Level B Data Stream 1, HD and SD inputs; Data format as indicated in Data Stream 2 for 3G Level A inputs. | R | 15 |
| | | YDATA_FORMAT_DS1 | 3-0 | Data format as indicated in Luma channel for 3G Level B Data Stream 1, HD and SD inputs; Data format as indicated in Data Stream 1 for 3G Level A inputs. | R | 15 |
| 007h | DATA_FORMAT_DS2 | RSVD | 15-14 | Reserved. | R | 0 |
| | | VD_STD_DS2 | 13-8 | Detected Video Standard for Data Stream 2 (3G Level B only). | R | 29 |
| | | CDATA_FORMAT_DS2 | 7-4 | Data Format as indicated in Chroma channel for Data Stream 2 (3G Level B only). | R | 15 |
| | | YDATA_FORMAT_DS2 | 3-0 | Data Format as indicated in Luma channel for Data Stream 2 (3G Level B only). | R | 15 |

Table 4-29: Video Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|--------------|-------|---|-----|---------|
| | | RSVD | 15 | Reserved. | RW | 0 |
| 008h | IO_CONFIG | STAT2_CONFIG | 14-10 | Configure STAT2 output pin: 00000: H Blanking when TIM_861 = 0; HSYNC when TIM_861 = 1 00001: V Blanking when TIM_861 = 0; VSYNC when TIM_861 = 1 00010: F bit when TIM_861 = 0; Data Enable (DE) when TIM_861 = 1 00011: LOCKED 00100: Y/1ANC: ANC indication (SD), Luma ANC indication (HD), Data Stream 1 ANC data indication (3G) 00101: C/2ANC: Chroma ANC indication (HD) or Data Stream 2 ANC data indication (3G) 00110: Data Error 00111: Video Error 01000: Audio Error 01001: EDH Detected 01010: Carrier Detect 01011: RATE_DET0 01100: RATE_DET1 01101 - 11111: Reserved | RW | 2 |
| | | STAT1_CONFIG | 9-5 | Configure STAT1 output pin. (Refer to above for decoding) | RW | 1 |
| | | STAT0_CONFIG | 4-0 | Configure STAT0 output pin. (Refer to above for decoding) | RW | 0 |
| | | RSVD | 15 | Reserved. | RW | 0 |
| 009h | IO_CONFIG2 | STAT5_CONFIG | 14-10 | Configure STAT5 output pin. (Refer to above for decoding) | RW | 6 |
| | | STAT4_CONFIG | 9-5 | Configure STAT4 output pin. (Refer to above for decoding) | RW | 4 |
| | | STAT3_CONFIG | 4-0 | Configure STAT3 output pin. (Refer to above for decoding) | RW | 3 |

Table 4-29: Video Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|-------------|--------------------|-----------------|-------|---|-----|---------|
| | | RSVD | 15-4 | Reserved. | RW | 0 |
| | | ANC_DATA_SWITCH | 3 | Switches between FIFO memories. | RW | 0 |
| | | ANC_DATA_DEL | 2 | Remove Ancillary Data from output video stream, set to Luma and Chroma blanking values. | RW | 0 |
| 00Ah | ANC_CONTROL | HD_ANC_Y1_C2 | 1 | Extract Ancillary data from Luma and Chroma channels (HD inputs) Extract Ancillary data from Data Stream 1 and Data Stream 2 (3G Level A inputs) Extract Ancillary data from Luma and Chroma channels of Data Stream 1 (3G Level B inputs, when ANC_EXT_SEL_DS2_DS1 = 0) Extract Ancillary data from Luma and Chroma channels of Data Stream 2 (3G Level B inputs, when ANC_EXT_SEL_DS2_DS1 = 1) | RW | 0 |
| | | HD_ANC_C2 | 0 | Extract Ancillary data only from Chroma channel (HD inputs) Extract Ancillary data only from Data Stream 2 (3G Level A inputs) Extract Ancillary data only from Chroma channel of Data Stream 1 (3G Level B inputs, when ANC_EXT_SEL_DS2_DS1 = 0) Extract Ancillary data only from Chroma channel of Data Stream 2 (3G Level B inputs, when ANC_EXT_SEL_DS2_DS1 = 1) | RW | 0 |
| 00Bh | ANC_LINE_A | RSVD | 15-11 | Reserved. | R/W | 0 |
| | | ANC_LINE_A | 10-0 | Video Line to extract Ancillary data from. | R/W | 0 |
| 00Ch | ANC_LINE_B | RSVD | 15-11 | Reserved. | R/W | 0 |
| | | ANC_LINE_B | 10-0 | Second video Line to extract Ancillary data from. | R/W | 0 |
| 00Dh - 00Eh | RSVD | RSVD | 15-0 | Reserved. | R | 0 |
| 00Fh | ANC_TYPE_1_AP 1 | ANC_TYPE1_DS1 | 15-0 | Programmable DID/SDID pair #1 to extract from 3G Level B Data Stream 1, 3G Level A, HD and SD input formats ([15:8] = DID, [7:0] =SDID). | R/W | 0 |
| 010h | ANC_TYPE_2_AP 1 | ANC_TYPE2_DS1 | 15-0 | Programmable DID/SDID pair #2 to extract from 3G Level B Data Stream 1, 3G Level A, HD and SD input formats ([15:8] = DID, [7:0] =SDID). | R/W | 0 |

Table 4-29: Video Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|--------------------------|--------------------|------|--|-----|---------|
| 011h | ANC_TYPE_3 _AP1 | ANC_TYPE3_DS1 | 15-0 | Programmable DID/SDID pair #3 to extract from 3G Level B Data Stream 1, 3G Level A, HD and SD input formats ([15:8] = DID, [7:0] =SDID). | R/W | 0 |
| 012h | ANC_TYPE_4 _AP1 | ANC_TYPE4_DS1 | 15-0 | Programmable DID/SDID pair #4 to extract from 3G Level B Data Stream 1, 3G Level A, HD and SD input formats ([15:8] = DID, [7:0] =SDID). | R/W | 0 |
| 013h | ANC_TYPE_5 _AP1 | ANC_TYPE5_DS1 | 15-0 | Programmable DID/SDID pair #5 to extract from 3G Level B Data Stream 1, 3G Level A, HD and SD input formats ([15:8] = DID, [7:0] =SDID). | R/W | 0 |
| 014h | ANC_TYPE_1 _AP2 | ANC_TYPE1_DS2 | 15-0 | Programmable DID/SDID pair #1 to extract from 3G Level B Data Stream 2 ([15:8] = DID, [7:0] =SDID). | R/W | 0 |
| 015h | ANC_TYPE_2 _AP2 | ANC_TYPE2_DS2 | 15-0 | Programmable DID/SDID pair #2 to extract from 3G Level B Data Stream 2 ([15:8] = DID, [7:0] =SDID). | R/W | 0 |
| 016h | ANC_TYPE_3 _AP2 | ANC_TYPE3_DS2 | 15-0 | Programmable DID/SDID pair #3 to extract from 3G Level B Data Stream 2 ([15:8] = DID, [7:0] =SDID). | R/W | 0 |
| 017h | ANC_TYPE_4 _AP2 | ANC_TYPE4_DS2 | 15-0 | Programmable DID/SDID pair #4 to extract from 3G Level B Data Stream 2 ([15:8] = DID, [7:0] =SDID). | R/W | 0 |
| 018h | ANC_TYPE_5 _AP2 | ANC_TYPE5_DS2 | 15-0 | Programmable DID/SDID pair #5 to extract from 3G Level B Data Stream 2 ([15:8] = DID, [7:0] =SDID). | R/W | 0 |
| 019h | VIDEO_FORMAT _352_A_1 | VIDEO_FORMAT_2_DS1 | 15-8 | SMPTE ST 352 embedded packet – byte 2. | R | 0 |
| | | VIDEO_FORMAT_1_DS1 | 7-0 | SMPTE ST 352 embedded packet – byte 1: [7]: Version identifier [6:0]: Video Payload Identifier. | R | 0 |
| 01Ah | VIDEO_FORMAT _352_B_1 | VIDEO_FORMAT_4_DS1 | 15-8 | SMPTE ST 352 embedded packet – byte 4. | R | 0 |
| | | VIDEO_FORMAT_3_DS1 | 7-0 | SMPTE ST 352 embedded packet – byte 3. | R | 0 |
| 01Bh | VIDEO_FORMAT _352_A_2 | VIDEO_FORMAT_2_DS2 | 15-8 | SMPTE ST 352 embedded packet – byte 2 (3G Data Stream 2 only). | R | 0 |
| | | VIDEO_FORMAT_1_DS2 | 7-0 | SMPTE ST 352 embedded packet – byte 1 (3G Data Stream 2 only): [7]: Version identifier [6:0]: Video Payload Identifier. | R | 0 |

Table 4-29: Video Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default | |
|---------|------------------------|---|-------|--|-----|---------|--|
| 01Ch | VIDEO_FORMAT_352_B_2 | VIDEO_FORMAT_4_DS2 | 15-8 | SMPTE ST 352 embedded packet – byte 4 (3G Data Stream 2 only). | R | 0 | |
| | | VIDEO_FORMAT_3_DS2 | 7-0 | SMPTE ST 352 embedded packet – byte 3 (3G Data Stream 2 only). | R | 0 | |
| 01Dh | VIDEO_FORMAT_352_INS_A | VIDEO_FORMAT_2_INS | 15-8 | SMPTE ST 352 packet - byte 2 to be embedded after Level B to Level A conversion. | R/W | 0 | |
| | | VIDEO_FORMAT_1_INS | 7-0 | SMPTE ST 352 packet - byte 1 to be embedded after Level B to Level A conversion. | R/W | 0 | |
| 01Eh | VIDEO_FORMAT_352_INS_B | VIDEO_FORMAT_4_INS | 15-8 | SMPTE ST 352 packet - byte 4 to be embedded after Level B to Level A conversion. | R/W | 0 | |
| | | VIDEO_FORMAT_3_INS | 7-0 | SMPTE ST 352 packet - byte 3 to be embedded after Level B to Level A conversion. | R/W | 0 | |
| 01Fh | RASTER_STRUC_1 | RSVD | 15-14 | Reserved. | R | 0 | |
| | | WORDS_PER_ACTLINE | 13-0 | Words Per Active Line. | R | 0 | |
| 020h | RASTER_STRUC_2 | RSVD | 15-14 | Reserved. | R | 0 | |
| | | WORDS_PER_LINE | 13-0 | Total Words Per Line. | R | 0 | |
| 021h | RASTER_STRUC_3 | RSVD | 15-11 | Reserved. | R | 0 | |
| | | LINES_PER_FRAME | 10-0 | Total Lines Per Frame. | R | 0 | |
| 022h | RASTER_STRUC_4 | RATE_SEL_READBACK | 15-14 | Read back detected data rate: 0 = HD, 1,3=SD, 2=3G | R | 0 | |
| | | M | 13 | Specifies detected M value 0: 1.000 1: 1.001 | R | 0 | |
| | | Note: In certain systems, due to greater ppm offsets in the crystal, the 'M' bit may not assert properly. In such cases, bits 3:0 in Register 06Fh can be increased to a maximum value of 4. | | | | | |
| | | STD_LOCK | 12 | Video standard lock. | R | 0 | |
| | | INT_PROG | 11 | Interlaced or progressive. | R | 0 | |
| | | ACTLINE_PER_FIELD | 10-0 | Active lines per frame. | R | 0 | |

Table 4-29: Video Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|-------------|-----------------|---------------|------|---|-----|---------|
| 023h | FLYWHEEL_STATUS | RSVD | 15-5 | Reserved. | R | 0 |
| | | V_LOCK_DS2 | 4 | Indicates that the timing signal generator is locked to vertical timing (3G Level B Data Stream 2 only). | R | 0 |
| | | H_LOCK_DS2 | 3 | Indicates that the timing signal generator is locked to horizontal timing (3G Level B Data Stream 2 only). | R | 0 |
| | | RSVD | 2 | Reserved. | R | 0 |
| | | V_LOCK_DS1 | 1 | Indicates that the timing signal generator is locked to vertical timing (3G Level B Data Stream 1, 3G Level A, HD and SD inputs). | R | 0 |
| | | H_LOCK_DS1 | 0 | Indicates that the timing signal generator is locked to horizontal timing (3G Level B Data Stream 1, 3G Level A, HD and SD inputs). | R | 0 |
| 024h | RATE_SEL | RSVD | 15-3 | Reserved. | R | 0 |
| | | AUTO/MAN | 2 | Detect data rate automatically (1) or program manually (0). | R/W | 1 |
| | | RATE_SEL_TOP | 1-0 | Programmable rate select in manual mode: 0 = HD, 1,3=SD, 2=3G | R/W | 0 |
| 025h | TIM_861_FORMAT | RSVD | 15-7 | Reserved. | R | 0 |
| | | FORMAT_ERR | 6 | Indicates standard is not recognized for CEA 861 conversion. | R | 1 |
| | | FORMAT_ID_861 | 5-0 | CEA-861 format ID of input video stream. Refer to Table 4-9 . | R | 0 |
| 026h | TIM_861_CFG | RSVD | 15-3 | Reserved. | R | 0 |
| | | VSYNC_INVERT | 2 | Invert output VSYNC pulse. | R/W | 0 |
| | | HSYNC_INVERT | 1 | Invert output HSYNC pulse. | R/W | 0 |
| | | TRS_861 | 0 | Sets the timing reference outputs to DFP timing mode when set to '1'. By default, the timing reference outputs follow CEA-861 timing mode. Only valid when TIM_861 is set to '1'. | R/W | 0 |
| 027h - 036h | RSVD | RSVD | – | Reserved. | R | 0 |

Table 4-29: Video Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|----------|---------------|------------------|-------|---|-----|---------|
| | | RSVD | 15-11 | Reserved. | R | 0 |
| 037h | ERROR_MASK_1 | ERROR_MASK_1 | 10-0 | Error mask for global error vector (3G Level B Data Stream 1, 3G Level A, HD, SD): bit[0]: EAV_ERR_DS1 mask bit[1]: SAV_ERR_DS1 mask bit[2]: LNUM_ERR_DS1 mask bit[3]: YCRC_ERR_DS1 mask bit[4]: CCRC_ERR_DS1 mask bit[5]: YCS_ERR_DS1 mask bit[6]: CCS_ERR_DS1 mask bit[7]: Reserved bit[8]: AP_CRC_ERR mask bit[9]: FF_CRC_ERR mask bit[10]: VD_STD_ERR_DS1 mask | R/W | 0 |
| | | RSVD | 15-7 | Reserved. | R | 0 |
| 038h | ERROR_MASK_2 | ERROR_MASK_2 | 6-0 | Error mask for global error vector (3G Level B Data Stream 2 only): bit[0]: EAV_ERR_DS2 mask bit[1]: SAV_ERR_DS2 mask bit[2]: LNUM_ERR_DS2 mask bit[3]: YCRC_ERR_DS2 mask bit[4]: CCRC_ERR_DS2 mask bit[5]: YCS_ERR_DS2 mask bit[6]: CCS_ERR_DS2 mask | R/W | 0 |
| | | RSVD | 15-5 | Reserved. | R | 0 |
| | | SCLK_INV | 4 | Invert polarity of output serial audio clock. | R/W | 0 |
| | | AMCLK_INV | 3 | Invert polarity of output audio master clock. | R/W | 0 |
| 039h | AGC_CTRL | RSVD | 2 | Reserved. | R/W | 0 |
| | | AMCLK_SEL | 1-0 | Audio Master Clock Select. 0: 128 fs 1: 256 fs 2: 512 fs | R/W | 0 |
| 03Ah-6Bh | RSVD | RSVD | 15-0 | Reserved. | R | 0 |
| | | RSVD | 15-6 | Reserved. | R/W | 0 |
| 06Ch | CLK_GEN | DEL_LINE_CLK_SEL | 5 | Chooses between the in-phase (0) and quadrature (1) clocks for DDR mode. | R/W | 0 |
| | | DEL_LINE_OFFSET | 4-0 | Controls the offset for the delay line. | R/W | 0 |

Table 4-29: Video Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|-----------|-----------------------|-----------------------|-------|--|-----|---------|
| 06Dh | IO_DRIVE_STRENGTH | RSVD | 15-6 | Reserved. | R/W | 0 |
| | | IO_DS_CTRL_DOUT_MSB | 5-4 | Drive strength adjustment for DOUT[19:10] outputs and PCLK output: 00: 4mA; 01: 8mA; 10: 10mA(1.8V), 12mA(3.3V); 11: 12mA(1.8V), 16mA(3.3V) | R/W | 2 |
| | | IO_DS_CTRL_STAT | 3-2 | Drive strength adjustment for STAT[5:0] outputs: 00: 4mA; 01: 6mA; 10: 8mA(1.8V), 10mA(3.3V); 11: 10mA(1.8V), 12mA(3.3V) | R/W | 2 |
| | | IO_DS_CTRL_DOUT_LSB | 1-0 | Drive strength adjustment for DOUT[9:0] outputs: 00: 4mA; 01: 6mA; 10: 8mA(1.8V), 10mA(3.3V); 11: 10mA(1.8V), 12mA(3.3V) | R/W | 3 |
| 06Eh | RSVD | RSVD | 15-0 | Reserved. | R/W | 0 |
| 06Fh | RSVD | RSVD | 15-4 | Reserved. | R/W | 0 |
| | M_DETECTION_TOLERANCE | M_DETECTION_TOLERANCE | 3-0 | Sets the detection tolerance. | R/W | 2 |
| 070h-084h | RSVD | RSVD | 15-0 | Reserved. | R/W | 0 |
| | RSVD | RSVD | 15-11 | Reserved. | R/W | 0 |
| 085h | LOCK_NOISE_IMM_INCR | LOCK_NOISE_IMM_INCR | 10 | Enables extra noise-immunity on SMPTE detected lock when HIGH by forcing detection of three TRS words with the last two TRS words having the same alignment before locking to SMPTE. Enable this only for AUTO/MAN = HIGH. | RW | 0 |
| | RSVD | RSVD | 9-0 | Reserved. | R/W | 0 |

4.21.2 SD Audio Core Registers

Note: The GS2970A only accepts write/read commands to/from the SD Audio Register Map when the audio core is locked to the incoming SD video format.

Table 4-30: SD Audio Core Configuration and Status Registers

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|----------------|-------|--|-----|---------|
| | | RSVD | 15-14 | Reserved. | R/W | 0 |
| | | ALL_DEL | 13 | Selects deletion of all audio data and all audio control packets. 0: Do not delete existing audio packets 1: Delete existing audio packets | R/W | 0 |
| | | MUTE_ALL | 12 | Mute all output channels. 0: Normal 1: Muted | R/W | 0 |
| | | ACS_USE_SECOND | 11 | Extract Audio Channel Status from second channel pair. | R/W | 0 |
| | | CLEAR_AUDIO | 10 | Clears all audio FIFO buffers and puts them in start-up state. | R/W | 0 |
| 400h | CFG_AUD | OS_SEL | 9-8 | Specifies the audio FIFO buffer size. 00: 36 samples deep, 26 sample start-up count 01: 22 samples deep, 12 sample start-up count 10: 16 samples deep, 6 sample start-up count 11: Reserved Note: The default 36-sample deep FIFO size is not supported if each audio channel must have the same sample delay. | R/W | 0 |
| | | LSB_FIRSTD | 7 | Causes the channel 7 and 8 output format to use LSB first. 0: MSB first 1: LSB first | R/W | 0 |
| | | LSB_FIRSTC | 6 | Causes the channel 5 and 6 output format to use LSB first. 0: MSB first 1: LSB first | R/W | 0 |
| | | LSB_FIRSTB | 5 | Causes the channel 3 and 4 output format to use LSB first. 0: MSB first 1: LSB first | R/W | 0 |
| | | LSB_FIRSTA | 4 | Causes the channel 1 and 2 output format to use LSB first. 0: MSB first 1: LSB first | R/W | 0 |

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|--------------|-----|---|------|---------|
| 400h | CFG_AUD | IDB | 3-2 | Specifies the Secondary audio group to extract. 00: Audio group #1 01: Audio group #2 10: Audio group #3 11: Audio group #4 Note 1: Should IDA and IDB be set to the same value, they automatically revert to their default values. Note 2: The Mute function will remove invalid data. | R/W | 1 |
| | | IDA | 1-0 | Specifies the Primary audio group to extract. 00: Audio group #1 01: Audio group #2 10: Audio group #3 11: Audio group #4 Note 1: Should IDA and IDB be set to the same value, they automatically revert to their default values. Note 2: The Mute function will remove invalid data. | R/W | 0 |
| 401h | DBN_ERR | EXT_DET3_4B | 15 | Set when Secondary group channels 3 and 4 have extended data. Write '1' to clear. | ROCW | 0 |
| | | EXT_DET1_2B | 14 | Set when Secondary group channels 1 and 2 have extended data. Write '1' to clear. | ROCW | 0 |
| | | EXT_DET3_4A | 13 | Set when Primary group channels 3 and 4 have extended data. Write '1' to clear. | ROCW | 0 |
| | | EXT_DET1_2A | 12 | Set when Primary group channels 1 and 2 have extended data. Write '1' to clear. | ROCW | 0 |
| | | CTL_DBNB_ERR | 11 | Set when Secondary group control packet Data Block Number sequence is discontinuous. Write '1' to clear. | ROCW | 0 |
| | | CTL_DBNA_ERR | 10 | Set when Primary group control packet Data Block Number sequence is discontinuous. Write '1' to clear. | ROCW | 0 |
| | | EXT_DBNB_ERR | 9 | Set when Secondary group extended data packet Data Block Number sequence is discontinuous. Write '1' to clear. | ROCW | 0 |

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|---------------|------|---|------|---------|
| 401h | DBN_ERR | EXT_DBNA_ERR | 8 | Set when Primary group extended data packet Data Block Number sequence is discontinuous. Write '1' to clear. | ROCW | 0 |
| | | SAMP_DBNB_ERR | 7 | Set when Secondary group data packet Data Block Number sequence is discontinuous. Write '1' to clear. | ROCW | 0 |
| | | SAMP_DBNA_ERR | 6 | Set when Primary group data packet Data Block Number sequence is discontinuous. Write '1' to clear. | ROCW | 0 |
| | | CTRB_DET | 5 | Set when Secondary group audio control packet is detected. Write '1' to clear. | ROCW | 0 |
| | | CTRA_DET | 4 | Set when Primary group audio control packet is detected. Write '1' to clear. | ROCW | 0 |
| | | ACS_DET3_4B | 3 | Secondary group audio status detected for channels 3 and 4. Write '1' to clear. | ROCW | 0 |
| | | ACS_DET1_2B | 2 | Secondary group audio status detected for channels 1 and 2. Write '1' to clear. | ROCW | 0 |
| | | ACS_DET3_4A | 1 | Primary group audio status detected for channels 3 and 4. Write '1' to clear. | ROCW | 0 |
| | | ACS_DET1_2A | 0 | Primary group audio status detected for channels 1 and 2. Write '1' to clear. | ROCW | 0 |
| | | RSVD | 15-2 | Reserved. | R/W | 0 |
| 402h | REGEN | ACS_APPLY | 1 | Cause channel status data in ACSR[183:0] to be transferred to the channel status replacement mechanism. The transfer does not occur until the next status boundary. | R/W | 0 |
| | | ACS_REGEN | 0 | Specifies that Audio Channel Status of all channels should be replaced with ACSR[183:0] field. 0: Do not replace Channel Status 1: Replace Channel Status of all channels | R/W | 0 |

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|-----------------|---------------|--|-------|--|------|---------|
| 403h | AUD_DET | IDB_READBACK | 15-14 | Actual value of IDB in the hardware. | R | 1 |
| | | IDA_READBACK | 13-12 | Actual value of IDA in the hardware. | R | 0 |
| | | XDPG4_DET | 11 | Set while embedded Group 4 audio extended packets are detected. | R | 0 |
| | | XDPG3_DET | 10 | Set while embedded Group 3 audio extended packets are detected. | R | 0 |
| | | XDPG2_DET | 9 | Set while embedded Group 2 audio extended packets are detected. | R | 0 |
| | | XDPG1_DET | 8 | Set while embedded Group 1 audio extended packets are detected. | R | 0 |
| | | ADPG4_DET | 7 | Set while Group 4 audio data packets are detected. | R | 0 |
| | | ADPG3_DET | 6 | Set while Group 3 audio data packets are detected. | R | 0 |
| | | ADPG2_DET | 5 | Set while Group 2 audio data packets are detected. | R | 0 |
| | | ADPG1_DET | 4 | Set while Group 1 audio data packets are detected. | R | 0 |
| | | ACS_APPLY_WAITD | 3 | Set while output channels 7 and 8 are waiting for a status boundary to apply the ACSR[183:0] data. | R | 0 |
| | | ACS_APPLY_WAITC | 2 | Set while output channels 5 and 6 are waiting for a status boundary to apply the ACSR[183:0] data. | R | 0 |
| | | ACS_APPLY_WAITB | 1 | Set while output channels 3 and 4 are waiting for a status boundary to apply the ACSR[183:0] data. | R | 0 |
| ACS_APPLY_WAITA | 0 | Set while output channels 1 and 2 are waiting for a status boundary to apply the ACSR[183:0] data. | R | 0 | | |
| 404h | CSUM_ERR_DET | RSVD | 15-1 | Reserved. | R/W | 0 |
| | | CSUM_ERROR | 0 | Embedded packet checksum error detected. Cleared on write. | ROCW | 0 |
| 405h | CH_MUTE | RSVD | 15-8 | Reserved. | R/W | 0 |
| | | MUTE | 7-0 | Mute output channels 8..1 Where bits 7:0 = channel 8:1 1: Mute 0: Normal | R/W | 0 |

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|-------------------------|----------------|------|---|-----|---------|
| 406h | CH_VALID | RSVD | 15-8 | Reserved. | R/W | 0 |
| | | CH4_VALIDB | 7 | Secondary group channel 4 sample validity flag. | R | 0 |
| | | CH3_VALIDB | 6 | Secondary group channel 3 sample validity flag. | R | 0 |
| | | CH2_VALIDB | 5 | Secondary group channel 2 sample validity flag. | R | 0 |
| | | CH1_VALIDB | 4 | Secondary group channel 1 sample validity flag. | R | 0 |
| | | CH4_VALIDA | 3 | Primary group channel 4 sample validity flag. | R | 0 |
| | | CH3_VALIDA | 2 | Primary group channel 3 sample validity flag. | R | 0 |
| | | CH2_VALIDA | 1 | Primary group channel 2 sample validity flag. | R | 0 |
| | | CH1_VALIDA | 0 | Primary group channel 1 sample validity flag. | R | 0 |
| 407h | SD_AUDIO_ERR OR_MASK | RSVD | 15 | Reserved. | R/W | 0 |
| | | EN_NOT_LOCKED | 14 | Asserts interrupt when LOCKED signal is not asserted. | R/W | 0 |
| | | EN_NO_VIDEO | 13 | Asserts interrupt when video format is unknown. | R/W | 0 |
| | | EN_CSUM_ERROR | 12 | Asserts interrupt when checksum error is detected. | R/W | 0 |
| | | EN_ACS_DET3_4B | 11 | Asserts interrupt when EN_ACS_DET3_4B flag is set. | R/W | 0 |
| | | EN_ACS_DET1_2B | 10 | Asserts interrupt when EN_ACS_DET1_2B flag is set. | R/W | 0 |
| | | EN_ACS_DET3_4A | 9 | Asserts interrupt when EN_ACS_DET3_4A flag is set. | R/W | 0 |
| | | EN_ACS_DET1_2A | 8 | Asserts interrupt when EN_ACS_DET1_2A flag is set. | R/W | 0 |
| | | EN_CTRB_DET | 7 | Asserts interrupt when EN_CTRB_DET flag is set. | R/W | 0 |
| | | EN_CTRA_DET | 6 | Asserts interrupt when EN_CTRA_DET flag is set. | R/W | 0 |
| | | EN_DBNB_ERR | 5 | Asserts interrupt when EN_DBNB_ERR flag is set. | R/W | 0 |
| | | EN_DBNA_ERR | 4 | Asserts interrupt when EN_DBNA_ERR flag is set. | R/W | 0 |

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|----------------------|--------------|-------|---|-----|---------|
| 407h | SD_AUDIO_ERR_OR_MASK | EN_ADPG4_DET | 3 | Asserts interrupt when the ADPG4_DET flag is set. | R/W | 0 |
| | | EN_ADPG3_DET | 2 | Asserts interrupt when the ADPG3_DET flag is set. | R/W | 0 |
| | | EN_ADPG2_DET | 1 | Asserts interrupt when the ADPG2_DET flag is set. | R/W | 0 |
| | | EN_ADPG1_DET | 0 | Asserts interrupt when the ADPG1_DET flag is set. | R/W | 0 |
| 408h | CFG_OUTPUT | ASWLD | 15-14 | Output channels 7 and 8 word length. 00: 24 bits 01: 20 bits 10: 16 bits 11: Automatic 20-bit or 24-bit | R/W | 3 |
| | | ASWLC | 13-12 | Output channels 5 and 6 word length. (See above for decoding) | R/W | 3 |
| | | ASWLB | 11-10 | Output channels 3 and 4 word length. (See above for decoding) | R/W | 3 |
| | | ASWLA | 9-8 | Output channels 1 and 2 word length. (See above for decoding) | R/W | 3 |
| | | AMD | 7-6 | Output channels 7 and 8 format selector. 00: AES/EBU audio output 01: Serial audio output: Left justified; MSB first 10: Serial audio output: Right justified; MSB first 11: I ² S serial audio output | R/W | 3 |
| | | AMC | 5-4 | Output channels 5 and 6 format selector. (See above for decoding). | R/W | 3 |
| | | AMB | 3-2 | Output channels 3 and 4 format selector. (See above for decoding). | R/W | 3 |
| | | AMA | 1-0 | Output channels 1 and 2 format selector. (See above for decoding). | R/W | 3 |

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|-------------|---------------|----------|-------|---|-----|---------|
| | | RSVD | 15-12 | Reserved. | R/W | 0 |
| 409h | OUTPUT_SEL_1 | OP4_SRC | 11-9 | Output channel 4 source selector. 000: Primary audio group channel 1 001: Primary audio group channel 2 010: Primary audio group channel 3 011: Primary audio group channel 4 100: Secondary audio group channel 1 101: Secondary audio group channel 2 110: Secondary audio group channel 3 111: Secondary audio group channel 4 | R/W | 3 |
| | | OP3_SRC | 8-6 | Output channel 3 source selector (Decode as above). | R/W | 2 |
| | | OP2_SRC | 5-3 | Output channel 2 source selector (Decode as above). | R/W | 1 |
| | | OP1_SRC | 2-0 | Output channel 1 source selector (Decode as above). | R/W | 0 |
| | | RSVD | 15-12 | Reserved. | R/W | 0 |
| 40Ah | OUTPUT_SEL_2 | OP8_SRC | 11-9 | Output channel 8 source selector. 000: Primary audio group channel 1 001: Primary audio group channel 2 010: Primary audio group channel 3 011: Primary audio group channel 4 100: Secondary audio group channel 1 101: Secondary audio group channel 2 110: Secondary audio group channel 3 111: Secondary audio group channel 4 | R/W | 7 |
| | | OP7_SRC | 8-6 | Output channel 7 source selector (Decode as above). | R/W | 6 |
| | | OP6_SRC | 5-3 | Output channel 6 source selector (Decode as above). | R/W | 5 |
| | | OP5_SRC | 2-0 | Output channel 5 source selector (Decode as above). | R/W | 4 |
| 40Bh - 41Fh | RSVD | RSVD | – | Reserved. | – | – |

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|------------------|----------|------|--|-----|---------|
| 420h | AFNA12 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | AFN1_2A | 8-0 | Primary group audio frame number for channels 1 and 2. | R | 0 |
| 421h | AFNA34 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | AFN3_4A | 8-0 | Primary group audio frame number for channels 3 and 4. | R | 0 |
| 422h | RATEA | RSVD | 15-8 | Reserved. | R/W | 0 |
| | | RATE3_4A | 7-5 | Primary group sampling frequency for channels 3 and 4 | R | 0 |
| | | ASX3_4A | 4 | Primary group asynchronous mode for channels 3 and 4. | R | 0 |
| | | RATE1_2A | 3-1 | Primary group sampling frequency for channels 1 and 2. | R | 0 |
| | | ASX1_2A | 0 | Primary group asynchronous mode for channels 1 and 2. | R | 0 |
| 423h | ACT_A | RSVD | 15-4 | Reserved. | R/W | 0 |
| | | ACTA | 3-0 | Primary group active channels. | R | 0 |
| 424h | PRIM_AUD_DELAY_1 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL1A_1 | 8-1 | Primary Audio group delay data for channel 1. | R | 0 |
| | | EBIT1A | 0 | Primary Audio group delay data valid flag for channel 1. | R | 0 |
| 425h | PRIM_AUD_DELAY_2 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL1A_2 | 8-0 | Primary Audio group delay data for channel 1. | R | 0 |
| 426h | PRIM_AUD_DELAY_3 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL1A_3 | 8-0 | Primary Audio group delay data for channel 1. | R | 0 |
| 427h | PRIM_AUD_DELAY_4 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL2A_4 | 8-1 | Primary Audio group delay data for channel 2. | R | 0 |
| | | EBIT2A | 0 | Primary Audio group delay data valid flag for channel 2. | R | 0 |
| 428h | PRIM_AUD_DELAY_5 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL2A_5 | 8-0 | Primary Audio group delay data for channel 2. | R | 0 |
| 429h | PRIM_AUD_DELAY_6 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL2A_6 | 8-0 | Primary Audio group delay data for channel 2. | R | 0 |

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|-------------------|----------|------|--|-----|---------|
| 42Ah | PRIM_AUD_DELAY_7 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL3A_7 | 8-1 | Primary Audio group delay data for channel 3. | R | 0 |
| | | EBIT3A | 0 | Primary Audio group delay data valid flag for channel 3. | R | 0 |
| 42Bh | PRIM_AUD_DELAY_8 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL3A_8 | 8-0 | Primary Audio group delay data for channel 3. | R | 0 |
| 42Ch | PRIM_AUD_DELAY_9 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL3A_9 | 8-0 | Primary Audio group delay data for channel 3. | R | 0 |
| 42Dh | PRIM_AUD_DELAY_10 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL4A_10 | 8-1 | Primary Audio group delay data for channel 4. | R | 0 |
| | | EBIT4A | 0 | Primary Audio group delay data valid flag for channel 4. | R | 0 |
| 42Eh | PRIM_AUD_DELAY_11 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL4A_11 | 8-0 | Primary Audio group delay data for channel 4. | R | 0 |
| 42Fh | PRIM_AUD_DELAY_12 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL4A_12 | 8-0 | Primary Audio group delay data for channel 4. | R | 0 |
| 430h | AFNB12 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | AFN1_2B | 8-0 | Secondary group audio frame number for channels 1 and 2. | R | 0 |
| 431h | AFNB34 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | AFN3_4B | 8-0 | Secondary group audio frame number for channels 3 and 4. | R | 0 |
| 432h | RATEB | RSVD | 15-8 | Reserved. | R | 0 |
| | | RATE3_4B | 7-5 | Secondary group sampling frequency for channels 3 and 4. | R | 0 |
| | | ASX3_4B | 4 | Secondary group asynchronous mode for channels 3 and 4. | R | 0 |
| | | RATE1_2B | 3-1 | Secondary group sampling frequency for channels 1 and 2. | R | 0 |
| | | ASX1_2B | 0 | Secondary group asynchronous mode for channels 1 and 2. | R | 0 |
| 433h | ACT_B | RSVD | 15-4 | Reserved. | R/W | 0 |
| | | ACTB | 3-0 | Secondary group active channels. | R | 0 |

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|------------------|----------|------|--|-----|---------|
| 434h | SEC_AUD_DELAY_1 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL1B_1 | 8-1 | Secondary Audio group delay data for channel 1. | R | 0 |
| | | EBIT1B | 0 | Secondary Audio group delay data valid flag for channel 1. | R | 0 |
| 435h | SEC_AUD_DELAY_2 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL1B_2 | 8-0 | Secondary Audio group delay data for channel 1. | R | 0 |
| 436h | SEC_AUD_DELAY_3 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL1B_3 | 8-0 | Secondary Audio group delay data for channel 1. | R | 0 |
| 437h | SEC_AUD_DELAY_4 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL2B_4 | 8-1 | Secondary Audio group delay data for channel 2. | R | 0 |
| | | EBIT2B | 0 | Secondary Audio group delay data valid flag for channel 2. | R | 0 |
| 438h | SEC_AUD_DELAY_5 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL2B_5 | 8-0 | Secondary Audio group delay data for channel 2. | R | 0 |
| 439h | SEC_AUD_DELAY_6 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL2B_6 | 8-0 | Secondary Audio group delay data for channel 2. | R | 0 |
| 43Ah | SEC_AUD_DELAY_7 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL3B_7 | 8-1 | Secondary Audio group delay data for channel 3. | R | 0 |
| | | EBIT3B | 0 | Secondary Audio group delay data valid flag for channel 3. | R | 0 |
| 43Bh | SEC_AUD_DELAY_8 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL3B_8 | 8-0 | Secondary Audio group delay data for channel 3. | R | 0 |
| 43Ch | SEC_AUD_DELAY_9 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL3B_9 | 8-0 | Secondary Audio group delay data for channel 3. | R | 0 |
| 43Dh | SEC_AUD_DELAY_10 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL4B_10 | 8-1 | Secondary Audio group delay data for channel 4. | R | 0 |
| | | EBIT4B | 0 | Secondary Audio group delay data valid flag for channel 4. | R | 0 |

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------------|-------------|------|--|-----|---------|
| 43Eh | SEC_AUD_DELAY_11 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL4B_11 | 8-0 | Secondary Audio group delay data for channel 4. | R | 0 |
| 43Fh | SEC_AUD_DELAY_12 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL4B_12 | 8-0 | Secondary Audio group delay data for channel 4. | R | 0 |
| 440h | ACSR1_2A_BYTE_0_1 | ACSR1_2A_0 | 15-0 | Bytes 0 [7:0] and 1 [15:8] of audio group A channel status for channels 1 and 2 | R | 0 |
| 441h | ACSR1_2A_BYTE_2_3 | ACSR1_2A_2 | 15-0 | Bytes 2 [7:0] and 3 [15:8] of audio group A channel status for channels 1 and 2 | R | 0 |
| 442h | ACSR1_2A_BYTE_4_5 | ACSR1_2A_4 | 15-0 | Bytes 4 [7:0] and 5 [15:8] of audio group A channel status for channels 1 and 2 | R | 0 |
| 443h | ACSR1_2A_BYTE_6_7 | ACSR1_2A_6 | 15-0 | Bytes 6 [7:0] and 7 [15:8] of audio group A channel status for channels 1 and 2 | R | 0 |
| 444h | ACSR1_2A_BYTE_8_9 | ACSR1_2A_8 | 15-0 | Bytes 8 [7:0] and 9 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 445h | ACSR1_2A_BYTE_10_11 | ACSR1_2A_10 | 15-0 | Bytes 10 [7:0] and 11 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 446h | ACSR1_2A_BYTE_12_13 | ACSR1_2A_12 | 15-0 | Bytes 12 [7:0] and 13 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 447h | ACSR1_2A_BYTE_14_15 | ACSR1_2A_14 | 15-0 | Bytes 14 [7:0] and 15 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 448h | ACSR1_2A_BYTE_16_17 | ACSR1_2A_16 | 15-0 | Bytes 16 [7:0] and 17 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 449h | ACSR1_2A_BYTE_18_19 | ACSR1_2A_18 | 15-0 | Bytes 18 [7:0] and 19 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 44Ah | ACSR1_2A_BYTE_20_21 | ACSR1_2A_20 | 15-0 | Bytes 20 [7:0] and 21 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 44Bh | ACRS1_2A_BYTE22 | ACSR1_2A_22 | 15-0 | Bytes 22 of audio group A channel status for channels 1 and 2. | R | 0 |
| 450h | ACSR3_4A_BYTE0_1 | ACSR3_4A_0 | 15-0 | Bytes 0 [7:0] and 1 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 451h | ACSR3_4A_BYTE2_3 | ACSR3_4A_2 | 15-0 | Bytes 2 [7:0] and 3 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------------|-------------|------|--|-----|---------|
| 452h | ACSR3_4A_BYTE_4_5 | ACSR3_4A_4 | 15-0 | Bytes 4 [7:0] and 5 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 453h | ACSR3_4A_BYTE_6_7 | ACSR3_4A_6 | 15-0 | Bytes 6 [7:0] and 7 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 454h | ACSR3_4A_BYTE_8_9 | ACSR3_4A_8 | 15-0 | Bytes 8 [7:0] and 9 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 455h | ACSR3_4A_BYTE_10_11 | ACSR3_4A_10 | 15-0 | Bytes 10 [7:0] and 11 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 456h | ACSR3_4A_BYTE_12_13 | ACSR3_4A_12 | 15-0 | Bytes 12 [7:0] and 13 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 457h | ACSR3_4A_BYTE_14_15 | ACSR3_4A_14 | 15-0 | Bytes 14 [7:0] and 15 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 458h | ACSR3_4A_BYTE_16_17 | ACSR3_4A_16 | 15-0 | Bytes 16 [7:0] and 17 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 459h | ACSR3_4A_BYTE_18_19 | ACSR3_4A_18 | 15-0 | Bytes 18 [7:0] and 19 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 45Ah | ACSR3_4A_BYTE_20_21 | ACSR3_4A_20 | 15-0 | Bytes 20 [7:0] and 21 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 45Bh | ACSR3_4A_BYTE_22 | RSVD | 15-8 | Reserved. | R/W | 0 |
| | | ACSR3_4A_22 | 7-0 | Bytes 22 of audio group A channel status for channels 3 and 4. | R | 0 |
| 460h | ACSR1_2B_BYTE_0_1 | ACSR1_2B_0 | 15-0 | Bytes 0 [7:0] and 1 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 461h | ACSR1_2B_BYTE_2_3 | ACSR1_2B_2 | 15-0 | Bytes 2 [7:0] and 3 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 462h | ACSR1_2B_BYTE_4_5 | ACSR1_2B_4 | 15-0 | Bytes 4 [7:0] and 5 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 463h | ACSR1_2B_BYTE_6_7 | ACSR1_2B_6 | 15-0 | Bytes 6 [7:0] and 7 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 464h | ACSR1_2B_BYTE_8_9 | ACSR1_2B_8 | 15-0 | Bytes 8 [7:0] and 9 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 465h | ACSR1_2B_BYTE_10_11 | ACSR1_2B_10 | 15-0 | Bytes 10 [7:0] and 11 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|------------------------|-------------|------|--|-----|---------|
| 466h | ACSR1_2B_BYTE 12_13 | ACSR1_2B_12 | 15-0 | Bytes 12 [7:0] and 13 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 467h | ACSR1_2B_BYTE 14_15 | ACSR1_2B_14 | 15-0 | Bytes 14 [7:0] and 15 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 468h | ACSR1_2B_BYTE 16_17 | ACSR1_2B_16 | 15-0 | Bytes 16 [7:0] and 17 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 469h | ACSR1_2B_BYTE 18_19 | ACSR1_2B_18 | 15-0 | Bytes 18 [7:0] and 19 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 46Ah | ACSR1_2B_BYTE 20_21 | ACSR1_2B_20 | 15-0 | Bytes 20 [7:0] and 21 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 46Bh | ACSR1_2B_BYTE 22 | RSVD | 15-8 | Reserved. | R/W | 0 |
| | | ACSR1_2B_22 | 7-0 | Bytes 22 of audio group B channel status for channels 1 and 2. | R | 0 |
| 470h | ACSR3_4B_BYTE 0_1 | ACSR3_4B_0 | 15-0 | Bytes 0 [7:0] and 1 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 471h | ACSR3_4B_BYTE 2_3 | ACSR3_4B_2 | 15-0 | Bytes 2 [7:0] and 3 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 472h | ACSR3_4B_BYTE 4_5 | ACSR3_4B_4 | 15-0 | Bytes 4 [7:0] and 5 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 473h | ACSR3_4B_BYTE 6_7 | ACSR3_4B_6 | 15-0 | Bytes 6 [7:0] and 7 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 474h | ACSR3_4B_BYTE 8_9 | ACSR3_4B_8 | 15-0 | Bytes 8 [7:0] and 9 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 475h | ACSR3_4B_BYTE 10_11 | ACSR3_4B_10 | 15-0 | Bytes 10 [7:0] and 11 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 476h | ACSR3_4B_BYTE 12_13 | ACSR3_4B_12 | 15-0 | Bytes 12 [7:0] and 13 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 477h | ACSR3_4B_BYTE 14_15 | ACSR3_4B_14 | 15-0 | Bytes 14 [7:0] and 15 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 478h | ACSR3_4A_BYTE 16_17 | ACSR3_4B_16 | 15-0 | Bytes 16 [7:0] and 17 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 479h | ACSR3_4A_BYTE 18_19 | ACSR3_4B_18 | 15-0 | Bytes 18 [7:0] and 19 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |

Table 4-30: SD Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------------|-------------|------|---|-----|---------|
| 47Ah | ACSR3_4A_BYTE_20_21 | ACSR3_4B_20 | 15-0 | Bytes 20 [7:0] and 21 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 47Bh | ACSR3_4A_BYTE_22 | ACSR3_4B_22 | 15-0 | Bytes 22 of audio group B channel status for channels 3 and 4. | R | 0 |
| 480h | ACSR_BYTE_0 | ACSR_BYTE0 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register for 23 registers. | R | 0 |
| 481h | ACSR_BYTE_1 | ACSR_BYTE1 | 7-0 | – | W | 0 |
| 482h | ACSR_BYTE_2 | ACSR_BYTE2 | 7-0 | – | W | 0 |
| 483h | ACSR_BYTE_3 | ACSR_BYTE3 | 7-0 | – | W | 0 |
| 484h | ACSR_BYTE_4 | ACSR_BYTE4 | 7-0 | – | W | 0 |
| 485h | ACSR_BYTE_5 | ACSR_BYTE5 | 7-0 | – | W | 0 |
| 486h | ACSR_BYTE_6 | ACSR_BYTE6 | 7-0 | – | W | 0 |
| 487h | ACSR_BYTE_7 | ACSR_BYTE7 | 7-0 | – | W | 0 |
| 488h | ACSR_BYTE_8 | ACSR_BYTE8 | 7-0 | – | W | 0 |
| 489h | ACSR_BYTE_9 | ACSR_BYTE9 | 7-0 | – | W | 0 |
| 48Ah | ACSR_BYTE_10 | ACSR_BYTE10 | 7-0 | – | W | 0 |
| 48Bh | ACSR_BYTE_11 | ACSR_BYTE11 | 7-0 | – | W | 0 |
| 48Ch | ACSR_BYTE_12 | ACSR_BYTE12 | 7-0 | – | W | 0 |
| 48Dh | ACSR_BYTE_13 | ACSR_BYTE13 | 7-0 | – | W | 0 |
| 48Eh | ACSR_BYTE_14 | ACSR_BYTE14 | 7-0 | – | W | 0 |
| 48Fh | ACSR_BYTE_15 | ACSR_BYTE15 | 7-0 | – | W | 0 |
| 490h | ACSR_BYTE_16 | ACSR_BYTE16 | 7-0 | – | W | 0 |
| 491h | ACSR_BYTE_17 | ACSR_BYTE17 | 7-0 | – | W | 0 |
| 492h | ACSR_BYTE_18 | ACSR_BYTE18 | 7-0 | – | W | 0 |
| 493h | ACSR_BYTE_19 | ACSR_BYTE19 | 7-0 | – | W | 0 |
| 494h | ACSR_BYTE_20 | ACSR_BYTE20 | 7-0 | – | R/W | 0 |
| 495h | ACSR_BYTE_21 | ACSR_BYTE21 | 7-0 | – | R/W | 0 |
| 496h | ACSR_BYTE_22 | ACSR_BYTE22 | 7-0 | – | R/W | 0 |

4.21.3 HD and 3G Audio Core Registers

Note: The GS2970A only accepts write/read commands to/from the HD/3G Audio Register Map when the audio core is locked to the incoming HD or 3G video format.

Table 4-31: HD and 3G Audio Core Configuration and Status Registers

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|----------------|-------|--|-----|---------|
| 200h | CFG_AUD | ECC_OFF | 15 | Disables ECC error correction. | R/W | 0 |
| | | ALL_DEL | 14 | Selects deletion of all audio data and all audio control packets 0: Do not delete existing audio control packets 1: Delete existing audio control packets. | R/W | 0 |
| | | MUTE_ALL | 13 | Mute all output channels 0: Normal 1: Muted | R/W | 0 |
| | | ACS_USE_SECOND | 12 | Extract Audio Channel Status from second channel pair. | R/W | 0 |
| | | ASWLB | 11-10 | Secondary group output word length. 00: 24 bits 01: 20 bits 10: 16 bits 11: invalid | R/W | 3 |
| | | ASWLA | 9-8 | Primary group output word length. 00: 24 bits 01: 20 bits 10: 16 bits 11: invalid | R/W | 3 |
| | | AMB | 7-6 | Secondary group output format selector. 00: AES/EBU audio output 01: Serial audio output: left justified MSB first 10: Serial audio output: right justified. MSB first 11: I2S serial audio output | R/W | 3 |
| | | AMA | 5-4 | Primary group output format selector. 00: AES/EBU audio output 01: Serial audio output: left justified MSB first 10: Serial audio output: right justified MSB first 11: I2S serial audio output | R/W | 3 |

Table 4-31: HD and 3G Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|-------------|------|---|------|---------|
| 200h | CFG_AUD | IDB | 3-2 | Specifies the Secondary audio group to extract. 00: Audio group #1 01: Audio group #2 10: Audio group #3 11: Audio group #4 Note: Should IDA and IDB be set to the same value, they automatically revert to their default values. | R/W | 1 |
| | | IDA | 1-0 | Specifies the Primary audio group to extract. 00: Audio group #1 01: Audio group #2 10: Audio group #3 11: Audio group #4 Note: Should IDA and IDB be set to the same value, they automatically revert to their default values. | R/W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| | | DBNB_ERR | 7 | Set when Secondary group audio Data Block Number sequence is discontinuous. | ROCW | 0 |
| | | DBNA_ERR | 6 | Set when Primary group audio Data Block Number sequence is discontinuous. | ROCW | 0 |
| | | CTRB_DET | 5 | Set when Secondary group audio control packet is detected. | ROCW | 0 |
| 201h | ACS_DET | CTRA_DET | 4 | Set when Primary group audio control packet is detected. | ROCW | 0 |
| | | ACS_DET3_4B | 3 | Secondary group audio status detected for channels 3 and 4. | ROCW | 0 |
| | | ACS_DET1_2B | 2 | Secondary group audio status detected for channels 1 and 2. | ROCW | 0 |
| | | ACS_DET3_4A | 1 | Primary group audio status detected for channels 3 and 4. | ROCW | 0 |
| | | ACS_DET1_2A | 0 | Primary group audio status detected for channels 1 and 2. | ROCW | 0 |

Table 4-31: HD and 3G Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|----------------|------|---|------|---------|
| 202h | AUD_DET1 | RSVD | 15-9 | Reserved. | R | 0 |
| | | IDB_READBACK | 8-7 | Actual value of IDB in the hardware. | R | 1 |
| | | IDA_READBACK | 6-5 | Actual value of IDA in the hardware. | R | 0 |
| | | ADPG4_DET | 4 | Set while Group 4 audio data packets are detected. | R | 0 |
| | | ADPG3_DET | 3 | Set while Group 3 audio data packets are detected. | R | 0 |
| | | ADPG2_DET | 2 | Set while Group 2 audio data packets are detected. | R | 0 |
| | | ADPG1_DET | 1 | Set while Group 1 audio data packets are detected. | R | 0 |
| | | ACS_APPLY_WAIT | 0 | ACS_APPLY_WAIT: Set while output channels 1 and 2 are waiting for a status boundary to apply the ACSR[183:0] data. | R | 0 |
| 203h | AUD_DET2 | RSVD | 15-2 | Reserved. | R/W | 0 |
| | | ECCA_ERROR | 1 | Primary group audio data packet error detected. | ROCW | 0 |
| | | ECCB_ERROR | 0 | Secondary group audio data packet error detected. | ROCW | 0 |
| 204h | REGEN | RSVD | 15-2 | Reserved. | R/W | 0 |
| | | ACS_APPLY | 1 | Cause channel status data in ACSR[183:0] to be transferred to the channel status replacement mechanism. The transfer does not occur until the next status boundary. | R/W | 0 |
| | | ACS_REGEN | 0 | Specifies that Audio Channel Status of all channels should be replaced with ACSR[183:0] field. 0: Do not replace Channel Status 1: Replace Channel Status of all channels | R/W | 0 |
| 205h | CH_MUTE | RSVD | 15 | Reserved. | R/W | 0 |
| | | MUTEB | 7-4 | Mute Secondary output channels 4..1 Where bits 7:4 = channel 4:1 1: Mute 0: Normal | R/W | 0 |
| | | MUTEA | 3-0 | Mute Primary output channels 4..1 Where bits 3:0 = channel 4:1 1: Mute 0: Normal | R/W | 0 |

Table 4-31: HD and 3G Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|------------|------|---|-----|---------|
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| | | CH4_VALIDB | 7 | Secondary group channel 4 sample validity flag. | R | 0 |
| | | CH3_VALIDB | 6 | Secondary group channel 3 sample validity flag. | R | 0 |
| | | CH2_VALIDB | 5 | Secondary group channel 2 sample validity flag. | R | 0 |
| 206h | CH_VALID | CH1_VALIDB | 4 | Secondary group channel 1 sample validity flag. | R | 0 |
| | | CH4_VALIDA | 3 | Primary group channel 4 sample validity flag. | R | 0 |
| | | CH3_VALIDA | 2 | Primary group channel 3 sample validity flag. | R | 0 |
| | | CH2_VALIDA | 1 | Primary group channel 2 sample validity flag. | R | 0 |
| | | CH1_VALIDA | 0 | Primary group channel 1 sample validity flag. | R | 0 |

Table 4-31: HD and 3G Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|--------------|-------------------------|--|-----|--|-----|---------|
| 207h | HD_AUDIO_ERR OR_MASK | RSVD | 15 | Reserved. | R/W | 0 |
| | | EN_MISSING_PHASE | 14 | Asserts $\overline{\text{AUDIO_ERROR}}$ when chosen group's phase data is missing | R/W | 0 |
| | | EN_ACS_DET3_4B | 13 | Asserts $\overline{\text{AUDIO_ERROR}}$ when ACS_DET3_4B flag is set. | R/W | 0 |
| | | EN_ACS_DET1_2B | 12 | Asserts $\overline{\text{AUDIO_ERROR}}$ when ACS_DET1_2B flag is set. | R/W | 0 |
| | | EN_ACS_DET3_4A | 11 | Asserts $\overline{\text{AUDIO_ERROR}}$ when ACS_DET3_4A flag is set. | R/W | 0 |
| | | EN_ACS_DET1_2A | 10 | Asserts $\overline{\text{AUDIO_ERROR}}$ when ACS_DET1_2A flag is set. | R/W | 0 |
| | | EN_CTRB_DET | 9 | Asserts $\overline{\text{AUDIO_ERROR}}$ when CTRB_DET flag is set. | R/W | 0 |
| | | EN_CTRA_DET | 8 | Asserts $\overline{\text{AUDIO_ERROR}}$ when CTRA_DET flag is set. | R/W | 0 |
| | | EN_DBNB_ERR | 7 | Asserts $\overline{\text{AUDIO_ERROR}}$ when DBNB_ERR flag is set. | R/W | 0 |
| | | EN_DBNA_ERR | 6 | Asserts $\overline{\text{AUDIO_ERROR}}$ when DBNA_ERR flag is set. | R/W | 0 |
| | | EN_ECCB_ERR | 5 | Asserts $\overline{\text{AUDIO_ERROR}}$ when ECCB_ERR flag is set. | R/W | 0 |
| | | EN_ECCA_ERR | 4 | Asserts $\overline{\text{AUDIO_ERROR}}$ when ECCA_ERR flag is set. | R/W | 0 |
| | | EN_ADPG4_DET | 3 | Asserts $\overline{\text{AUDIO_ERROR}}$ when ADPG4_DET flag is set. | R/W | 0 |
| | | EN_ADPG3_DET | 2 | Asserts $\overline{\text{AUDIO_ERROR}}$ when ADPG3_DET flag is set. | R/W | 0 |
| | | EN_ADPG2_DET | 1 | Asserts $\overline{\text{AUDIO_ERROR}}$ when ADPG2_DET flag is set. | R/W | 0 |
| EN_ADPG1_DET | 0 | Asserts $\overline{\text{AUDIO_ERROR}}$ when ADPG1_DET flag is set. | R/W | 0 | | |

Table 4-31: HD and 3G Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|----------------|-------|--|-----|---------|
| | | RSVD | 15-11 | Reserved. | R/W | 0 |
| | | SEL_PHASE_SRC | 10 | Selects between the Primary and Secondary embedded phase info. | R/W | 0 |
| | | LSB_FIRSTB | 9 | Causes the Secondary group serial output formats to use LSB first. | R/W | 0 |
| | | LSB_FIRSTA | 8 | Causes the Primary group serial output formats to use LSB first. | R/W | 0 |
| | | FORCE_M | 7 | Disables M value detection and forces M value to that specified by FORCE_MEQ1001. | R/W | 0 |
| | | FORCE_MEQ1001 | 6 | Specifies M value when FORCE_M is set. 1: M= 1.001 0: M = 1.000 | R/W | 0 |
| 208h | CFG_AUD_2 | IGNORE_PHASE | 5 | Causes the Demultiplexer to ignore the embedded clock info in both the Primary and Secondary group audio data packets. Clock is generated based on the video format and M value. | R/W | 0 |
| | | FORCE_ACLK128 | 4 | Causes the core to ignore embedded clock info and derive phase information from ACLK128. | R/W | 0 |
| | | EN_NOT_LOCKED | 3 | Asserts interrupt when locked is not asserted. | R/W | 0 |
| | | EN_NO_VIDEO | 2 | Asserts interrupt when the video format is unknown. | R/W | 0 |
| | | EN_NO_PHASEB | 1 | Asserts $\overline{\text{AUDIO_ERROR}}$ when NO_PHASEB_DATA is set. | R/W | 0 |
| | | EN_NO_PHASEA | 0 | Asserts $\overline{\text{AUDIO_ERROR}}$ when NO_PHASEA_DATA is set. | R/W | 0 |
| | | RSVD | 15-3 | Reserved. | R/W | 0 |
| 209h | CFG_AUD_3 | MISSING_PHASE | 2 | Embedded phase info for chosen group missing or incorrect. | R | 0 |
| | | NO_PHASEB_DATA | 1 | Secondary group has invalid embedded clock information. | R | 0 |
| | | NO_PHASEA_DATA | 0 | Primary group has invalid embedded clock information. | R | 0 |

Table 4-31: HD and 3G Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|-------------|---------------|----------|-------|---|-----|---------|
| | | RSVD | 15-12 | Reserved. | R | 0 |
| 20Ah | OUTPUT_SEL_1 | OP4_SRC | 11-9 | Output channel 4 source selector. 000: Primary audio group channel 1 001: Primary audio group channel 2 010: Primary audio group channel 3 011: Primary audio group channel 4 100: Secondary audio group channel 1 101: Secondary audio group channel 2 110: Secondary audio group channel 3 111: Secondary audio group channel 4 | R/W | 3 |
| | | OP3_SRC | 8-6 | Output channel 3 source selector (Decode as above). | R/W | 2 |
| | | OP2_SRC | 5-3 | Output channel 2 source selector (Decode as above). | R/W | 1 |
| | | OP1_SRC | 2-0 | Output channel 1 source selector (Decode as above). | R/W | 0 |
| | | RSVD | 15-12 | Reserved. | R/W | 0 |
| 20Bh | OUTPUT_SEL_2 | OP8_SRC | 11-9 | Output channel 8 source selector. 000: Primary audio group channel 1 001: Primary audio group channel 2 010: Primary audio group channel 3 011: Primary audio group channel 4 100: Secondary audio group channel 1 101: Secondary audio group channel 2 110: Secondary audio group channel 3 111: Secondary audio group channel 4 | R/W | 7 |
| | | OP7_SRC | 8-6 | Output channel 7 source selector (Decode as above). | R/W | 6 |
| | | OP6_SRC | 5-3 | Output channel 6 source selector (Decode as above). | R/W | 5 |
| | | OP5_SRC | 2-0 | Output channel 5 source selector (Decode as above). | R/W | 4 |
| 20Ch - 21Fh | RSVD | RSVD | – | Reserved. | – | – |
| 220h | AFNA | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | AFNA | 8-0 | Primary group audio frame number. | R | 0 |

Table 4-31: HD and 3G Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|-------------|------------------|-----------|------|---|-----|---------|
| 221h | RATEA | RSVD | 15-4 | Reserved. | R/W | 0 |
| | | RATEA | 3-1 | Primary group sampling frequency for channels 1 and 2. | R | 0 |
| | | ASXA | 0 | Primary group asynchronous mode for channels 1 and 2. | R | 0 |
| 222h | ACTA | RSVD | 15-4 | Reserved. | R/W | 0 |
| | | ACTA | 3-0 | Primary group active channels. | R | 0 |
| 223h | PRIM_AUD_DELAY_1 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL1_2A_1 | 8-1 | Primary Audio group delay data for channels 1 and 2 [7:0]. | R | 0 |
| | | EBIT1_2A | 0 | Primary Audio group delay data valid flag for channels 1 and 2. | R | 0 |
| 224h | PRIM_AUD_DELAY_2 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL1_2A_2 | 8-0 | Primary Audio group delay data for channels 1 and 2 [16:8]. | R | 0 |
| 225h | PRIM_AUD_DELAY_3 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL1_2A_3 | 8-0 | Primary Audio group delay data for channels 1 and 2 [25:17]. | R | 0 |
| 226h | PRIM_AUD_DELAY_4 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL3_4A_4 | 8-1 | Primary Audio group delay data for channels 3 and 4 [7:0]. | R | 0 |
| | | EBIT3_4A | 0 | Primary Audio group delay data valid flag for channels 3 and 4. | R | 0 |
| 227h | PRIM_AUD_DELAY_5 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL3_4A_5 | 8-0 | Primary Audio group delay data for channels 3 and 4 [16:8]. | R | 0 |
| 228h | PRIM_AUD_DELAY_6 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL3_4A_6 | 8-0 | Primary Audio group delay data for channels 3 and 4 [25:17]. | R | 0 |
| 229h - 22Fh | RSVD | RSVD | – | Reserved. | R/W | 0 |
| 230h | AFNB | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | AFNB | 8-0 | Secondary group audio frame number. | R | 0 |
| 231h | RATEB | RSVD | 15-4 | Reserved. | R/W | 0 |
| | | RATEB | 3-1 | Secondary group sampling frequency for channels 1 and 2. | R | 0 |
| | | ASXB | 0 | Secondary group asynchronous mode for channels 1 and 2. | R | 0 |

Table 4-31: HD and 3G Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|-------------|-------------------|------------|------|--|-----|---------|
| 232h | ACTB | RSVD | 15-4 | Reserved. | R/W | 0 |
| | | ACTB | 3-0 | Secondary group active channels. | R | 0 |
| 233h | SEC_AUD_DELAY_1 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL1_2B_1 | 8-1 | Secondary Audio group delay data valid flag for channels 1 and 2. | R | 0 |
| | | EBIT1_2B | 0 | Secondary Audio group delay data for channels 1 and 2 [7:0]. | R | 0 |
| 234h | SEC_AUD_DELAY_2 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL1_2B_2 | 8-0 | Secondary Audio group delay data for channels 1 and 2 [16:8]. | R | 0 |
| 235h | SEC_AUD_DELAY_3 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL1_2B_3 | 8-0 | Secondary Audio group delay data for channels 1 and 2 [25:17]. | R | 0 |
| 236h | SEC_AUD_DELAY_4 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL3_4B_4 | 8-1 | Secondary Audio group delay data for channels 3 and 4 [7:0]. | R | 0 |
| | | EBIT3_4B | 0 | Secondary Audio group delay data valid flag for channels 3 and 4. | R | 0 |
| 237h | SEC_AUD_DELAY_5 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL3_4B_5 | 8-0 | Secondary Audio group delay data for channels 3 and 4 [16:8]. | R | 0 |
| 238h | SEC_AUD_DELAY_6 | RSVD | 15-9 | Reserved. | R/W | 0 |
| | | DEL3_4B_6 | 8-0 | Secondary Audio group delay data for channels 3 and 4 [25:17]. | R | 0 |
| 239h - 23Fh | RSVD | RSVD | – | Reserved. | R/W | 0 |
| 240h | ACSR1_2A_BYTE_0_1 | ACSR1_2A_0 | 15-0 | Bytes 0 [7:0] and 1 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 241h | ACSR1_2A_BYTE_2_3 | ACSR1_2A_2 | 15-0 | Bytes 2 [7:0] and 3 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 242h | ACSR1_2A_BYTE_4_5 | ACSR1_2A_4 | 15-0 | Bytes 4 [7:0] and 5 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 243h | ACSR1_2A_BYTE_6_7 | ACSR1_2A_6 | 15-0 | Bytes 6 [7:0] and 7 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 244h | ACSR1_2A_BYTE_8_9 | ACSR1_2A_8 | 15-0 | Bytes 8 [7:0] and 9 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |

Table 4-31: HD and 3G Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|----------------|------------------------|-------------|------|--|-----|---------|
| 245h | ACSR1_2A_BYTE 10_11 | ACSR1_2A_10 | 15-0 | Bytes 10 [7:0] and 11 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 246h | ACSR1_2A_BYTE 12_13 | ACSR1_2A_12 | 15-0 | Bytes 12 [7:0] and 13 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 247h | ACSR1_2A_BYTE 14_15 | ACSR1_2A_14 | 15-0 | Bytes 14 [7:0] and 15 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 248h | ACSR1_2A_BYTE 16_17 | ACSR1_2A_16 | 15-0 | Bytes 16 [7:0] and 17 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 249h | ACSR1_2A_BYTE 18_19 | ACSR1_2A_18 | 15-0 | Bytes 18 [7:0] and 19 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 24Ah | ACSR1_2A_BYTE 20_21 | ACSR1_2A_20 | 15-0 | Bytes 20 [7:0] and 21 [15:8] of audio group A channel status for channels 1 and 2. | R | 0 |
| 24Bh | ACSR1_2A_BYTE 22 | RSVD | 15-8 | Reserved. | R/W | 0 |
| | | ACSR1_2A_22 | 7-0 | Bytes 22 of audio group A channel status for channels 1 and 2. | R | 0 |
| 24Ch - 24Fh | RSVD | RSVD | 15-0 | Reserved. | R/W | 0 |
| 250h | ACSR3_4A_BYTE 0_1 | ACSR3_4A_0 | 15-0 | Bytes 0 [7:0] and 1 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 251h | ACSR3_4A_BYTE 2_3 | ACSR3_4A_2 | 15-0 | Bytes 2 [7:0] and 3 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 252h | ACSR3_4A_BYTE 4_5 | ACSR3_4A_4 | 15-0 | Bytes 4 [7:0] and 5 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 253h | ACSR3_4A_BYTE 6_7 | ACSR3_4A_6 | 15-0 | Bytes 6 [7:0] and 7 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 254h | ACSR3_4A_BYTE 8_9 | ACSR3_4A_8 | 15-0 | Bytes 8 [7:0] and 9 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 255h | ACSR3_4A_BYTE 10_11 | ACSR3_4A_10 | 15-0 | Bytes 10 [7:0] and 11 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 256h | ACSR3_4A_BYTE 12_13 | ACSR3_4A_12 | 15-0 | Bytes 12 [7:0] and 13 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 257h | ACSR3_4A_BYTE 14_15 | ACSR3_4A_14 | 15-0 | Bytes 14 [7:0] and 15 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |

Table 4-31: HD and 3G Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|----------------|------------------------|-------------|------|--|-----|---------|
| 258h | ACSR3_4A_BYTE 16_17 | ACSR3_4A_16 | 15-0 | Bytes 16 [7:0] and 17 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 259h | ACSR3_4A_BYTE 18_19 | ACSR3_4A_18 | 15-0 | Bytes 18 [7:0] and 19 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 25Ah | ACSR3_4A_BYTE 20_21 | ACSR3_4A_20 | 15-0 | Bytes 20 [7:0] and 21 [15:8] of audio group A channel status for channels 3 and 4. | R | 0 |
| 25Bh | ACSR3_4A_BYTE 22 | RSVD | 15-8 | Reserved. | R/W | 0 |
| | | ACSR3_4A_22 | 7-0 | Bytes 22 of audio group A channel status for channels 3 and 4. | R | 0 |
| 25Ch - 25Fh | RSVD | RSVD | 15-0 | Reserved. | R/W | 0 |
| 260h | ACSR1_2B_BYTE 0_1 | ACSR1_2B_0 | 15-0 | Bytes 0 [7:0] and 1 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 261h | ACSR1_2B_BYTE 2_3 | ACSR1_2B_2 | 15-0 | Bytes 2 [7:0] and 3 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 262h | ACSR1_2B_BYTE 4_5 | ACSR1_2B_4 | 15-0 | Bytes 4 [7:0] and 5 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 263h | ACSR1_2B_BYTE 6_7 | ACSR1_2B_6 | 15-0 | Bytes 6 [7:0] and 7 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 264h | ACSR1_2B_BYTE 8_9 | ACSR1_2B_8 | 15-0 | Bytes 8 [7:0] and 9 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 265h | ACSR1_2B_BYTE 10_11 | ACSR1_2B_10 | 15-0 | Bytes 10 [7:0] and 11 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 266h | ACSR1_2B_BYTE 12_13 | ACSR1_2B_12 | 15-0 | Bytes 12 [7:0] and 13 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 267h | ACSR1_2B_BYTE 14_15 | ACSR1_2B_14 | 15-0 | Bytes 14 [7:0] and 15 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 268h | ACSR1_2B_BYTE 16_17 | ACSR1_2B_16 | 15-0 | Bytes 16 [7:0] and 17 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 269h | ACSR1_2B_BYTE 18_19 | ACSR1_2B_18 | 15-0 | Bytes 18 [7:0] and 19 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |
| 26Ah | ACSR1_2B_BYTE 20_21 | ACSR1_2B_20 | 15-0 | Bytes 20 [7:0] and 21 [15:8] of audio group B channel status for channels 1 and 2. | R | 0 |

Table 4-31: HD and 3G Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|----------------|------------------------|-------------|------|--|-----|---------|
| 26Bh | ACSR1_2B_BYTE 22 | RSVD | 15-8 | Reserved. | R/W | 0 |
| | | ACSR1_2B_22 | 7-0 | Bytes 22 of audio group B channel status for channels 1 and 2. | R | 0 |
| 26Ch - 26Fh | RSVD | RSVD | 15-0 | Reserved. | R/W | 0 |
| 270h | ACSR3_4B_BYTE 0_1 | ACSR3_4B_0 | 15-0 | Bytes 0 [7:0] and 1 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 271h | ACSR3_4B_BYTE 2_3 | ACSR3_4B_2 | 15-0 | Bytes 2 [7:0] and 3 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 272h | ACSR3_4B_BYTE 4_5 | ACSR3_4B_4 | 15-0 | Bytes 4 [7:0] and 5 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 273h | ACSR3_4B_BYTE 6_7 | ACSR3_4B_6 | 15-0 | Bytes 6 [7:0] and 7 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 274h | ACSR3_4B_BYTE 8_9 | ACSR3_4B_8 | 15-0 | Bytes 8 [7:0] and 9 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 275h | ACSR3_4B_BYTE 10_11 | ACSR3_4B_10 | 15-0 | Bytes 10 [7:0] and 11 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 276h | ACSR3_4B_BYTE 12_13 | ACSR3_4B_12 | 15-0 | Bytes 12 [7:0] and 13 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 277h | ACSR3_4B_BYTE 14_15 | ACSR3_4B_14 | 15-0 | Bytes 14 [7:0] and 15 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 278h | ACSR3_4B_BYTE 16_17 | ACSR3_4B_16 | 15-0 | Bytes 16 [7:0] and 17 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 279h | ACSR3_4B_BYTE 18_19 | ACSR3_4B_18 | 15-0 | Bytes 18 [7:0] and 19 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 27Ah | ACSR3_4B_BYTE 20_21 | ACSR3_4B_20 | 15-0 | Bytes 20 [7:0] and 21 [15:8] of audio group B channel status for channels 3 and 4. | R | 0 |
| 27Bh | ACSR3_4B_BYTE 22 | RSVD | 15-8 | Reserved. | R/W | 0 |
| | | ACSR3_4B_22 | 7-0 | Bytes 22 of audio group B channel status for channels 3 and 4. | R | 0 |
| 27Ch - 27Fh | RSVD | RSVD | 15-0 | Reserved. | R/W | 0 |

Table 4-31: HD and 3G Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|----------|------|--|-----|---------|
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 280h | ACSR_BYTE_0 | ACSR0 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 281h | ACSR_BYTE_1 | ACSR1 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 282h | ACSR_BYTE_2 | ACSR2 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 283h | ACSR_BYTE_3 | ACSR3 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 284h | ACSR_BYTE_4 | ACSR4 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 285h | ACSR_BYTE_5 | ACSR5 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 286h | ACSR_BYTE_6 | ACSR6 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |

Table 4-31: HD and 3G Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|----------|------|--|-----|---------|
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 287h | ACSR_BYTE_7 | ACSR7 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 288h | ACSR_BYTE_8 | ACSR8 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 289h | ACSR_BYTE_9 | ACSR9 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 28Ah | ACSR_BYTE_10 | ACSR10 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 28Bh | ACSR_BYTE_11 | ACSR11 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 28Ch | ACSR_BYTE_12 | ACSR12 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 28Dh | ACSR_BYTE_13 | ACSR13 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |

Table 4-31: HD and 3G Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|----------|------|--|-----|---------|
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 28Eh | ACSR_BYTE_14 | ACSR14 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 28Fh | ACSR_BYTE_15 | ACSR15 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 290h | ACSR_BYTE_16 | ACSR16 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 291h | ACSR_BYTE_17 | ACSR17 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 292h | ACSR_BYTE_18 | ACSR18 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 293h | ACSR_BYTE_19 | ACSR19 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 294h | ACSR_BYTE_20 | ACSR20 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |

Table 4-31: HD and 3G Audio Core Configuration and Status Registers (Continued)

| Address | Register Name | Bit Name | Bit | Description | R/W | Default |
|---------|---------------|----------|------|--|-----|---------|
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 295h | ACSR_BYTE_21 | ACSR21 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| | | RSVD | 15-8 | Reserved. | R/W | 0 |
| 296h | ACSR_BYTE_22 | ACSR22 | 7-0 | Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register starting at register 280h and ending at register 296h. | W | 0 |
| 297h | RSVD | RSVD | 15-0 | Reserved. | R | 29 |

Table 4-32: ANC Extraction FIFO Access Registers

| Address | Register Name | Bit | Description | R/W | Default |
|-------------|-----------------|------|--|-----|---------|
| 800h - BFFh | ANC_PACKET_BANK | 15-0 | Extracted Ancillary Data 91024 words. Bit 15-8: Most Significant Word (MSW). Bit 7-0: Least Significant Word (LSW). See Section 4.18.8. | R | 0 |

Legend:

R = Read only

ROCW = Read Only, Clear on Write

R/W = Read or Write

W = Write only

4.22 JTAG Test Operation

When the JTAG/ $\overline{\text{HOST}}$ pin of the GS2970A is set HIGH, the host interface port is configured for JTAG test operation. In this mode, pins E7, F8, F7, and E8 become TDO, TCK, TMS, and TDI. In addition, the $\overline{\text{RESET_TRST}}$ pin operates as the test reset pin.

Boundary scan testing using the JTAG interface is enabled in this mode.

There are two ways in which JTAG can be used:

1. As a stand-alone JTAG interface to be used at in-circuit ATE (Automatic Test Equipment) during PCB assembly.
2. Under control of a host processor for applications such as system power on self tests.

When the JTAG tests are applied by ATE, care must be taken to disable any other devices driving the digital I/O pins. If the tests are to be applied only at ATE, this can be

accomplished with tri-state buffers used in conjunction with the JTAG/ $\overline{\text{HOST}}$ input signal. This is shown in Figure 4-53.

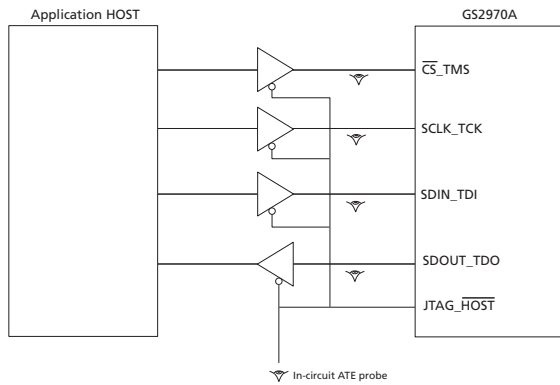


Figure 4-53: In-Circuit JTAG

Alternatively, if the test capabilities are to be used in the system, the host processor may still control the JTAG/ $\overline{\text{HOST}}$ input signal, but some means for tri-stating the host must exist in order to use the interface at ATE. This is represented in Figure 4-54.

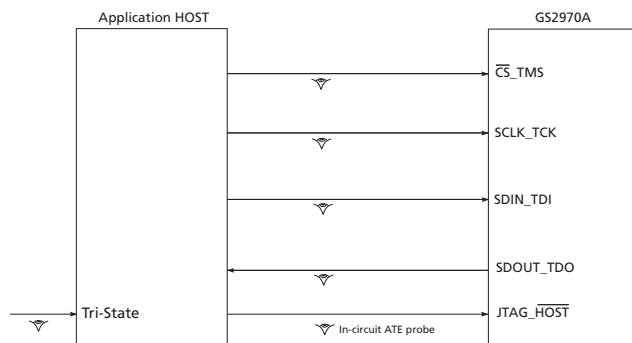


Figure 4-54: System JTAG

Scan coverage is limited to digital pins only. There is no scan coverage for analog pins VCO, SDO/ $\overline{\text{SDO}}$, RSET, LF, and CP_RES.

The JTAG/ $\overline{\text{HOST}}$ pin must be held LOW during scan and therefore has no scan coverage.

Please contact your Semtech representative to obtain the BSDL model for the GS2970A.

4.23 Device Power-up

Because the GS2970A is designed to operate in a multi-voltage environment, any power-up sequence is allowed. The charge pump, phase detector, core logic, serial digital output and I/O buffers can all be powered up in any order.

Note: Power ramp-up time (10% to 90%) $\geq 40\mu\text{s}$.

4.24 Device Reset

Note: At power-up, the device must be reset to operate correctly.

In order to initialize all internal operating conditions to their default states, hold the $\overline{\text{RESET_TRST}}$ signal LOW for a minimum of $t_{\text{reset}} = 1\text{ms}$ after all power supplies are stable. There are no requirements for power supply sequencing.

When held in reset, all device outputs are driven to a high-impedance state.

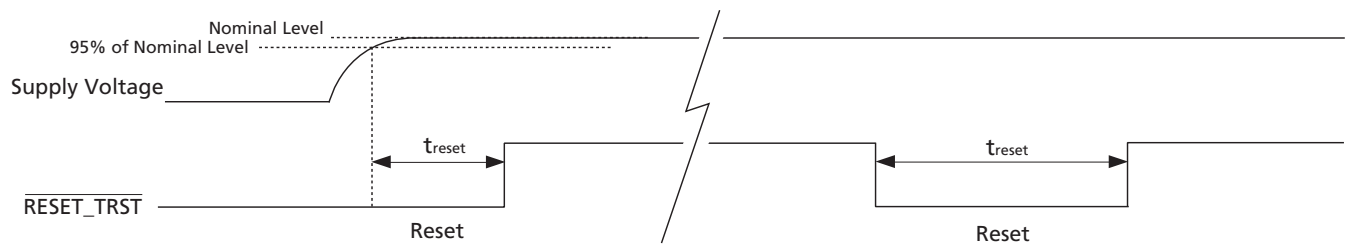


Figure 4-55: Reset Pulse

4.25 Standby Mode

The STANDBY pin reduces power to a minimum by disabling all circuits except for the register configuration. Upon removal of the signal to the STANDBY pin, the device returns to its previous operating condition within 1 second, without requiring input from the host interface.

Note: In standby mode or reset, the crystal buffer output remains enabled. This allows users to reset the GS2970A device without resetting other downstream devices that are using the same reference. This also allows users to put the GS2970A device in standby mode and still use the loop-through mode.

5. Application Reference Design

5.1 Typical Application Circuit

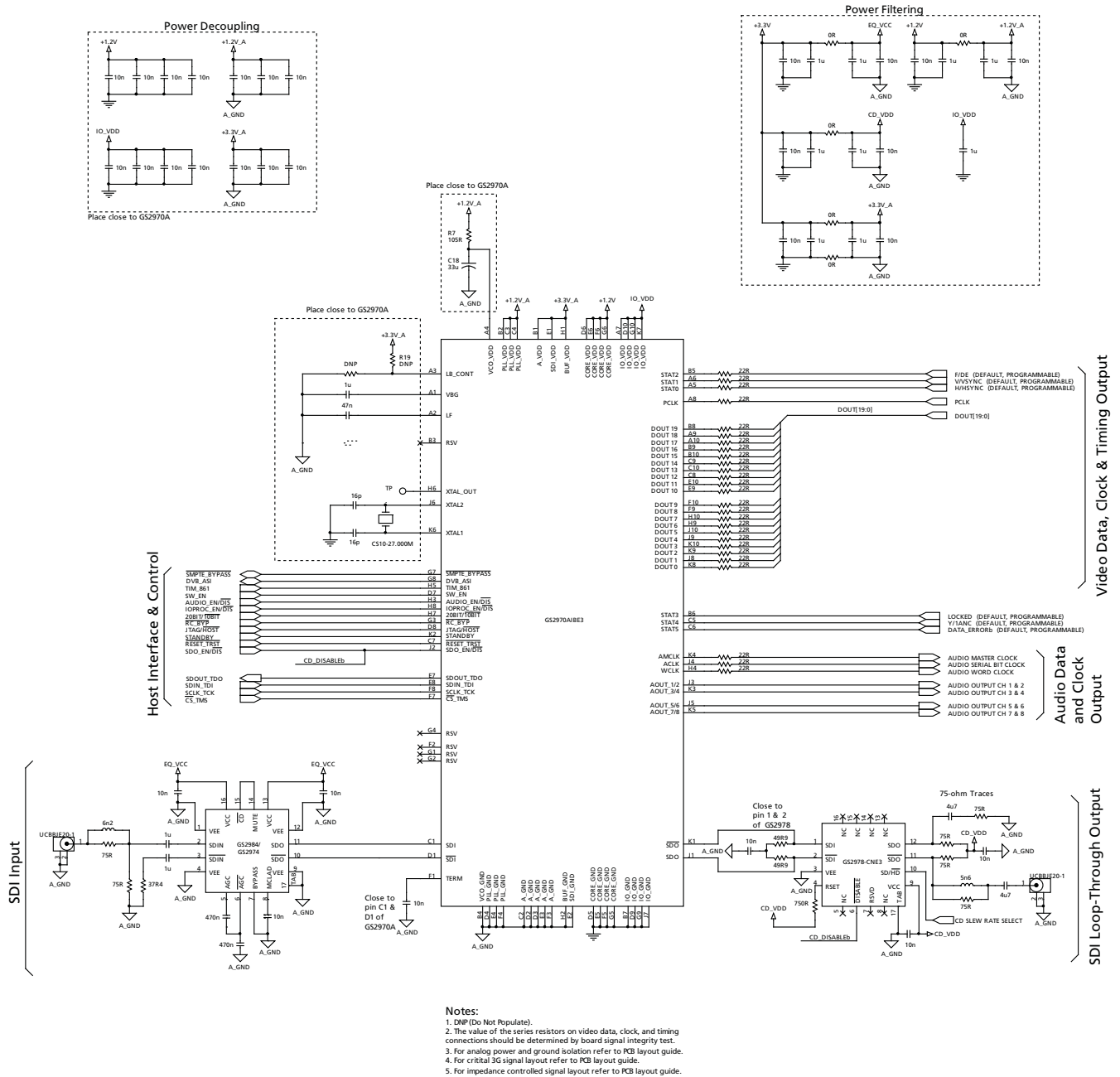


Figure 5-1: Typical Application Circuit

6. References & Relevant Standards

Table 6-1: SMPTE Standards References

| | |
|--------------|---|
| SMPTE ST 125 | Component video signal 4:2:2 – bit parallel interface |
| SMPTE ST 259 | 10-bit 4:2:2 Component and 4fsc Composite Digital Signals - Serial Digital Interface |
| SMPTE ST 260 | 1125 / 60 high definition production system – digital representation and bit parallel interface |
| SMPTE ST 267 | Bit parallel digital interface – component video signal 4:2:2 16 x 9 aspect ratio |
| SMPTE ST 272 | Formatting AES/EBU Audio and Auxiliary Data into Digital Video Ancillary Data Space |
| SMPTE ST 274 | 1920 x 1080 scanning analog and parallel digital interfaces for multiple picture rates |
| SMPTE ST 291 | Ancillary Data Packet and Space Formatting |
| SMPTE ST 292 | Bit-Serial Digital Interface for High-Definition Television Systems |
| SMPTE ST 293 | 720 x 483 active line at 59.94Hz progressive scan production – digital representation |
| SMPTE ST 296 | 1280 x 720 scanning, analog and digital representation and analog interface |
| SMPTE ST 299 | 24-Bit Digital Audio Format for HDTV Bit-Serial Interface |
| SMPTE ST 352 | Video Payload Identification for Digital Television Interfaces |
| SMPTE ST 424 | Television - 3Gb/s Signal/Data Serial Interface |
| SMPTE ST 425 | Television - 3Gb/s Signal/Data Serial Interface - Source Image Format Mapping |
| SMPTE RP165 | Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television |
| SMPTE RP168 | Definition of Vertical Interval Switching Point for Synchronous Video Switching |

7. Package & Ordering Information

7.1 Package Dimensions

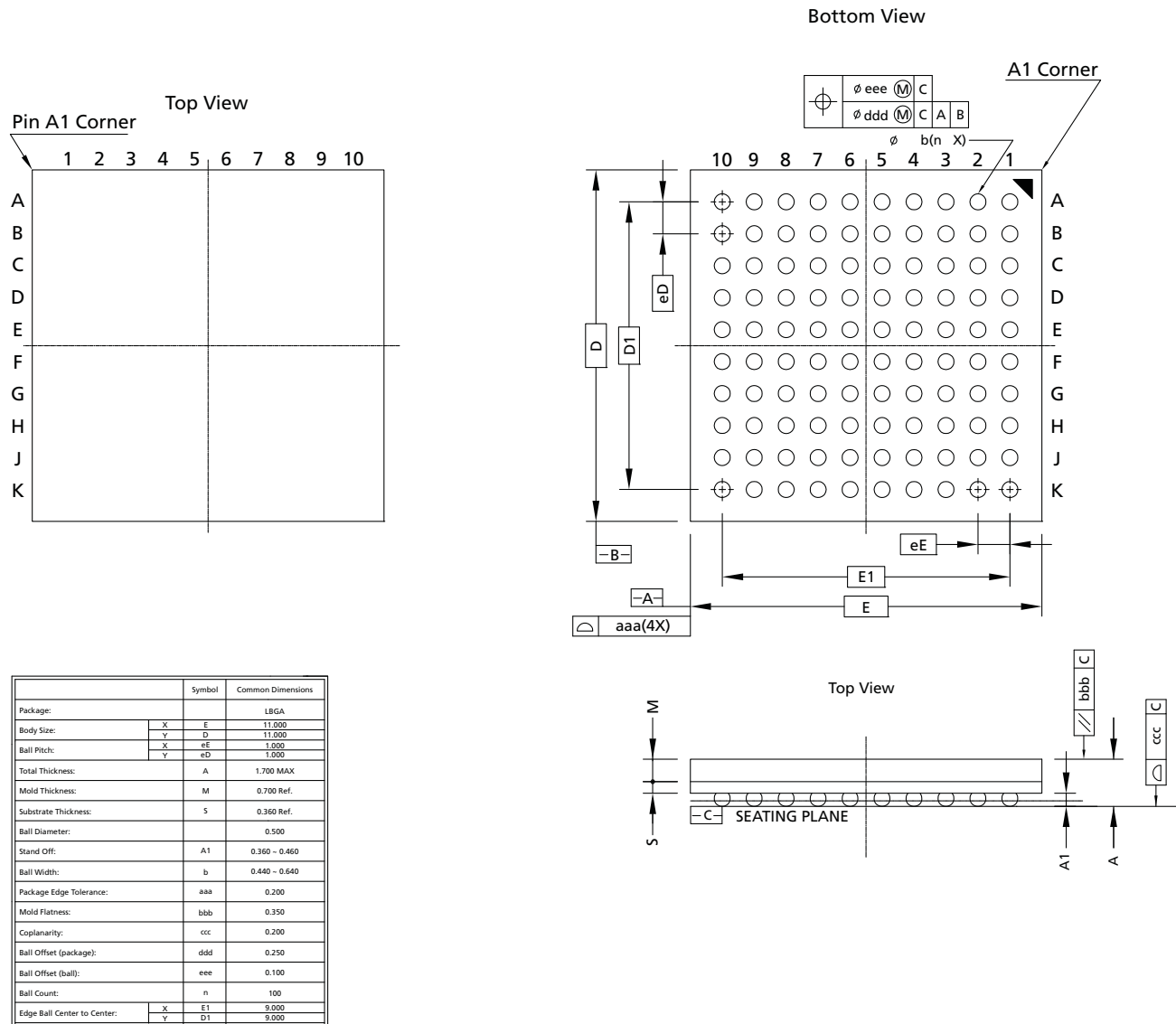


Figure 7-1: Package Dimensions

7.2 Packaging Data

Table 7-1: Packaging Data

| Parameter | Value |
|--|---|
| Package Type | 11mm x 11mm 100-ball LBGA |
| Package Drawing Reference | JEDEC M0192 (with exceptions noted in Package Dimensions on page 146). |
| Moisture Sensitivity Level | 3 |
| Junction to Case Thermal Resistance, θ_{j-c} | 15.4°C/W |
| Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow) | 37.1°C/W |
| Junction to Board Thermal Resistance, θ_{j-b} | 26.4°C/W |
| Psi, ψ | 0.4°C/W |
| Pb-free and RoHS Compliant | Yes |

7.3 Marking Diagram

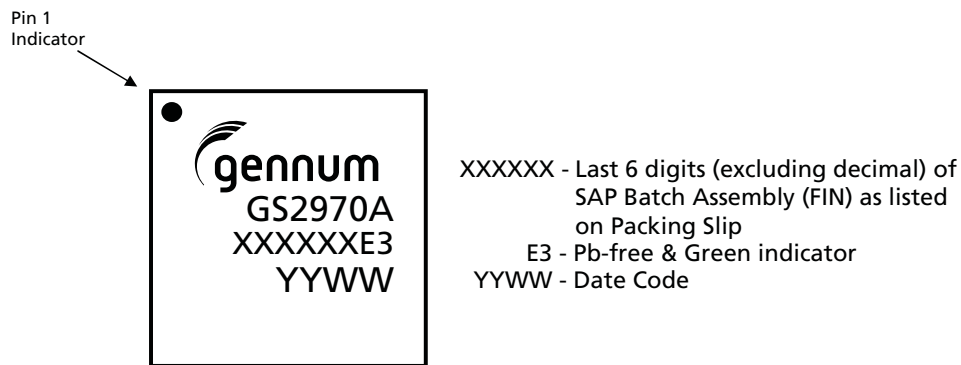


Figure 7-2: GS2970A Marking Diagram

7.4 Solder Reflow Profiles

The GS2970A is available in a Pb-free package. It is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 7-3.

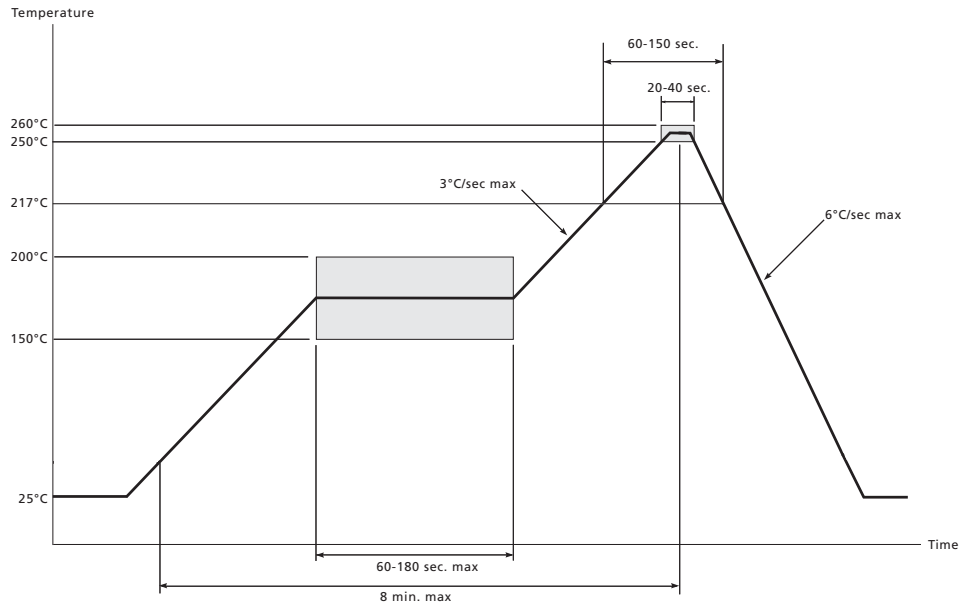


Figure 7-3: Pb-free Solder Reflow Profile

7.5 Ordering Information

Table 7-2: GS2970A Ordering Information

| Part Number | Package | Pb-free | Temperature Range |
|---------------------------------------|--------------|---------|-------------------|
| GS2970AIBE3 | 100-ball BGA | Yes | -40°C to 85°C |
| GS2970AIBTE3 (250pc tape and reel) | 100-ball BGA | Yes | -40°C to 85°C |



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Contact Information

Semtech Corporation
Gennum Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com



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