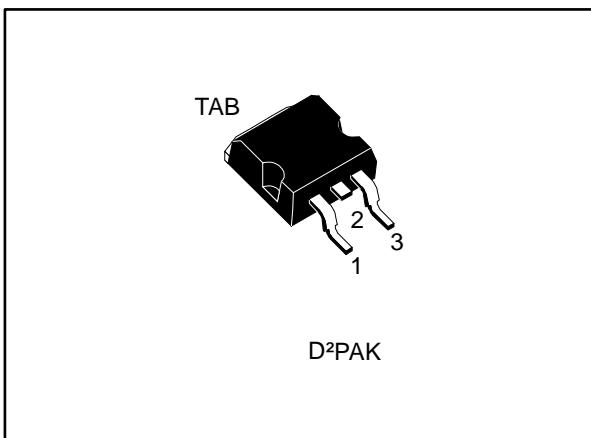
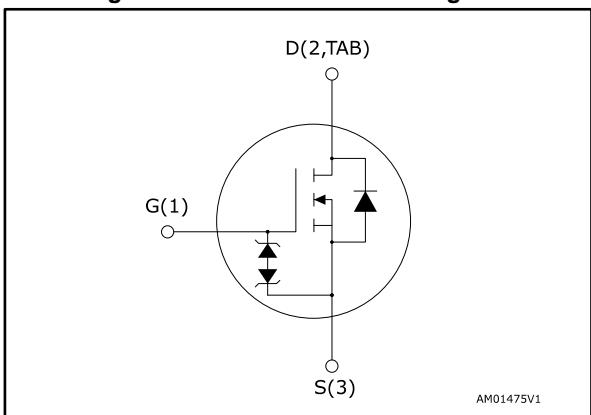


## N-channel 800 V, 0.29 Ω typ., 14 A MDmesh™ K5 Power MOSFET in a D<sup>2</sup>PAK package

Datasheet - production data



**Figure 1: Internal schematic diagram**



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB17N80K5	800 V	0.34 Ω	14 A

- Industry's lowest R<sub>DS(on)</sub> x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

**Table 1: Device summary**

Order code	Marking	Package	Packing
STB17N80K5	17N80K5	D <sup>2</sup> PAK	Tape and reel

## Contents

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	14	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	9	A
$I_{DM}^{(1)}$	Drain current (pulsed)	56	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	170	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
$T_J$	Operating junction temperature range	- 55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

**Notes:**

(1) Pulse width limited by safe operating area

(2)  $I_{SD} \leq 14$  A,  $di/dt = 100$  A/ $\mu\text{s}$ ;  $V_{DS}$  peak <  $V_{(BR)DSS}$ ,  $V_{DD} = 640$  V(3)  $V_{DS} \leq 640$  V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.74	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	30	$^\circ\text{C}/\text{W}$

**Notes:**(1) When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	4.7	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50$ V)	340	mJ

## 2 Electrical characteristics

$T_C = 25^\circ\text{C}$  unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	800			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 800 \text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0 \text{ V}, V_{DS} = 800 \text{ V}$ $T_C = 125^\circ\text{C}$ <sup>(1)</sup>			50	$\mu\text{A}$
$I_{\text{GSS}}$	Gate body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DD} = V_{GS}, I_D = 250 \mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 7 \text{ A}$		0.29	0.34	$\Omega$

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{\text{iss}}$	Input capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0 \text{ V}$	-	866	-	$\text{pF}$
$C_{\text{oss}}$	Output capacitance		-	64	-	$\text{pF}$
$C_{\text{rss}}$	Reverse transfer capacitance		-	0.42	-	$\text{pF}$
$C_{o(\text{tr})}$ <sup>(1)</sup>	Equivalent capacitance time related	$V_{DS} = 0 \text{ to } 640 \text{ V}, V_{GS} = 0 \text{ V}$	-	142	-	$\text{pF}$
$C_{o(\text{er})}$ <sup>(2)</sup>	Equivalent capacitance energy related		-	51	-	$\text{pF}$
$R_g$	Intrinsic gate resistance	$f = 1 \text{ MHz}, I_D = 0 \text{ A}$	-	5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 640 \text{ V}, I_D = 14 \text{ A}$ $V_{GS} = 10 \text{ V}$ (see Figure 15: "Test circuit for gate charge behavior")	-	26	-	nC
$Q_{gs}$	Gate-source charge		-	7.2	-	nC
$Q_{gd}$	Gate-drain charge		-	15.2	-	nC

**Notes:**

<sup>(1)</sup> $C_{o(\text{tr})}$  is a constant capacitance value that gives the same charging time as  $C_{\text{oss}}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

<sup>(2)</sup> $C_{o(\text{er})}$  is a constant capacitance value that gives the same stored energy as  $C_{\text{oss}}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400 \text{ V}$ , $I_D = 7 \text{ A}$ , $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$ (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	14.8	-	ns
$t_r$	Rise time		-	10.8	-	ns
$t_{d(off)}$	Turn-off delay time		-	84.3	-	ns
$t_f$	Fall time		-	10.1	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		14	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		56	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 14 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 14 \text{ A}$ , $dI/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 60 \text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	439		ns
$Q_{rr}$	Reverrse recovery charge		-	6.37		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	29		A
$t_{rr}$	Reverse recovery time		-	626		ns
$Q_{rr}$	Reverse recovery charge	$I_{SD} = 14 \text{ A}$ , $dI/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	8.36		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	26.7		A

**Notes:**

(1) Pulse width limited by safe operating area

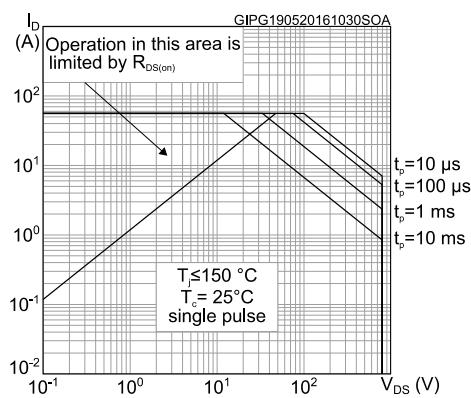
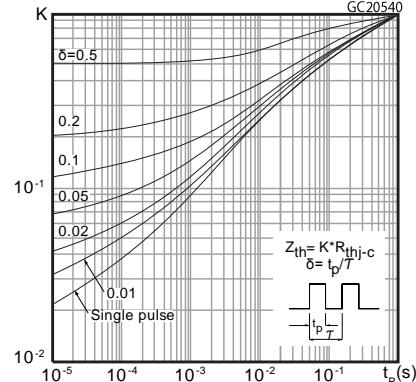
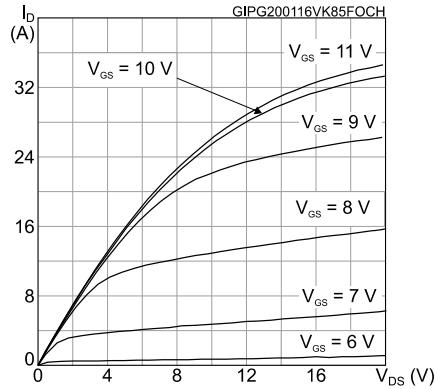
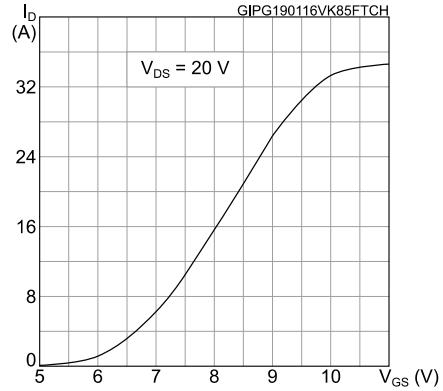
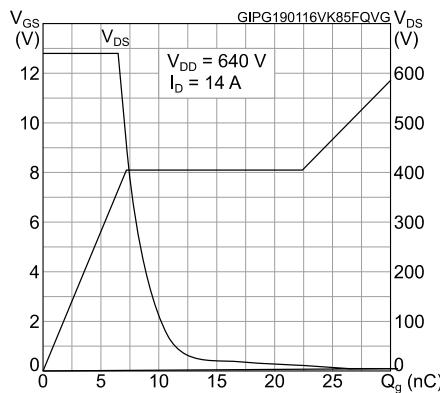
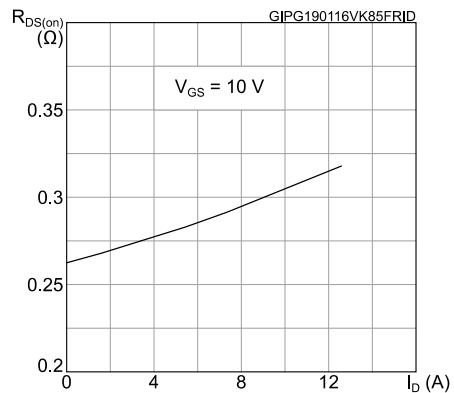
(2) Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

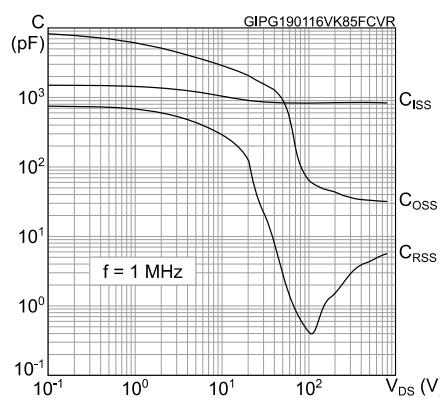
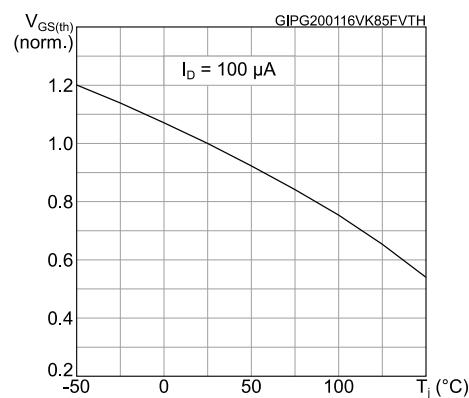
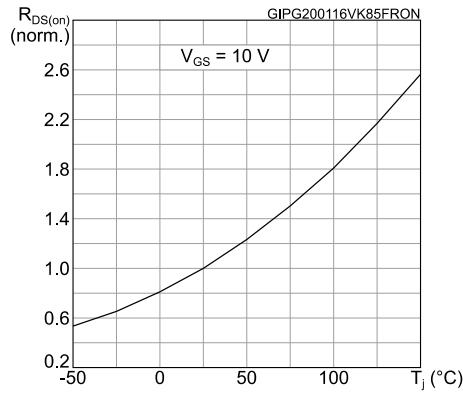
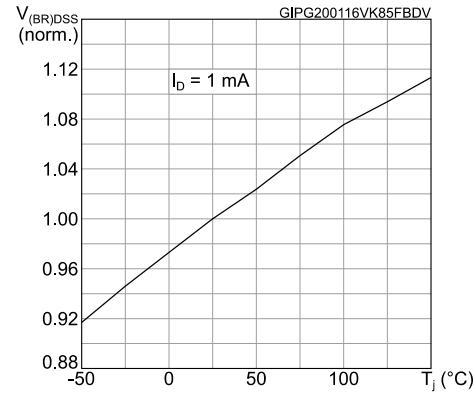
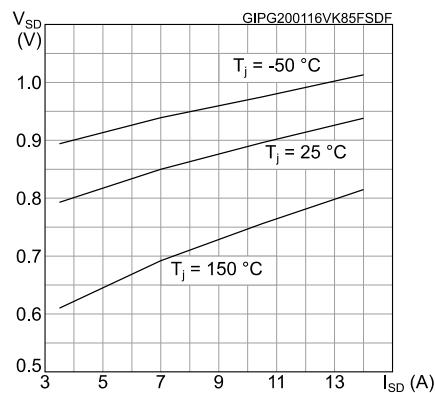
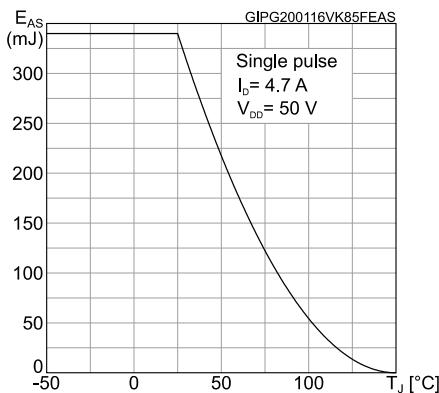
Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$ , $I_D = 0 \text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

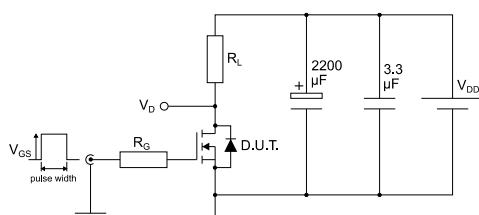
## 2.2 Electrical characteristics (curves)

**Figure 2: Safe operating area****Figure 3: Thermal impedance****Figure 4: Output characteristics****Figure 5: Transfer characteristics****Figure 6: Gate charge vs gate-source voltage****Figure 7: Static drain-source on-resistance**

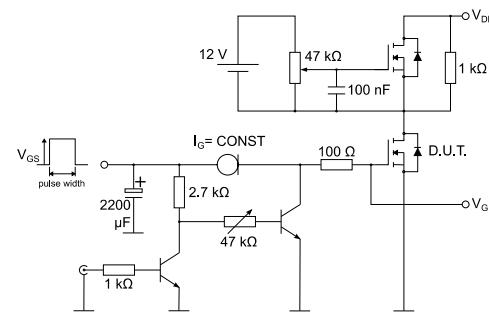
**Figure 8: Capacitance variations****Figure 9: Normalized gate threshold voltage vs temperature****Figure 10: Normalized on-resistance vs temperature****Figure 11: Normalized  $V_{(BR)DSS}$  vs temperature****Figure 12: Source-drain diode forward characteristics****Figure 13: Maximum avalanche energy vs starting  $T_J$** 

### 3 Test circuits

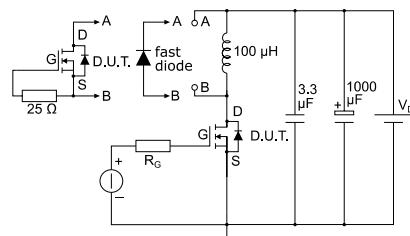
**Figure 14: Test circuit for resistive load switching times**



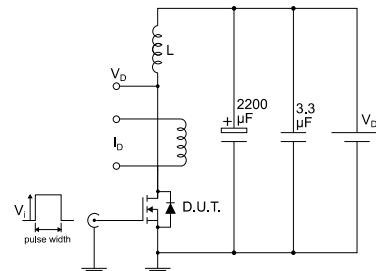
**Figure 15: Test circuit for gate charge behavior**



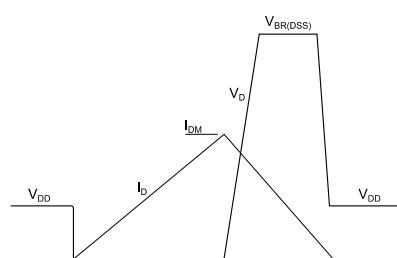
**Figure 16: Test circuit for inductive load switching and diode recovery times**



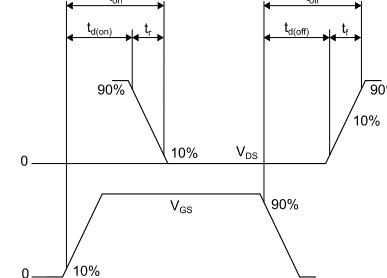
**Figure 17: Unclamped inductive load test circuit**



**Figure 18: Unclamped inductive waveform**



**Figure 19: Switching time waveform**



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).  
ECOPACK® is an ST trademark.

### 4.1 D<sup>2</sup>PAK (TO-263) package information

Figure 20: D<sup>2</sup>PAK (TO-263) type A package outline

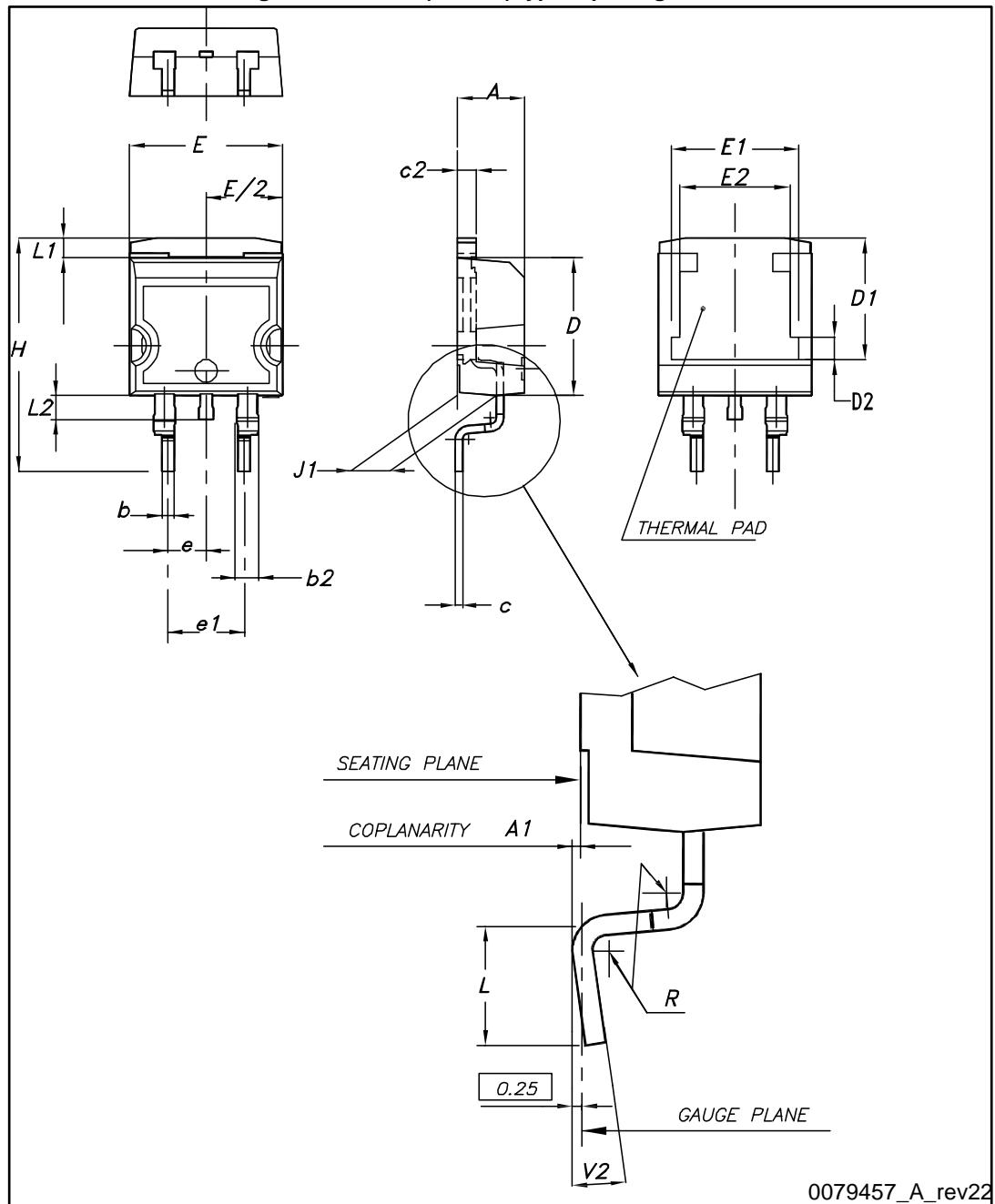
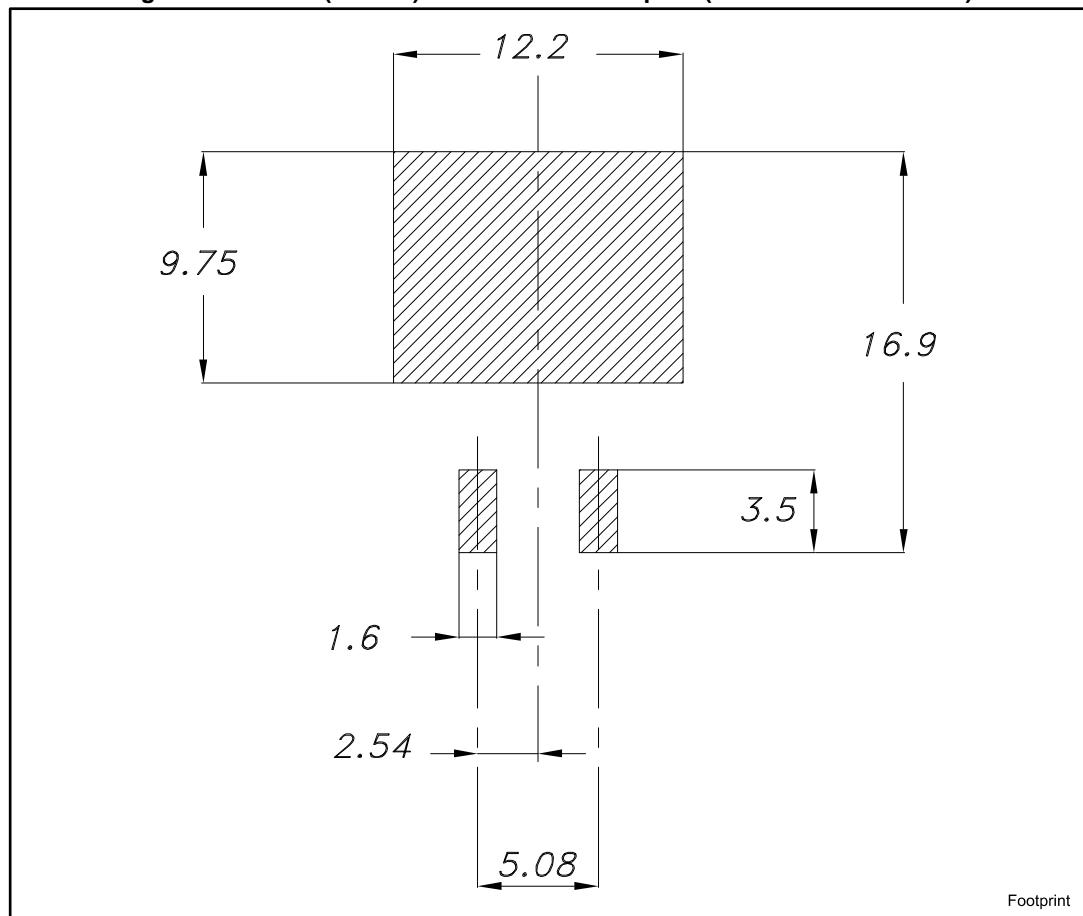


Table 10: D<sup>2</sup>PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 21: D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)

## 4.2 D<sup>2</sup>PAK (TO-263) packing information

Figure 22: Tape outline

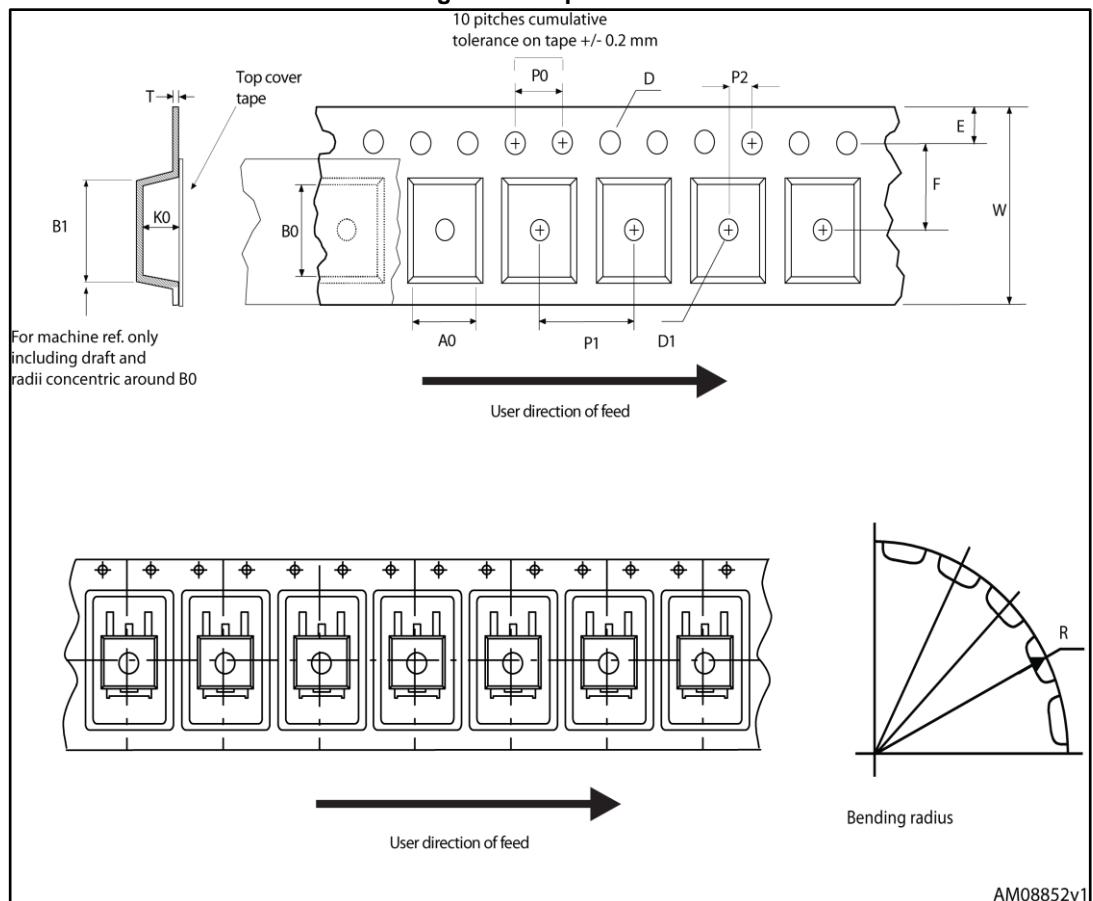
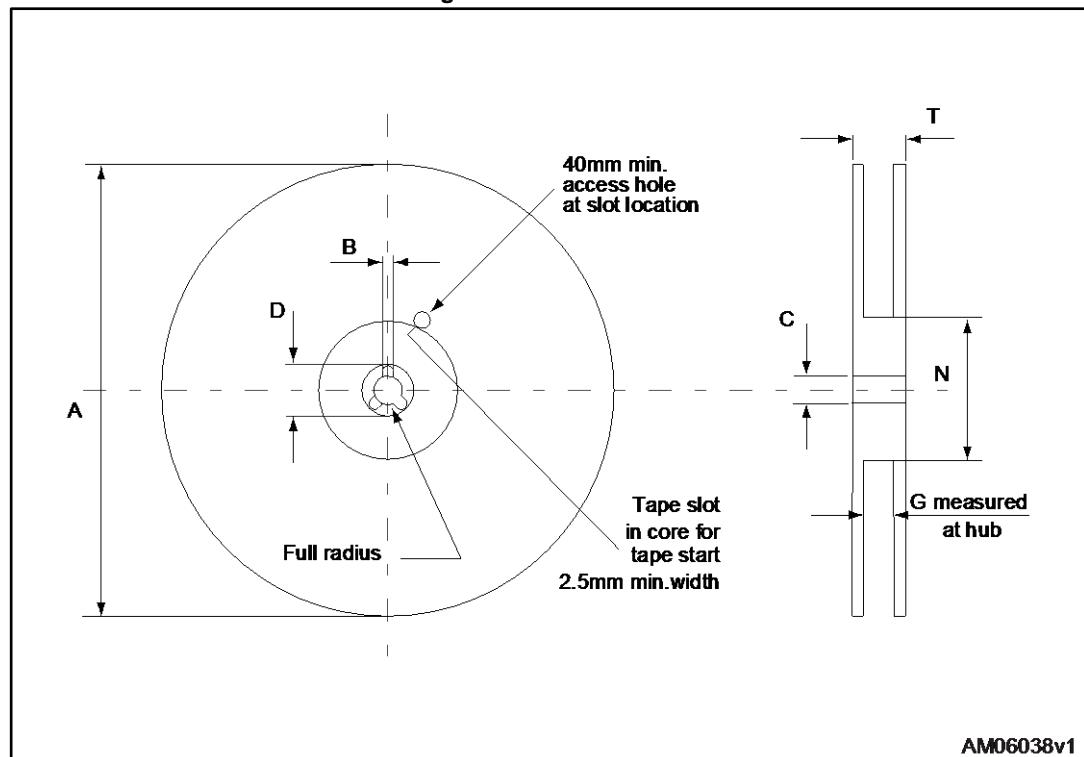


Figure 23: Reel outline

Table 11: D<sup>2</sup>PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## 5 Revision history

Table 12: Document revision history

Date	Revision	Changes
02-Apr-2015	1	First release.
20-May-2016	2	Modified: <i>Table 2: "Absolute maximum ratings"</i> and <i>Table 3: "Thermal data"</i> . Added: <i>Section 3.1: "Electrical characteristics (curves)"</i> . Minor text changes.

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**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литер Н,  
помещение 100-Н Офис 331