# SC16C650B

## 5 V, 3.3 V and 2.5 V UART with 32-byte FIFOs and infrared (IrDA) encoder/decoder

Rev. 04 — 14 September 2009 Product data sheet

## 1. General description

The SC16C650B is a Universal Asynchronous Receiver and Transmitter (UART) used for serial data communications. Its principal function is to convert parallel data into serial data, and vice versa. The UART can handle serial data rates up to 3 Mbit/s.

The SC16C650B is pin compatible with the ST16C650A and it will power-up to be functionally equivalent to the 16C450. Programming of control registers enables the added features of the SC16C650B. Some of these added features are the 32-byte receive and transmit FIFOs, automatic hardware or software flow control and infrared encoding/decoding. The selectable auto-flow control feature significantly reduces software overload and increases system efficiency while in FIFO mode by automatically controlling serial data flow using $\overline{RTS}$ output and $\overline{CTS}$ input signals. The SC16C650B also provides DMA mode data transfers through FIFO trigger levels and the $\overline{RXRDY}$ and $\overline{TXRDY}$ signals. On-board status registers provide the user with error indications, operational status, and modem interface control. System interrupts may be tailored to meet user requirements. An internal loopback capability allows on-board diagnostics.

The SC16C650B operates at 5 V, 3.3 V and 2.5 V, and the industrial temperature range, and is available in plastic PLCC44, LQFP48, and HVQFN32 packages.

## 2. Features

- Single channel
- 5 V, 3.3 V and 2.5 V operation
- 5 V tolerant on input only pins[1]
- Industrial temperature range (–40 °C to +85 °C)
- After reset, all registers are identical to the typical 16C450 register set
- Capable of running with all existing generic 16C450 software
- Pin compatibility with the industry-standard ST16C450/550, TL16C450/550, PC16C450/550. Software compatible with ST16C650.
- Up to 3 Mbit/s transmit/receive operation at 5 V, 2 Mbit/s at 3.3 V, and 1 Mbit/s at 2.5 V
- 32 byte transmit FIFO
- 32 byte receive FIFO with error flags
- Programmable auto-$\overline{RTS}$ and auto-$\overline{CTS}$
  - In auto-$\overline{CTS}$ mode, $\overline{CTS}$ controls transmitter
  - In auto-$\overline{RTS}$ mode, RX FIFO contents and threshold control $\overline{RTS}$
- Automatic software/hardware flow control

1. For data bus pins D7 to D0, see Table 26 “Limiting values”.

- Programmable Xon/Xoff characters
- Software selectable baud rate generator
- Supports IrDA version 1.0 (up to 115.2 kbit/s)
- Four selectable Receive and Transmit FIFO interrupt trigger levels
- Standard modem interface or infrared IrDA encoder/decoder interface
- Sleep mode
- Standard asynchronous error and framing bits (Start, Stop, and Parity Overrun Break)
- Independent receiver clock input
- Transmit, Receive, Line Status, and Data Set interrupts independently controlled
- Fully programmable character formatting:
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no-parity formats
  - 1, $1\frac{1}{2}$, or 2-stop bit
  - Baud generation (DC to 3 Mbit/s)
- False start-bit detection
- Complete status reporting capabilities
- 3-state output TTL drive capabilities for bidirectional data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
- Prioritized interrupt system controls
- Modem control functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, $\overline{DCD}$)

## 3. Ordering information

**Table 1. Ordering information**

*Industrial: $V_{CC}$ = 2.5 V, 3.3 V or 5 V ± 10 %; $T_{amb}$ = −40 °C to +85 °C.*

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| SC16C650BIA44 | PLCC44 | plastic leaded chip carrier; 44 leads | SOT187-2 |
| SC16C650BIB48 | LQFP48 | plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |
| SC16C650BIBS | HVQFN32 | plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm | SOT617-1 |

## 4. Block diagram

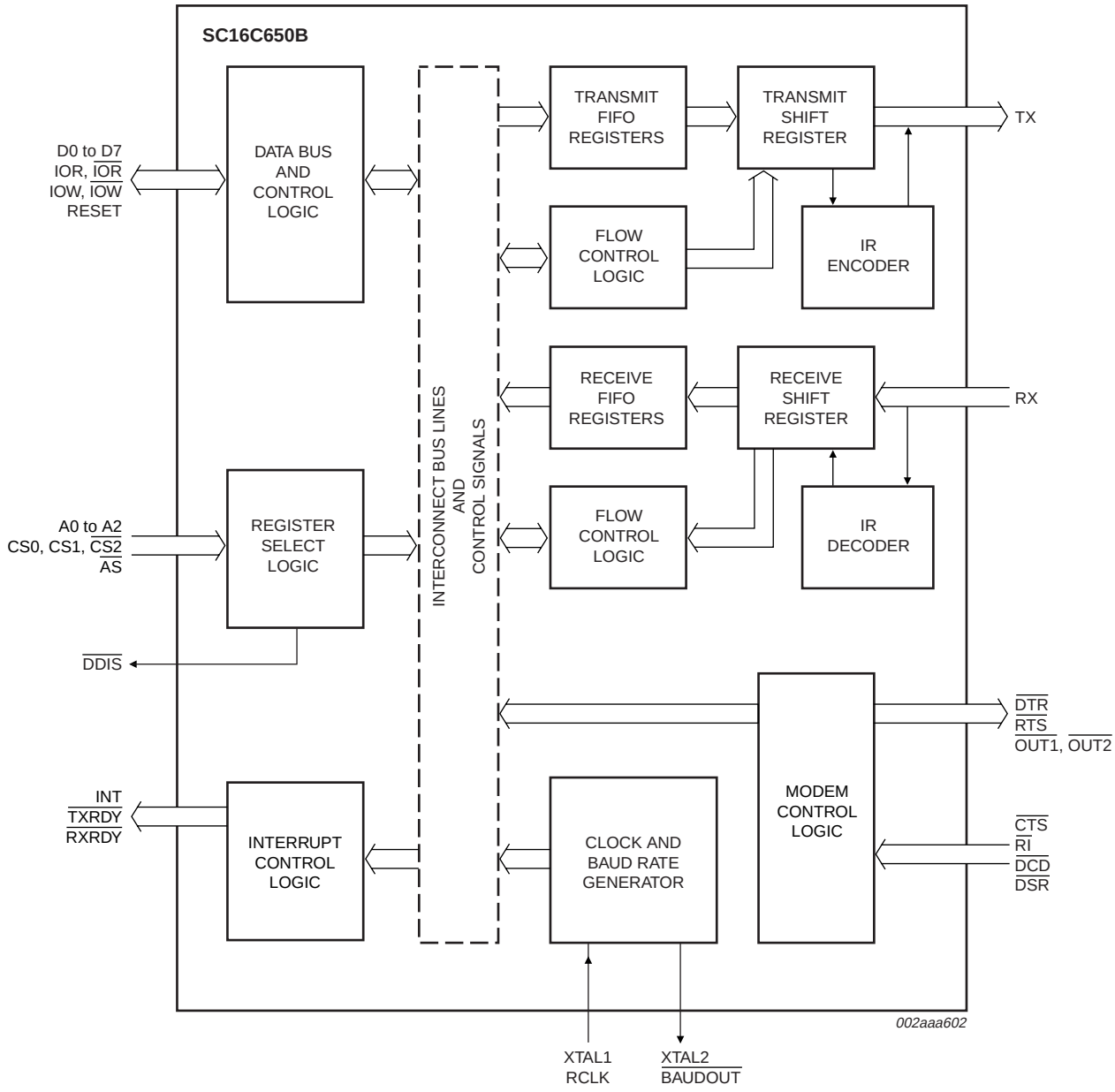



**Fig 1. Block diagram**

# 5. Pinning information

## 5.1 Pinning

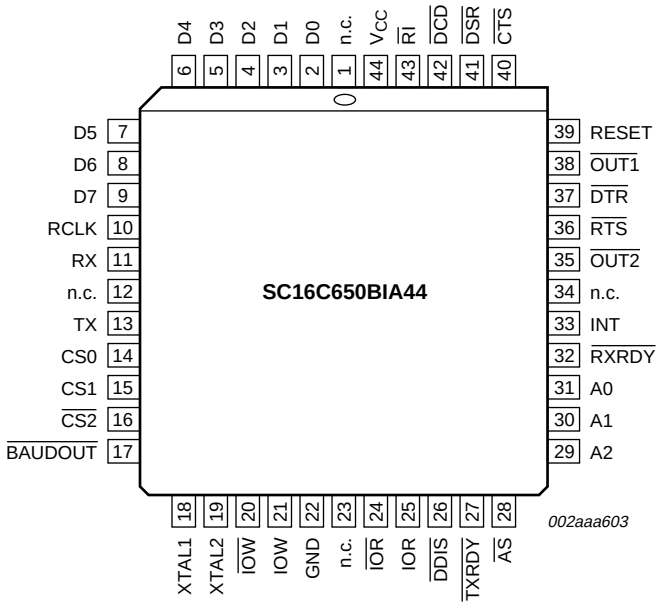



**Fig 2. Pin configuration for PLCC44**

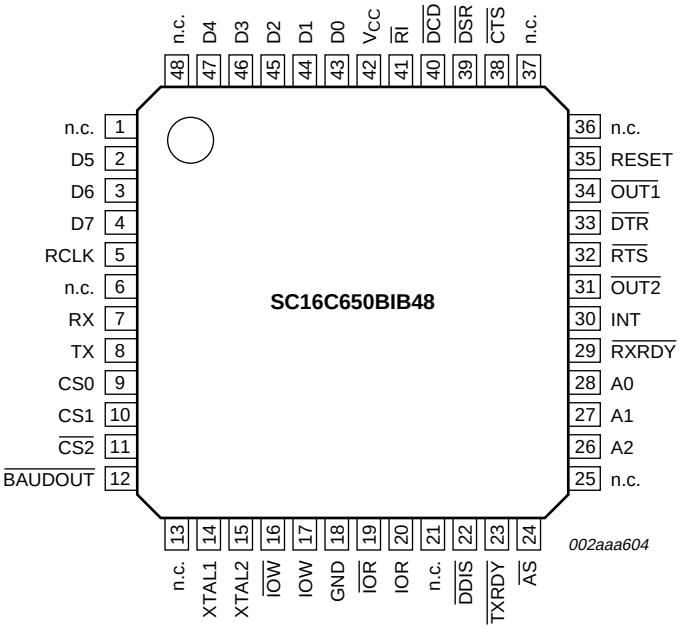



**Fig 3. Pin configuration for LQFP48**

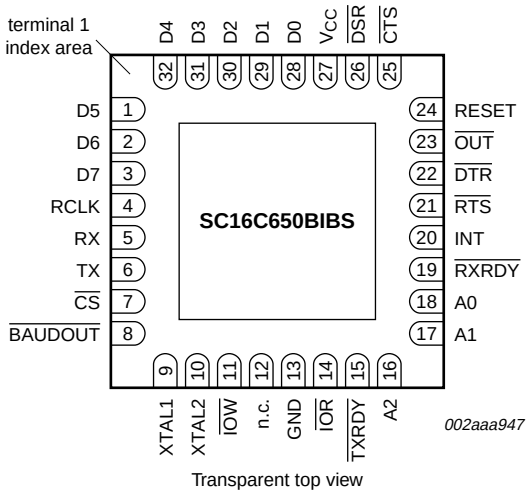



**Fig 4. Pin configuration for HVQFN32**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | | | Type | Description |
|---|---|---|---|---|---|
| | PLCC44 | LQFP48 | HVQFN32 | | |
| A0 | 31 | 28 | 18 | I | **Register select.** A0 to A2 are sued during read and write operations to select the UART register to read from or write to. Refer to Table 3 for register addresses and refer to signal $\overline{AS}$ description. |
| A1 | 30 | 27 | 17 | I | |
| A2 | 29 | 26 | 16 | I | |
| $\overline{AS}$ | 28 | 24 | - | I | **Address strobe.** When $\overline{AS}$ is active (LOW), A0, A1 and A2 and CS0 CS1 and $\overline{CS2}$ drive the internal select logic directly. When $\overline{AS}$ is HIGH, the register select and chip select signals are held at the logic levels they were in when the LOW-to-HIGH transition of $\overline{AS}$ occurred. |
| $\overline{BAUDOUT}$ | 17 | 12 | 8 | O | **Baud out.** $\overline{BAUDOUT}$ is a 16× clock signal for the transmitter section of the UART. The clock rate is established by the reference oscillator frequency divided by a divisor specified in the baud generator divisor latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to RCLK. |
| CS0 | 14 | 9 | - | I | **Chip select.** When CS0 and CS1 are HIGH and $\overline{CS2}$ is LOW, these 3 inputs select the UART. When any of these inputs are inactive, the UART remains inactive (refer to $\overline{AS}$ description). |
| CS1 | 15 | 10 | - | I | |
| $\overline{CS2}$ | 16 | 11 | - | I | |
| $\overline{CS}$ | - | - | 7 | I | |
| $\overline{CTS}$ | 40 | 38 | 25 | I | **Clear to send.** $\overline{CTS}$ is a modem status signal. Its condition can be checked by reading bit 4 ($\overline{CTS}$) of the Modem Status Register (MSR). MSR[0] ($\Delta\overline{CTS}$) indicates that $\overline{CTS}$ has changed states since the last read from the MSR. If the modem status interrupt is enabled when $\overline{CTS}$ changes levels and the auto-$\overline{CTS}$ mode is not enabled, an interrupt is generated. $\overline{CTS}$ is also used in the auto-$\overline{CTS}$ mode to control the transmitter. |

**Table 2. Pin description** *...continued*

| Symbol | Pin | | | Type | Description |
|---|---|---|---|---|---|
| | PLCC44 | LQFP48 | HVQFN32 | | |
| D0 | 2 | 43 | 28 | I/O | **Data bus.** Eight data lines with 3-state outputs provide a bidirectional path for data, control and status information between the UART and the CPU. |
| D1 | 3 | 44 | 29 | I/O | |
| D2 | 4 | 45 | 30 | I/O | |
| D3 | 5 | 46 | 31 | I/O | |
| D4 | 6 | 47 | 32 | I/O | |
| D5 | 7 | 2 | 1 | I/O | |
| D6 | 8 | 3 | 2 | I/O | |
| D7 | 9 | 4 | 3 | I/O | |
| $\overline{DCD}$ | 42 | 40 | - | I | **Data carrier detect.** $\overline{DCD}$ is a modem status signal. Its condition can be checked by reading MSR[7] ($\overline{DCD}$). MSR[3] ($\Delta\overline{DCD}$) indicates that $\overline{DCD}$ has changed states since the last read from the MSR. If the modem status interrupt is enabled when $\overline{DCD}$ changes levels, an interrupt is generated. |
| $\overline{DDIS}$ | 26 | 22 | - | O | **Driver disable.** $\overline{DDIS}$ is active (LOW) when the CPU is reading data. When inactive (HIGH), $\overline{DDIS}$ can disable an external transceiver. |
| $\overline{DSR}$ | 41 | 39 | 26 | I | **Data set ready.** $\overline{DSR}$ is a modem status signal. Its condition can be checked by reading MSR[5] ($\overline{DSR}$). MSR[1] ($\Delta\overline{DSR}$) indicates $\overline{DSR}$ has changed levels since the last read from the MSR. If the modem status interrupt is enabled when $\overline{DSR}$ changes levels, an interrupt is generated. |
| $\overline{DTR}$ | 37 | 33 | 22 | O | **Data terminal ready.** When active (LOW), $\overline{DTR}$ informs a modem or data set that the UART is ready to establish communication. $\overline{DTR}$ is placed in the active level by setting the $\overline{DTR}$ bit of the Modem Control Register. $\overline{DTR}$ is placed in the inactive level either as a result of a Master Reset, during loopback mode operation, or clearing the $\overline{DTR}$ bit. |
| INT | 33 | 30 | 20 | O | **Interrupt.** When active (HIGH), INT informs the CPU that the UART has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data that is available or timed out (FIFO mode only), an empty transmitter holding register or an enabled modem status interrupt. INT is reset (deactivated) either when the interrupt is serviced or as a result of a Master Reset. |
| $\overline{OUT1}$ | 38 | 34 | - | O | **Outputs 1 and 2.** These are user-designated output terminals that are set to the active (low) level by setting respective Modem Control Register (MCR) bits ($\overline{OUT1}$ and $\overline{OUT2}$). $\overline{OUT1}$ and $\overline{OUT2}$ are set to the inactive (HIGH) level as a result of Master Reset, during loopback mode operations, or by clearing bit 2 ($\overline{OUT1}$) or bit 3 ($\overline{OUT2}$) of the MCR. |
| $\overline{OUT2}$ | 35 | 31 | - | O | |
| $\overline{OUT}$ | - | - | 23 | O | |
| RCLK | 10 | 5 | 4 | I | **Receiver clock.** RCLK is the 16× baud rate clock for the receiver section of the UART. |
| IOR | 25 | 20 | - | I | **Read inputs.** When either $\overline{IOR}$ or IOR is active (LOW or HIGH, respectively) while the UART is selected, the CPU is allowed to read status information or data from a selected UART register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied to its inactive level (i.e., IOR tied LOW or $\overline{IOR}$ tied HIGH). |
| $\overline{IOR}$ | 24 | 19 | 14 | I | |

**Table 2. Pin description** *...continued*

| Symbol | Pin | | | Type | Description |
|---|---|---|---|---|---|
| | PLCC44 | LQFP48 | HVQFN32 | | |
| RESET | 39 | 35 | 24 | I | **Master Reset.** When active (HIGH), MR clears most UART registers and sets the levels of various output signals. |
| $\overline{RI}$ | 43 | 41 | - | I | **Ring indicator.** $\overline{RI}$ is a modem status signal. Its condition can be checked by reading MSR[6] ($\overline{RI}$). MSR[2] ($\Delta\overline{RI}$) indicates that $\overline{RI}$ has changed from a LOW to a HIGH level since the last read from the MSR. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated. |
| $\overline{RTS}$ | 36 | 32 | 21 | O | **Request to send.** When active, $\overline{RTS}$ informs the modem or data set that the UART is ready to receive data. $\overline{RTS}$ is set to the active level by setting the $\overline{RTS}$ modem control register bit and is set to the inactive (HIGH) level either as a result of a Master Reset or during loopback mode operations or by clearing bit 1 ($\overline{RTS}$) of the MCR. In the auto-$\overline{RTS}$ mode, $\overline{RTS}$ is set to the inactive level by the receiver threshold control logic. |
| $\overline{RXRDY}$ | 32 | 29 | 19 | O | **Receiver ready.** Receiver direct memory access (DMA) signaling is available with $\overline{RXRDY}$. When operating in the FIFO mode, one of two types of DMA signaling can be selected using the FIFO Control Register bit 3 (FCR[3]). When operating in the 16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multi-transfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied. In DMA mode 0 (FCR[0] = 0 or FCR[0] = 1, FCR[3] = 0), when there is at least one character in the receiver FIFO or Receive Holding Register, $\overline{RXRDY}$ is active (LOW). When $\overline{RXRDY}$ has been active but there are no characters in the FIFO or holding register, $\overline{RXRDY}$ goes inactive (HIGH). In DMA mode 1 (FCR[0] = 1, FCR[3] = 1), when the trigger level or the time-out has been reached, $\overline{RXRDY}$ goes active (LOW); when it has been active but there are no more characters in the FIFO or holding register, it goes inactive (HIGH). |
| RX | 11 | 7 | 5 | I | **Serial data input.** RX is serial data input from a connected communications device. |
| TX | 13 | 8 | 6 | O | **Serial data output.** TX is composite serial data output to a connected communication device. TX is set to the marking (HIGH) level as a result of Master Reset. |
| $\overline{TXRDY}$ | 27 | 23 | 15 | O | **Transmitter ready.** Transmitter DMA signaling is available with $\overline{TXRDY}$. When operating in the FIFO mode, one of two types of DMA signaling can be selected using FCR[3]. When operating in the 16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multi-transfer DMA in which multiple transfers are made continuously until the transmit FIFO has been filled. |
| $V_{CC}$ | 44 | 42 | 27 | power | **2.5 V, 3 V or 5 V supply voltage.** |
| GND | 22 | 18 | 13[1] | power | **Ground voltage.** |
| IOW | 21 | 17 | - | I | **Write inputs.** When either $\overline{IOW}$ or IOW is active (LOW or HIGH, respectively) and while the UART is selected, the CPU is allowed to write control words or data into a selected UART register. Only one of these inputs is required to transfer data during a write operation; the other input should be tied to its inactive level (i.e., IOW tied LOW or $\overline{IOW}$ tied HIGH). |
| $\overline{IOW}$ | 20 | 16 | 11 | I | |

**Table 2. Pin description** *...continued*

| Symbol | Pin | | | Type | Description |
|---|---|---|---|---|---|
| | PLCC44 | LQFP48 | HVQFN32 | | |
| XTAL1 | 18 | 14 | 9 | I | **Crystal connection or external clock input.** |
| XTAL2[2] | 19 | 15 | 10 | O | **Crystal connection or the inversion of XTAL1 if XTAL1 is driven.** |
| n.c. | 1, 12, 23, 34 | 1, 6, 13, 21, 25, 36, 37, 48 | 12 | - | not connected |

[1] HVQFN32 package die supply ground is connected to both GND pin and exposed center pad. GND pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

[2] In Sleep mode, XTAL2 is left floating.

# 6. Functional description

The SC16C650B provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character (character orientated protocol). Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The SC16C650B is fabricated with an advanced CMOS process to achieve low drain power and high speed requirements.

The SC16C650B is an upward solution that provides 32 bytes of transmit and receive FIFO memory, instead of none in the 16C450, or 16 bytes in the 16C550. The SC16C650B is designed to work with high speed modems and shared network environments that require fast data processing time. Increased performance is realized in the SC16C650B by the larger transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. In addition, the four selectable levels of FIFO trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance, especially when operating in a multi-channel environment. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The SC16C650B is capable of operation up to 3 Mbit/s with a 48 MHz external clock input (at 5 V).

The rich feature set of the SC16C650B is available through internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger level, selectable TX and RX baud rates, modem interface controls, and a Sleep mode are some of these features.

## 6.1 Internal registers

The SC16C650B provides 17 internal registers for monitoring and control. These registers are shown in Table 3. Twelve registers are similar to those already available in the standard 16C550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO control register (FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user accessible ScratchPad Register (SPR). Beyond the general 16C550 features and capabilities, the SC16C650B offers an enhanced feature register set (EFR, Xon1/Xoff1, Xon2/Xoff2) that provides on-board hardware/software flow control. Register functions are more fully described in the following paragraphs.

**Table 3. Internal registers decoding**

| A2 | A1 | A0 | Read mode | Write mode |
|---|---|---|---|---|
| **General register set (THR/RHR, IER/ISR, MCR/MSR, FCR, LCR/LSR, SPR)[1]** | | | | |
| 0 | 0 | 0 | Receive Holding Register | Transmit Holding Register |
| 0 | 0 | 1 | Interrupt Enable Register | Interrupt Enable Register |
| 0 | 1 | 0 | Interrupt Status Register | FIFO Control Register |
| 0 | 1 | 1 | Line Control Register | Line Control Register |
| 1 | 0 | 0 | Modem Control Register | Modem Control Register |
| 1 | 0 | 1 | Line Status Register | n/a |
| 1 | 1 | 0 | Modem Status Register | n/a |
| 1 | 1 | 1 | Scratchpad Register | Scratchpad Register |
| **Baud rate register set (DLL/DLM)[2]** | | | | |
| 0 | 0 | 0 | LSB of Divisor Latch | LSB of Divisor Latch |
| 0 | 0 | 1 | MSB of Divisor Latch | MSB of Divisor Latch |
| **Enhanced register set (EFR, Xon1, Xoff1, Xon2, Xoff2)[3]** | | | | |
| 0 | 1 | 0 | Enhanced Feature Register | Enhanced Feature Register |
| 1 | 0 | 0 | Xon1 word | Xon1 word |
| 1 | 0 | 1 | Xon2 word | Xon2 word |
| 1 | 1 | 0 | Xoff1 word | Xoff1 word |
| 1 | 1 | 1 | Xoff2 word | Xoff2 word |

[1] These registers are accessible only when LCR[7] is a logic 0.

[2] These registers are accessible only when LCR[7] is a logic 1.

[3] Enhanced Feature Register, Xon1, Xon2 and Xoff1, Xoff2 are accessible only when the LCR is set to BFh.

## 6.2 FIFO operation

The 32-byte transmit and receive data FIFOs are enabled by the FIFO Control Register bit 0 (FCR[0]). With 16C550 devices, the user can set the receive trigger level, but not the transmit trigger level. The SC16C650B provides independent trigger levels for both receiver and transmitter. To remain compatible with SC16C550, the transmit interrupt trigger level is set to 16 following a reset. It should be noted that the user can set the transmit trigger levels by writing to the FCR register, but activation will not take place until EFR[4] is set to a logic 1. The receiver FIFO section includes a time-out function to ensure

data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached.

**Table 4. Flow control mechanism**

| Selected trigger level (characters) | INT pin activation | Negate $\overline{RTS}$ or send Xoff | Assert $\overline{RTS}$ or send Xon |
|---|---|---|---|
| 8 | 8 | 8 | 0 |
| 16 | 16 | 16 | 7 |
| 24 | 24 | 24 | 15 |
| 28 | 28 | 28 | 23 |

## 6.3 Hardware flow control

When automatic hardware flow control is enabled, the SC16C650B monitors the $\overline{CTS}$ pin for a remote buffer overflow indication and controls the $\overline{RTS}$ pin for local buffer overflows. Automatic hardware flow control is selected by setting EFR[6] (RTS) and EFR[7] (CTS) to a logic 1. If $\overline{CTS}$ changes from a logic 0 to a logic 1 indicating a flow control request, ISR[5] will be set to a logic 1 (if enabled via IER[6,7]), and the SC16C650B will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the $\overline{CTS}$ input returns to a logic 0, indicating more data may be sent.

With the auto-RTS function enabled, an interrupt is generated when the receive FIFO reaches the programmed trigger level. The $\overline{RTS}$ pin will not be forced to a logic 1 (RTS off), until the receive FIFO reaches the next trigger level. However, the $\overline{RTS}$ pin will return to a logic 0 after the data buffer (FIFO) is unloaded to the next trigger level below the programmed trigger level. However, under the above described conditions, the SC16C650B will continue to accept data until the receive FIFO is full.

## 6.4 Software flow control

When software flow control is enabled, the SC16C650B compares one or two sequential receive data characters with the programmed Xon or Xoff character value(s). If received character(s) match the programmed Xoff values, the SC16C650B will halt transmission (TX) as soon as the current character(s) has completed transmission. When a match occurs, the receive ready (if enabled via Xoff IER[5]) flags will be set and the interrupt output pin (if receive interrupt is enabled) will be activated. Following a suspension due to a match of the Xoff characters' values, the SC16C650B will monitor the receive data stream for a match to the Xon1, Xon2 character value(s). If a match is found, the SC16C650B will resume operation and clear the flags (ISR[4]).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset, the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the SC16C650B compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO. When using a software flow control the Xon/Xoff characters cannot be used for data transfer.

In the event that the receive buffer is overfilling and flow control needs to be executed, the SC16C650B automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The SC16C650B sends the Xoff1/Xoff2 characters as soon as received data passes the programmed trigger level. To clear this condition, the SC16C650B will transmit the programmed Xon1/Xon2 characters as soon as receive data drops below the next low or programmed trigger level.

## 6.5 Special feature software flow control

A special feature is provided to detect an 8-bit character when EFR[5] is set. When 8-bit character is detected, it will be placed on the user-accessible data stack along with normal incoming RX data. This condition is selected in conjunction with EFR[3:0]. Note that software flow control should be turned off when using this special mode by setting EFR[3:0] to a logic 0.

The SC16C650B compares each incoming receive character with Xoff2 data. If a match exists, the received data will be transferred to the FIFO, and ISR[4] will be set to indicate detection of a special character. Although Table 8 “SC16C650B internal registers” shows each X-register with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register bits LCR[1:0] define the number of character bits, i.e., either 5 bits, 6 bits, 7 bits or 8 bits. The word length selected by LCR[1:0] also determine the number of bits that will be used for the special character comparison. Bit 0 in the X-registers corresponds with the LSB bit for the receive character.

## 6.6 Hardware/software and time-out interrupts

Three special interrupts have been added to monitor the hardware and software flow control. The interrupts are enabled by IER[7:5]. Care must be taken when handling these interrupts. Following a reset, the transmitter interrupt is enabled, the SC16C650B will issue an interrupt to indicate that the Transmit Holding Register is empty. This interrupt must be serviced prior to continuing operations. The ISR register provides the current singular highest priority interrupt only. It could be noted that CTS and RTS interrupts have lowest interrupt priority. A condition can exist where a higher priority interrupt may mask the lower priority CTS/RTS interrupt(s). Only after servicing the higher pending interrupt will the lower priority CTS/RTS interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time-Out have the same interrupt priority (when enabled by IER[0]). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case, the SC16C650B FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should re-check LSR[0] for additional characters. A Receive Time-Out will not occur if the receive FIFO is empty. The time-out counter is reset at the center of each stop bit received or each time the Receive Holding Register (RHR) is read. The actual time-out value is 4 character time.

## 6.7 Programmable baud rate generator

The SC16C650B supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example, a 33.6 kbit/s modem that employs data compression may require a 115.2 kbit/s input data rate. A 128.0 kbit/s ISDN modem that supports data compression may need an input data rate of 460.8 kbit/s.

A single baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable baud rate generator is capable of accepting an input clock up to 48 MHz, as required for supporting a 3 Mbit/s data rate. The SC16C650B can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal (parallel resonant, 22 pF to 33 pF load) is connected externally between the XTAL1 and XTAL2 pins (see Figure 5). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates (see Table 5).

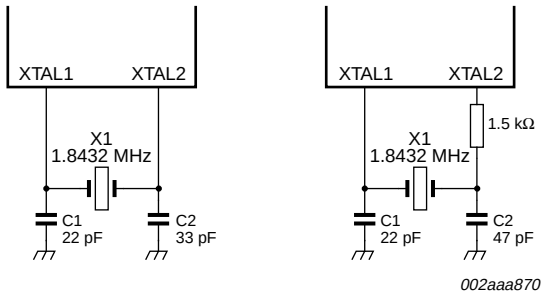



**Fig 5. Crystal oscillator connection**

The generator divides the input 16× clock by any divisor from 1 to ($2^{16} - 1$). The SC16C650B divides the basic crystal or external clock by 16. The frequency of the $\overline{\text{BAUDOUT}}$ output pin is exactly 16× (16 times) the selected baud rate ($\overline{\text{BAUDOUT}}$ = 16 × baud rate). Customized baud rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Setting MCR[7] to a logic 1 provides an additional divide-by-4, whereas setting MCR[7] to a logic 0 only divides by 1 (see Table 5 and Figure 6).

Programming the baud rate generator registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 5 shows selectable baud rates when using a 1.8432 MHz crystal and setting MCR[7] to a logic 0.

For custom baud rates, the divisor value can be calculated using Equation 1:

$$divisor\ (in\ decimal) = \frac{XTAL1\ clock\ frequency}{serial\ data\ rate \times 16} \quad (1)$$

**Table 5. Baud rates using 1.8432 MHz or 3.072 MHz crystal**

| Using 1.8432 MHz crystal | | | Using 3.072 MHz crystal | | |
|---|---|---|---|---|---|
| **Desired baud rate** | **Divisor for 16× clock** | **Baud rate error** | **Desired baud rate** | **Divisor for 16× clock** | **Baud rate error** |
| 50 | 2304 | | 50 | 3840 | |
| 75 | 1536 | | 75 | 2560 | |
| 110 | 1047 | 0.026 | 110 | 1745 | 0.026 |
| 134.5 | 857 | 0.058 | 134.5 | 1428 | 0.034 |
| 150 | 768 | | 150 | 1280 | |
| 300 | 384 | | 300 | 640 | |
| 600 | 192 | | 600 | 320 | |
| 1200 | 96 | | 1200 | 160 | |
| 1800 | 64 | | 1800 | 107 | 0.312 |
| 2000 | 58 | 0.69 | 2000 | 96 | |
| 2400 | 48 | | 2400 | 80 | |
| 3600 | 32 | | 3600 | 53 | 0.628 |
| 4800 | 24 | | 4800 | 40 | |
| 7200 | 16 | | 7200 | 27 | 1.23 |
| 9600 | 12 | | 9600 | 20 | |
| 19200 | 6 | | 19200 | 10 | |
| 38400 | 3 | | 38400 | 5 | |
| 56000 | 2 | 2.86 | | | |

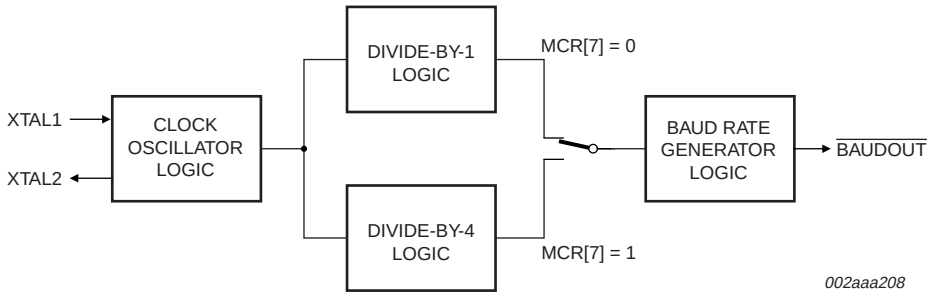



**Fig 6. Baud rate generator circuitry**

## 6.8 DMA operation

The SC16C650B FIFO trigger level provides additional flexibility to the user for block mode operation. The user can optionally operate the transmit and receive FIFOs in the DMA mode (FCR[3]). The DMA mode affects the state of the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ output pins. Table 6 and Table 7 show this.

**Remark:** DMA operation is not supported in the HVQFN32 package.

**Table 6. Effect of DMA mode on state of $\overline{\text{RXRDY}}$ pin**

| Non-DMA mode | DMA mode |
|---|---|
| 1 = FIFO empty | 0-to-1 transition when FIFO empties |
| 0 = at least 1 byte in FIFO | 1-to-0 transition when FIFO reaches trigger level, or time-out occurs |

**Table 7. Effect of DMA mode on state of $\overline{\text{TXRDY}}$ pin**

| Non-DMA mode | DMA mode |
|---|---|
| 1 = at least 1 byte in FIFO | 0-to-1 transition when FIFO becomes full |
| 0 = FIFO empty | 1-to-0 transition when FIFO has 1 empty space |

## 6.9 Sleep mode

The SC16C650B is designed to operate with low power consumption. A special Sleep mode is included to further reduce power consumption when the chip is not being used. With EFR[4] and IER[4] enabled (set to a logic 1), the SC16C650B enters the Sleep mode, but resumes normal operation when a start bit is detected, a change of state on any of the modem input pins $\overline{\text{RI}}$, $\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DCD}}$, RX pin, or a transmit data is provided by the user. If the Sleep mode is enabled and the SC16C650B is awakened by one of the conditions described above, it will return to the Sleep mode automatically after the last character is transmitted or read by the user. In any case, the Sleep mode will not be entered while an interrupt(s) is pending. The SC16C650B will stay in the Sleep mode of operation until it is disabled by setting IER[4] to a logic 0.

## 6.10 Loopback mode

The internal loopback capability allows on-board diagnostics. In the loopback mode, the normal modem interface pins are disconnected and reconfigured for loopback internally. MCR[3:0] register bits are used for controlling loopback diagnostic testing. In the loopback mode, $\overline{\text{OUT1}}$ (bit 2) and $\overline{\text{OUT2}}$ (bit 3) in the MCR register control the modem $\overline{\text{RI}}$ and $\overline{\text{DCD}}$ inputs, respectively. MCR signals $\overline{\text{DTR}}$ (bit 0) and $\overline{\text{RTS}}$ (bit 1) are used to control the modem $\overline{\text{DSR}}$ and $\overline{\text{CTS}}$ inputs, respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (see Figure 7). The $\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DCD}}$, and $\overline{\text{RI}}$ are disconnected from their normal modem control input pins, and instead are connected internally to $\overline{\text{DTR}}$, $\overline{\text{RTS}}$, $\overline{\text{OUT1}}$ and $\overline{\text{OUT2}}$. Loopback test data is entered into the Transmit Holding Register via the user data bus interface, D0 to D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loopback connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface D0 to D7. The user optionally compares the received data to the initial transmitted data for verifying error-free operation of the UART TX/RX circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational. However, the interrupts can only be read using lower four bits of the Modem Status Register (MSR[3:0]) instead of the four Modem Status Register bits 7:4. The interrupts are still controlled by the IER.

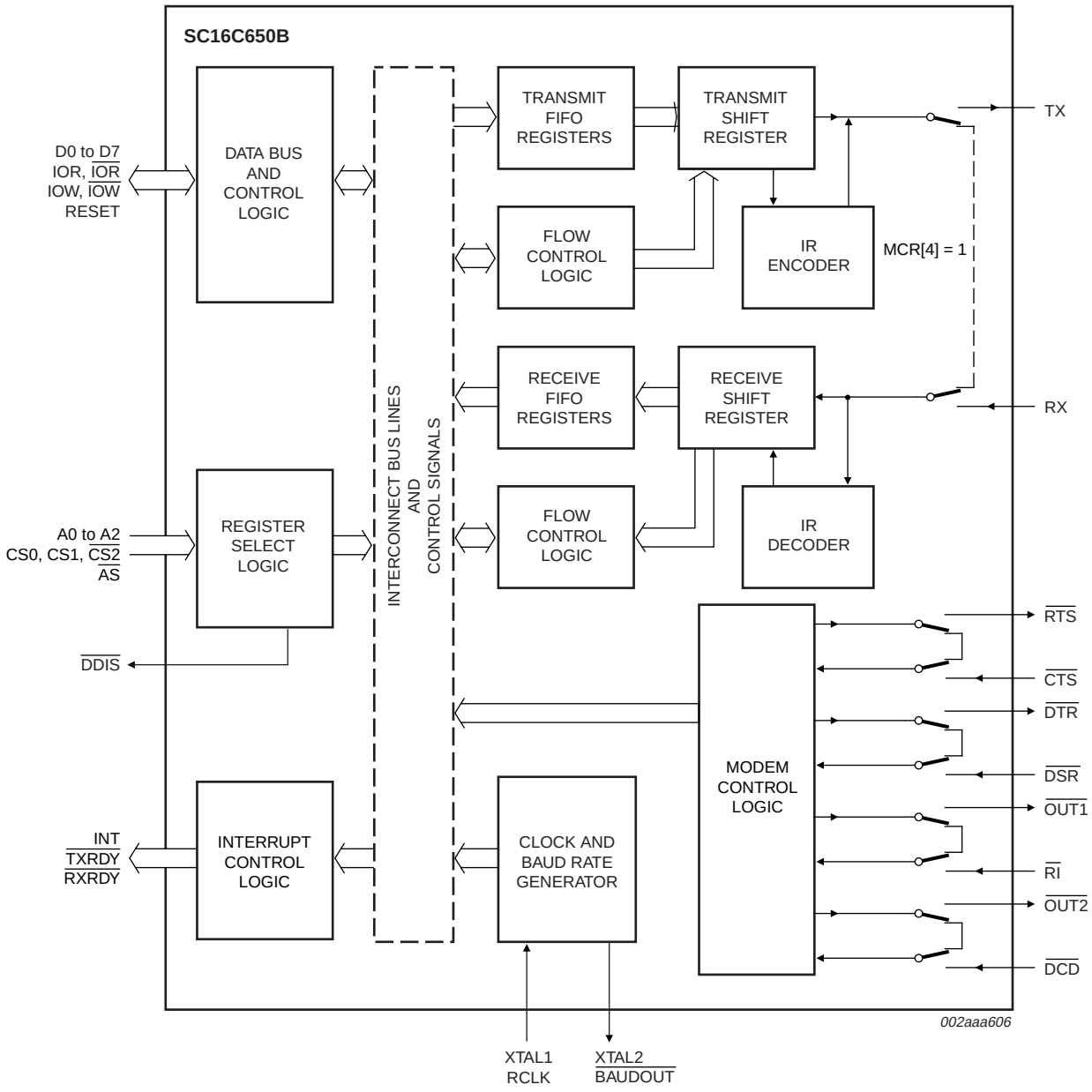



**Fig 7. Internal loopback mode diagram**

# 7. Register descriptions

Table 8 details the assigned bit functions for the seventeen SC16C650B internal registers. The assigned bit functions are more fully defined in Section 7.1 through Section 7.11.

**Table 8. SC16C650B internal registers**

| A2 | A1 | A0 | Register | Default [1] | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **General register set[2]** | | | | | | | | | | | | |
| 0 | 0 | 0 | RHR | XX | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0 | 0 | 0 | THR | XX | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0 | 0 | 1 | IER | 00 | CTS interrupt [3] | RTS interrupt [3] | Xoff interrupt [3] | Sleep mode[3] | modem status interrupt | receive line status interrupt | transmit holding register | receive holding register |
| 0 | 1 | 0 | FCR | 00 | RCVR trigger (MSB) | RCVR trigger (LSB) | TX trigger (MSB)[3] | TX trigger (LSB)[3] | DMA mode select[4] | XMIT FIFO reset | RCVR FIFO reset | FIFO enable |
| 0 | 1 | 0 | ISR | 01 | FIFOs enabled | FIFOs enabled | INT priority bit 4 | INT priority bit 3 | INT priority bit 2 | INT priority bit 1 | INT priority bit 0 | INT status |
| 0 | 1 | 1 | LCR | 00 | divisor latch enable | set break | set parity | even parity | parity enable | stop bits | word length bit 1 | word length bit 0 |
| 1 | 0 | 0 | MCR | 00 | Clock select[3] | IR enable[3] | INT type select[3] | loopback | $\overline{OUT2}$[5] | $\overline{OUT1}$, $\overline{OUT}$[6] | $\overline{RTS}$ | $\overline{DTR}$ |
| 1 | 0 | 1 | LSR | 60 | FIFO data error | trans. empty | trans. holding empty | break interrupt | framing error | parity error | overrun error | receive data ready |
| 1 | 1 | 0 | MSR | X0 | DCD | RI | DSR | CTS | $\Delta\overline{DCD}$ | $\Delta\overline{RI}$ | $\Delta\overline{DSR}$ | $\Delta\overline{CTS}$ |
| 1 | 1 | 1 | SPR | FF | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| **Special register set[7]** | | | | | | | | | | | | |
| 0 | 0 | 0 | DLL | XX | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0 | 0 | 1 | DLM | XX | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 |
| **Enhanced register set[8]** | | | | | | | | | | | | |
| 0 | 1 | 0 | EFR | 00 | Auto CTS | Auto RTS | Special char. select | Enable IER[4:7], ISR[4,5], FCR[4,5], MCR[5:7] | Cont-3 Tx, Rx control | Cont-2 Tx, Rx control | Cont-1 Tx, Rx control | Cont-0 Tx, Rx control |
| 1 | 0 | 0 | Xon1 | 00 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 1 | 0 | 1 | Xon2 | 00 | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 |
| 1 | 1 | 0 | Xoff1 | 00 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 1 | 1 | 1 | Xoff2 | 00 | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 |

[1] The value shown represents the register's initialized HEX value; X = n/a.

[2] These registers are accessible only when LCR[7] = 0.

[3] These bits are only accessible when EFR[4] is set.

[4] This function is not supported in the HVQFN32 package, and should not be written.

[5] $\overline{OUT2}$ pin is not supported in the HVQFN32 package, and this bit should not be written.

[6] This bit controls the $\overline{OUT}$ pin in the HVQFN32 package, and $\overline{OUT1}$ in the other packages.

[7] The Special register set is accessible only when LCR[7] is set to a logic 1.

[8] Enhanced Feature Register (EFR), Xon1, Xon2 Xoff1, Xoff2 are accessible only when LCR is set to BFh.

## 7.1 Transmit Holding Register (THR) and Receive Holding Register (RHR)

The serial transmitter section consists of an 8-bit Transmit Holding Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D[7:0]) to the THR, providing that the THR or TSR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the THR empty flag is set (logic 0 = FIFO full; logic 1 = at least one FIFO location available).

The serial receive section also contains an 8-bit Receive Holding Register (RHR). Receive data is removed from the SC16C650B and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the 16× clock rate. After $7\frac{1}{2}$ clocks, the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled, and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

## 7.2 Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INT output pin.

**Table 9. Interrupt Enable Register bits description**

| Bit | Symbol | Description |
|---|---|---|
| 7 | IER[7] | CTS interrupt.<br>logic 0 = disable the CTS interrupt (normal default condition)<br>logic 1 = enable the CTS interrupt. The SC16C650B issues an interrupt when the CTS pin transitions from a logic 0 to a logic 1. |
| 6 | IER[6] | RTS interrupt.<br>logic 0 = disable the RTS interrupt (normal default condition)<br>logic 1 = enable the RTS interrupt. The SC16C650B issues an interrupt when the RTS pin transitions from a logic 0 to a logic 1. |
| 5 | IER[5] | Xoff interrupt.<br>logic 0 = disable the software flow control, receive Xoff interrupt (normal default condition).<br>logic 1 = enable the software flow control, receive Xoff interrupt. See Section 6.4 “Software flow control” for details. |
| 4 | IER[4] | Sleep mode.<br>logic 0 = disable Sleep mode (normal default condition)<br>logic 1 = enable Sleep mode. See Section 6.9 “Sleep mode” for details. |
| 3 | IER[3] | Modem Status Interrupt.<br>logic 0 = disable the modem status register interrupt (normal default condition)<br>logic 1 = enable the modem status register interrupt |

**Table 9. Interrupt Enable Register bits description** *...continued*

| Bit | Symbol | Description |
|---|---|---|
| 2 | IER[2] | Receive Line Status interrupt. This interrupt will be issued whenever a fully assembled receive character is transferred from RSR to the RHR/FIFO, i.e., data ready, LSR[0].<br>logic 0 = disable the receiver line status interrupt (normal default condition)<br>logic 1 = enable the receiver line status interrupt |
| 1 | IER[1] | Transmit Holding Register interrupt. This interrupt will be issued whenever the THR is empty, and is associated with LSR[1].<br>logic 0 = disable the transmitter empty interrupt (normal default condition)<br>logic 1 = enable the transmitter empty interrupt |
| 0 | IER[0] | Receive Holding Register interrupt. This interrupt will be issued when the FIFO has reached the programmed trigger level, or is cleared when the FIFO drops below the trigger level in the FIFO mode of operation.<br>logic 0 = disable the receiver ready interrupt (normal default condition)<br>logic 1 = enable the receiver ready interrupt |

### 7.2.1 IER versus receive FIFO interrupt mode operation

When the receive FIFO (FCR[0] = logic 1), and receive interrupts (IER[0] = logic 1) are enabled, the receive interrupts and register status will reflect the following:

- The receive data available interrupts are issued to the external CPU when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.
- FIFO status will also be reflected in the user accessible ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.
- The data ready bit (LSR[0]) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

### 7.2.2 IER versus receive/transmit FIFO polled mode operation

When FCR[0] = logic 1, resetting IER[3:0] enables the SC16C650B in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR, either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

- LSR[0] will be a logic 1 as long as there is one byte in the receive FIFO.
- LSR[4:1] will provide the type of errors encountered, if any.
- LSR[5] will indicate when the transmit FIFO is empty.
- LSR[6] will indicate when both the transmit FIFO and transmit shift register are empty.
- LSR[7] will indicate any FIFO data errors.

## 7.3 FIFO Control Register (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receive FIFO trigger levels, and select the DMA mode.

### 7.3.1 DMA mode

#### 7.3.1.1 Mode 0 (FCR bit 3 = 0)

Set and enable the interrupt for each single transmit or receive operation, and is similar to the 16C450 mode. Transmit Ready ($\overline{\text{TXRDY}}$) will go to a logic 0 whenever an empty transmit space is available in the Transmit Holding Register (THR). Receive Ready ($\overline{\text{RXRDY}}$) will go to a logic 0 whenever the Receive Holding Register (RHR) is loaded with a character.

#### 7.3.1.2 Mode 1 (FCR bit 3 = 1)

Set and enable the interrupt in a block mode operation. The transmit interrupt is set when the transmit FIFO is below the programmed trigger level. The receive interrupt is set when the receive FIFO fills to the programmed trigger level. However, the FIFO continues to fill regardless of the programmed level until the FIFO is full. $\overline{\text{RXRDY}}$ remains a logic 0 as long as the FIFO fill level is above the programmed trigger level.

### 7.3.2 FIFO mode

**Table 10. FIFO Control Register bits description**

| Bit | Symbol | Description |
|---|---|---|
| 7:6 | FCR[7] (MSB), FCR[6] (LSB) | RCVR trigger. These bits are used to set the trigger level for the receive FIFO interrupt.<br>An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However, the FIFO will continue to be loaded until it is full. Refer to Table 11. |
| 5:4 | FCR[5] (MSB), FCR[4] (LSB) | Logic 0 or cleared is the default condition; TX trigger level = 16.<br>These bits are used to set the trigger level for the transmit FIFO interrupt. The SC16C650B will issue a transmit empty interrupt when the number of characters in FIFO drops below the selected trigger level. Refer to Table 12. |
| 3 | FCR[3] | DMA mode select.<br>logic 0 = set DMA mode ‘0’ (normal default condition)<br>logic 1 = set DMA mode ‘1’<br>**Transmit operation in mode ‘0’:** When the SC16C650B is in the 16C450 mode (FIFOs disabled; FCR[0] = logic 0) or in the FIFO mode (FIFOs enabled; FCR[0] = logic 1; FCR[3] = logic 0), and when there are no characters in the transmit FIFO or transmit holding register, the $\overline{\text{TXRDY}}$ pin will be a logic 0. Once active, the $\overline{\text{TXRDY}}$ pin will go to a logic 1 after the first character is loaded into the transmit holding register.<br>**Receive operation in mode ‘0’:** When the SC16C650B is in 16C450 mode, or in the FIFO mode (FCR[0] = logic 1; FCR[3] = logic 0) and there is at least one character in the receive FIFO, the $\overline{\text{RXRDY}}$ pin will be a logic 0. Once active, the $\overline{\text{RXRDY}}$ pin will go to a logic 1 when there are no more characters in the receiver. |

**Table 10. FIFO Control Register bits description** *…continued*

| Bit | Symbol | Description |
|---|---|---|
| 3 (cont.) | | **Transmit operation in mode '1':** When the SC16C650B is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1), the $\overline{\text{TXRDY}}$ pin will be a logic 1 when the transmit FIFO is completely full. It will be a logic 0 when FIFO has 1 empty space.<br>**Receive operation in mode '1':** When the SC16C650B is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1) and the trigger level has been reached, or a Receive Time-Out has occurred, the $\overline{\text{RXRDY}}$ pin will go to a logic 0. Once activated, it will go to a logic 1 after there are no more characters in the FIFO. |
| 2 | FCR[2] | XMIT FIFO reset.<br>logic 0 = no FIFO transmit reset (normal default condition)<br>logic 1 = clears the contents of the transmit FIFO and resets the FIFO counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO. |
| 1 | FCR[1] | RCVR FIFO reset.<br>logic 0 = no FIFO receive reset (normal default condition)<br>logic 1 = clears the contents of the receive FIFO and resets the FIFO counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO. |
| 0 | FCR[0] | FIFO enable.<br>logic 0 = disable the transmit and receive FIFO (normal default condition)<br>logic 1 = enable the transmit and receive FIFO. **This bit must be a logic 1 when other FCR bits are written to, or they will not be programmed.** |

**Table 11. RCVR trigger levels**

| FCR[7] | FCR[6] | RX FIFO trigger level (bytes) |
|---|---|---|
| 0 | 0 | 8 |
| 0 | 1 | 16 |
| 1 | 0 | 24 |
| 1 | 1 | 28 |

**Table 12. TX FIFO trigger levels**

| FCR[5] | FCR[4] | TX FIFO trigger level (bytes) |
|---|---|---|
| 0 | 0 | 16 |
| 0 | 1 | 8 |
| 1 | 0 | 24 |
| 1 | 1 | 30 |

## 7.4 Interrupt Status Register (ISR)

The SC16C650B provides six levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. However, it should be noted that only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after re-reading the interrupt status bits. Table 13 “Interrupt source” shows the data values (bits 0:5) for the six prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

**Table 13. Interrupt source**

| Priority level | ISR[5] | ISR[4] | ISR[3] | ISR[2] | ISR[1] | ISR[0] | Source of the interrupt |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | LSR (receiver Line Status Register) |
| 2 | 0 | 0 | 0 | 1 | 0 | 0 | RXRDY (Received Data Ready) |
| 2 | 0 | 0 | 1 | 1 | 0 | 0 | RXRDY (Receive Data time-out) |
| 3 | 0 | 0 | 0 | 0 | 1 | 0 | TXRDY (Transmitter Holding Register Empty) |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | MSR (Modem Status Register) |
| 5 | 0 | 1 | 0 | 0 | 0 | 0 | RXRDY (Received Xoff signal) / Special character |
| 6 | 1 | 0 | 0 | 0 | 0 | 0 | CTS, RTS change of state |

**Table 14. Interrupt Status Register bits description**

| Bit | Symbol | Description |
|---|---|---|
| 7:6 | ISR[7:6] | FIFOs enabled. These bits are set to a logic 0 when the FIFO is not being used. They are set to a logic 1 when the FIFOs are enabled.<br>logic 0 or cleared = default condition |
| 5:4 | ISR[5:4] | INT priority bits 4:3. These bits are enabled when EFR[4] is set to a logic 1. ISR[4] indicates that matching Xoff character(s) have been detected. ISR[5] indicates that CTS, RTS have been generated. Note that once set to a logic 1, the ISR[4] bit will stay a logic 1 until Xon character(s) are received.<br>logic 0 or cleared = default condition |
| 3:1 | ISR[3:1] | INT priority bits 2:0. These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (see Table 13).<br>logic 0 or cleared = default condition |
| 0 | ISR[0] | INT status.<br>logic 0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.<br>logic 1 = no interrupt pending (normal default condition) |

## 7.5 Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

**Table 15. Line Control Register bits description**

| Bit | Symbol | Description |
|---|---|---|
| 7 | LCR[7] | Divisor latch enable. The internal baud rate counter latch and Enhanced Feature mode enable.<br>logic 0 = divisor latch disabled (normal default condition)<br>logic 1 = divisor latch and enhanced feature register enabled |
| 6 | LCR[6] | Set break. When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR[6] to a logic 0.<br>logic 0 = no TX break condition (normal default condition)<br>logic 1 = forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition |
| 5 | LCR[5] | Set parity. If the parity bit is enabled, LCR[5] selects the forced parity format. Programs the parity conditions (see Table 16).<br>logic 0 = parity is not forced (normal default condition)<br>LCR[5] = logic 1 and LCR[4] = logic 0: parity bit is forced to a logic 1 for the transmit and receive data<br>LCR[5] = logic 1 and LCR[4] = logic 1: parity bit is forced to a logic 0 for the transmit and receive data |
| 4 | LCR[4] | Even parity. If the parity bit is enabled with LCR[3] set to a logic 1, LCR[4] selects the even or odd parity format.<br>logic 0 = odd parity is generated by forcing an odd number of logic 1s in the transmitted data. The receiver must be programmed to check the same format (normal default condition).<br>logic 1 = even parity is generated by forcing an even number of logic 1s in the transmitted data. The receiver must be programmed to check the same format. |
| 3 | LCR[3] | Parity enable. Parity or no parity can be selected via this bit.<br>logic 0 = no parity (normal default condition)<br>logic 1 = a parity bit is generated during the transmission, receiver checks the data and parity for transmission errors |
| 2 | LCR[2] | Stop bits. The length of stop bit is specified by this bit in conjunction with the programmed word length (see Table 17).<br>logic 0 or cleared = default condition |
| 1:0 | LCR[1:0] | Word length bits 1, 0. These two bits specify the word length to be transmitted or received (see Table 18).<br>logic 0 or cleared = default condition |

**Table 16. LCR[5] parity selection**

| LCR[5] | LCR[4] | LCR[3] | Parity selection |
|---|---|---|---|
| X | X | 0 | no parity |
| 0 | 0 | 1 | odd parity |
| 0 | 1 | 1 | even parity |
| 1 | 0 | 1 | force parity ‘1’ |
| 1 | 1 | 1 | forced parity ‘0’ |

**Table 17. LCR[2] stop bit length**

| LCR[2] | Word length | Stop bit length (bit times) |
|---|---|---|
| 0 | 5, 6, 7, 8 | 1 |
| 1 | 5 | 1-½ |
| 1 | 6, 7, 8 | 2 |

**Table 18. LCR[1:0] word length**

| LCR[1] | LCR[0] | Word length |
|---|---|---|
| 0 | 0 | 5 |
| 0 | 1 | 6 |
| 1 | 0 | 7 |
| 1 | 1 | 8 |

## 7.6 Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

**Table 19. Modem Control Register bits description**

| Bit | Symbol | Description |
|---|---|---|
| 7 | MCR[7] | Clock select.<br>logic 0 = divide-by-1. The input clock (crystal or external) is divided by 16 and then presented to the programmable Baud Rate Generator (BGR) without further modification, i.e., divide-by-1 (normal default condition).<br>logic 1 = divide-by-4. The divide-by-1 clock described in MCR[7] equals a logic 0, is further divided by four (see also Section 6.7 “Programmable baud rate generator”). |
| 6 | MCR[6] | IR enable.<br>logic 0 = enable the standard modem receive and transmit input/output interface (normal default condition)<br>logic 1 = enable infrared IrDA receive and transmit inputs/outputs. While in this mode, the TX/RX output/inputs are routed to the infrared encoder/decoder. The data input and output levels will conform to the IrDA infrared interface requirement. As such, while in this mode, the infrared TX output will be a logic 0 during idle data conditions. |

**Table 19. Modem Control Register bits description** *…continued*

| Bit | Symbol | Description |
|---|---|---|
| 5 | MCR[5] | INT type select.<br>logic 0 = enable interrupt output mode (normal default condition)<br>logic 1 = enable open source interrupt output mode. Provides shared interrupts by producing a wire-OR output driver capability for interrupts. This output appears at the INT pin. When using this option, an external pull-down resistor of 200 Ω to 500 Ω must be tied from the INT pin to ground to provide an acceptable logic 0 level |
| 4 | MCR[4] | Loopback. Enable the local loopback mode (diagnostics). In this mode the transmitter output ($\overline{TX}$) and the receiver input ($\overline{RX}$), $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$ are disconnected from the SC16C650B I/O pins. Internally the modem data and control pins are connected into a loopback data configuration (see Figure 7). In this mode, the receiver and transmitter interrupts remain fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are switched to the lower four bits of the Modem Control. Interrupts continue to be controlled by the IER register.<br>logic 0 = disable loopback mode (normal default condition)<br>logic 1 = enable local loopback mode (diagnostics) |
| 3 | MCR[3] | $\overline{OUT2}$. In the loopback mode this bit is used to control the modem $\overline{DCD}$ signal via $\overline{OUT2}$.<br>logic 0 = $\overline{OUT2}$ is at logic 1. In the loopback mode, sets $\overline{OUT2}$ ($\overline{DCD}$) internally to a logic 1.<br>logic 1 = OUT2 is at logic 0. In the loopback mode, sets $\overline{OUT2}$ ($\overline{DCD}$) internally to a logic 0. |
| 2 | MCR[2] | $\overline{OUT1}$, $\overline{OUT}$. In the loopback mode, this bit is used to control modem $\overline{RI}$ interface signal via $\overline{OUT1}$ ($\overline{OUT}$ in the HVQFN32 package).<br>logic 0 = $\overline{OUT1}$/$\overline{OUT}$ is at logic 1. In the loopback mode, sets $\overline{RI}$ internally to logic 1.<br>logic 1 = OUT1/OUT is set at logic 0. In the loopback mode, sets $\overline{RI}$ internally to logic 0. |
| 1 | MCR[1] | $\overline{RTS}$<br>logic 0 = force $\overline{RTS}$ output to a logic 1 (normal default condition)<br>logic 1 = force $\overline{RTS}$ output to a logic 0 |
| 0 | MCR[0] | $\overline{DTR}$<br>logic 0 = force $\overline{DTR}$ output to a logic 1 (normal default condition)<br>logic 1 = force $\overline{DTR}$ output to a logic 0 |

## 7.7 Line Status Register (LSR)

This register provides the status of data transfers between the SC16C650B and the CPU.

**Table 20. Line Status Register bits description**

| Bit | Symbol | Description |
|---|---|---|
| 7 | LSR[7] | FIFO data error.<br>logic 0 = no error (normal default condition)<br>logic 1 = at least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when LSR register is read. |
| 6 | LSR[6] | THR and TSR empty. This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the transmit holding register and the transmit shift register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode, this bit is set to '1' whenever the transmit FIFO and transmit shift register are both empty. |
| 5 | LSR[5] | THR empty. This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the transmit holding register into the transmitter shift register. The bit is reset to a logic 0 concurrently with the loading of the transmit holding register by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO. |
| 4 | LSR[4] | Break interrupt.<br>logic 0 = no break condition (normal default condition)<br>logic 1 = the receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO. |
| 3 | LSR[3] | Framing error.<br>logic 0 = no framing error (normal default condition)<br>logic 1 = framing error. The receive character did not have a valid stop bit(s). In the FIFO mode, this error is associated with the character at the top of the FIFO. |
| 2 | LSR[2] | Parity error.<br>logic 0 = no parity error (normal default condition)<br>logic 1 = parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO. |
| 1 | LSR[1] | Overrun error.<br>logic 0 = no overrun error (normal default condition).<br>logic 1 = overrun error. A data overrun error occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case, the previous data in the shift register is overwritten. Note that under this condition, the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error. |
| 0 | LSR[0] | Receive data ready.<br>logic 0 = no data in receive holding register or FIFO (normal default condition)<br>logic 1 = data has been received and is saved in the receive holding register or FIFO |

## 7.8 Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem, or other peripheral device to which the SC16C650B is connected. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

**Table 21. Modem Status Register bits description**

| Bit | Symbol | Description |
|---|---|---|
| 7 | MSR[7] | Data Carrier Detect. DCD (active HIGH, logic 1). Normally this bit is the complement of the $\overline{DCD}$ input. In the loopback mode this bit is equivalent to the OUT2 bit in the MCR register. |
| 6 | MSR[6] | Ring Indicator. RI (active HIGH, logic 1). Normally this bit is the complement of the $\overline{RI}$ input. In the loopback mode this bit is equivalent to the OUT1 bit in the MCR register. |
| 5 | MSR[5] | Data Set Ready. DSR (active HIGH, logic 1). Normally this bit is the complement of the $\overline{DSR}$ input. In loopback mode this bit is equivalent to the DTR bit in the MCR register. |
| 4 | MSR[4] | Clear To Send. CTS. $\overline{CTS}$ functions as hardware flow control signal input if it is enabled via EFR[7]. Flow control (when enabled) allows starting and stopping the transmissions based on the external modem $\overline{CTS}$ signal. A logic 1 at the $\overline{CTS}$ pin will stop SC16C650B transmissions as soon as current character has finished transmission. Normally MSR[4] is the complement of the $\overline{CTS}$ input. However, in the loopback mode, this bit is equivalent to the RTS bit in the MCR register. |
| 3 | MSR[3] | $\Delta\overline{DCD}$ [1]<br>logic 0 = no $\overline{DCD}$ change (normal default condition)<br>logic 1 = the $\overline{DCD}$ input to the SC16C650B has changed state since the last time it was read. A modem Status Interrupt will be generated. |
| 2 | MSR[2] | $\Delta\overline{RI}$ [1]<br>logic 0 = no $\overline{RI}$ change (normal default condition)<br>logic 1 = the $\overline{RI}$ input to the SC16C650B has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated. |
| 1 | MSR[1] | $\Delta\overline{DSR}$ [1]<br>logic 0 = no $\overline{DSR}$ change (normal default condition)<br>logic 1 = the $\overline{DSR}$ input to the SC16C650B has changed state since the last time it was read. A modem Status Interrupt will be generated. |
| 0 | MSR[0] | $\Delta\overline{CTS}$ [1]<br>logic 0 = no $\overline{CTS}$ change (normal default condition)<br>logic 1 = the $\overline{CTS}$ input to the SC16C650B has changed state since the last time it was read. A modem Status Interrupt will be generated. |

[1] Whenever any MSR bit 3:0 is set to logic 1, a Modem Status Interrupt will be generated.

## 7.9 Scratchpad Register (SPR)

The SC16C650B provides a temporary data register to store 8 bits of user information.

## 7.10 Enhanced Feature Register (EFR)

Enhanced features are enabled or disabled using this register.

Bits 0 through 4 provide single or dual character software flow control selection. When the Xon1 and Xon2 and/or Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential numbers.

**Table 22. Enhanced Feature Register bits description**

| Bit | Symbol | Description |
|---|---|---|
| 7 | EFR[7] | Automatic CTS flow control.<br>logic 0 = Automatic CTS flow control is disabled (normal default condition)<br>logic 1 = enable Automatic CTS flow control. Transmission will stop when $\overline{CTS}$ goes to a logic 1. Transmission will resume when the $\overline{CTS}$ pin returns to a logic 0. |
| 6 | EFR[6] | Automatic RTS flow control. Automatic RTS may be used for hardware flow control by enabling EFR[6]. When Auto-RTS is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and $\overline{RTS}$ will go to a logic 1 at the next trigger level. $\overline{RTS}$ will return to a logic 0 when data is unloaded below the next lower trigger level (programmed trigger level 1). The state of this register bit changes with the status of the hardware flow control. $\overline{RTS}$ functions normally when hardware flow control is disabled.<br>0 = Automatic RTS flow control is disabled (normal default condition)<br>1 = enable Automatic RTS flow control |
| 5 | EFR[5] | Special Character Detect.<br>logic 0 = special character detect disabled (normal default condition)<br>logic 1 = special character detect enabled. The SC16C650B compares each incoming receive character with Xoff2 data. If a match exists, the received data will be transferred to FIFO and ISR[4] will be set to indicate detection of special character. Bit 0 in the X-registers corresponds with the LSB bit for the receive character. When this feature is enabled, the normal software flow control must be disabled (EFR[3:0] must be set to a logic 0). |
| 4 | EFR[4] | Enhanced function control bit. The content of IER[7:4], ISR[5:4], FCR[5:4], and MCR[7:5] can be modified and latched. After modifying any bits in the enhanced registers, EFR[4] can be set to a logic 0 to latch the new values. This feature prevents existing software from altering or overwriting the SC16C650B enhanced functions.<br>logic 0 = disable (normal default condition)<br>logic 1 = enable |
| 3:0 | EFR[3:0] | Cont-3:0 Tx, Rx control. Logic 0 or cleared is the default condition. Combinations of software flow control can be selected by programming these bits. See Table 23. |

**Table 23. Software flow control functions[1]**

| Cont-3 | Cont-2 | Cont-1 | Cont-0 | TX, RX software flow controls |
|---|---|---|---|---|
| 0 | 0 | X | X | No transmit flow control |
| 1 | 0 | X | X | Transmit Xon1/Xoff1 |
| 0 | 1 | X | X | Transmit Xon2/Xoff2 |
| 1 | 1 | X | X | Transmit Xon1 and Xon2/Xoff1 and Xoff2 |
| X | X | 0 | 0 | No receive flow control |
| X | X | 1 | 0 | Receiver compares Xon1/Xoff1 |
| X | X | 0 | 1 | Receiver compares Xon2/Xoff2 |
| 1 | 0 | 1 | 1 | Transmit Xon1/Xoff1 |
| | | | | Receiver compares Xon1 and Xon2, Xoff1 and Xoff2 |
| 0 | 1 | 1 | 1 | Transmit Xon2/Xoff2 |
| | | | | Receiver compares Xon1 and Xon2/Xoff1 and Xoff2 |
| 1 | 1 | 1 | 1 | Transmit Xon1 and Xon2/Xoff1 and Xoff2 |
| | | | | Receiver compares Xon1 and Xon2/Xoff1 and Xoff2 |

[1] When using a software flow control the Xon/Xoff characters cannot be used for data transfer.

## 7.11 SC16C650B external reset conditions

**Table 24. Reset state for registers**

| Register | Reset state |
|---|---|
| IER | IER[7:0] = 0 |
| ISR | ISR[7:1] = 0; ISR[0] = 1 |
| LCR | LCR[7:0] = 0 |
| MCR | MCR[7:0] = 0 |
| LSR | LSR[7] = 0; LSR[6:5] = 1; LSR[4:0] = 0 |
| MSR | MSR[7:4] = input signals; MSR[3:0] = 0 |
| FCR | FCR[7:0] = 0 |
| EFR | EFR[7:0] = 0 |

**Table 25. Reset state for outputs**

| Output | Reset state |
|---|---|
| TX | HIGH |
| $\overline{\text{RTS}}$ | HIGH |
| $\overline{\text{DTR}}$ | HIGH |
| $\overline{\text{RXRDY}}$ | HIGH |
| $\overline{\text{TXRDY}}$ | LOW |
| INT | LOW |

# 8. Limiting values

**Table 26. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | - | 7 | V |
| $V_n$ | voltage on any other pin | at D7 to D0 | GND – 0.3 | $V_{CC}$ + 0.3 | V |
| | | at any input only pin | GND – 0.3 | 5.3 | V |
| $T_{amb}$ | ambient temperature | operating in free air | –40 | +85 | °C |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $P_{tot}$/pack | total power dissipation per package | | - | 500 | mW |

# 9. Static characteristics

**Table 27. Static characteristics**

*$T_{amb}$ = –40 °C to +85 °C; tolerance of $V_{CC}$ ± 10 %, unless otherwise specified.*

| Symbol | Parameter | Conditions | | $V_{CC}$ = 2.5 V | | $V_{CC}$ = 3.3 V | | $V_{CC}$ = 5.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| $V_{IL(clk)}$ | clock LOW-level input voltage | | | –0.3 | +0.45 | –0.3 | +0.6 | –0.5 | +0.6 | V |
| $V_{IH(clk)}$ | clock HIGH-level input voltage | | | 1.8 | $V_{CC}$ | 2.4 | $V_{CC}$ | 3.0 | $V_{CC}$ | V |
| $V_{IL}$ | LOW-level input voltage | | | –0.3 | +0.65 | –0.3 | +0.8 | –0.5 | +0.8 | V |
| $V_{IH}$ | HIGH-level input voltage | | | 1.6 | - | 2.0 | - | 2.2 | $V_{CC}$ | V |
| $V_{OL}$ | LOW-level output voltage | on all outputs | [1] | | | | | | | |
| | | $I_{OL}$ = 5 mA (data bus) | | - | - | - | - | - | 0.4 | V |
| | | $I_{OL}$ = 4 mA (other outputs) | | - | - | - | 0.4 | - | - | V |
| | | $I_{OL}$ = 2 mA (data bus) | | - | 0.4 | - | - | - | - | V |
| | | $I_{OL}$ = 1.6 mA (other outputs) | | - | 0.4 | - | - | - | - | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = –5 mA (data bus) | | - | - | - | - | 2.4 | - | V |
| | | $I_{OH}$ = –1 mA (other outputs) | | - | - | 2.0 | - | - | - | V |
| | | $I_{OH}$ = –800 µA (data bus) | | 1.85 | - | - | - | - | - | V |
| | | $I_{OH}$ = –400 µA (other outputs) | | 1.85 | - | - | - | - | - | V |
| $I_{LIL}$ | LOW-level input leakage current | | | - | ±10 | - | ±10 | - | ±10 | µA |
| $I_{L(clk)}$ | clock leakage current | | | - | ±30 | - | ±30 | - | ±30 | µA |
| $I_{CC(AV)}$ | average supply current | f = 5 MHz | | - | 3.5 | - | 4.5 | - | 4.5 | mA |
| $I_{CC(sleep)}$ | sleep mode supply current | f = 5 MHz | [2] | - | 50 | - | 50 | - | 50 | µA |
| $C_i$ | input capacitance | | | - | 5 | - | 5 | - | 5 | pF |
| $R_{pu(int)}$ | internal pull-up resistance | | | 500 | - | 500 | - | 500 | - | kΩ |

[1] Except for XTAL2, $V_{OL}$ = 1 V typically.

[2] Sleep current might be higher if there is activity on the data bus during Sleep mode.

## 10. Dynamic characteristics

**Table 28. Dynamic characteristics**

*$T_{amb}$ = −40 °C to +85 °C; tolerance of $V_{CC}$ ± 10 %, unless otherwise specified.*

| Symbol | Parameter | Conditions | | $V_{CC}$ = 2.5 V | | $V_{CC}$ = 3.3 V | | $V_{CC}$ = 5.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{WL}$ | pulse width LOW | | | 15 | - | 13 | - | 10 | - | ns |
| $t_{WH}$ | pulse width HIGH | | | 15 | - | 13 | - | 10 | - | ns |
| $f_{XTAL1}$ | frequency on pin XTAL1 | | [1] | - | 16 | - | 32 | - | 48 | MHz |
| $t_{4w}$ | address strobe width | | | 45 | - | 35 | - | 25 | - | ns |
| $t_{5s}$ | address set-up time | | | 5 | - | 5 | - | 1 | - | ns |
| $t_{5h}$ | address hold time | | | 5 | - | 5 | - | 5 | - | ns |
| $t_{6s}$ | chip select set-up time to $\overline{AS}$ | | | 10 | - | 5 | - | 0 | - | ns |
| $t_{6h}$ | address hold time | | | 0 | - | 0 | - | 0 | - | ns |
| $t_{6s'}$ | address set-up time | | [2] | 10 | - | 10 | - | 5 | - | ns |
| $t_{6h}$ | chip select hold time | | | 0 | - | 0 | - | 0 | - | ns |
| $t_{7d}$ | $\overline{IOR}$ delay from chip select | | | 10 | - | 10 | - | 10 | - | ns |
| $t_{7w}$ | $\overline{IOR}$ strobe width | 25 pF load | | 77 | - | 26 | - | 23 | - | ns |
| $t_{7h}$ | chip select hold time from $\overline{IOR}$ | | | 0 | - | 0 | - | 0 | - | ns |
| $t_{7h'}$ | address hold time | | [2] | 5 | - | 5 | - | 5 | - | ns |
| $t_{8d}$ | $\overline{IOR}$ delay from address | | | 10 | - | 10 | - | 10 | - | ns |
| $t_{9d}$ | read cycle delay | 25 pF load | | 20 | - | 20 | - | 20 | - | ns |
| $t_{11d}$ | $\overline{IOR}$ to $\overline{DDIS}$ delay | 25 pF load | | - | 100 | - | 35 | - | 30 | ns |
| $t_{12d}$ | delay from $\overline{IOR}$ to data | 25 pF load | | - | 77 | - | 26 | - | 23 | ns |
| $t_{12h}$ | data disable time | 25 pF load | | - | 15 | - | 15 | - | 15 | ns |
| $t_{13d}$ | $\overline{IOW}$ delay from chip select | | | 10 | - | 10 | - | 10 | - | ns |
| $t_{13w}$ | $\overline{IOW}$ strobe width | | | 20 | - | 20 | - | 15 | - | ns |
| $t_{13h}$ | chip select hold time from $\overline{IOW}$ | | | 0 | - | 0 | - | 0 | - | ns |
| $t_{14d}$ | $\overline{IOW}$ delay from address | | | 10 | - | 10 | - | 10 | - | ns |
| $t_{15d}$ | write cycle delay | | | 25 | - | 25 | - | 20 | - | ns |
| $t_{16s}$ | data set-up time | | | 20 | - | 20 | - | 15 | - | ns |
| $t_{16h}$ | data hold time | | | 15 | - | 5 | - | 5 | - | ns |
| $t_{17d}$ | delay from $\overline{IOW}$ to output | 25 pF load | | - | 100 | - | 33 | - | 29 | ns |
| $t_{18d}$ | delay to set interrupt from Modem input | 25 pF load | | - | 100 | - | 24 | - | 23 | ns |
| $t_{19d}$ | delay to reset interrupt from $\overline{IOR}$ | 25 pF load | | - | 100 | - | 24 | - | 23 | ns |
| $t_{20d}$ | delay from stop to set interrupt | | [3] | - | $1T_{RCLK}$ | - | $1T_{RCLK}$ | - | $1T_{RCLK}$ | s |
| $t_{21d}$ | delay from $\overline{IOR}$ to reset interrupt | 25 pF load | | - | 100 | - | 29 | - | 28 | ns |

**Table 28. Dynamic characteristics** *…continued*

*$T_{amb}$ = −40 °C to +85 °C; tolerance of $V_{CC}$ ± 10 %, unless otherwise specified.*

| Symbol | Parameter | Conditions | | $V_{CC}$ = 2.5 V | | $V_{CC}$ = 3.3 V | | $V_{CC}$ = 5.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{22d}$ | delay from start to set interrupt | | | - | 100 | - | 45 | - | 40 | ns |
| $t_{23d}$ | delay from $\overline{IOW}$ to transmit start | | [3] | $8T_{RCLK}$ | $24T_{RCLK}$ | $8T_{RCLK}$ | $24T_{RCLK}$ | $8T_{RCLK}$ | $24T_{RCLK}$ | s |
| $t_{24d}$ | delay from $\overline{IOW}$ to reset interrupt | | | - | 100 | - | 45 | - | 40 | ns |
| $t_{25d}$ | delay from stop to set $\overline{RXRDY}$ | | [3] | - | $1T_{RCLK}$ | - | $1T_{RCLK}$ | - | $1T_{RCLK}$ | s |
| $t_{26d}$ | delay from $\overline{IOR}$ to reset $\overline{RXRDY}$ | | | - | 100 | - | 45 | - | 40 | ns |
| $t_{27d}$ | delay from $\overline{IOW}$ to set $\overline{TXRDY}$ | | | - | 100 | - | 45 | - | 40 | ns |
| $t_{28d}$ | delay from start to reset $\overline{TXRDY}$ | | [3] | - | $8T_{RCLK}$ | - | $8T_{RCLK}$ | - | $8T_{RCLK}$ | s |
| $t_{RESET}$ | RESET pulse width | | [4] | 100 | - | 40 | - | 40 | - | ns |
| N | baud rate divisor | | | 1 | $2^{16} - 1$ | 1 | $2^{16} - 1$ | 1 | $2^{16} - 1$ | |

[1] Applies to external clock; crystal oscillator max 24 MHz.

[2] Applicable only when $\overline{AS}$ is tied LOW.

[3] RCLK is an internal signal derived from Divisor Latch LSB (DLL) and Divisor Latch MSB (DLM) divisor latches.

[4] RESET pulse must happen when these signals are inactive: $\overline{CS}$, CS0, CS1, $\overline{CS2}$, IOR, $\overline{IOR}$, IOW, $\overline{IOW}$.

## 10.1 Timing diagrams

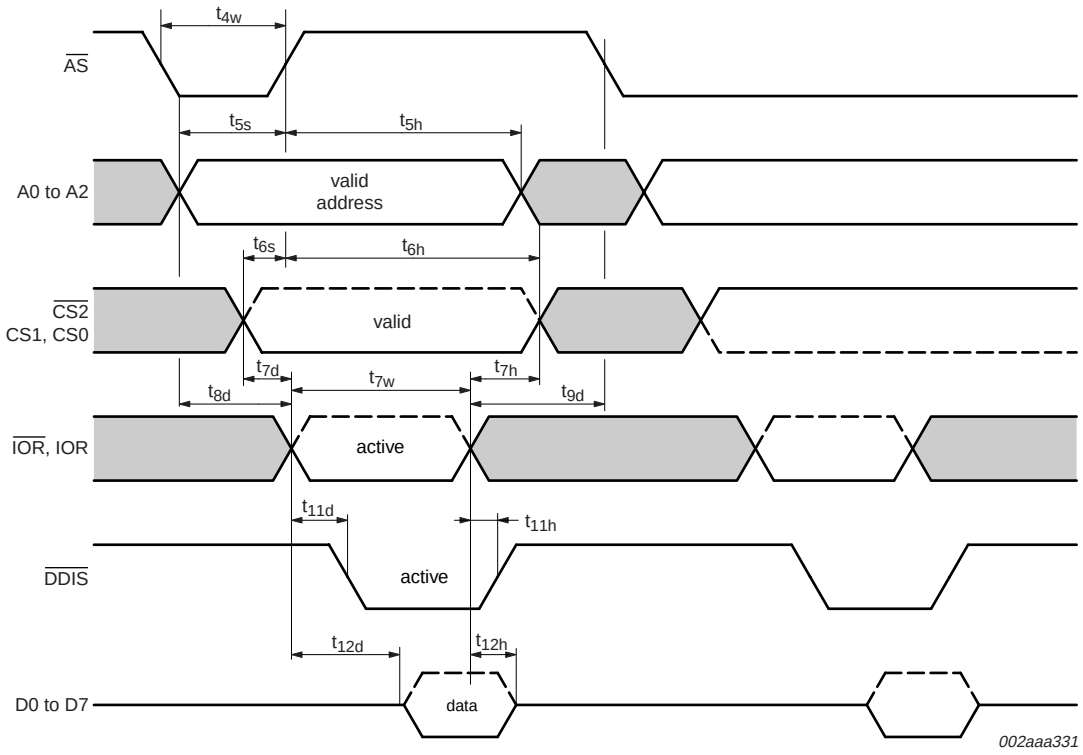



**Fig 8. General read timing when using $\overline{AS}$ signal**

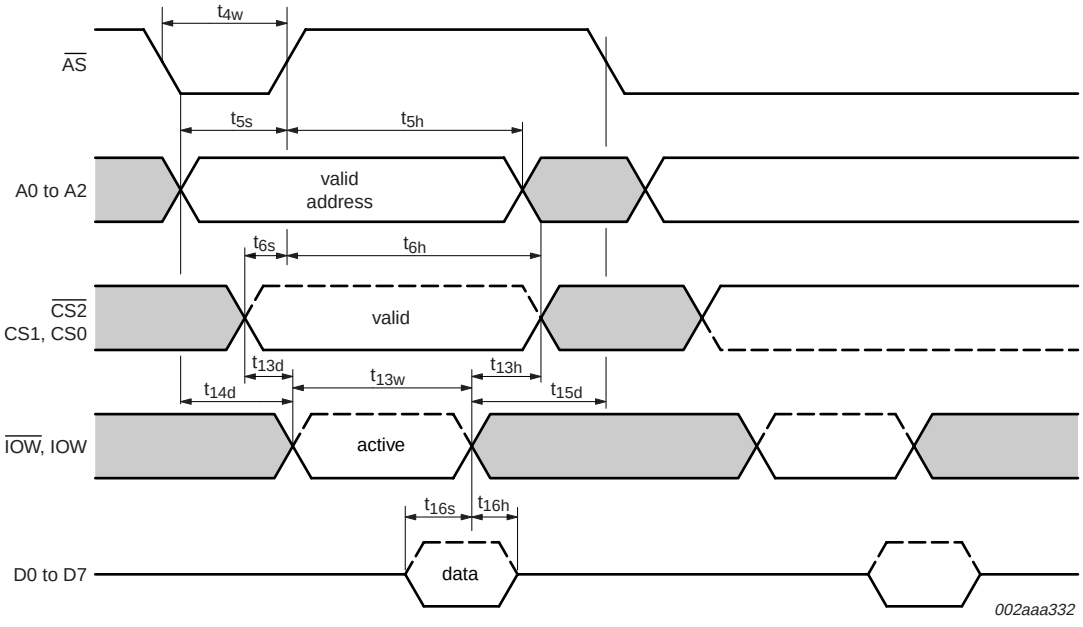



**Fig 9. General write timing when using $\overline{AS}$ signal**

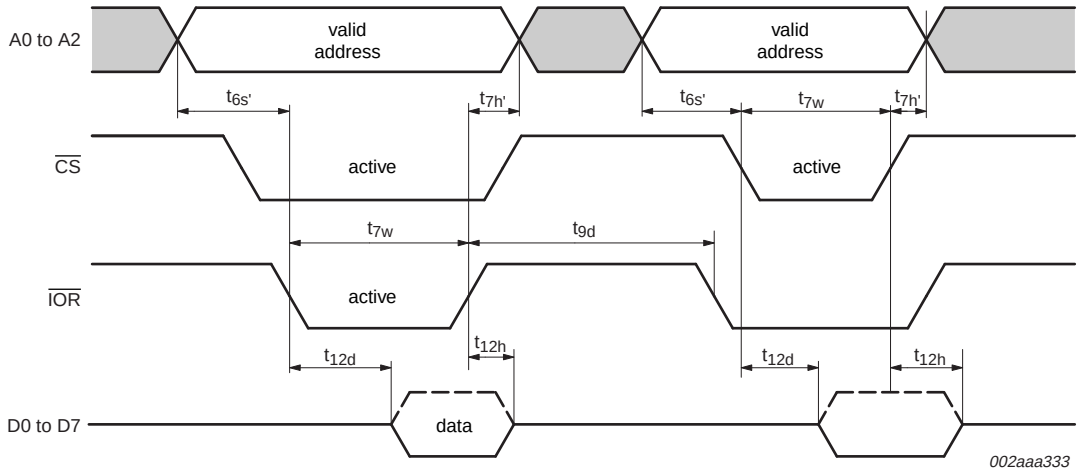



**Fig 10. General read timing when $\overline{AS}$ is tied to GND**

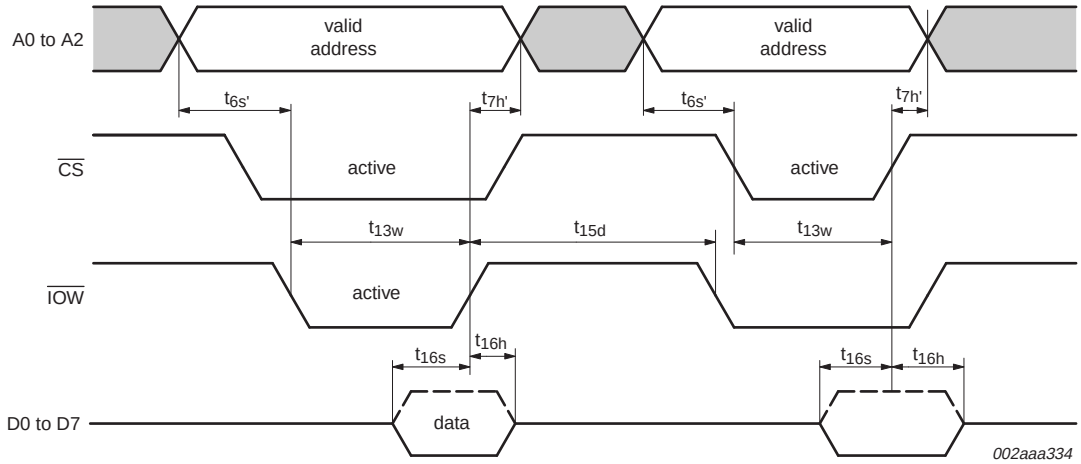



**Fig 11. General write timing when $\overline{AS}$ is tied to GND**

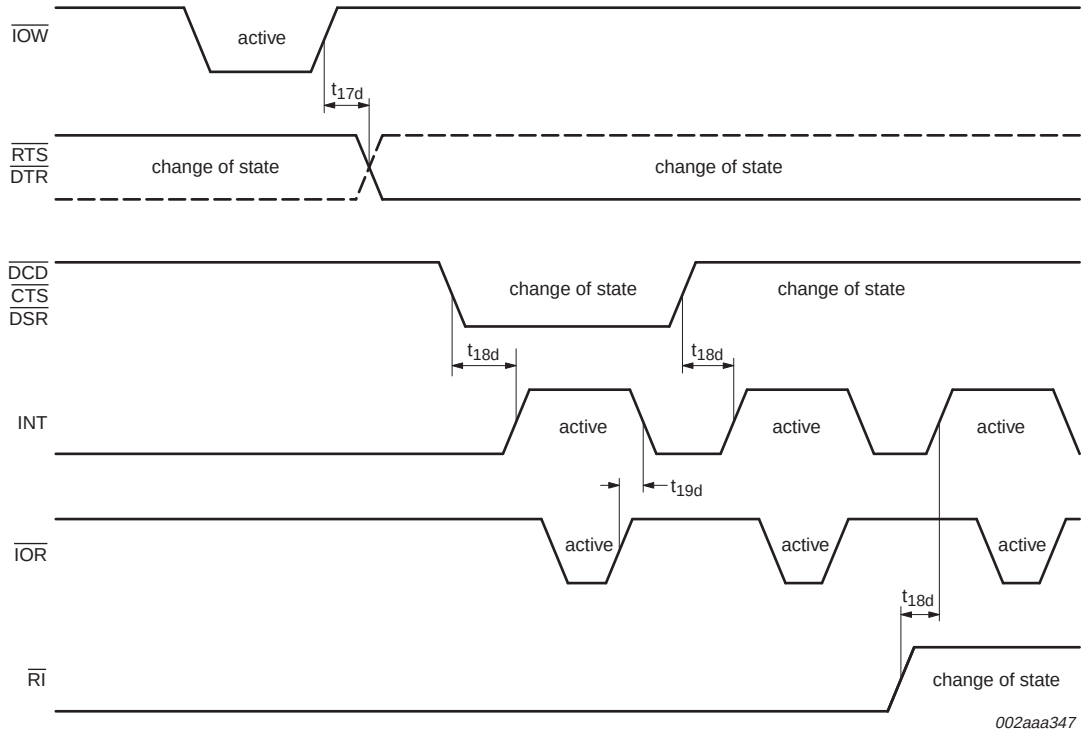
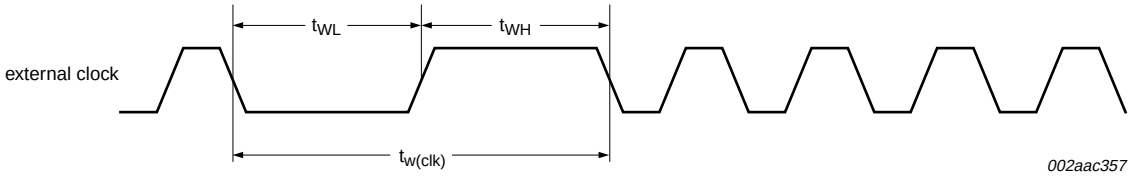



**Fig 12. Modem input/output timing**




$$f_{XTAL1} = \frac{1}{t_{w(clk)}}$$

**Fig 13. External clock timing**

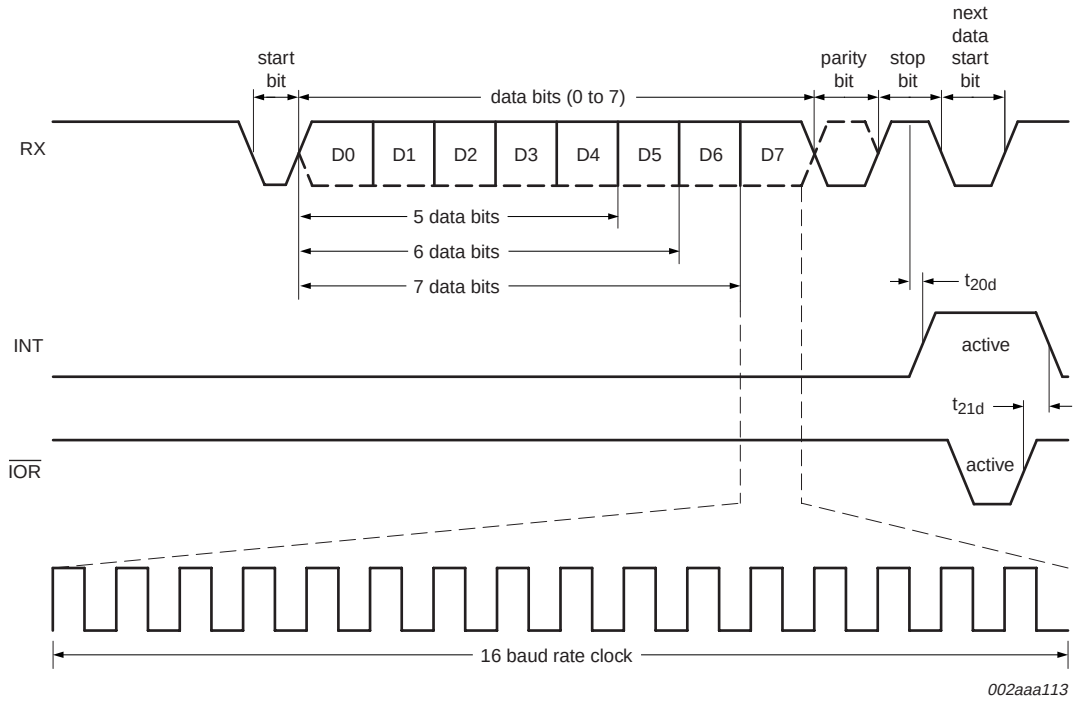



**Fig 14. Receive timing**

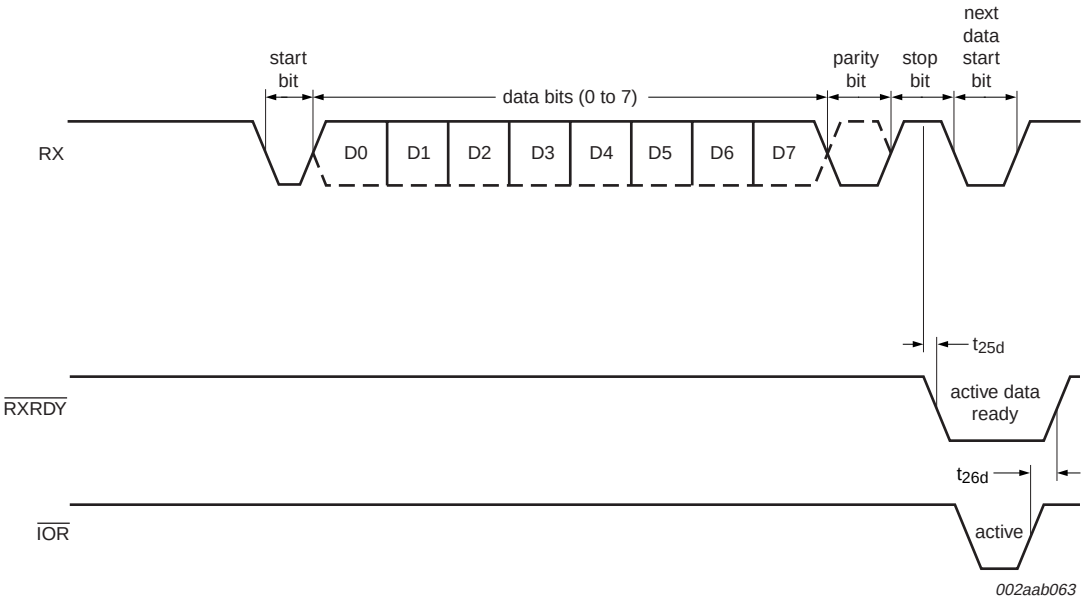



**Fig 15. Receive ready timing in non-FIFO mode**

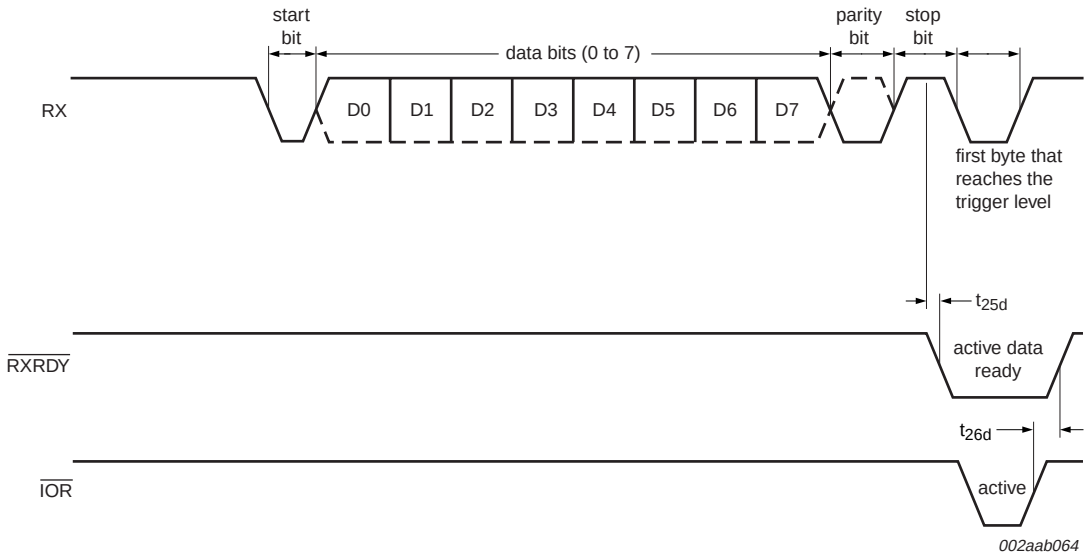



**Fig 16. Receive ready timing in FIFO mode**

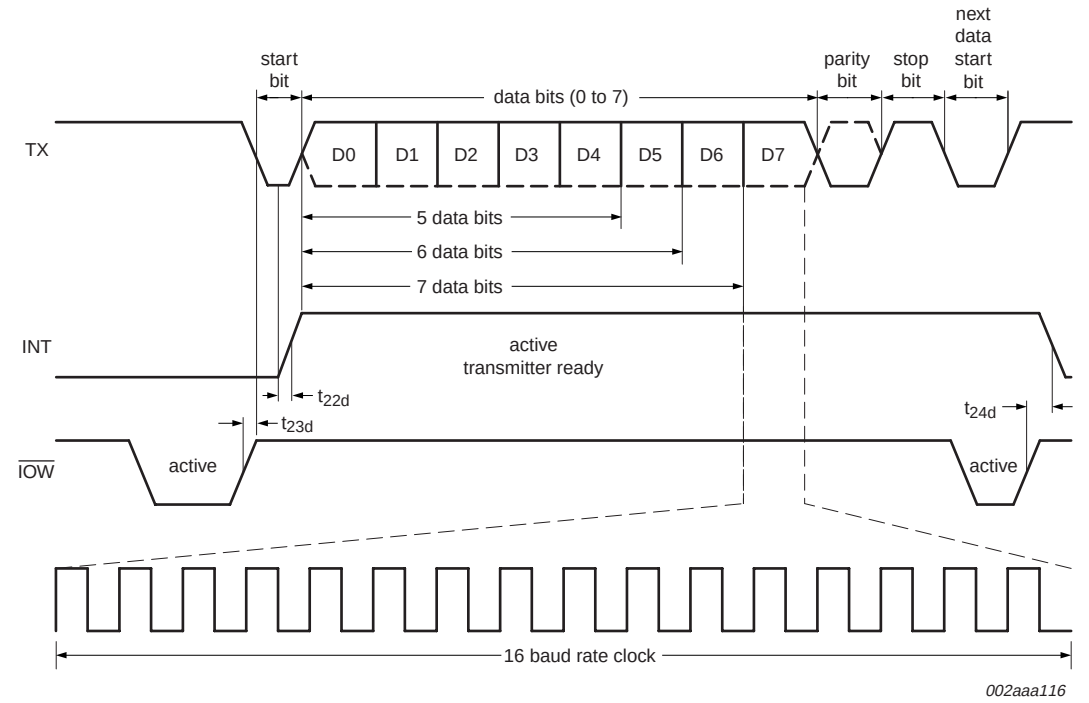



**Fig 17. Transmit timing**

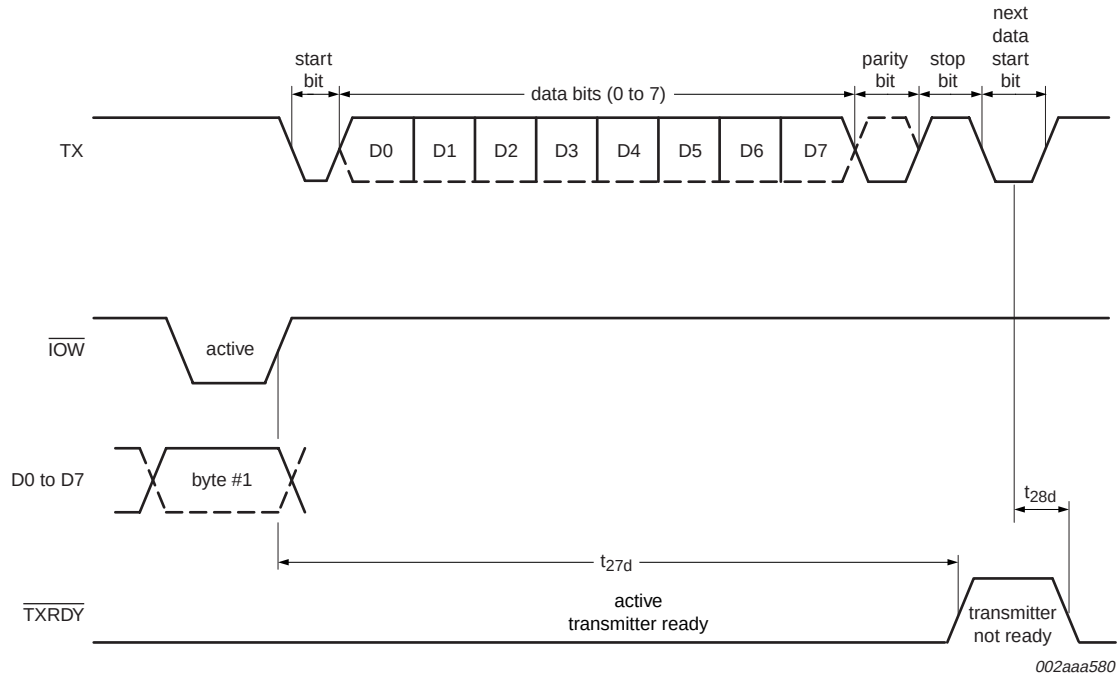



**Fig 18. Transmit ready timing in non-FIFO mode**

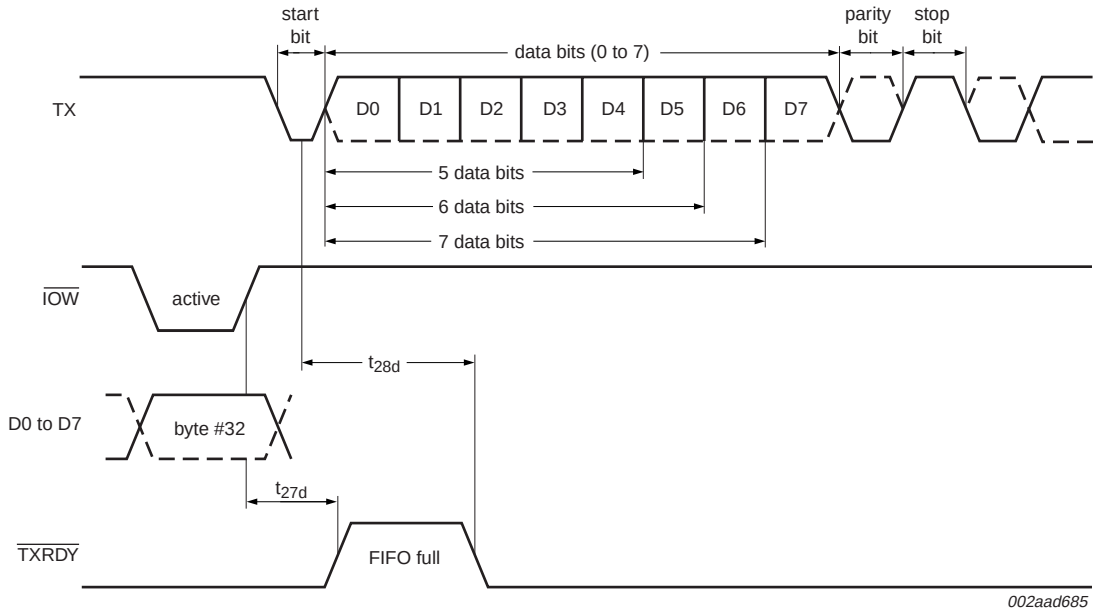



**Fig 19. Transmit ready timing in FIFO mode (DMA mode '1')**

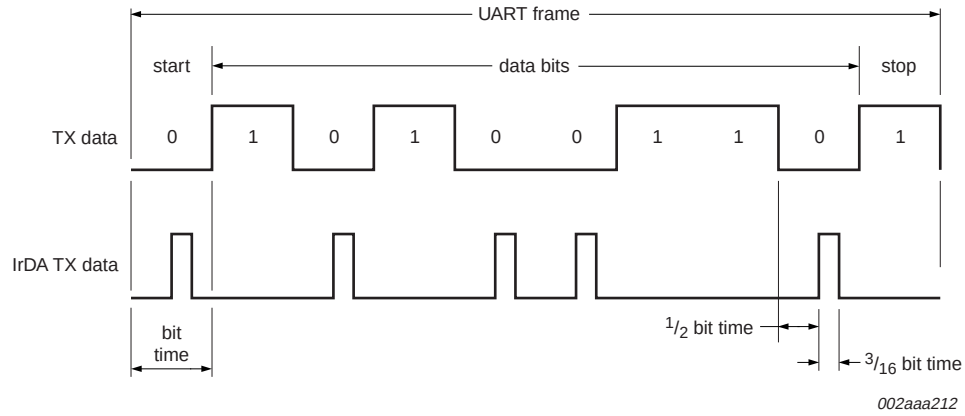



**Fig 20. Infrared transmit timing**

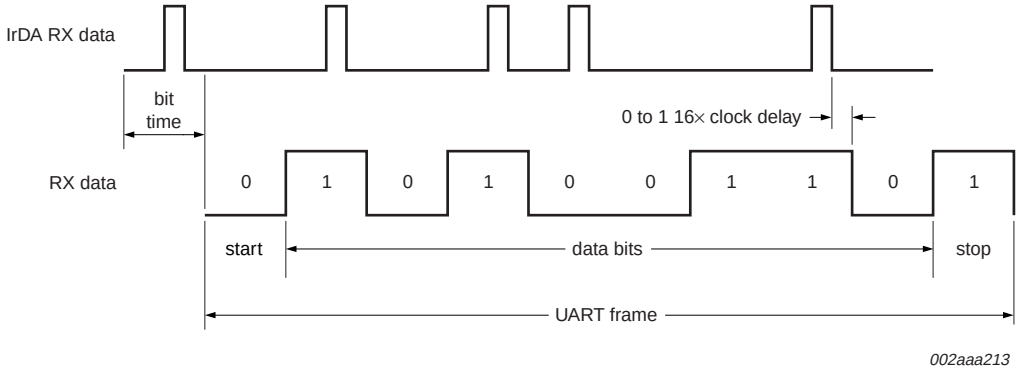
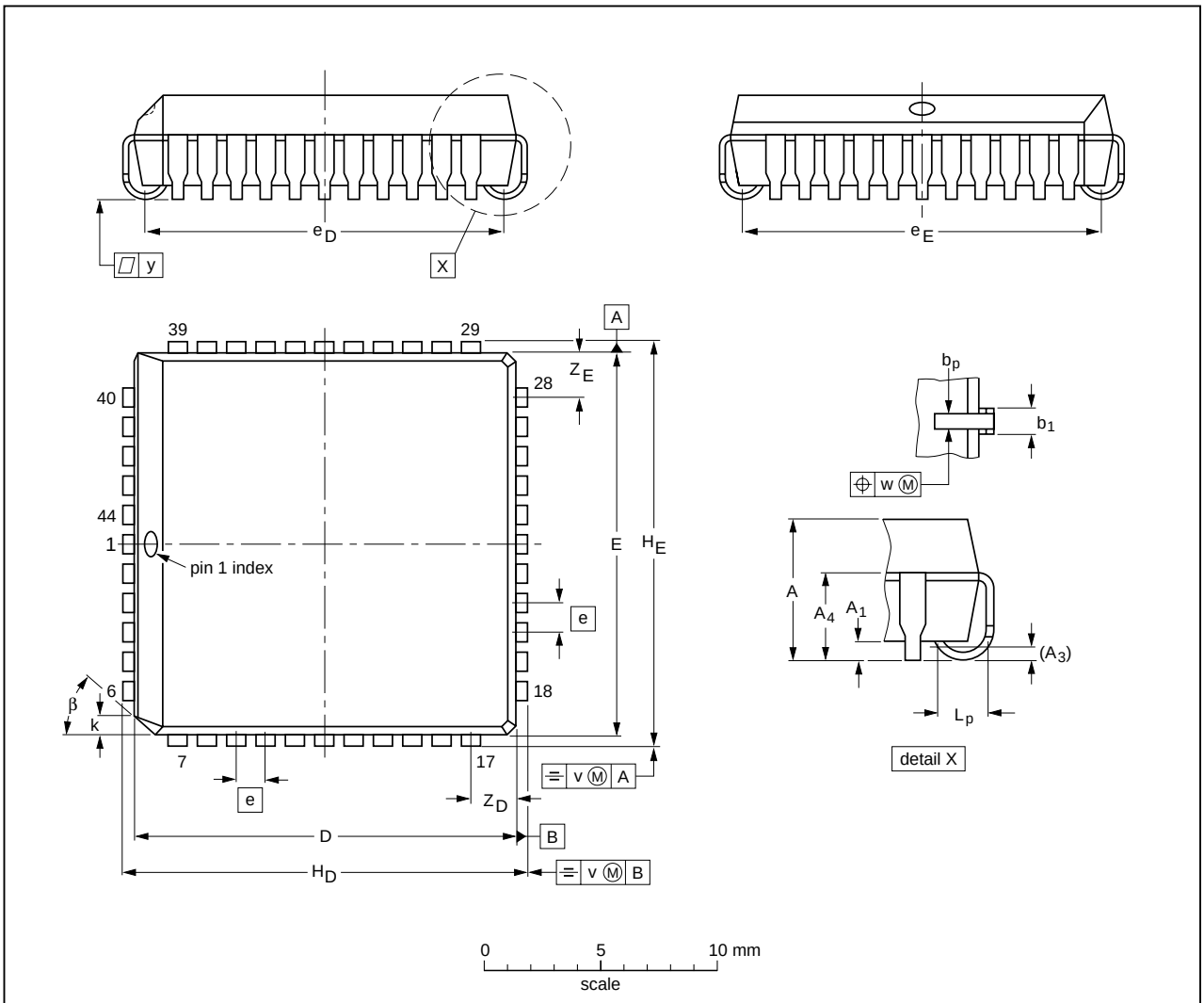



**Fig 21. Infrared receive timing**

# 11. Package outline

**PLCC44: plastic leaded chip carrier; 44 leads** **SOT187-2**




**DIMENSIONS (mm dimensions are derived from the original inch dimensions)**

| UNIT | A | $A_1$ min. | $A_3$ | $A_4$ max. | $b_p$ | $b_1$ | $D^{(1)}$ | $E^{(1)}$ | e | $e_D$ | $e_E$ | $H_D$ | $H_E$ | k | $L_p$ | v | w | y | $Z_D^{(1)}$ max. | $Z_E^{(1)}$ max. | β |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.57<br>4.19 | 0.51 | 0.25 | 3.05 | 0.53<br>0.33 | 0.81<br>0.66 | 16.66<br>16.51 | 16.66<br>16.51 | 1.27 | 16.00<br>14.99 | 16.00<br>14.99 | 17.65<br>17.40 | 17.65<br>17.40 | 1.22<br>1.07 | 1.44<br>1.02 | 0.18 | 0.18 | 0.1 | 2.16 | 2.16 | 45° |
| inches | 0.180<br>0.165 | 0.02 | 0.01 | 0.12 | 0.021<br>0.013 | 0.032<br>0.026 | 0.656<br>0.650 | 0.656<br>0.650 | 0.05 | 0.63<br>0.59 | 0.63<br>0.59 | 0.695<br>0.685 | 0.695<br>0.685 | 0.048<br>0.042 | 0.057<br>0.040 | 0.007 | 0.007 | 0.004 | 0.085 | 0.085 | |

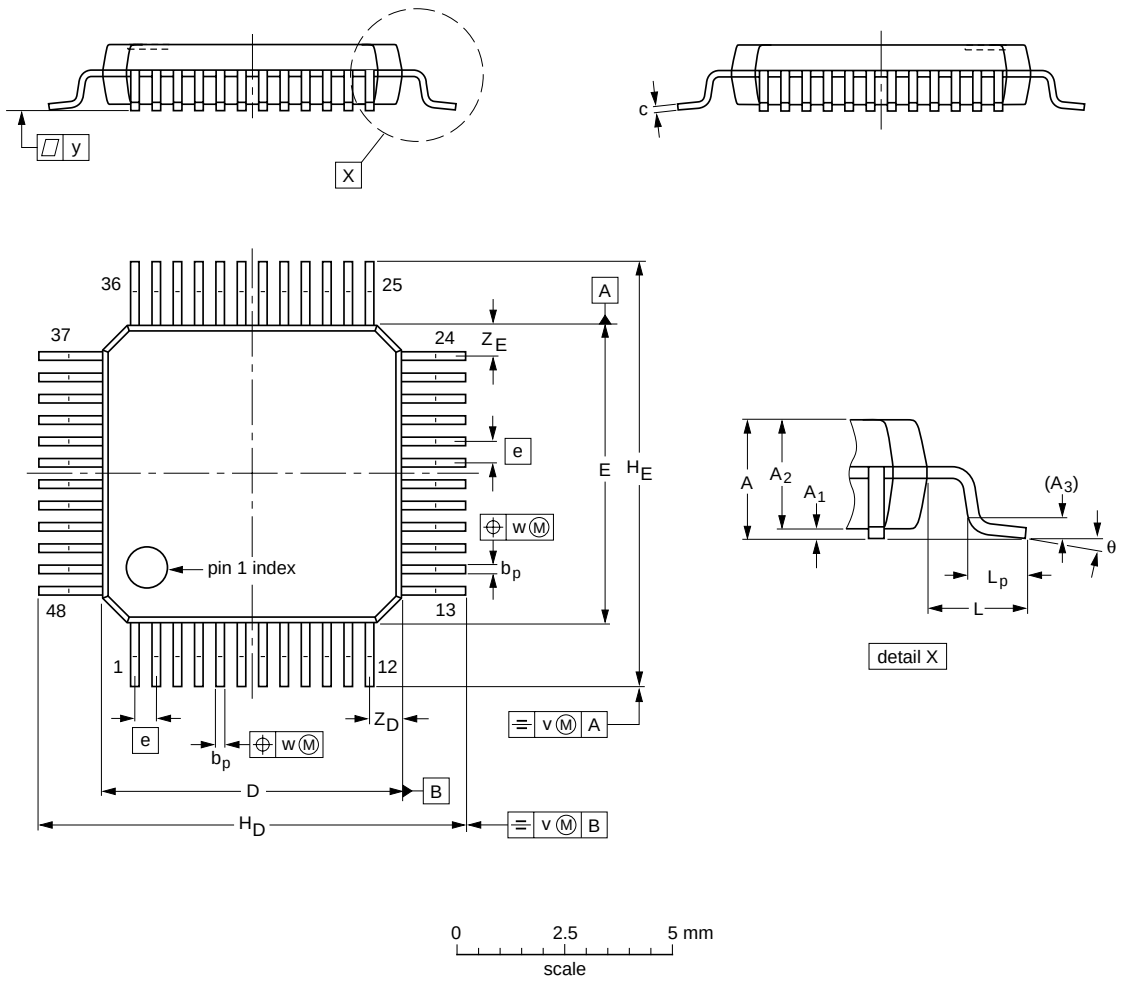
**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT187-2 | 112E10 | MS-018 | EDR-7319 | | | ~~99-12-27~~<br>01-11-14 |

**Fig 22. Package outline SOT187-2 (PLCC44)**

**LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm** **SOT313-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.6 | 0.20<br>0.05 | 1.45<br>1.35 | 0.25 | 0.27<br>0.17 | 0.18<br>0.12 | 7.1<br>6.9 | 7.1<br>6.9 | 0.5 | 9.15<br>8.85 | 9.15<br>8.85 | 1 | 0.75<br>0.45 | 0.2 | 0.12 | 0.1 | 0.95<br>0.55 | 0.95<br>0.55 | $7^o$<br>$0^o$ |

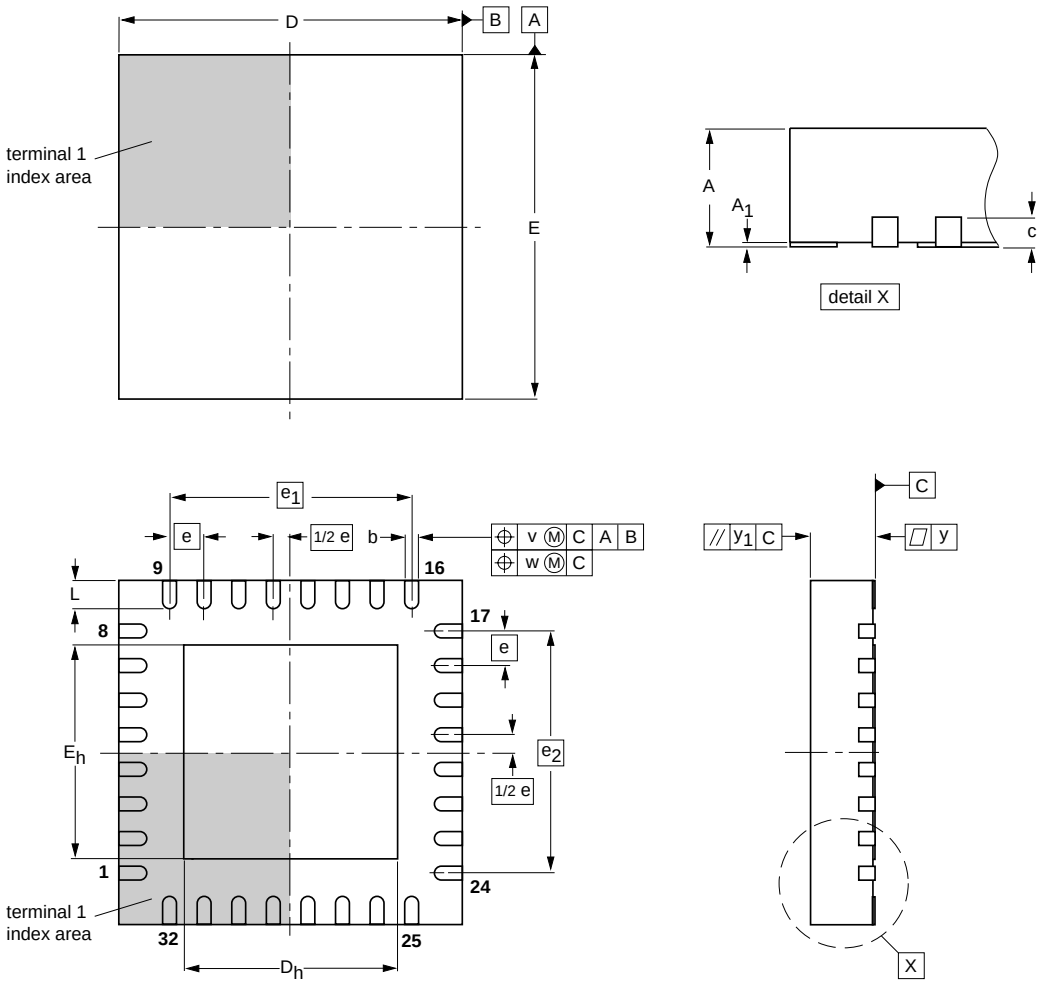
**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT313-2 | 136E05 | MS-026 | | | | ~~00-01-19~~<br>03-02-25 |

**Fig 23. Package outline SOT313-2 (LQFP48)**

**HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm** **SOT617-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max. | $A_1$ | b | c | D(1) | $D_h$ | E(1) | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 5.1<br>4.9 | 3.25<br>2.95 | 5.1<br>4.9 | 3.25<br>2.95 | 0.5 | 3.5 | 3.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT617-1 | - - - | MO-220 | - - - | | | ~~01-08-08~~<br>02-10-18 |

**Fig 24. Package outline SOT617-1 (HVQFN32)**

# 12. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 25) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 29 and 30

**Table 29. SnPb eutectic process (from J-STD-020C)**

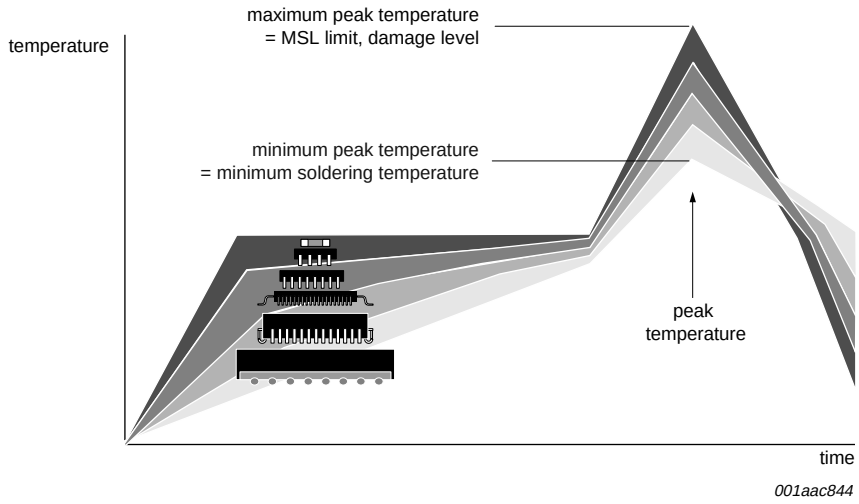
| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 30. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 25.




MSL: Moisture Sensitivity Level

**Fig 25. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 13. Abbreviations

**Table 31. Abbreviations**

| Acronym | Description |
|---|---|
| CPU | Central Processing Unit |
| DLL | Divisor Latch LSB |
| DLM | Divisor Latch MSB |
| DMA | Direct Memory Access |
| FIFO | First-In, First-Out |
| ISDN | Integrated Service Digital Network |
| LSB | Least Significant Bit |
| MSB | Most Significant Bit |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 32. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| SC16C650B_4 | 20090914 | Product data sheet | - | SC16C650B-03 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• DIP40 package option (type number SC16C650BIN40) removed | | | |

**Table 32. Revision history** *...continued*

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| Modifications: | • Section 2 “Features”, 3rd bullet: changed from “5 V tolerant inputs” to “5 V tolerant on input only pins”, and added Footnote 1.<br>• Table 2 “Pin description”:<br>– added (new) Table note [1] and its reference at HVQFN32 pin 13 (GND)<br>– Description for signal $\overline{DDIS}$ changed from “$\overline{DDIS}$ is active (LOW) when the CPU is not reading data. When active, $\overline{DDIS}$ can disable an external transceiver.” to “$\overline{DDIS}$ is active (LOW) when the CPU is reading data. When inactive (HIGH), $\overline{DDIS}$ can disable an external transceiver.”<br>• Section 6.8 “DMA operation”:<br>– 3rd sentence: changed from “... the state of the RXRDY and TXRDY output pins.” to “... the state of the $\overline{RXRDY}$ and $\overline{TXRDY}$ output pins.”<br>– added Remark<br>• Section 7 “Register descriptions”:<br>– first paragraph: changed from “... for the fifteen SC16C650B internal registers.” to “... for the seventeen SC16C650B internal registers.”<br>• Table 8 “SC16C650B internal registers”:<br>– descriptive text below table title moved to (new) Table note [3]<br>– removed shading from 9 table cells; added reference to Table note [3]<br>– deleted reference to Table note [4] at MCR[2]<br>– Table note [4] changed from “These functions are not supported ...” to “This function is not supported ...”<br>– added (new) Table note [5] and its reference at MCR[3]<br>– added (new) Table note [6] and its reference at FCR[3] and MCR[2]<br>– MCR bit 2 changed from “$\overline{OUT1}$” to “$\overline{OUT1}$, $\overline{OUT}$”<br>– MCR bit 3 changed from “$\overline{OUT2}$, INT enable” to “$\overline{OUT2}$”<br>• Table 19 “Modem Control Register bits description”:<br>– description of MCR[5]: removed references to IRQA pin<br>– description of MCR[5]: logic 0: changed from “enable active or 3-State interrupt output mode” to “enable interrupt output mode”<br>– description of MCR[5]: logic 1, second sentence changed from “Provides shared interrupts in the STD mode by producing ...” to “Provides shared interrupts by producing ...”<br>– description of MCR[3] re-written<br>– description of MCR[2] re-written<br>• Table 25 “Reset state for outputs”: deleted “(STD mode)” from the Reset state column for $\overline{RXRDY}$, $\overline{TXRDY}$ and INT outputs<br>• Table 26 “Limiting values”:<br>– parameter description for symbol $V_n$ changed from “voltage at any pin” to “voltage on any other pin”; added separate conditions for “at D7 to D0” and “at any input only pin”<br>– parameter description for symbol $T_{amb}$ changed from “operating temperature” to “ambient temperature”; added condition “operating in free air”<br>– symbol for ‘total power dissipation per package” changed from “$P_{tot(pack)}$” to “$P_{tot}$/pack” | | | |

**Table 32. Revision history** *...continued*

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| Modifications: (continued) | • Table 27 “Static characteristics”:<br>– table title changed (was “DC electrical characteristics”)<br>– descriptive text below table title changed from “$V_{CC}$ = 2.5 V, 3.3 V or 5.0 V ±10%” to “tolerance of $V_{CC}$ ± 10 %”<br>– symbol “$V_{IL(CK)}$” changed to “$V_{IL(clk)}$”<br>– symbol “$V_{IH(CK)}$” changed to “$V_{IH(clk)}$”<br>– parameter description for $V_{OL}$: moved “on all outputs” to Conditions column<br>– symbol/parameter “$I_{CL}$, clock leakage” changed to “$I_{L(clk)}$, clock leakage current”<br>– symbol/parameter “$I_{CC}$, average power supply current” changed to “$I_{CC(AV)}$, average supply current”<br>– added $I_{CC(sleep)}$ specification<br>– Table note [1]: changed “$x_2$” to “XTAL2”<br>– (old) Table note [2] deleted (and its reference at $R_{pu(int)}$)<br>– added (new) Table note [2] and its reference at $I_{CC(sleep)}$<br>• Table 28 “Dynamic characteristics”:<br>– table title changed (was “AC electrical characteristics”<br>– descriptive text below table title changed from “$V_{CC}$ = 2.5 V, 3.3 V or 5.0 V ±10%” to “tolerance of $V_{CC}$ ± 10 %”<br>– symbol “$t_{1w}$, $t_{2w}$, clock pulse duration” is split into two parameters “$t_{WH}$, pulse width HIGH” and “$t_{WL}$, pulse width LOW”<br>– symbol “$t_{3w}$, oscillator/clock frequency” changed to “$f_{XTAL1}$, frequency on pin XTAL1”<br>– symbols $t_{20d}$, $t_{23d}$, $t_{25d}$, $t_{28d}$: unit changed from “$R_{clk}$” to “s”; values are appended with “$T_{RCLK}$” and referenced to (new) Table note [3]<br>– parameter description for $t_{RESET}$ changed from “Reset pulse width” to “RESET pulse width”; added reference to (new) Table note [4]<br>– unit for parameter “baud rate divisor”: deleted “$R_{clk}$” (N is a number)<br>• Figure 13 “External clock timing”:<br>– symbol changed from “$t_{1w}$” to “$t_{WH}$”<br>– symbol changed from “$t_{2w}$” to “$t_{WL}$”<br>– symbol changed from “$t_{3w}$” to “$t_{w(clk)}$”<br>– added equation<br>• Figure 15, Figure 16, Figure 18, Figure 19: changed from “DATA BITS (5-8)” to “data bits (0 to 7)”<br>• Figure 19: in waveform for signals D0 to D7, changed “BYTE #16” to “byte #32” | | | |
| SC16C650B-03 (9397 750 14451) | 20041210 | Product data | - | SC16C650B-02 |
| Modifications: | • There is no modification to the data sheet. However, reader is advised to refer to *AN10333 (Rev. 02) “SC16CXXXB baud rate deviation tolerance” (9397 750 14411)* that was released together with this revision. | | | |
| SC16C650B-02 (9397 750 13317) | 20040603 | Product data | - | SC16C650B-01 |
| SC16C650B-01 (9397 750 11994) | 20040330 | Product data | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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