# ADD-A-PAK Generation VII Power Modules Thyristor/Diode and Thyristor/Thyristor, 45 A/60 A

ADD-A-PAK

| PRODUCT SUMMARY | |
|---|---|
| $I_{T(AV)}$ or $I_{F(AV)}$ | 45 A/60 A |
| Type | Modules - Thyristor, Standard |

## FEATURES

- High voltage
- Industrial standard package
- Low thermal resistance
- UL approved file E78996
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

## BENEFITS

- Excellent thermal performances obtained by the usage of exposed direct bonded copper substrate
- Up to 1600 V
- High surge capability
- Easy mounting on heatsink

## MECHANICAL DESCRIPTION

The ADD-A-PAK generation VII, new generation of ADD-A-PAK module, combines the excellent thermal performances obtained by the usage of exposed direct bonded copper substrate, with advanced compact simple package solution and simplified internal structure with minimized number of interfaces.

## ELECTRICAL DESCRIPTION

These modules are intended for general purpose high voltage applications such as high voltage regulated power supplies, lighting circuits, temperature and motor speed control circuits, UPS, and battery charger.

| MAJOR RATINGS AND CHARACTERISTICS | | | | |
|---|---|---|---|---|
| SYMBOL | CHARACTERISTICS | VS-VSK.41 | VS-VSK.56 | UNITS |
| $I_{T(AV)}$ or $I_{F(AV)}$ | 85 °C | 45 | 60 | A |
| $I_{O(RMS)}$ | As AC switch | 100 | 135 | |
| $I_{TSM}$, $I_{FSM}$ | 50 Hz | 850 | 1200 | |
| | 60 Hz | 890 | 1256 | |
| $I^2t$ | 50 Hz | 3.61 | 7.20 | $kA^2s$ |
| | 60 Hz | 3.30 | 6.57 | |
| $I^2\sqrt{t}$ | | 36.1 | 72 | $kA^2\sqrt{s}$ |
| $V_{RRM}$ | Range | 400 to 1600 | 400 to 1600 | V |
| $T_{Stg}$ | | -40 to 125 | | °C |
| $T_J$ | | -40 to 125 | | °C |



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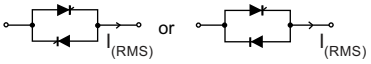
## ELECTRICAL SPECIFICATIONS

### VOLTAGE RATINGS

| TYPE NUMBER | VOLTAGE CODE | $V_{RRM}$, MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V | $V_{RSM}$, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V | $V_{DRM}$, MAXIMUM REPETITIVE PEAK OFF-STATE VOLTAGE, GATE OPEN CIRCUIT V | $I_{RRM}$, $I_{DRM}$ AT 125 °C mA |
|---|---|---|---|---|---|
| VS-VSK.41<br>VS-VSK.56 | 04 | 400 | 500 | 400 | 15 |
| | 06 | 600 | 700 | 600 | |
| | 08 | 800 | 900 | 800 | |
| | 10 | 1000 | 1100 | 1000 | |
| | 12 | 1200 | 1300 | 1200 | |
| | 14 | 1400 | 1500 | 1400 | |
| | 16 | 1600 | 1700 | 1600 | |

### ON-STATE CONDUCTION

| PARAMETER | SYMBOL | TEST CONDITIONS | | | VSK.41 | VSK.56 | UNITS |
|---|---|---|---|---|---|---|---|
| Maximum average on-state current (thyristors) | $I_{T(AV)}$ | 180° conduction, half sine wave, $T_C$ = 85 °C | | | 45 | 60 | A |
| Maximum average forward current (diodes) | $I_{F(AV)}$ | | | | | | |
| Maximum continuous RMS on-state current, as AC switch | $I_{O(RMS)}$ |  | | | 100 | 135 | |
| Maximum peak, one-cycle non-repetitive on-state or forward current | $I_{TSM}$ or $I_{FSM}$ | t = 10 ms | No voltage reapplied | Sinusoidal half wave, initial $T_J$ = $T_J$ maximum | 850 | 1200 | |
| | | t = 8.3 ms | | | 890 | 1256 | |
| | | t = 10 ms | 100 % $V_{RRM}$ reapplied | | 715 | 1000 | |
| | | t = 8.3 ms | | | 750 | 1056 | |
| Maximum $I^2t$ for fusing | $I^2t$ | t = 10 ms | No voltage reapplied | Initial $T_J$ = $T_J$ maximum | 3.61 | 7.20 | $kA^2s$ |
| | | t = 8.3 ms | | | 3.30 | 6.57 | |
| | | t = 10 ms | 100 % $V_{RRM}$ reapplied | | 2.56 | 5.10 | |
| | | t = 8.3 ms | | | 2.33 | 4.56 | |
| Maximum $I^2\sqrt{t}$ for fusing | $I^2\sqrt{t}$ (1) | t = 0.1 ms to 10 ms, no voltage reapplied<br>$T_J$ = $T_J$ maximum | | | 36.1 | 72 | $kA^2\sqrt{s}$ |
| Maximum value or threshold voltage | $V_{T(TO)}$ (2) | Low level (3) | $T_J$ = $T_J$ maximum | | 1.08 | 0.91 | V |
| | | High level (4) | | | 1.12 | 1.02 | |
| Maximum value of on-state slope resistance | $r_t$ (2) | Low level (3) | $T_J$ = $T_J$ maximum | | 4.7 | 4.27 | mΩ |
| | | High level (4) | | | 4.5 | 3.77 | |
| Maximum peak on-state or forward voltage | $V_{TM}$ | $I_{TM} = \pi \times I_{T(AV)}$ | $T_J$ = 25 °C | | 1.81 | 1.7 | V |
| | $V_{FM}$ | $I_{FM} = \pi \times I_{F(AV)}$ | | | | | |
| Maximum non-repetitive rate of rise of turned on current | dI/dt | $T_J$ = 25 °C, from 0.67 $V_{DRM}$,<br>$I_{TM} = \pi \times I_{T(AV)}$, $I_g$ = 500 mA, $t_r$ < 0.5 µs, $t_p$ > 6 µs | | | 150 | | A/µs |
| Maximum holding current | $I_H$ | $T_J$ = 25 °C, anode supply = 6 V,<br>resistive load, gate open circuit | | | 200 | | mA |
| Maximum latching current | $I_L$ | $T_J$ = 25 °C, anode supply = 6 V, resistive load | | | 400 | 400 | |

**Notes**

(1) $I^2t$ for time $t_x = I^2\sqrt{t} \times \sqrt{t_x}$

(2) Average power = $V_{T(TO)} \times I_{T(AV)} + r_t \times (I_{T(RMS)})^2$

(3) 16.7 % x π x $I_{AV}$ < I < π x $I_{AV}$

(4) I > π x $I_{AV}$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## TRIGGERING

| PARAMETER | SYMBOL | TEST CONDITIONS | | VS-VSK.41 | VS-VSK.56 | UNITS |
|---|---|---|---|---|---|---|
| Maximum peak gate power | $P_{GM}$ | | | 10 | | W |
| Maximum average gate power | $P_{G(AV)}$ | | | 2.5 | | |
| Maximum peak gate current | $I_{GM}$ | | | 2.5 | | A |
| Maximum peak negative gate voltage | - $V_{GM}$ | | | 10 | | V |
| Maximum gate voltage required to trigger | $V_{GT}$ | $T_J$ = -40 °C | Anode supply = 6 V resistive load | 4.0 | | |
| | | $T_J$ = 25 °C | | 2.5 | | |
| | | $T_J$ = 125 °C | | 1.7 | | |
| Maximum gate current required to trigger | $I_{GT}$ | $T_J$ = -40 °C | Anode supply = 6 V resistive load | 270 | | mA |
| | | $T_J$ = 25 °C | | 150 | | |
| | | $T_J$ = 125 °C | | 80 | | |
| Maximum gate voltage that will not trigger | $V_{GD}$ | $T_J$ = 125 °C, rated $V_{DRM}$ applied | | 0.25 | | V |
| Maximum gate current that will not trigger | $I_{GD}$ | $T_J$ = 125 °C, rated $V_{DRM}$ applied | | 6 | | mA |

## BLOCKING

| PARAMETER | SYMBOL | TEST CONDITIONS | VS-VSK.41 | VS-VSK.56 | UNITS |
|---|---|---|---|---|---|
| Maximum peak reverse and off-state leakage current at $V_{RRM}$, $V_{DRM}$ | $I_{RRM}$, $I_{DRM}$ | $T_J$ = 125 °C, gate open circuit | 15 | | mA |
| Maximum RMS insulation voltage | $V_{INS}$ | 50 Hz | 3000 (1 min)<br>3600 (1 s) | | V |
| Maximum critical rate of rise of off-state voltage | dV/dt | $T_J$ = 125 °C, linear to 0.67 $V_{DRM}$ | 1000 | | V/µs |

## THERMAL AND MECHANICAL SPECIFICATIONS

| PARAMETER | | SYMBOL | TEST CONDITIONS | VS-VSK.41 | VS-VSK.56 | UNITS |
|---|---|---|---|---|---|---|
| Junction operating and storage temperature range | | $T_J$, $T_{Stg}$ | | -40 to 125 | | °C |
| Maximum internal thermal resistance, junction to case per leg | | $R_{thJC}$ | DC operation | 0.44 | 0.35 | °C/W |
| Typical thermal resistance, case to heatsink per module | | $R_{thCS}$ | Mounting surface flat, smooth and greased | 0.1 | | |
| Mounting torque ± 10 % | to heatsink | | A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound. | 4 | | Nm |
| | busbar | | | 3 | | |
| Approximate weight | | | | 75 | | g |
| | | | | 2.7 | | oz. |
| Case style | | | JEDEC® | AAP GEN VII (TO-240AA) | | |

## ΔR CONDUCTION PER JUNCTION

| DEVICES | SINE HALF WAVE CONDUCTION | | | | | RECTANGULAR WAVE CONDUCTION | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 180° | 120° | 90° | 60° | 30° | 180° | 120° | 90° | 60° | 30° | |
| VSK.41.. | 0.110 | 0.131 | 0.17 | 0.23 | 0.342 | 0.085 | 0.138 | 0.177 | 0.235 | 0.345 | °C/W |
| VSK.56.. | 0.088 | 0.104 | 0.134 | 0.184 | 0.273 | 0.07 | 0.111 | 0.143 | 0.189 | 0.275 | |

**Note**

- Table shows the increment of thermal resistance $R_{thJC}$ when devices operate at different conduction angles than DC


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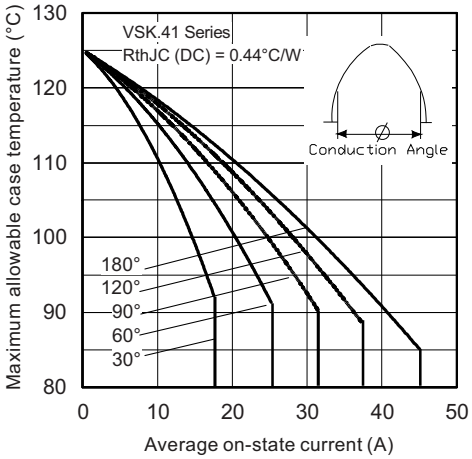


Fig. 1 - Current Ratings Characteristics

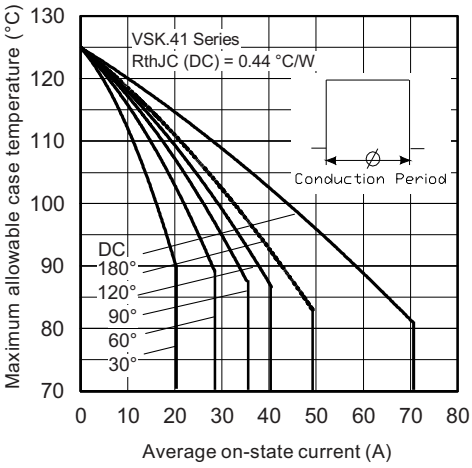


Fig. 2 - Current Ratings Characteristics

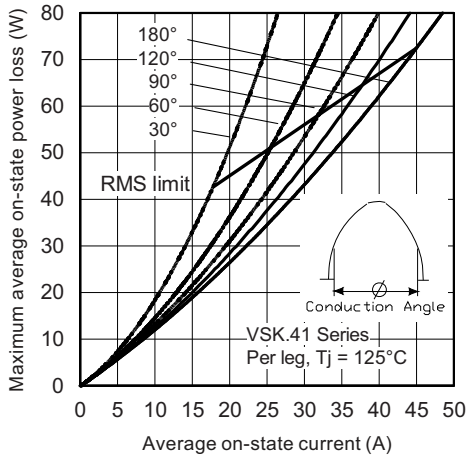


Fig. 3 - On-State Power Loss Characteristics

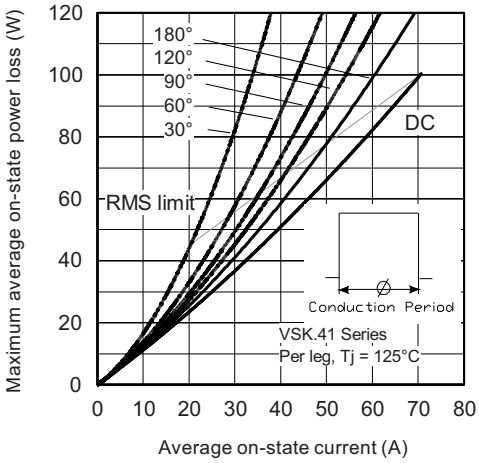


Fig. 4 - On-State Power Loss Characteristics

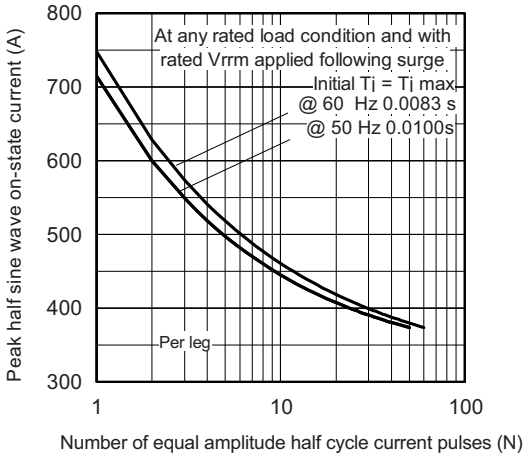


Fig. 5 - Maximum Non-Repetitive Surge Current

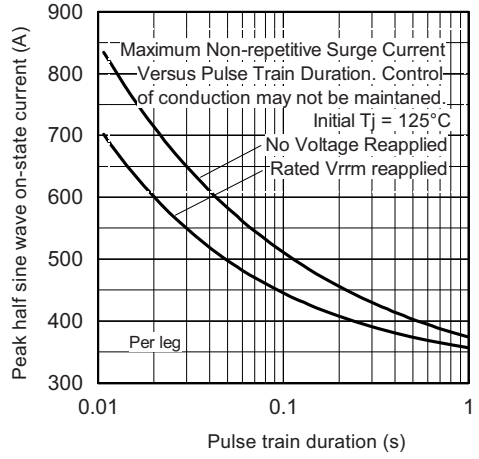


Fig. 6 - Maximum Non-Repetitive Surge Current


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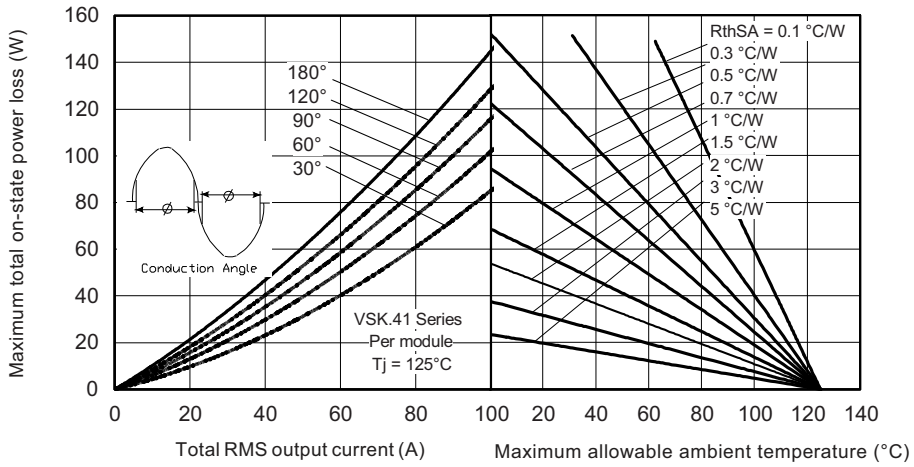


Fig. 7 - On-State Power Loss Characteristics

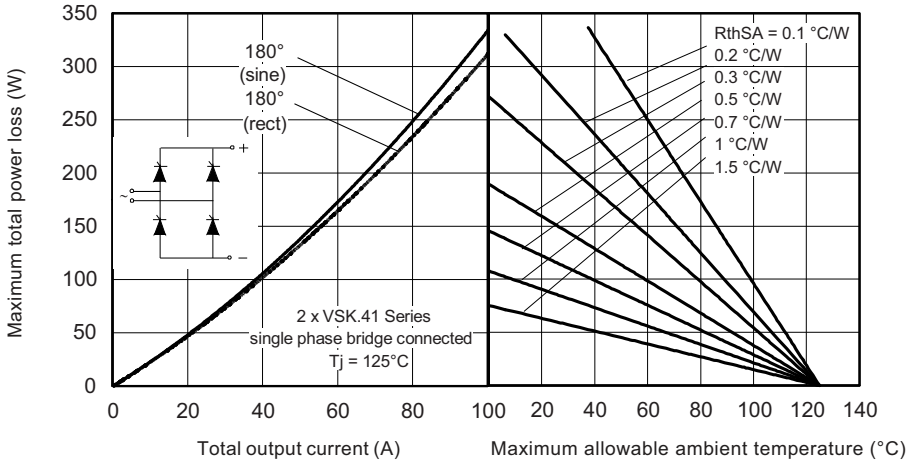


Fig. 8 - On-State Power Loss Characteristics

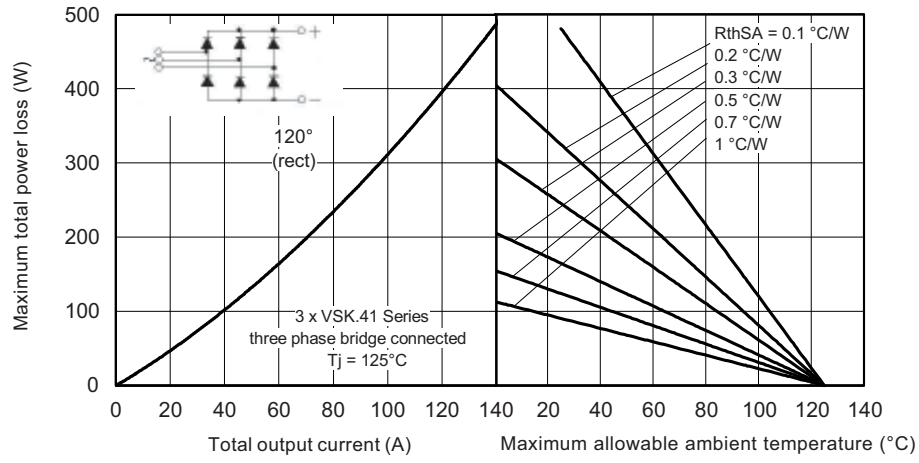


Fig. 9 - On-State Power Loss Characteristics


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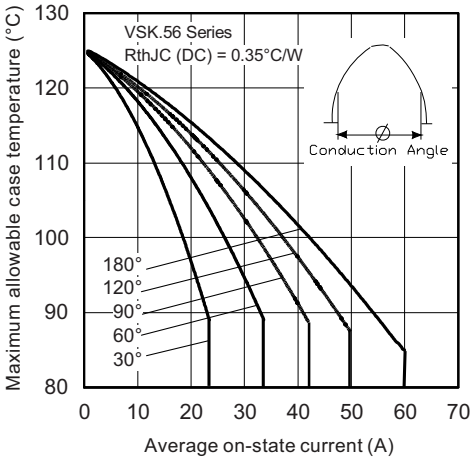


Fig. 10 - Current Ratings Characteristics

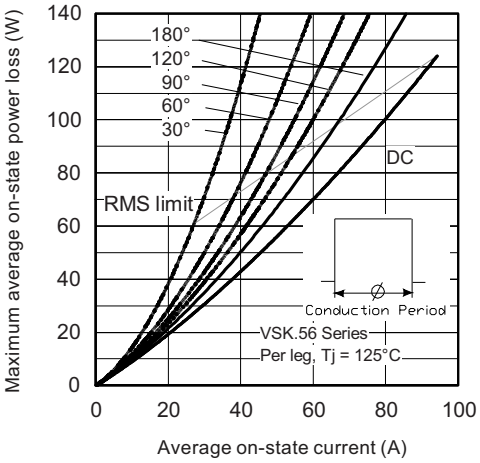


Fig. 13 - On-State Power Loss Characteristics

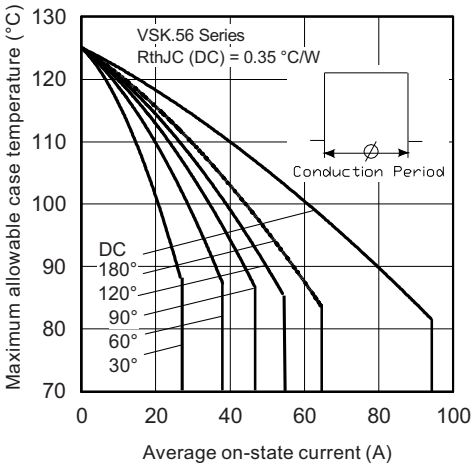


Fig. 11 - Current Ratings Characteristics

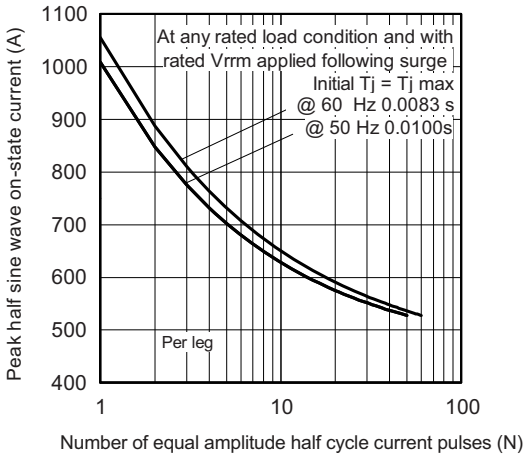


Fig. 14 - Maximum Non-Repetitive Surge Current

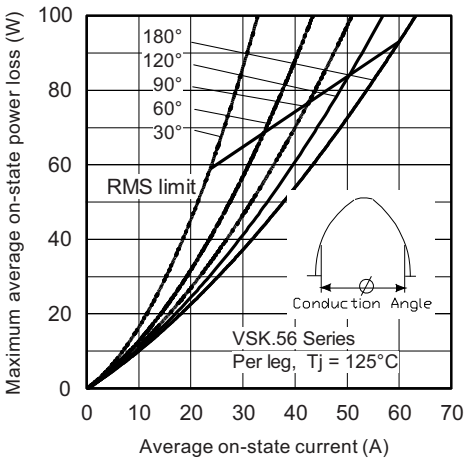


Fig. 12 - On-State Power Loss Characteristics

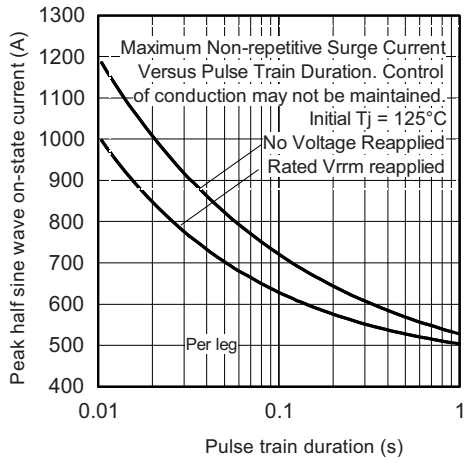


Fig. 15 - Maximum Non-Repetitive Surge Current


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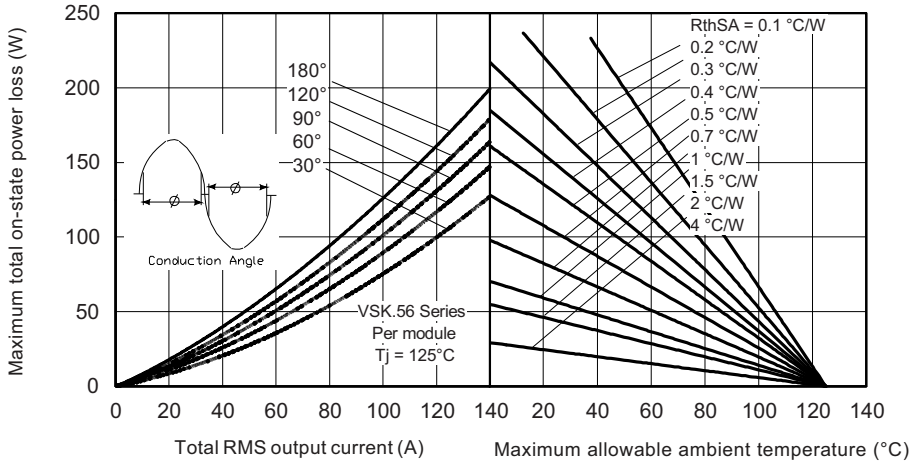


Fig. 16 - On-State Power Loss Characteristics

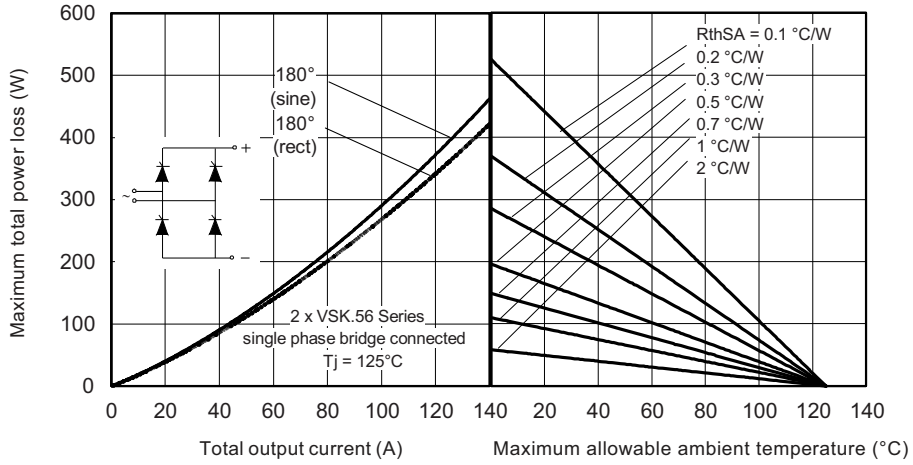


Fig. 17 - On-State Power Loss Characteristics

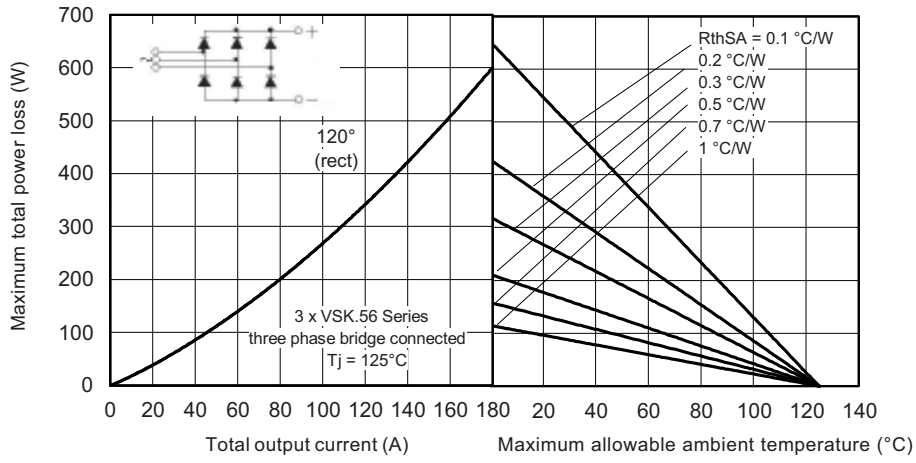


Fig. 18 - On-State Power Loss Characteristics


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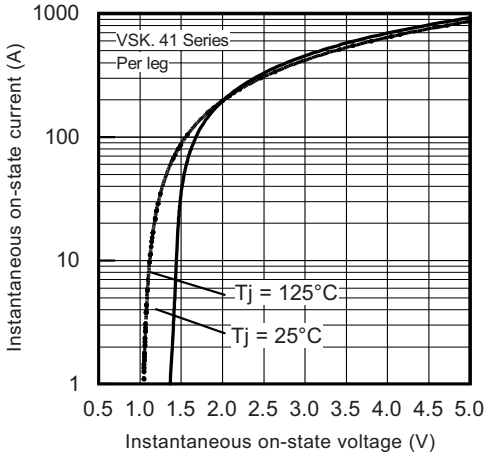


Fig. 19 - On-State Voltage Drop Characteristics

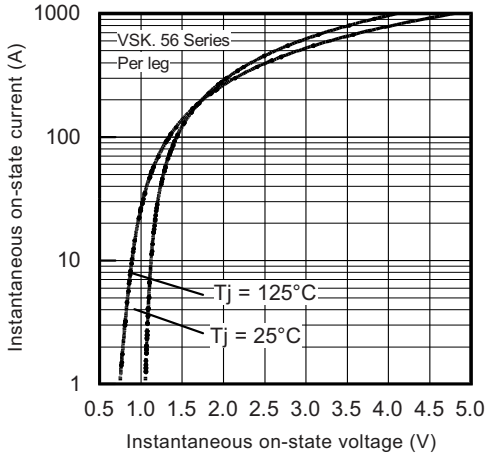


Fig. 20 - On-State Voltage Drop Characteristics

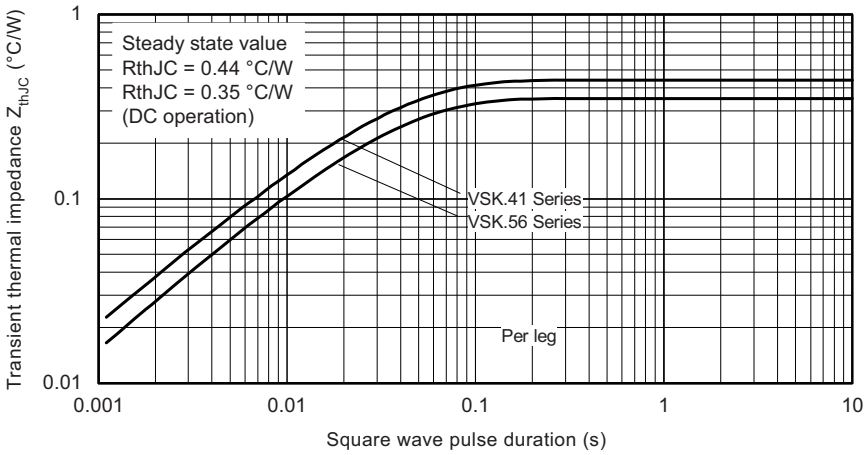


Fig. 21 - Thermal Impedance $Z_{thJC}$ Characteristics

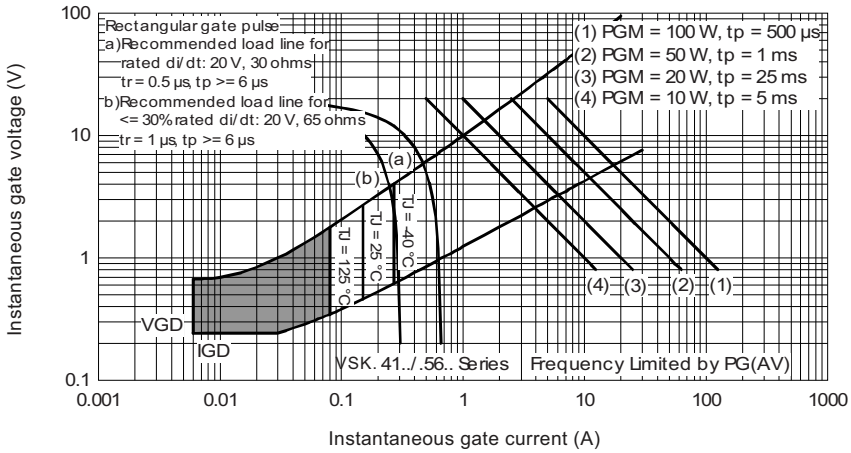


Fig. 22 - Gate Characteristics


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## ORDERING INFORMATION TABLE

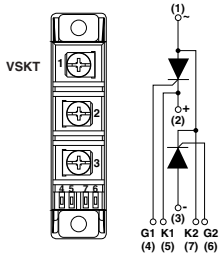
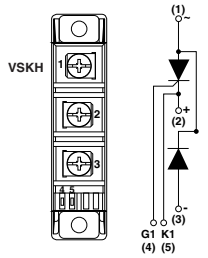
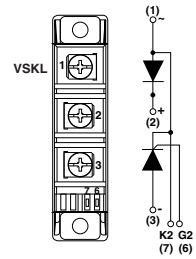
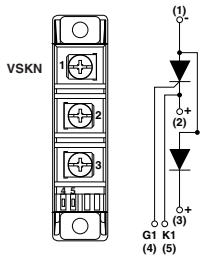
| Device code | VS-VS | K | T | 56 | / | 16 |
|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | | 5 |

1 - Vishay Semiconductors product
2 - Module type
3 - Circuit configuration (see Circuit configuration table)
4 - Current code — 41 = 45 A, 56 = 60 A
5 - Voltage code (see Voltage Ratings table)

**Note**

- To order the optional hardware go to www.vishay.com/doc?95172

## CIRCUIT CONFIGURATION

| CIRCUIT DESCRIPTION | CIRCUIT CONFIGURATION CODE | CIRCUIT DRAWING |
|---|---|---|
| Two SCRs doubler circuit | T |   |
| SCR/diode doubler circuit, positive control | H |   |
| SCR/diode doubler circuit, negative control | L |   |
| SCR/diode common anodes | N |   |

| LINKS TO RELATED DOCUMENTS | |
|---|---|
| Dimensions | www.vishay.com/doc?95368 |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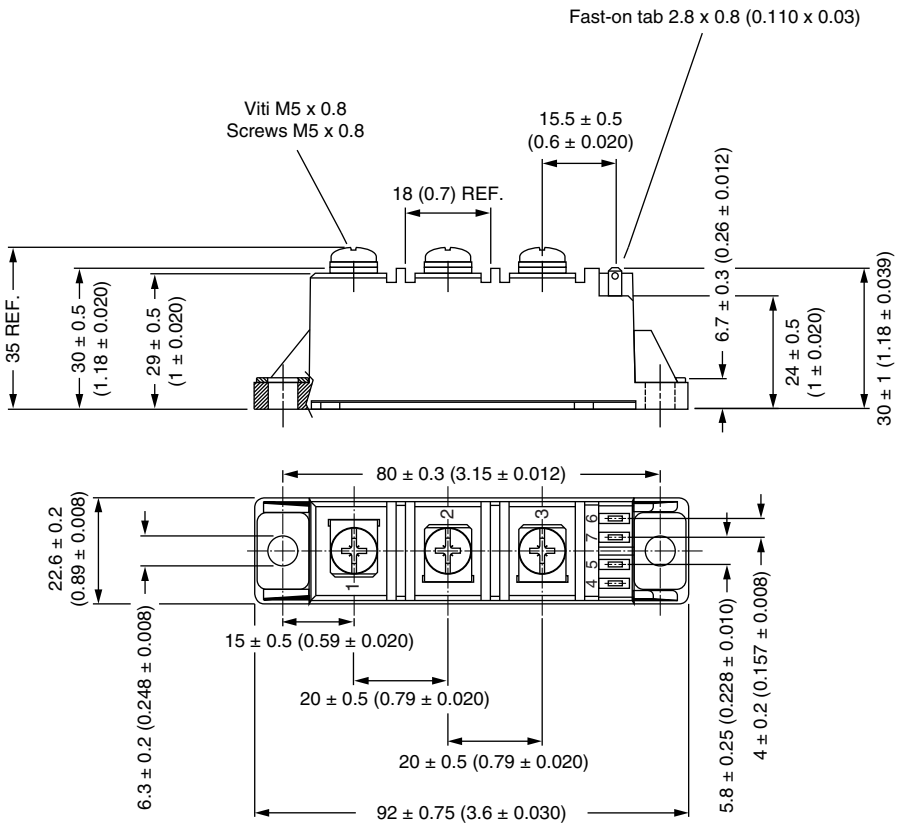
# ADD-A-PAK Generation VII - Thyristor

**DIMENSIONS** in millimeters (inches)



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**Наши контакты:**

**Телефон:** +7 812 627 14 35

**Электронная почта:** sales@st-electron.ru

**Адрес:** 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331