

# MC10LVEP16, MC100LVEP16

## 2.5V / 3.3V ECL Differential Receiver/Driver

### Description

The MC10/100LVEP16 is a world class differential receiver/driver. The device is functionally equivalent to the EL16, EP16 and LVEL16 devices. With output transition times significantly faster than the EL16 and LVEL16, the LVEP16 is ideally suited for interfacing with high frequency and low voltage (2.5 V) sources. Single-ended CLK input operation is limited to a  $V_{CC} \geq 3.0$  V in PECL mode, or  $V_{EE} \leq -3.0$  V in NECL mode.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The 100 Series contains temperature compensation.

### Features

- 240 ps Propagation Delay
- Maximum Frequency > 4 GHz Typical
- PECL Mode Operating Range:  $V_{CC} = 2.375$  V to 3.8 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  $V_{CC} = 0$  V with  $V_{EE} = -2.375$  V to  $-3.8$  V
- $V_{BB}$  Output
- Open Input Default State
- LVDS Input Compatible
- Pb-Free Packages are Available



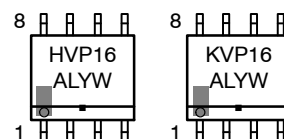
ON Semiconductor®

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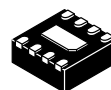
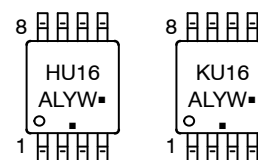
### MARKING DIAGRAMS\*



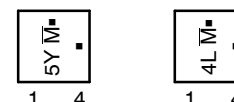
SOIC-8  
D SUFFIX  
CASE 751



TSSOP-8  
DT SUFFIX  
CASE 948R



DFN8  
MN SUFFIX  
CASE 506AA



H = MC10	A = Assembly Location
K = MC100	L = Wafer Lot
5Y = MC10	Y = Year
4L = MC100	W = Work Week
M = Date Code	■ = Pb-Free Package

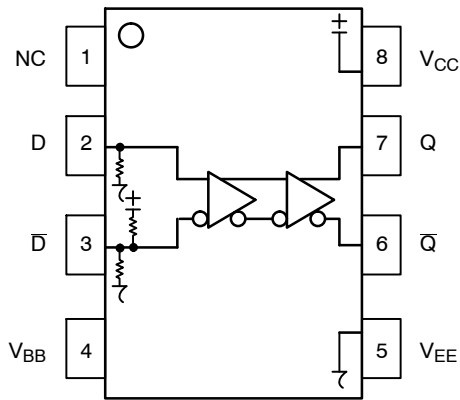
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

## MC10LVEP16, MC100LVEP16



**Figure 1. 8-Lead Pinout (Top View) and Logic Diagram**

**Table 1. PIN DESCRIPTION**

Pin	Function
D*, $\bar{D}$ **	ECL Data Inputs
Q, $\bar{Q}$	ECL Data Outputs
V <sub>BB</sub>	Ref. Voltage Output
V <sub>CC</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply
NC	No Connect
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

\* Pins will default LOW when left open.

\*\*Pins will default to  $V_{CC}/2$  when left open.

**Table 2. ATTRIBUTES**

Characteristics	Value
Internal Input Pulldown Resistor	75 k $\Omega$
Internal Input Pullup Resistor	37.5 k $\Omega$
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 4 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	167 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

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**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		6	V
$V_{EE}$	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-6	V
$V_I$	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 -6	V V
$I_{out}$	Output Current	Continuous Surge		50 100	mA mA
$I_{BB}$	$V_{BB}$ Sink/Source			$\pm 0.5$	mA
$T_A$	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 SOIC-8	190 130	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8	41 to 44	$^{\circ}\text{C}/\text{W}$
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8 TSSOP-8	185 140	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44	$^{\circ}\text{C}/\text{W}$
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
$T_{sol}$	Wave Solder  Pb Pb-Free	<2 to 3 sec @ 248 $^{\circ}\text{C}$ <2 to 3 sec @ 260 $^{\circ}\text{C}$		265 265	$^{\circ}\text{C}$
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	(Note 2)	DFN8	35 to 40	$^{\circ}\text{C}/\text{W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

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**Table 4. 10EP DC CHARACTERISTICS, PECL**  $V_{CC} = 2.5\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	17	22	27	17	22	27	17	22	28	mA
$V_{OH}$	Output HIGH Voltage (Note 4)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
$V_{OL}$	Output LOW Voltage (Note 4)	565	740	865	630	805	930	690	865	990	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Notes 5, 6)	1.2		2.5	1.2		2.5	1.2		2.5	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	D D	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.125 V to -1.3 V.
- All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .
- Do not use  $V_{BB}$  at  $V_{CC} < 3.0\text{ V}$ . Single ended input CLK pin operation is limited to  $V_{CC} \geq 3.0\text{ V}$  in PECL mode.
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 5. 10EP DC CHARACTERISTICS, PECL**  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 7)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	17	22	27	17	22	27	17	22	28	mA
$V_{OH}$	Output HIGH Voltage (Note 8)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
$V_{OL}$	Output LOW Voltage (Note 8)	1365	1540	1665	1430	1605	1730	1490	1665	1790	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	2090		2415	2155		2480	2215		2540	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	1365		1690	1430		1755	1490		1815	mV
$V_{BB}$	Output Voltage Reference (Note 9)	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10)	1.2		3.3	1.2		3.3	1.2		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	D D	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.925 V to -0.5 V.
- All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .
- Single ended input CLK pin operation is limited to  $V_{CC} \geq 3.0\text{ V}$  in PECL mode.
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 6. 10EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -3.8\text{ V}$  to  $-2.375\text{ V}$  (Note 11)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	17	22	27	17	22	27	17	22	28	mA
$V_{OH}$	Output HIGH Voltage (Note 12)	-1135	-1010	-885	-1070	-945	-820	-1010	-885	-760	mV
$V_{OL}$	Output LOW Voltage (Note 12)	-1935	-1760	-1635	-1870	-1695	-1570	-1810	-1635	-1510	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	-1210		-885	-1145		-820	-1085		-760	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	-1935		-1610	-1870		-1545	-1810		-1485	mV
$V_{BB}$	Output Voltage Reference (Note 13)	-1510	-1410	-1310	-1445	-1345	-1245	-1385	-1285	-1185	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 14)	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	D $\bar{D}$	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Input and output parameters vary 1:1 with  $V_{CC}$ .

12. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

13. Single ended input CLK pin operation is limited to  $V_{EE} \leq -3.0\text{ V}$  in NECL mode.

14.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 7. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 2.5\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 15)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	19	24	29	22	28	34	24	30	36	mA
$V_{OH}$	Output HIGH Voltage (Note 16)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
$V_{OL}$	Output LOW Voltage (Note 16)	555	730	900	555	730	900	555	730	900	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Notes 17, 18)	1.2		3.3	1.2		3.3	1.2		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	D $\bar{D}$	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

15. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $+0.125\text{ V}$  to  $-1.3\text{ V}$ .

16. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

17. Do not use  $V_{BB}$  at  $V_{CC} < 3.0\text{ V}$ . Single ended input CLK pin operation is limited to  $V_{CC} \geq 3.0\text{ V}$  in PECL mode.

18.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 8. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 19)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	19	24	29	22	28	34	24	30	36	mA
$V_{OH}$	Output HIGH Voltage (Note 20)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
$V_{OL}$	Output LOW Voltage (Note 20)	1355	1530	1700	1355	1530	1700	1355	1530	1700	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	1355		1700	1355		1700	1355		1700	mV
$V_{BB}$	Output Voltage Reference (Note 21)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 22)	1.2		3.3	1.2		3.3	1.2		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$\frac{D}{\bar{D}}$	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

19. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.925 V to -0.5 V.

20. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

21. Single ended input CLK pin operation is limited to  $V_{CC} \geq 3.0\text{ V}$  in PECL mode.

22.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 9. 100EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -3.8\text{ V}$  to  $-2.375\text{ V}$  (Note 23)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	19	24	29	22	28	34	24	30	36	mA
$V_{OH}$	Output HIGH Voltage (Note 24)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
$V_{OL}$	Output LOW Voltage (Note 24)	-1945	-1770	-1600	-1945	-1770	-1600	-1945	-1770	-1600	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	-1945		-1600	-1945		-1600	-1945		-1600	mV
$V_{BB}$	Output Voltage Reference (Note 25)	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 26)	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$\frac{D}{\bar{D}}$	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

23. Input and output parameters vary 1:1 with  $V_{CC}$ .

24. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

25. Single ended input CLK pin operation is limited to  $V_{EE} \leq -3.0\text{ V}$  in NECL mode.

26.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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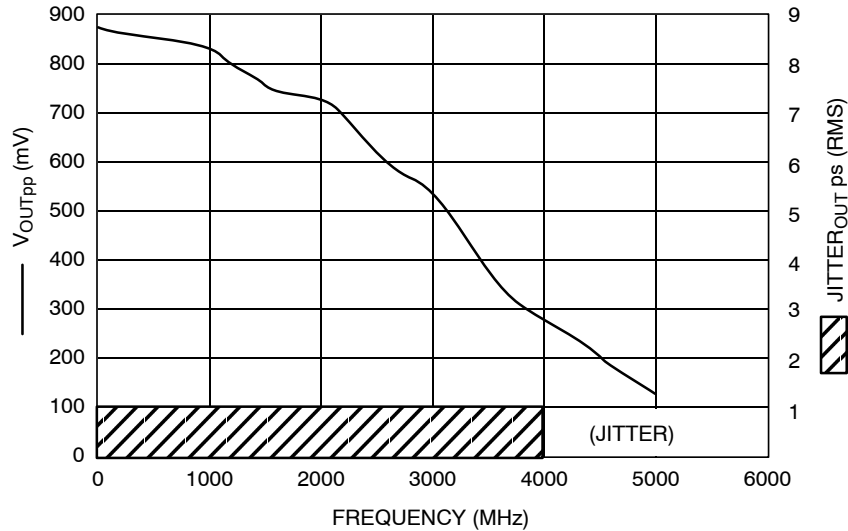
**Table 10. AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.8\text{ V}$  to  $-2.375\text{ V}$  or  $V_{CC} = 2.375\text{ V}$  to  $3.8\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 27)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Frequency (See Figure 2. $F_{max}/JITTER$ )		> 4			> 4			> 4		GHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential	150	220	300	170	240	320	190	260	330	ps
$t_{SKEW}$	Duty Cycle Skew (Note 28)		5.0	20		5.0	20		5.0	20	ps
$t_{JITTER}$	CLOCK Random Jitter (RMS) @ $\leq 1.0\text{ GHz}$ @ $\leq 1.5\text{ GHz}$ @ $\leq 2.0\text{ GHz}$ @ $\leq 2.5\text{ GHz}$ @ $\leq 3.0\text{ GHz}$ @ $\leq 3.5\text{ GHz}$		0.134 0.077 0.115 0.117 0.122 0.123	0.2 0.2 0.2 0.2 0.2 0.2		0.147 0.104 0.141 0.132 0.143 0.145	0.3 0.3 0.3 0.3 0.3 0.3		0.166 0.145 0.153 0.156 0.177 0.202	0.3 0.3 0.3 0.3 0.3 0.3	ps
$V_{PP}$	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
$t_r$ , $t_f$	Output Rise/Fall Times $Q, \bar{Q}$ (20% – 80%)	70	120	170	80	130	180	100	150	200	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

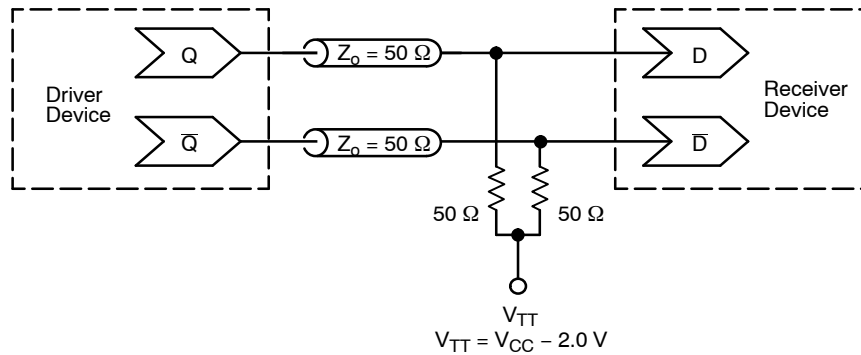
27. Measured using a 750 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

28. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.



**Figure 2.  $F_{max}/Jitter$**

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**Figure 3. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

### ORDERING INFORMATION

Device	Package	Shipping†
MC10LVEP16D	SOIC-8	98 Units / Rail
MC10LVEP16DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC10LVEP16DR2	SOIC-8	2500 / Tape & Reel
MC10LVEP16DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC10LVEP16DT	TSSOP-8	100 Units / Rail
MC10LVEP16DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC10LVEP16DTR2	TSSOP-8	2500 / Tape & Reel
MC10LVEP16DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC10LVEP16MNR4	DFN8	1000 / Tape & Reel
MC10LVEP16MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel
MC100LVEP16D	SOIC-8	98 Units / Rail
MC100LVEP16DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC100LVEP16DR2	SOIC-8	2500 / Tape & Reel
MC100LVEP16DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100LVEP16DT	TSSOP-8	100 Units / Rail
MC100LVEP16DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100LVEP16DTR2	TSSOP-8	2500 / Tape & Reel
MC100LVEP16DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100LVEP16MNR4	DFN8	1000 / Tape & Reel
MC100LVEP16MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



## MC10LVEP16, MC100LVEP16

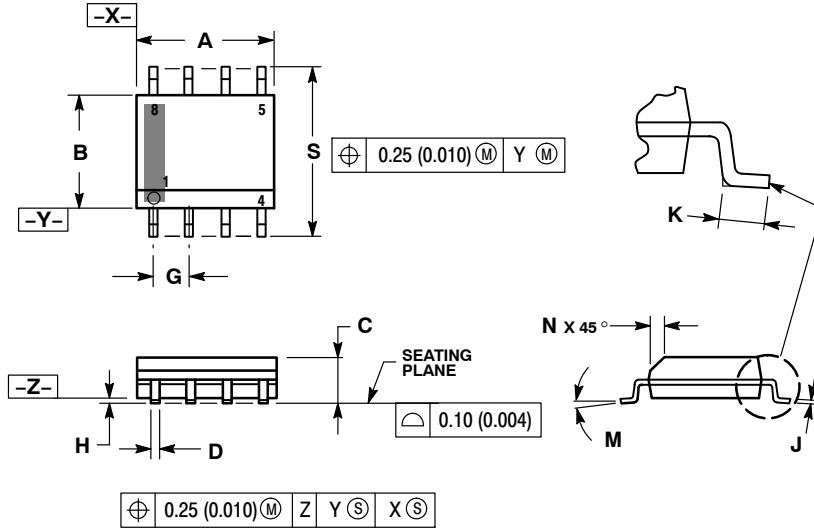
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC10LVEP16, MC100LVEP16

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AH

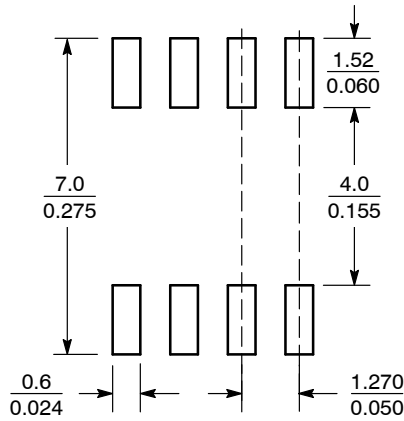


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



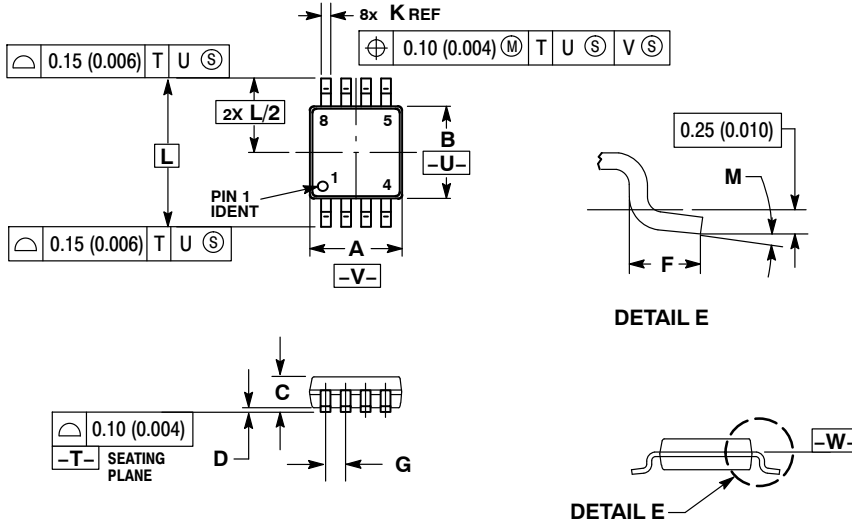
SCALE 6:1 ( $\frac{\text{mm}}{\text{inches}}$ )

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC10LVEP16, MC100LVEP16

## PACKAGE DIMENSIONS

TSSOP-8  
DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 948R-02  
ISSUE A



NOTES:

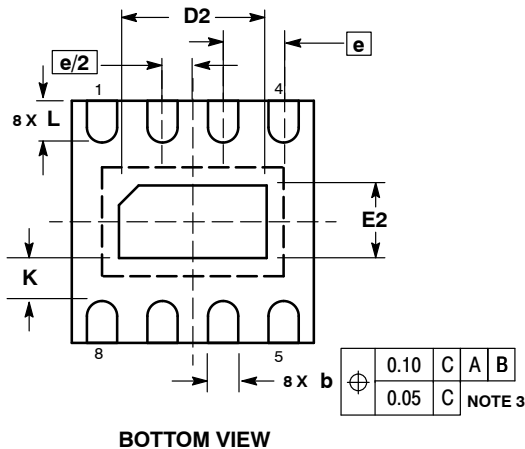
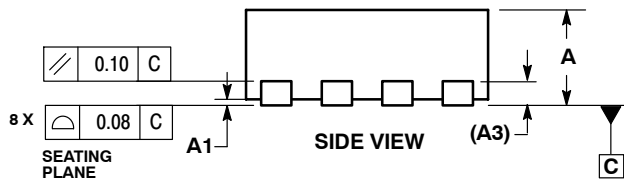
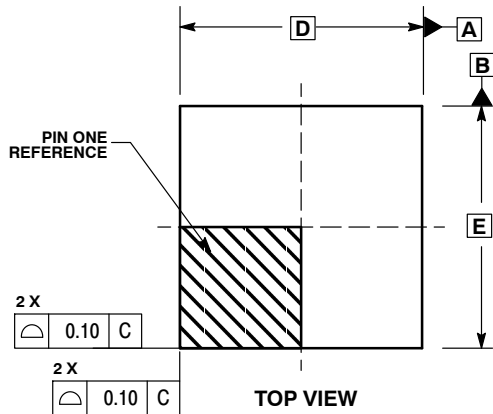
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

# MC10LVEP16, MC100LVEP16

## PACKAGE DIMENSIONS

DFN8  
CASE 506AA-01  
ISSUE D



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.20	---
L	0.25	0.35

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