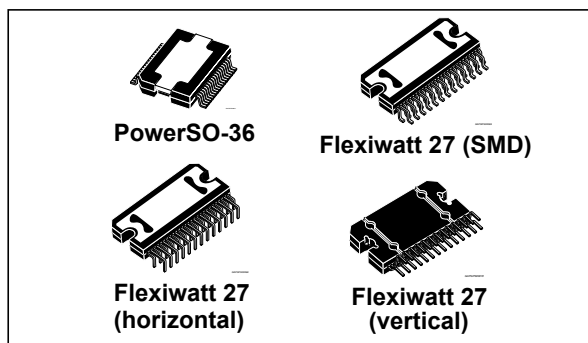


## High efficiency digital input automotive quad power amplifier with built-in diagnostics features, 'start stop' compatible

Datasheet - production data



- Programmable diagnostic pin
- CMOS compatible enable pin
- Thermal protection
- Pop free in mute to play transitions and viceversa

### Description

The TDA7803A is a single chip quad bridge amplifier in advanced BCD technology integrating: a full D/A converter, digital input for direct connection to I<sup>2</sup>S (or TDM) and powerful MOSFET output stages.

The integrated D/A converter allows the performance to reach an outstanding 115 dB S/N ratio with more than 110 dB of dynamic range.

Moreover the TDA7803A integrates an innovative high efficiency concept, optimized also for uncorrelated music signals. The device is designed to be compatible to battery modulation for class-G systems.

Thanks to this concept, the dissipated "output power" under average listening conditions can be reduced up to 50% when compared to the conventional class AB solutions.

The TDA7803A integrates also a programmable PLL that is able to lock at the input frequencies of 64\*Fs for all the input configurations.

The device is equipped with a full diagnostics array that communicates the status of each speaker through the I<sup>2</sup>C bus. The same I<sup>2</sup>C bus allows to control several configurations of the device.

The TDA7803A is able to play music down to 6 V supply voltage - so it is compatible with the so called 'start stop' battery profile recently adopted by several car makers (thus reducing the fuel consumption and the impact over the environment).

### Features



- AEC-Q100 qualified
- 24-bit digital processing
- 115 dB dynamic range (A-weighted)
- SB-I (SB - improved) high efficiency operation the highest 'non - class D' efficiency
- Parallel mode function availability
- High output power capability:
  - 4 x 27 W 4 Ω @ 14.4 V, 1 kHz, THD = 10%
  - 4 x 47 W 2 Ω @ 14.4 V, 1 kHz, THD = 10%
- Flexible mode control:
  - Full I<sup>2</sup>C bus driving 1.8V/3.3V) with four addresses selectable (only for PowerSO36 package option)
  - Independent front/rear play/ mute
  - Selectable digital gains for very-low noise line-out function
  - Digital diagnostic with DC and AC load detections
- Start-stop compatibility (operation down to 6V)
- Sample rates: 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- Flexible serial data port (1.8 V / 3.3 V):
  - I<sup>2</sup>S standard, TDM 4Ch, TDM 8Ch, TDM 16ch (8+8ch)
- Offset detector
- Independent front/rear clipping detector

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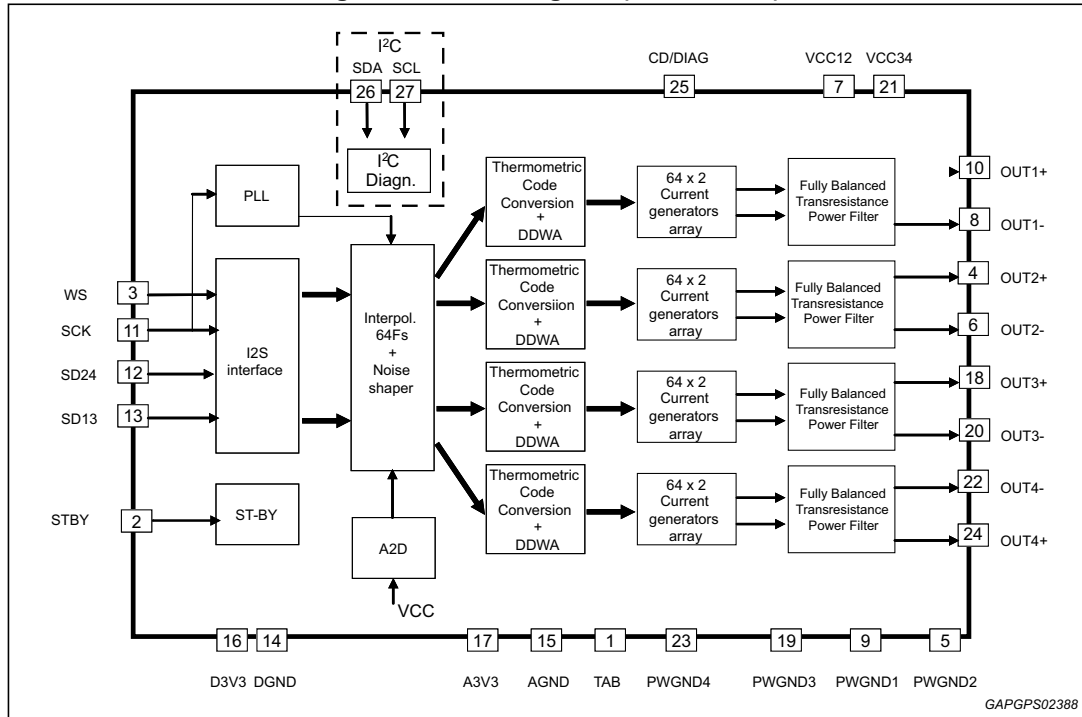
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# 1 Block diagram and pins description

## 1.1 Block diagram

Figure 1. Block diagram (Flexiwatt27)



## 1.2 Pins description

Figure 2. Pins connection diagrams

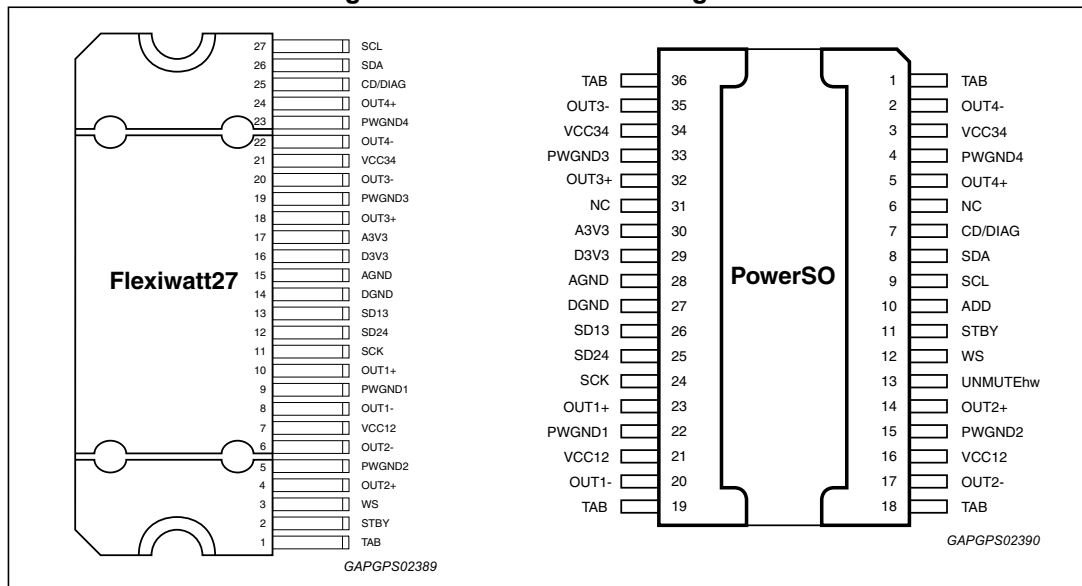




Table 1. Flexiwatt27 pins description

| N° | Pin     | Function  |                   |
|----|---------|---|-------------------|
| 1  | TAB     | TAB connection                                      | Ground            |
| 2  | STBY    | STBY pin  | Input             |
| 3  | WS      | Word select (I <sup>2</sup> S bus)                  | Logic Input       |
| 4  | OUT2+   | Channel 2 (Left Rear) positive output               | Power Output      |
| 5  | PWGND2  | Power ground channels 2                             | Power Ground      |
| 6  | OUT2-   | Channels 2 (Left Rear) negative output              | Power Output      |
| 7  | VCC12   | Channel 1 and 2 positive supply                     | Battery           |
| 8  | OUT1-   | Channel 1 (Left Front) negative output              | Power Output      |
| 9  | PWGND1  | Power ground channel 1                              | Power Ground      |
| 10 | OUT1+   | Channel 1 (Left Front) positive output              | Power Output      |
| 11 | SCK     | Serial clock (I <sup>2</sup> S bus)                 | Logic Input       |
| 12 | SD24    | Serial data channels 2 and 4 (I <sup>2</sup> S bus) | Logic Input       |
| 13 | SD13    | Serial data channels 1 and 3 (I <sup>2</sup> S bus) | Logic Input       |
| 14 | DGND    | Digital ground                                      | Signal Ground     |
| 15 | AGND    | Analog ground                                       | Signal Ground     |
| 16 | D3V3    | Digital 3.3V supply filter                          | Digital Regulator |
| 17 | A3V3    | Analog 3.3V supply filter                           | Analog Regulator  |
| 18 | OUT3+   | Channels 3 (right front) positive output            | Power Output      |
| 19 | PWGND3  | Power ground channel 3                              | Power Ground      |
| 20 | OUT3-   | Channels 3 (right front) negative output            | Power Output      |
| 21 | VCC34   | Channels 3 and 4 positive supply                    | Battery           |
| 22 | OUT4-   | Channels 4 (right rear) negative output             | Power Output      |
| 23 | PWGND4  | Power ground channel 4                              | Power Ground      |
| 24 | OUT4+   | Channels 4 (right rear) positive output             | Power Output      |
| 25 | CD/DIAG | Clip detector and diagnostic output                 | Open Drain Output |
| 26 | SDA     | I <sup>2</sup> C data                               | Signal Input      |
| 27 | SCL     | I <sup>2</sup> C clock                              | Signal Input      |

Table 2. PowerSO36 pins description

| N° | Pin      | Function  |                   |
|----|----------|---|-------------------|
| 1  | TAB      | Device slug connection                              | Ground            |
| 2  | OUT4-    | Channels 4 (right rear) negative output             | Power Output      |
| 3  | VCC34    | Channels 3 and 4 positive supply                    | Battery           |
| 4  | PWGND4   | Power ground channel 4                              | Power Ground      |
| 5  | OUT4+    | Channels 4 (right rear) positive output             | Power Output      |
| 6  | NC       | Not connected                                       | -                 |
| 7  | CD/DIAG  | Clip detector and diagnostic output                 | Open Drain Output |
| 8  | SDA      | I <sup>2</sup> C data                               | Signal Input      |
| 9  | SCL      | I <sup>2</sup> C clock                              | Signal Input      |
| 10 | ADD      | I <sup>2</sup> C Address                            | Logic Input       |
| 11 | STBY     | STBY pin  | Input             |
| 12 | WS       | Word select (I <sup>2</sup> S bus)                  | Logic Input       |
| 13 | UNMUTEhw | Unmute Hardware                                     | Logic Input       |
| 14 | OUT2+    | Channel 2 (Left Rear) positive output               | Power Output      |
| 15 | PWGND2   | Power ground channels 2                             | Power Ground      |
| 16 | VCC12    | Channel 1 and 2 positive supply                     | Battery           |
| 17 | OUT2-    | Channels 2 (Left Rear) negative output              | Power Output      |
| 18 | TAB      | Device slug connection                              | Ground            |
| 19 | TAB      | Device slug connection                              | Ground            |
| 20 | OUT1-    | Channel 1 (Left Front) negative output              | Power Output      |
| 21 | VCC12    | Channel 1 and 2 positive supply                     | Battery           |
| 22 | PWGND1   | Power ground channel 1                              | Power Ground      |
| 23 | OUT1+    | Channel 1 (Left Front) positive output              | Power Output      |
| 24 | SCK      | Serial clock (I <sup>2</sup> S bus)                 | Logic Input       |
| 25 | SD24     | Serial data channels 2 and 4 (I <sup>2</sup> S bus) | Logic Input       |
| 26 | SD13     | Serial data channels 1 and 3 (I <sup>2</sup> S bus) | Logic Input       |
| 27 | DGND     | Digital ground                                      | Signal Ground     |
| 28 | AGND     | Analog ground                                       | Signal Ground     |
| 29 | D3V3     | Digital 3.3V supply filter                          | Digital Regulator |
| 30 | A3V3     | Analog 3.3V supply filter                           | Analog Regulator  |
| 31 | NC       | Not connected                                       | -                 |
| 32 | OUT3+    | Channels 3 (right front) positive output            | Power Output      |
| 33 | PWGND3   | Power ground channel 3                              | Power Ground      |
| 34 | VCC34    | Channels 3 and 4 positive supply                    | Battery           |
| 35 | OUT3-    | Channels 3 (right front) negative output            | Power Output      |
| 36 | TAB      | Device slug connection                              | Ground            |

## 2 Application diagrams

Figure 3. I<sup>2</sup>C bus mode application diagram (Flexiwatt)

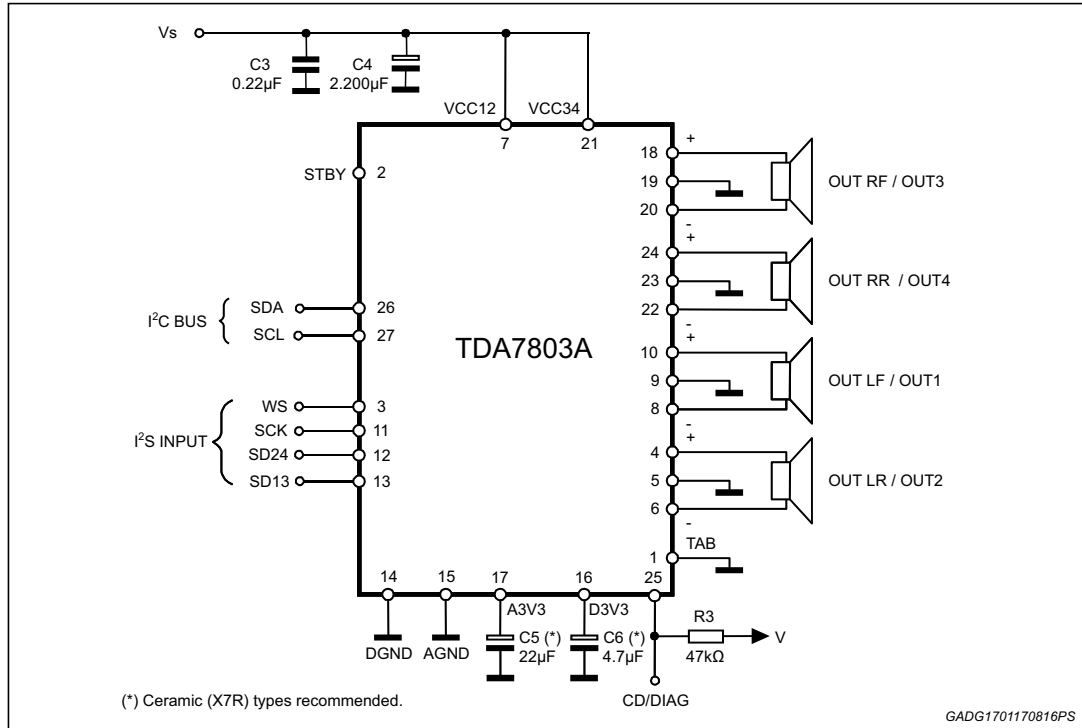
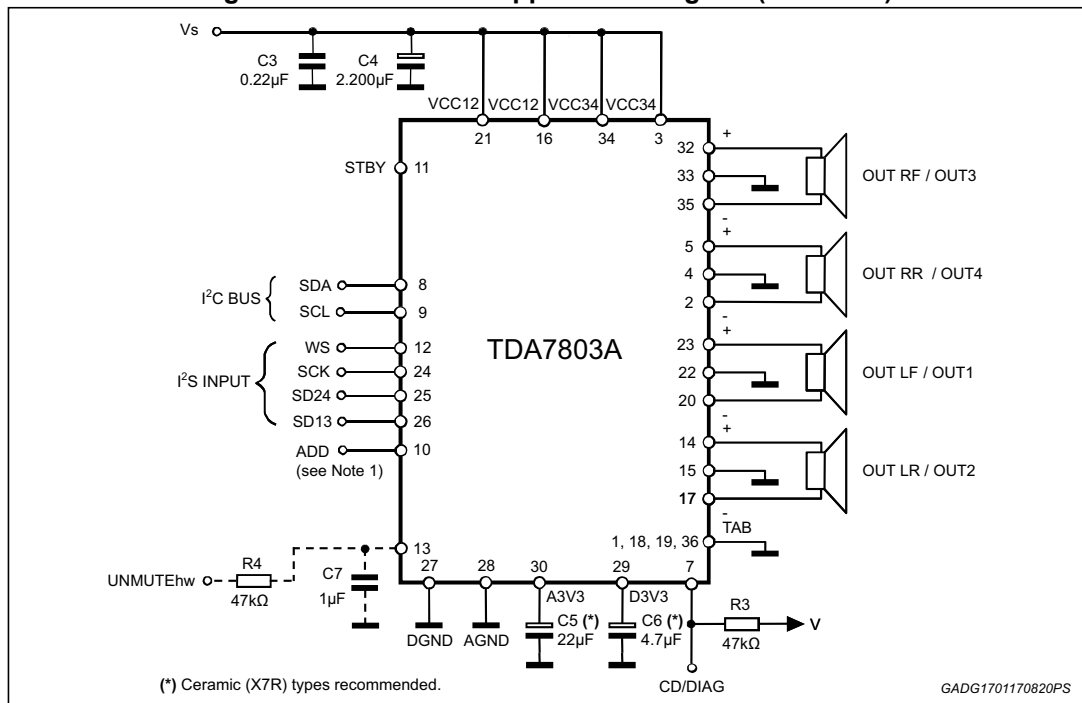


Figure 4. I<sup>2</sup>C bus mode application diagram (PowerSO)



1. Refer to [Section 9: I<sup>2</sup>C bus interface](#) for connection suggestions.

### 3 Electrical specification

#### 3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

| Symbol             | Parameter  | Value                             | Unit |
|--------------------|--|-----------------------------------|------|
| $V_S$              | DC supply voltage                                    | -0.3 to 28                        | V    |
| $V_{peak}$         | Transient supply voltage for $t = 100$ ms            | -0.3 to 50                        | V    |
| $V_{i2c}$          | I <sup>2</sup> C bus pins voltage                    | -0.3 to 4.6                       | V    |
| $V_{i2s}$          | I <sup>2</sup> S bus pins voltage                    | -0.3 to 4.6                       | V    |
| $V_{unmute}$       | Unmute hardware voltage (PSO36 only)                 | -0.3 to 4.6                       | V    |
| $V_{cd}$           | CD/Diag pin voltage                                  | -0.3 to 20                        | V    |
| $V_{stby}$         | STBY pin voltage                                     | -0.3 to 4.6                       | V    |
| $I_O$              | Output peak current (repetitive $f > 10$ Hz)         | internally limited <sup>(1)</sup> | A    |
| $P_{tot}$          | Power dissipation $T_{case} = 70$ °C                 | 85                                | W    |
| $T_{stg}, T_j$     | Storage and junction temperature                     | -55 to 150                        | °C   |
| $T_{amb}$          | Operative temperature range <sup>(2)</sup>           | -40 to 105                        | °C   |
| $C_{max}$          | Maximum capacitor vs. ground connected to the output | 10                                | nF   |
| ESD <sub>HBM</sub> | ESD protection HBM <sup>(3)</sup>                    | 2000                              | V    |
| ESD <sub>CDM</sub> | ESD protection CDM <sup>(3)</sup>                    | 500                               | V    |

1. Internally limited by overcurrent protection.
2. A suitable heatsink/dissipation system should be used to keep  $T_j$  inside the specified limits.
3. Conforming to Q100 ESD standard.

#### 3.2 Thermal data

Table 4. Thermal data

| Symbol           | Parameter                                  | Value | Unit |
|------------------|--|-------|------|
| $R_{th\ j-case}$ | Thermal resistance junction-to-case (max.) | 1     | °C/W |

### 3.3 Electrical characteristics

Referred to the test setup  $V_S = 14.4\text{ V}$ ;  $R_L = 4\ \Omega$ ;  $f = 1\text{ kHz}$ ; tested at  $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ ; functionality guaranteed for  $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ ; SB-I mode; unless otherwise specified.

**Table 5. Electrical characteristics**

| Symbol                    | Parameter   | Test condition  | Min. | Typ.  | Max. | Unit          |
|---------------------------|---|---|------|-------|------|---------------|
| <b>General</b>            |   |   |      |       |      |               |
| $V_S$                     | Supply voltage range  | $R_L = 4\ \Omega$   | 6    | -     | 18.5 | V             |
|                           |   | $R_L = 2\ \Omega$ , std_bridge  | 6    | -     | 16   | V             |
|                           |   | $R_L = 2\ \Omega$ , SBI   | 6    | -     | 16   | V             |
| $I_{SB}$                  | Standby current   | -   | -    | 1     | 4    | $\mu\text{A}$ |
| $I_q$                     | Total quiescent current in amplifier mode                                   | Mute condition  | -    | 170   | 210  | mA            |
| $I_{qECO}$                | Total quiescent current in ECO mode   | ECO mode  | -    | 35    | 40   | mA            |
| $A_M$                     | Mute attenuation  | -   | 80   | -     | -    | dB            |
| $V_{OS}$                  | Offset voltage  | Mute and play   | -25  | -     | +25  | mV            |
| $V_{lowM}$                | $V_{CC}$ low supply mute threshold (Min I <sup>2</sup> C setting - default) | Attenuation <0.5 dB, digital mute disabled                                | -    | -     | 5.6  | V             |
|                           |   | Attenuation $\geq$ 60 dB, digital mute disabled                           | 5    | -     | -    | V             |
| $V_{POWONRESET}$          | Supply voltage of power-on reset  | -   | -    | 3.5   | -    | V             |
| $V_{highM}$               | High supply mute threshold  | Attenuation = -6 dB   | 19   | -     | 21   | V             |
| <b>Audio performances</b> |   |   |      |       |      |               |
| $P_O$                     | Output power  | $R_L = 4\ \Omega$ ; max power <sup>(1)</sup>                              | 40   | 43    | -    | W             |
|                           |   | THD = 10 %  | 25   | 27    | -    | W             |
|                           |   | THD = 1 %   | 20   | 22    | -    | W             |
|                           |   | $R_L = 2\ \Omega$ ; THD 10%   | 44   | 47    | -    | W             |
|                           |   | $R_L = 2\ \Omega$ ; THD 1%  | 34   | 37    | -    | W             |
|                           |   | $R_L = 2\ \Omega$ ; max power <sup>(1)</sup>                              | 69   | 72    | -    | W             |
| THD <sub>SB</sub>         | Total harmonic distortion (Standard bridge)                                 | $P_O = 4\text{ W}$ , $f = 1\text{ kHz}$ , $G_{V1}$                        | -    | 0.015 | 0.04 | %             |
|                           |   | $P_O = 4\text{ W}$ , $f = 10\text{ kHz}$ , $G_{V1}$                       | -    | 0.15  | 0.5  | %             |
|                           |   | $R_L = 100\ \Omega$ input = -10 dBFS, $f = 1\text{ kHz}$ , $G_{V1,2,3,4}$ | -    | 0.01  | 0.02 | %             |
| THD                       | Total harmonic distortion (SBI mode)  | $P_O = 2\text{ W}$ , $f = 1\text{ kHz}$ , $G_{V1}$                        | -    | 0.015 | 0.04 | %             |
|                           |   | $P_O = 6\text{ W}$ , $f = 1\text{ kHz}$ , $G_{V1}$                        | -    | 0.02  | 0.06 | %             |

**Table 5. Electrical characteristics (continued)**

| Symbol   | Parameter   | Test condition  | Min.               | Typ. | Max. | Unit |
|--|---|---|--------------------|------|------|------|
| C <sub>T</sub> <sup>(2)</sup>                              | Cross talk  | f = 1 kHz   | -                  | 100  | -    | dB   |
|  |   | f = 10 kHz  | -                  | 80   | -    | dB   |
| G <sub>V1</sub>  | Voltage gain 1  | @ Amplitude = -18 dBFs                                  | 2.3                | 2.5  | -    | Vp   |
| G <sub>V2</sub>  | Voltage gain 2  |   | 1.25               | 1.35 | -    | Vp   |
| G <sub>V3</sub>  | Voltage gain 3  |   | 0.9                | 1    | -    | Vp   |
| G <sub>V4</sub>  | Voltage gain 4  |   | 0.4                | 0.55 | -    | Vp   |
| DR <sup>(2)</sup>  | Dynamic range   | A-wtd values, G <sub>V1</sub> gain                      | -                  | 115  | -    | dB   |
| E <sub>out1</sub>  | Output noise voltage<br>G <sub>V</sub> = G <sub>V1</sub><br>G <sub>V</sub> = G <sub>V4</sub>                  | A-wtd values  | -                  | 27   | 40   | μV   |
|  |   |   | -                  | 18   | -    |      |
| E <sub>out2</sub>  | Output noise voltage<br>G <sub>V</sub> = G <sub>V1</sub><br>G <sub>V</sub> = G <sub>V4</sub>                  | ITU-R 468   | -                  | 70   | 96   | μV   |
|  |   |   | -                  | 45   | -    |      |
| SNR <sup>(2)</sup>   | Signal to noise ratio   | A-wtd values, G <sub>V1</sub> gain                      | -                  | 115  | -    | dB   |
| ΔG <sub>v</sub>  | Channel Gain Mismatch   | -   | -0.5               | -    | 0.5  | dB   |
| SSR  | Supply slew rate  | -   | -                  | 1    | -    | V/μs |
| PSRR   | Power supply rejection ratio  | f = 1 kHz;<br>V <sub>r</sub> = 1 Vpk;                   | 60                 | 70   | -    | dB   |
| ΔV <sub>OITU</sub>   | ITU Pop filter output voltage<br>(standard bridge mode)   | Eco mode to mute transition and vice versa              | -                  | -    | 4    | mV   |
|  |   | Mute to Play and Play to Mute transition <sup>(3)</sup> | -                  | 0    | -    | mV   |
| <b>Clipping detector</b>                                   |   |   |                    |      |      |      |
| CD <sub>LK</sub>   | Clip det high leakage current   | CD off, V = 3.3 V                                       | -                  | 0    | 1    | μA   |
| CD <sub>SAT</sub>  | Clip det sat. voltage   | CD on; I <sub>CD</sub> = 1 mA                           | -                  | 50   | -    | mV   |
| CD1 <sub>THD</sub>   | Clip det THD threshold 1  | -   | -                  | 2    | 3    | %    |
| CD2 <sub>THD</sub>   | Clip det THD threshold 2  | -   | 4                  | 6    | 8    | %    |
| CD3 <sub>THD</sub>   | Clip det THD threshold 3  | -   | 9                  | 12   | 14   | %    |
| <b>Turn on diagnostics for parallel mode configuration</b> |   |   |                    |      |      |      |
| P <sub>gnd</sub>   | Short to GND det. (below this limit, the output is considered in short circuit to GND)                        | -   | -                  | -    | 1    | V    |
| P <sub>vs</sub>  | Short to V <sub>s</sub> det. (above this limit, the output is considered in short circuit to V <sub>s</sub> ) | -   | V <sub>s</sub> - 1 | -    | -    | V    |

Table 5. Electrical characteristics (continued)

| Symbol   | Parameter  | Test condition | Min.               | Typ. | Max.      | Unit       |
|--|--|----------------|--------------------|------|-----------|------------|
| Pnop   | Normal operation thresholds. (within these limits, the output is considered without faults). | -              | 2                  | -    | $V_S - 2$ | V          |
| Lsc  | Shorted load det.  | -              | -                  | -    | 0.7       | $\Omega$   |
| Lop  | Normal load det.   | -              | 1.3                | -    | 30        | $\Omega$   |
| Lnop   | Open load det.   | -              | 70                 | -    | -         | $\Omega$   |
| <b>Turn-on diagnostic for parallel mode configuration</b>    |  |                |                    |      |           |            |
| Lsc  | Shorted load det.  | -              | -                  | -    | 0.35      | $\Omega$   |
| Lop  | Normal load det.   | -              | 0.65               | -    | 15        | $\Omega$   |
| Lnop   | Open load det.   | -              | 35                 | -    | -         | $\Omega$   |
| Rss  | Soft Short Diagnostic threshold (below this value, soft short resistance is recognized)      | -              | 500                | -    | -         | $\Omega$   |
| <b>Turn-on diagnostic for line driver mode configuration</b> |  |                |                    |      |           |            |
| Pgnd   | Short to GND det. (below this limit, the output is considered in short circuit to GND)       | -              | -                  | -    | 1         | V          |
| Pvs  | Short to $V_S$ det. (above this limit, the output is considered in short circuit to $V_S$ )  | -              | $V_S - 1$          | -    | -         | V          |
| Pnop   | Normal operation thresholds. (within these limits, the output is considered without faults). | -              | 2                  | -    | $V_S - 2$ | V          |
| Lsc  | Shorted load det.  | -              | -                  | -    | 20        | $\Omega$   |
| Lop  | Normal load det.   | -              | 60                 | -    | 1400      | $\Omega$   |
| Lnop   | Open load det.   | -              | 2600               | -    | -         | $\Omega$   |
| Rss  | Soft Short Diagnostic threshold (below this value, soft short resistance is recognized)      | -              | 5.8 <sup>(4)</sup> | -    | -         | k $\Omega$ |
| <b>AC-diagnostic</b>   |  |                |                    |      |           |            |
| I <sub>ACTRESH</sub>   | AC diagnostic current threshold  | IB4 – D4= '0'  | 250                | 375  | 500       | mA         |
|  |  | IB4 – D4= '1'  | 125                | 187  | 250       | mA         |

**Table 5. Electrical characteristics (continued)**

| Symbol                              | Parameter   | Test condition   | Min.               | Typ.   | Max.               | Unit |
|-------------------------------------|---|--|--------------------|--------|--------------------|------|
| <b>Permanent diagnostics</b>        |   |  |                    |        |                    |      |
| Pgnd                                | Short to GND det. (below this limit, the output is considered in short circuit to GND)                        | Power amplifier in Mute or Play, one or more short circuits protection activated | -                  | -      | 1                  | V    |
| Pvs                                 | Short to V <sub>s</sub> det. (above this limit, the Output is considered in short circuit to V <sub>s</sub> ) | -  | V <sub>s</sub> - 1 | -      | -                  | V    |
| Pnop                                | Normal operation thresholds. (Within these limits, the output is considered without faults)                   | -  | 2                  | -      | V <sub>s</sub> - 2 | V    |
| L <sub>SC</sub>                     | Shorted load det.   | Parallel mode  | -                  | -      | 0.35               | Ω    |
|                                     |   | Speaker mode   | -                  | -      | 0.7                |      |
|                                     |   | Line driver mode   | -                  | -      | 20                 |      |
| L <sub>OP</sub>                     | Normal load det.  | Parallel mode  | 0.65               | -      | -                  | Ω    |
|                                     |   | Speaker mode   | 1.3                | -      | -                  |      |
|                                     |   | Line driver mode   | 60                 | -      | -                  |      |
| T <sub>ph</sub>                     | Thermal protection junction temperature   | Attenuation ≥60 dB   | -                  | 165    | -                  | °C   |
| T <sub>pl</sub>                     |   | Attenuation <0.5 dB  | -                  | 155    | -                  | °C   |
| T <sub>w1</sub>                     | Thermal warning junction temperature <sup>(5)</sup>   | -  | -                  | Tpl-5  | -                  | °C   |
| T <sub>w2</sub>                     |   | -  | -                  | Tpl-10 | -                  | °C   |
| T <sub>w3</sub>                     |   | -  | -                  | Tpl-20 | -                  | °C   |
| T <sub>w4</sub>                     |   | -  | -                  | Tpl-30 | -                  | °C   |
| <b>I<sup>2</sup>C bus interface</b> |   |  |                    |        |                    |      |
| f <sub>SCL</sub>                    | Clock frequency   | -  | -                  | -      | 400                | kHz  |
| V <sub>IL</sub>                     | Input low voltage   | -  | -                  | -      | 0.8                | V    |
| V <sub>IH</sub>                     | Input high voltage  | -  | 1.3                | -      | -                  | V    |
| V <sub>olmax</sub>                  | Maximum I2C data pin low voltage when current I <sub>sink</sub> is sinked                                     | I <sub>sink</sub> = 2 mA   | -                  | -      | 0.27               | V    |
|                                     |   | I <sub>sink</sub> = 8 mA   | -                  | -      | 0.7                | V    |
| I <sub>limax</sub>                  | Maximum input leakage current   | V = 3.6 V  | -                  | -      | 1                  | μA   |
| <b>STBY pin</b>                     |   |  |                    |        |                    |      |
| V <sub>ILSTBY</sub>                 | Input low voltage   | -  | -                  | -      | 1.2                | V    |
| V <sub>IHSTBY</sub>                 | Input high voltage  | -  | 2.4                | -      | -                  | V    |



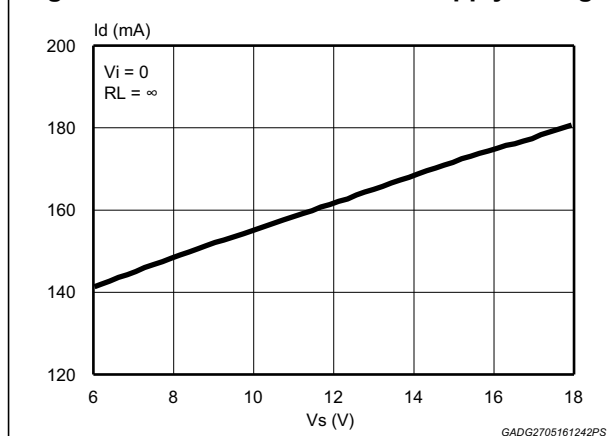
**Table 5. Electrical characteristics (continued)**

| Symbol                          | Parameter                              | Test condition                     | Min. | Typ. | Max. | Unit          |
|---------------------------------|--|------------------------------------|------|------|------|---------------|
| $I_{ILSTBY}$                    | Logic '0' output current               | $V_{IN} = 0.45\text{ V}$           | -    | -    | 1    | $\mu\text{A}$ |
| $I_{IHSTBY}$                    | Logic '1' input current                | $V_{IN} = 2.3\text{ V}$ (IB0 D4=0) | -    | -    | 1    | $\mu\text{A}$ |
| <b>I<sup>2</sup>S pins</b>      |  |                                    |      |      |      |               |
| $V_{IL-I2S}$                    | Input low voltage                      | -                                  | -    | -    | 0.8  | V             |
| $V_{IH-I2S}$                    | Input high voltage                     | -                                  | 1.3  | -    | -    | V             |
| $I_{IH}$                        | Input high current                     | @ $V_I = 3.3\text{ V}$             | -    | -    | 1    | $\mu\text{A}$ |
| $I_{IL}$                        | Input low current                      | @ $V_I = 0\text{ V}$               | -    | -    | 1    | $\mu\text{A}$ |
| <b>Unmute hardware (pin 13)</b> |  |                                    |      |      |      |               |
| $V_{HW\_UNMUTE}$                | Hardware unmute threshold (PSO36 only) | Attenuation $\geq 60\text{ dB}$    | -    | -    | 1.2  | V             |
|                                 |  | Attenuation $< 0.5\text{ dB}$      | 2.6  | -    | -    | V             |
| $I_{UNMUTE}$                    | Input high current                     | @ $V_I = 3.3\text{ V}$             | -    | -    | 1    | $\mu\text{A}$ |
|                                 | Input low current                      | @ $V_I = 0\text{ V}$               | -    | -    | 1    | $\mu\text{A}$ |

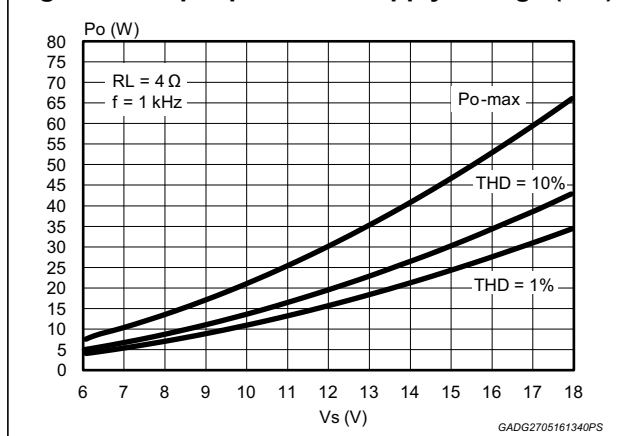
1. Square-wave input / saturated output.
2. Evaluated at bench during product validation.
3. Guaranteed by design (intrinsically immune from any pop at mute to play and play to mute transitions)
4. The values are the ones that guarantee the correct working of the diagnostic. Since the value is strongly dependent on the loudspeaker, we decided to target the values for the limits of open load and short load diagnostic.
5. Thermal warning junction temperature values could be changed via I<sup>2</sup>C bits IB5-d6,d7.

### 3.4 Electrical characteristics typical curves

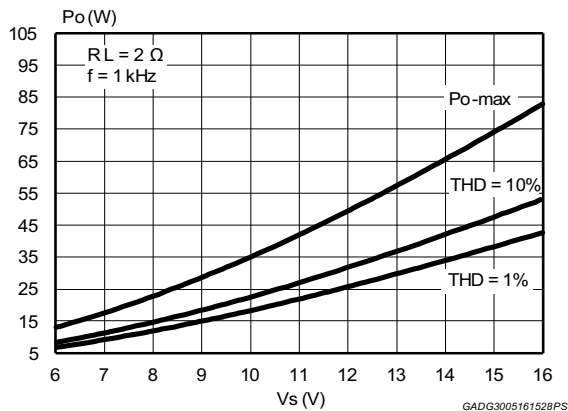
**Figure 5. Quiescent current vs. supply voltage**



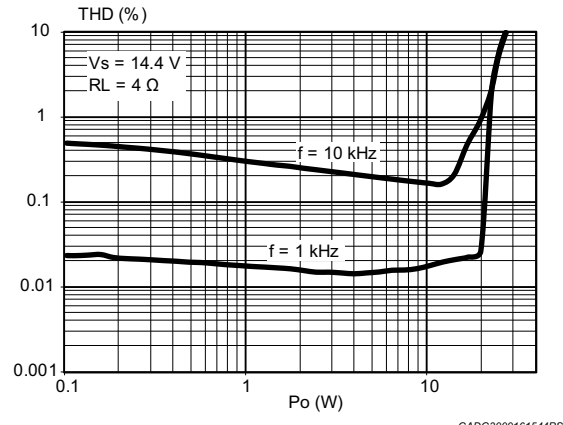
**Figure 6. Output power vs. supply voltage (4 Ω)**



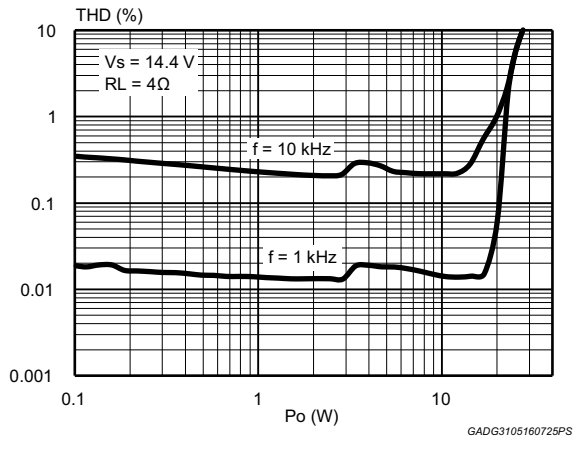
**Figure 7. Output power vs. supply voltage (2 Ω, STD mode)**



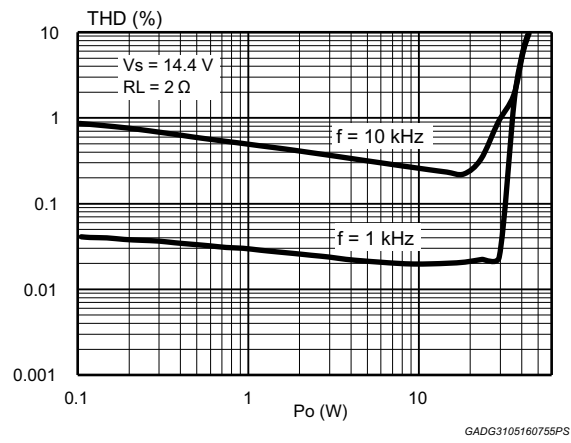
**Figure 8. Distortion vs. output power (4 Ω, STD mode)**



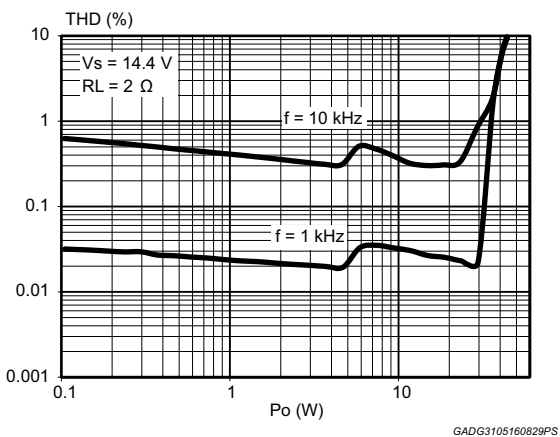
**Figure 9. Distortion vs. output power (4 Ω, SBI mode)**



**Figure 10. Distortion vs. output power (2 Ω, STD mode)**



**Figure 11. Distortion vs. output power (2 Ω, SBI mode)**



**Figure 12. Distortion vs. frequency (4 Ω)**

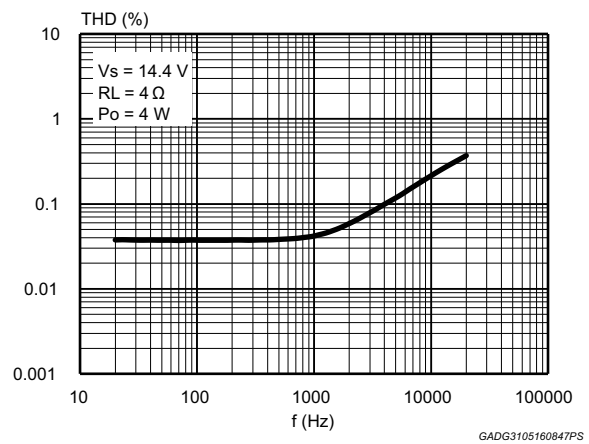


Figure 13. Distortion vs. frequency (2 Ω)

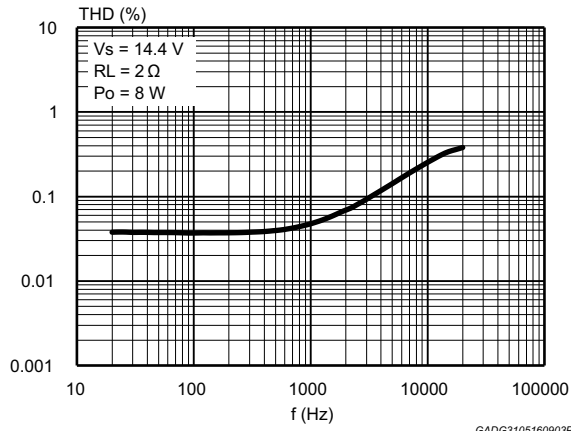


Figure 14. Distortion vs. output power (4 Ω,  $V_s = 6\text{ V}$ )

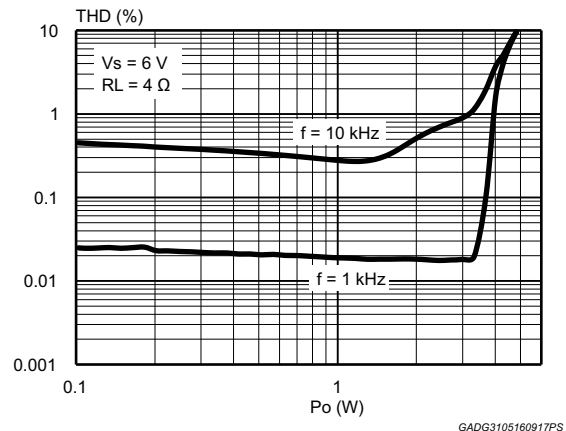


Figure 15. Distortion vs. output power (2 Ω,  $V_s = 6\text{ V}$ )

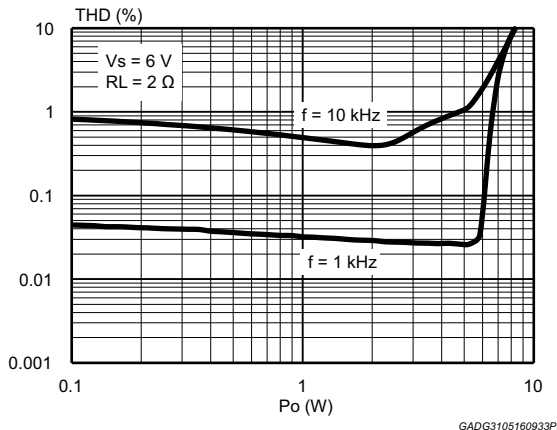


Figure 16.  $V_o$  vs.  $V_{in}$  (Gv1-2-3-4 settings)

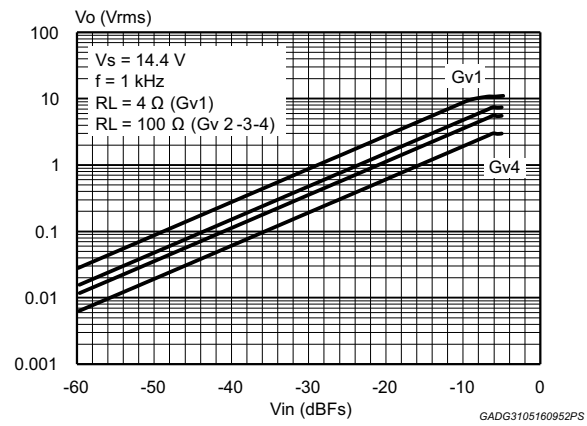


Figure 17.  $V_o$  vs.  $V_{in}$  (Gv1-2-3-4 settings + 6 dB dig. gain)

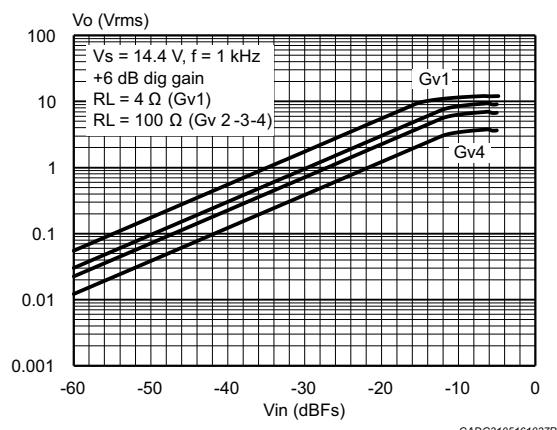
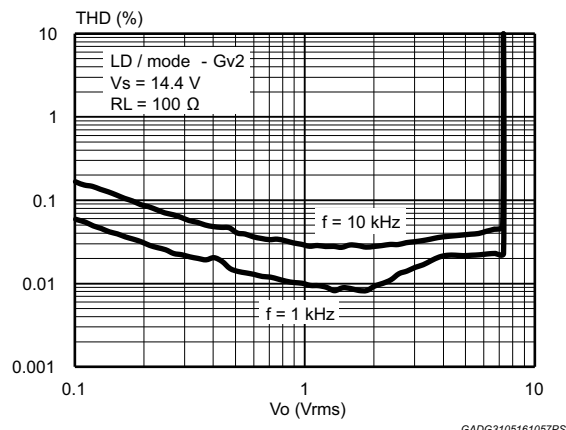
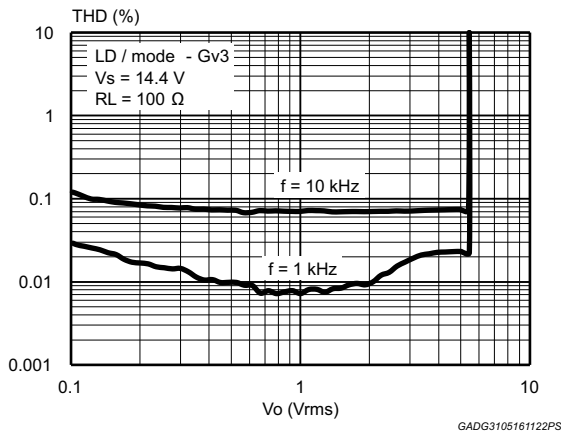


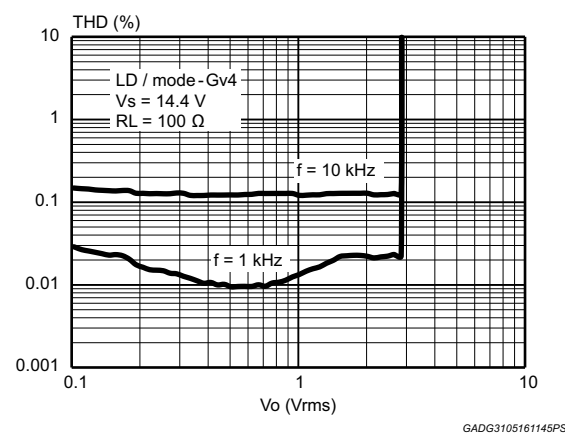
Figure 18. Distortion vs. output voltage (LD-Gv2)



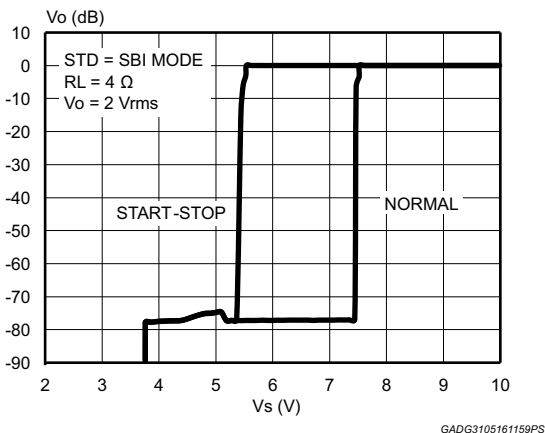
**Figure 19. Distortion vs. output voltage (LD-Gv3)**



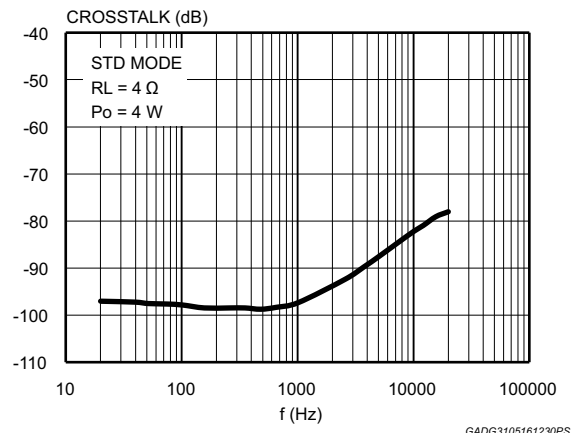
**Figure 20. Distortion vs. output voltage (LD-Gv4)**



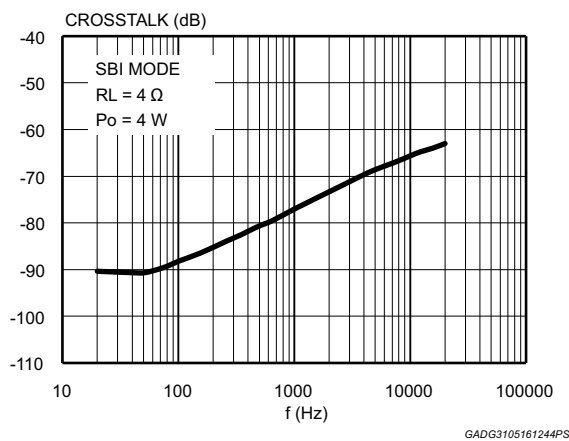
**Figure 21. Output attenuation vs. Vs**



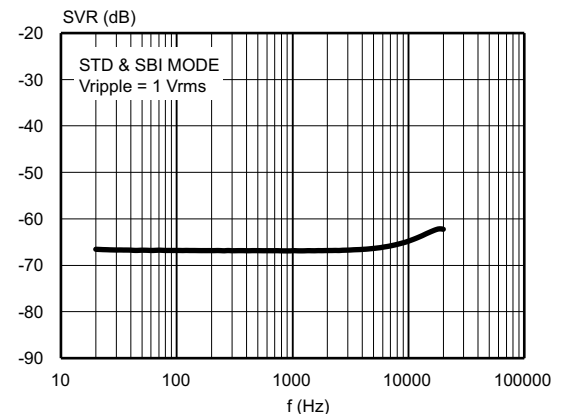
**Figure 22. Crosstalk vs. frequency (STD mode)**



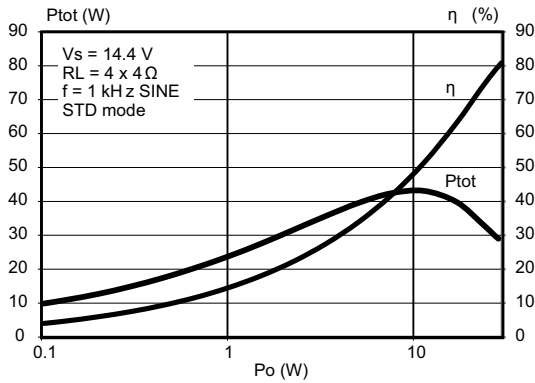
**Figure 23. Crosstalk vs. frequency (SBI mode)**



**Figure 24. Supply voltage rejection vs. frequency**

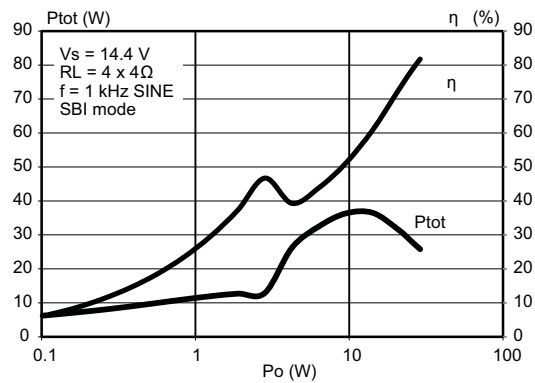


**Figure 25. Total power dissipation & efficiency vs. Po (4 Ω, STD, Sine)**



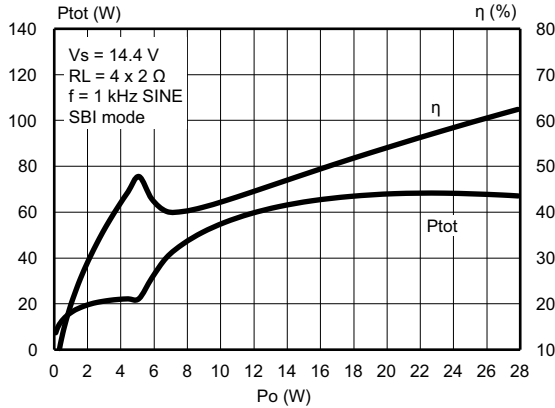
GADG0803170956PS

**Figure 26. Total power dissipation & efficiency vs. Po (4 Ω, SBI, Sine)**



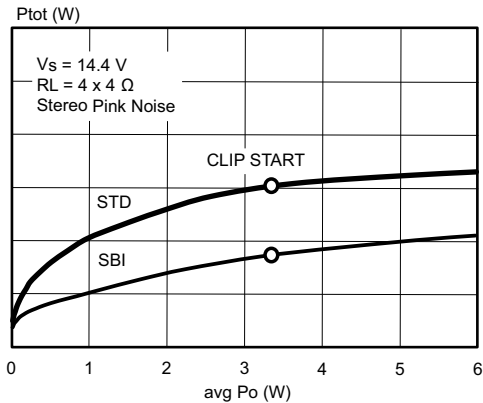
GADG0803171132PS

**Figure 27. Total power dissipation & efficiency vs. Po (2 Ω, SBI, Sine)**



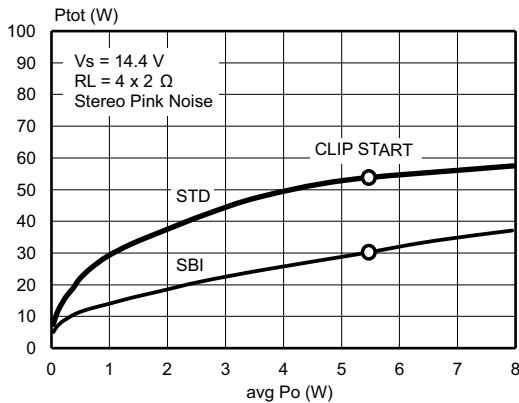
GADG3105161509PS

**Figure 28. Power dissipation vs. average Po (audio program simulation, 4 Ω)**



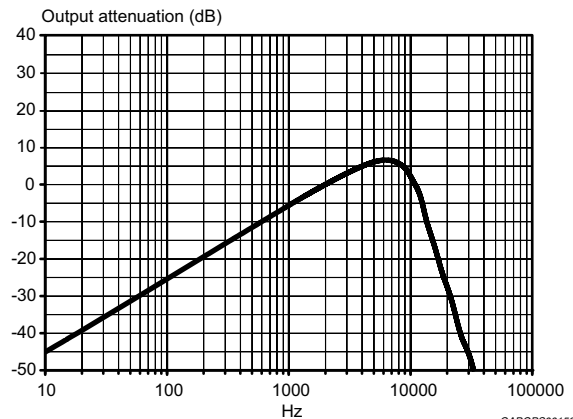
GADG3105161533PS

**Figure 29. Power dissipation vs. average Po (audio program simulation, 2 Ω)**



GADG3105161550PS

**Figure 30. ITU R-ARM frequency response, weighting filter for transient pop**



GAPGPS00153

## 4 Operation states

TDA7803A functionality is regulated by means of a finite state machine.

Finite state machine diagram is reported in [Figure 31](#).

Main states are:

- Standby
- ECO-mode
- Amplifier mode
- Turn-on diagnostic
- Permanent diagnostic

### 4.1 Standby state

When STBY pin is under VILSTBY voltage the amplifier is in stand-by state and the current consumption is very low.

### 4.2 ECO-mode state

When STBY pin is over VIHSTBY the amplifier is in a state of low current absorption, the ECO-mode. The short circuit protections are active and the amplifier is ready for receiving commands from micro-controller through I<sup>2</sup>C interface.

Outputs and A3V3 supply are biased at 0 V.

### 4.3 Amplifier-mode state

When TDA7803A is in ECO-mode state, IB7-d0 is set to "1", (Amplifier-ON), and I<sup>2</sup>S clock is present the amplifier moves to Amplifier-mode state.

The outputs are biased from 0 V to V<sub>cc</sub>/2 and the current consumption reaches "I<sub>q</sub>" level until the amplifier is set in MUTE or in PLAY with low level signal. User can move the amplifier from MUTE to PLAY and viceversa acting on IB2-d4, d3 bits.

A hardware unmute pin is available in PSO36 package only.

### 4.4 Turn-on and permanent diagnostic

TDA7803A provides a powerful and precise diagnostic both with speaker and line driver loads.

There are two main diagnostic states:

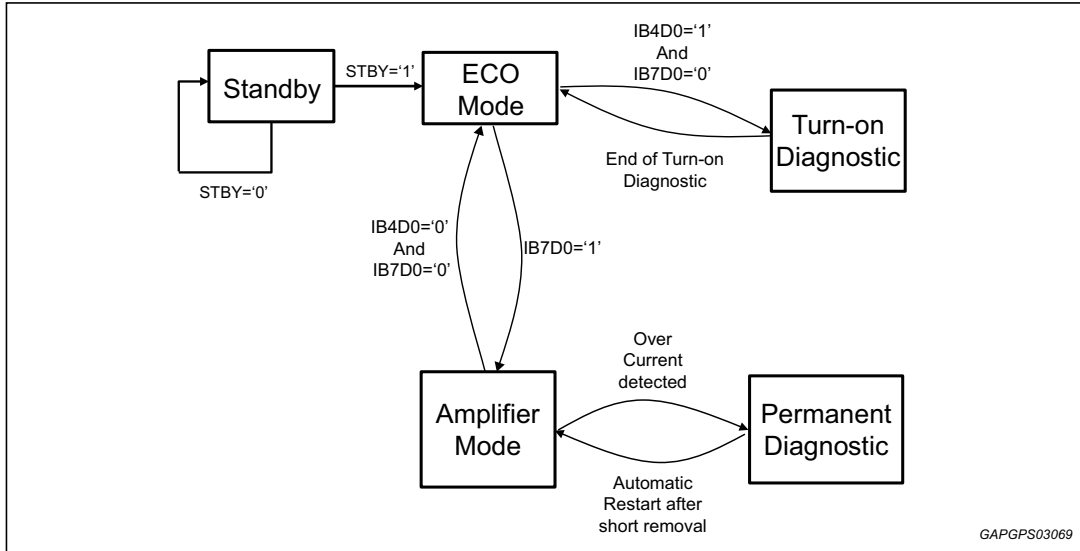
- Turn-on diagnostic
- Permanent diagnostic.

The Turn-on diagnostic could be run in ECO-mode state and is suggested for sensing the presence of faults before amplifier turn-on, in order to avoid unwanted or dangerous conditions due to wrong connections or absence of load.

The Permanent diagnostic is automatically run by TDA7803A when a fault occurs during PLAY and over current protections are triggered.

Turn-on and Permanent diagnostic functionality are described in [Section 6](#).

**Figure 31. State diagram**

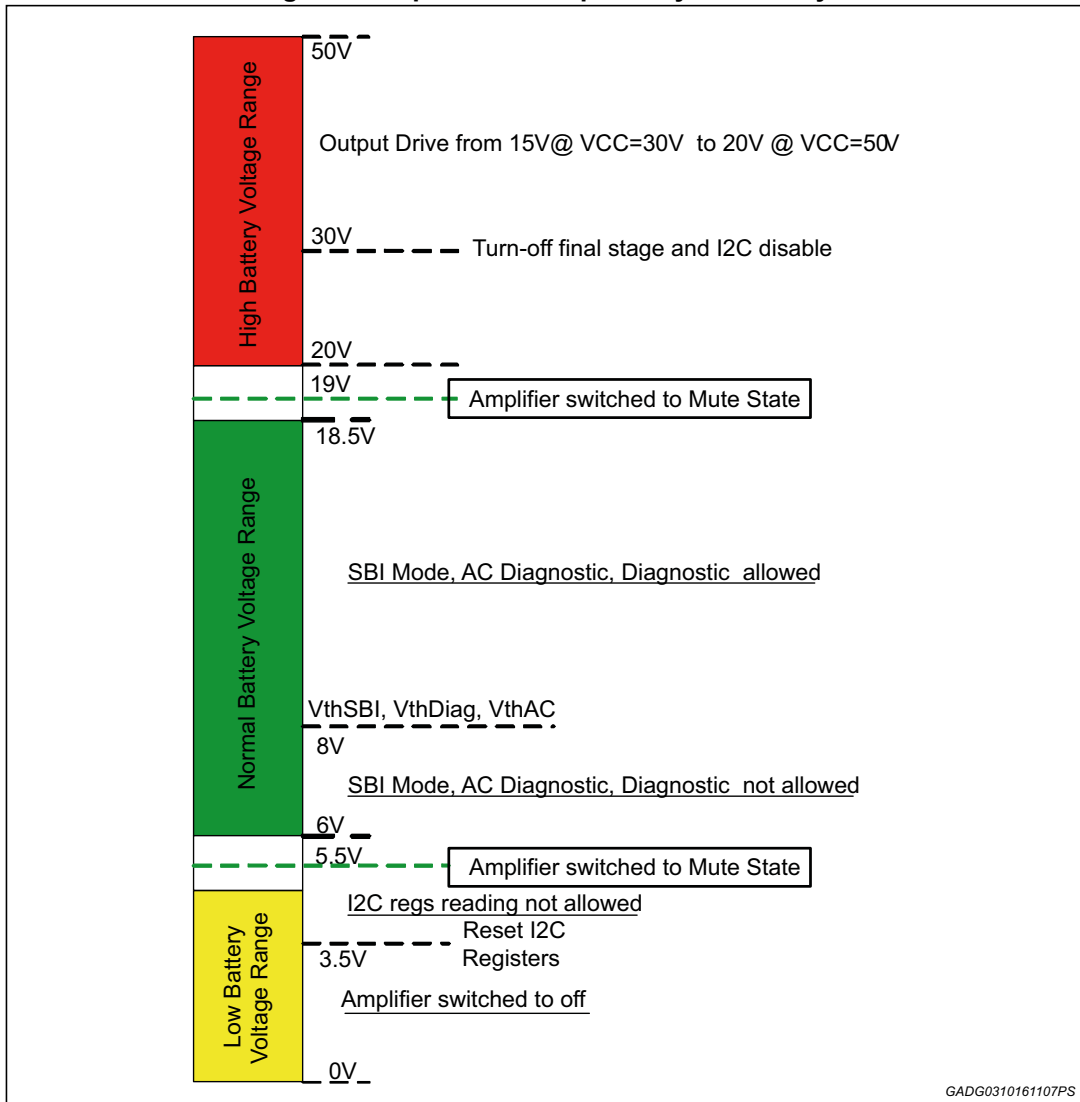


GAPGPS03069

## 5 Operation compatibility vs. battery

Here below the operation compatibility vs. the battery value is shown. For each battery voltage range, only a limited number of functions are available as it is shown below:

**Figure 32. Operation compatibility vs. battery**





## 6 Functional description

### 6.1 Voltage regulators timing

Pins D3V3 and A3V3 are respectively digital and analog internal regulators outputs. The D3V3 rises right after the STBY pin is at the logical value "1" and its rising time depends on the filter capacitor; the minimum value suggested for this filter is 4.7  $\mu$ F.

The A3V3 rises after any command that moves the amplifier from ECO - mode; the rising time depends on the combined effect of the external capacitor on the pin and of an internal 2 ms ramp: if the capacitor value is 22  $\mu$ F or lower, the internal ramp effect is dominant and the rising time will be about 2 ms. On the other hand, when the capacitor has a higher value, the rise time will be higher as well. The suggested value for this capacitor is 22  $\mu$ F at least.

### 6.2 Turn-on diagnostic description

The turn-on diagnostic is triggered on the rising edge of bit IB4 D0 when IB7 D0 is "0". This happens when the amplifier is in ECO - mode. It is possible to run one or more turn-on diagnostic sequences according to the following procedure:

1. wait the previous cycle is over
2. read the data bytes DB1, DB2, DB3 and DB4

Please note that all these instructions must be sent while the amplifier is still in ECO - mode (IB7 D0 = "0"), otherwise they won't be executed.

Turn-on diagnostic does not start if  $V_{CC}$  is below 8 V or one of the muting condition is present, (low battery mute, high voltage mute, PLL-unlock mute, thermal mute, hardware pin mute).

*Note:* The diagnostic enable bit (IB4 D0) must be set before the amplifier mode bit (IB7 D0). DB1, DB2, DB3 must be read before DB4 (after DB4 is read the DB1-2-3-4 are reset).

The detected faults are here described:

**Soft Short to GND:** it detects the presence of a resistor (see [Table 5](#) in "Turn-on diagnostic" section) connected between an output and ground, which could result in a wrong open load or short across load diagnostic result (causing an anomalous current consumption in some cases).

**Soft Short to VS:** it detects the presence of a resistor (see [Table 5](#) in "Turn-on diagnostic" section) connected between an output and battery, which could result in a wrong open load or short across load diagnostic result (causing an anomalous current consumption in some cases).

**Short to GND:** it detects the hard connection between an output and ground. The value of the short is able to pull the output between 1.5 V and ground.

**Short to VS:** it detects the hard connection between an output and battery. The value of the short is able to pull the output between (battery - 1.5 V) and battery.

**Short across the speaker:** it detects the hard connection across the speaker that is below a certain value. This value guarantees that the IC is able to drive any speaker configuration within the range specified in the datasheet.

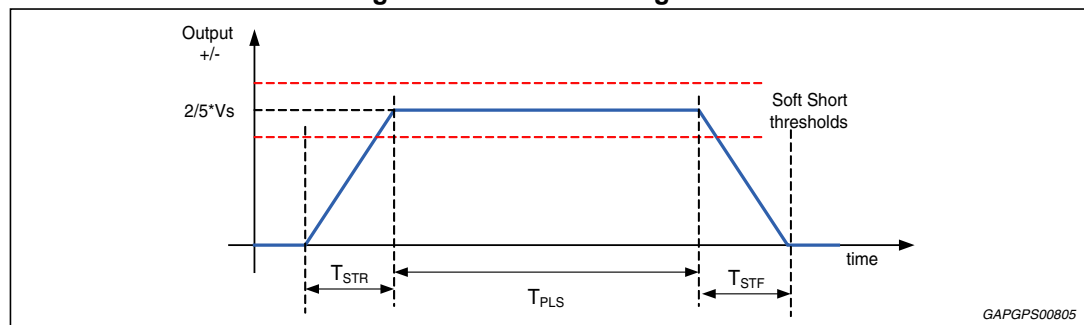
**Open Load:** it detects a non connected speaker condition.

The diagnostic's results are stored into DB1, DB2, DB3 and DB4 data registers (one for each channel) after the diagnostic is over.

The flow of the diagnostic includes some steps as described below.

- During the first part, the soft-short evaluation is performed. The outputs and an internal reference line are pulled up to a voltage of  $2/5 \cdot V_{battery}$  in a time  $T_{STR}$  and then compared for a time  $T_{PLS}$ . During the plateau time, the comparator outputs are read from the digital part. The outputs are then pulled down to zero (see Figure 33). The A3V3 supply is 0V and the output stage is in tri-state during this phase.

**Figure 33. Soft short diagnostic**



- If a soft short is detected, the short to GND/VCC evaluation follows. Pin A3V3 goes up as the amplifier stage is turned on; the power and the outputs are risen up to  $1/2 \cdot V_{battery}$  and then compared to  $(V_{battery} - 1.5 V)$  and  $1.5 V$  for a time  $T_{PLS}$ . At the end of the plateau ( $T_{PLS}$ ) output and A3V3 go back to 0V and the results obtained are written into the I<sup>2</sup>C Bus registers once the diagnostic is over. For soft short resistance above the defined thresholds, the normal, short or open load recognition is guaranteed.

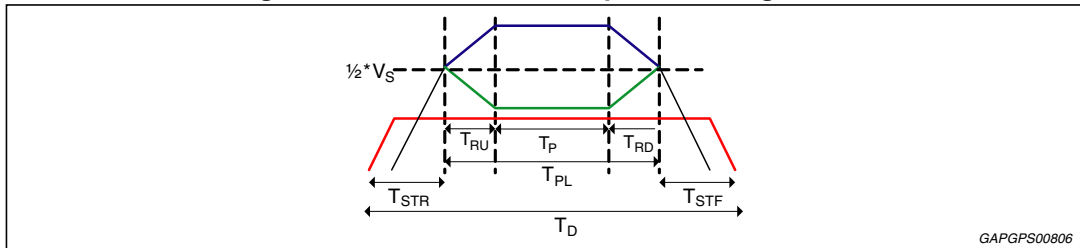
In case the short to VCC or GND is detected during this phase a '1' is written in DBx-D1/D0 (VCC/GND) but not in DBx-D6. In case the hard short is not detected a '1' is written all DBx-D6.

The turn-on diagnostic is then completed and the amplifier goes back to the ECO - mode.

- However, if a soft short is not detected, then we can also exclude the Short to Vs/GND, and don't need to be checked. In this case, short across the speaker and the open load evaluation can be performed. Pin A3V3 goes up as the amplifier stage is turned on and the outputs are risen up to  $1/2 \cdot V_{battery}$ . A first pulse for "Short load detection" is done: exploiting the presence of a D/A converter, a subsonic (inaudible) voltage pulse is digitally and internally generated and converted. The pulse amplitude increasing is stopped when the current flowing through the speaker  $I_{speaker}$  is the same as a prefixed one  $I_{high}$  (high current) or because it reaches the maximum value permitted. Since the differential output voltage  $V_o$  is well known, it is possible to keep monitored the value of the connected speaker during the transition and plateau. In the case the  $I_{speaker}$  will get to an higher value then  $I_{high}$ ,  $V_o < V_{short}$  (short circuit threshold) the result is short load (DBx - D3 = '1'), otherwise it is normal load (DBx - D3 = '0'); when  $I_{speaker}$  does not reach  $I_{high}$  the turn-on diagnostic is not completed yet because the result could be still normal or open load.
- This is called "Open load detection". If IB4 D1/D2 = 1 the power DMOS need to be changed again: the outputs are pulled down to zero, the DMOS are switched and then the outputs raised up to  $1/2 \cdot V_{battery}$  again. This sequence is done in order to avoid any pop noise during the power set. The procedure is the same as the previous case or in

case of IB4 (D1/D2) = 0. The pulse amplitude is stopped when the current flowing through the speaker  $I_{speaker}$  is the same as prefixed one  $I_{low}$  (low current) or because it reaches the maximum value permitted. When  $I_{speaker}$  reaches the value  $I_{low}$  and  $V_o < V_{open}$  (open load threshold) then the speaker can be considered as a normal load (DBx-D2='0'). In all other cases the result will be open load (DBx-D2='1') (see [Figure 34](#)).

**Figure 34. Short circuit and open load diagnostic**

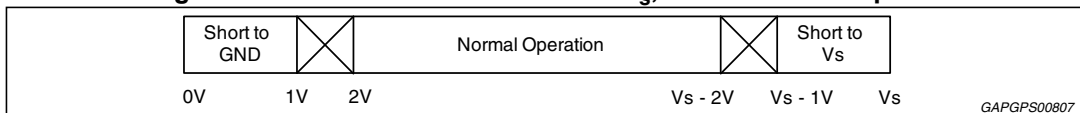


The whole diagnostic time depends on the number of pulses that are done. At least two pulses are done, but they could be three in case of open load. The values inserted into the [Table 6](#), are calculated basing on  $F_s = 48000$  Hz.

In all cases the fault is sent out to the registers only if it is stable throughout the whole plateau period. If this condition is not respected, any possible misconnections (Soft-short, Short to VCC/GND, Short Across or Open Load) won't be reported. The faults for the turn-on diagnostic are written in DB (1, 2, 3, 4) (D1, D2, D3, D4) (a byte for each channel and a bit for each fault). They are consistent if  $DB0 D6 = "1"$ . After a reading the data byte are reset.

The fault-detection thresholds for short to GND/  $V_s$  remain unchanged independently from the gain setting. They are as in [Figure 35](#).

**Figure 35. Short to GND and short to  $V_s$ , threshold description**



Concerning the short across the speaker / open speaker, the threshold changes from line driver mode and speaker mode diagnostic setting, as load expected are pretty different (either normal speaker's impedance or high impedance). Speaker or line driver mode is selectable from IB4 D2 for channels 1 and 3 and IB4 D1 for channel 2 and 4. The values in case of speaker mode are as in [Figure 36](#). The same thresholds will change as in [Figure 37](#), if line driver mode diagnostic is selected.

**Figure 36. Short across the speaker and open load threshold description, in speaker mode**

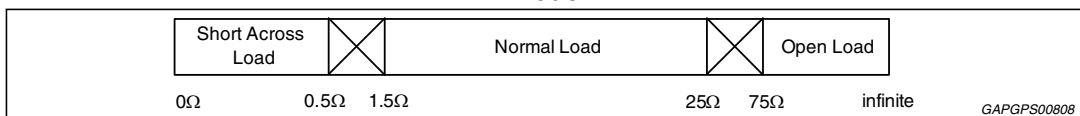


Figure 37. Short across the speaker and open load threshold description, line driver mode

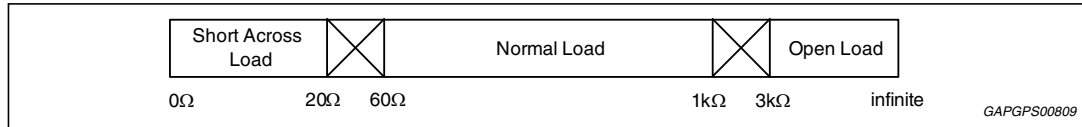


Table 6. Start-up pulse typical timings (F<sub>s</sub> = 48 kHz)

| Symbol                           | Parameter  | Min | Typ                | Max                  | Unit | Note   |
|----------------------------------|--|-----|--------------------|----------------------|------|--|
| T <sub>STR</sub>                 | Time to rise the outputs from 0V to a certain battery's percentage     | -   | 10 (+ 10)          | -                    | ms   | When A3V3 goes up, the reported number has to be added   |
| T <sub>STF</sub>                 | Time to rise the outputs from a certain battery's percentage to 0V     | -   | 10 (+ 10)          | -                    | ms   | When A3V3 goes down, the reported number has to be added   |
| T <sub>PLS</sub>                 | Plateau time for soft-short and short to VCC/GND diagnostic            | -   | 80                 | -                    | ms   | This time parameter is load independent and is not stretchable setting bit IB6[7:5]                          |
| T <sub>P</sub>                   | Plateau time for short circuit or open load diagnostic detection phase | -   | 80 <sup>(1)</sup>  | -                    | ms   | T <sub>P</sub> = 86 ms · X<br>when 140 ms - 2 · T <sub>RU</sub> > 80 ms                                      |
|                                  |  | -   |                    | -                    |      | T <sub>P</sub> = (140 ms - 2 · T <sub>RU</sub> ) · X<br>when 140 ms - 2 · T <sub>RU</sub> < 80 ms            |
| T <sub>PL</sub>                  | Pulse time for short circuit or open load diagnostic detection phase   | -   | 120                | 122.4 <sup>(2)</sup> | ms   | T <sub>P</sub> = (2 · T <sub>RU</sub> + T <sub>P</sub> ) · X   |
| X                                | Multiplier factor in case of diagnostic active                         | -   | 1,2,4,8            | -                    | -    | IB6[7:5] setting   |
| T <sub>RU</sub> =T <sub>RD</sub> | Ramp-up and ramp-down diagnostic pulse's time                          | -   | 5.8 <sup>(3)</sup> | -                    | -    | 2 ohm case   |
|                                  |  | -   | 8.3 <sup>(3)</sup> | -                    | ms   | 4 ohm case   |
| T <sub>SS</sub>                  | Soft-short diagnostic time   | -   | 100                | -                    | ms   | Output rising time + Output falling time + plateau time (no A3V3)  |
| T <sub>HS</sub>                  | Short to VCC and GND diagnostic time                                   | -   | 120                | -                    | ms   | A3V3 rising and falling time (10 ms x2) + Output rising and falling time + plateau time                      |
| T <sub>D</sub>                   | Short load and open load diagnostic time                               | -   | 148                | -                    | ms   | 2 ohm case (X=1)   |
|                                  |  | -   | 160                | -                    | ms   | 4 ohm case (X=1)   |
| T <sub>tot</sub>                 | Total diagnostic time  | -   | 260                | -                    | ms   | 4 ohm load and no faults (T <sub>tot</sub> = T <sub>SS</sub> + T <sub>D</sub> )                              |
|                                  |  | -   | 220                | -                    | ms   | Hard or soft short to supplies (T <sub>tot</sub> = T <sub>SS</sub> + T <sub>HS</sub> )                       |
|                                  |  | -   | 420                | -                    | ms   | Open load (X = 1, IB4 (D1/D2) = 0)<br>T <sub>tot</sub> = T <sub>SS</sub> + T <sub>D1</sub> + T <sub>D2</sub> |

**Table 6. Start-up pulse typical timings ( $F_s = 48$  kHz) (continued)**

| Symbol     | Parameter                             | Min | Typ | Max | Unit | Note                 |
|------------|---------------------------------------|-----|-----|-----|------|----------------------|
| $I_{high}$ | Test current for the short load pulse | -   | 200 | -   | mA   | For speaker mode     |
|            |                                       |     | 40  |     |      | For line driver mode |
| $I_{low}$  | Test current for the open load pulse  | -   | 40  | -   | mA   | For speaker mode     |
|            |                                       |     | 2   |     |      | For line driver mode |

1. For typical loudspeaker of 2 and 4 ohm.
2. These numbers are evaluated in simulation.
3. Typical values for 4  $\Omega$  and 2  $\Omega$  and zero offset. These numbers depend on the loudspeaker and also on the intrinsic offset of the amplifier. For 2  $\Omega$  loudspeaker, -30 mV offset and  $F_s = 48$  kHz  $T_{RU} = 21.2$  ms; for 4  $\Omega$  and same surrounding conditions  $T_{RU} = 22.1$  ms. Under these conditions  $T_{PL} = 122.4$  ms for 2  $\Omega$  and 124.4 for 4  $\Omega$ . For higher values the number are not reported here.

When the amplifier is biased and the IB4 D0 = "1", the permanent diagnostic is enabled. The turn-on diagnostic state is held until an over current event is triggered. When this happens, a new diagnostic cycle can start.

### 6.3 Permanent diagnostic

The detectable faults are (see [Table 5](#) for definitions):

- Short to GND
- Short to Vs
- Short across the speaker

Then following additional features are also provided:

- Input offset detection
- AC diagnostic

When an over current event occurs, TDA7803A has two different cycles that could react with:

- Restart cycle: it is a 2 ms pulse. During this period a check of the output is performed.
- Plateau cycle: it is an 80 ms cycle. During this period a check of the outputs is performed and the results of diagnostic analysis are written into the I<sup>2</sup>C bus.

TDA7803A has two different operating behaviors when an over current event is detected:

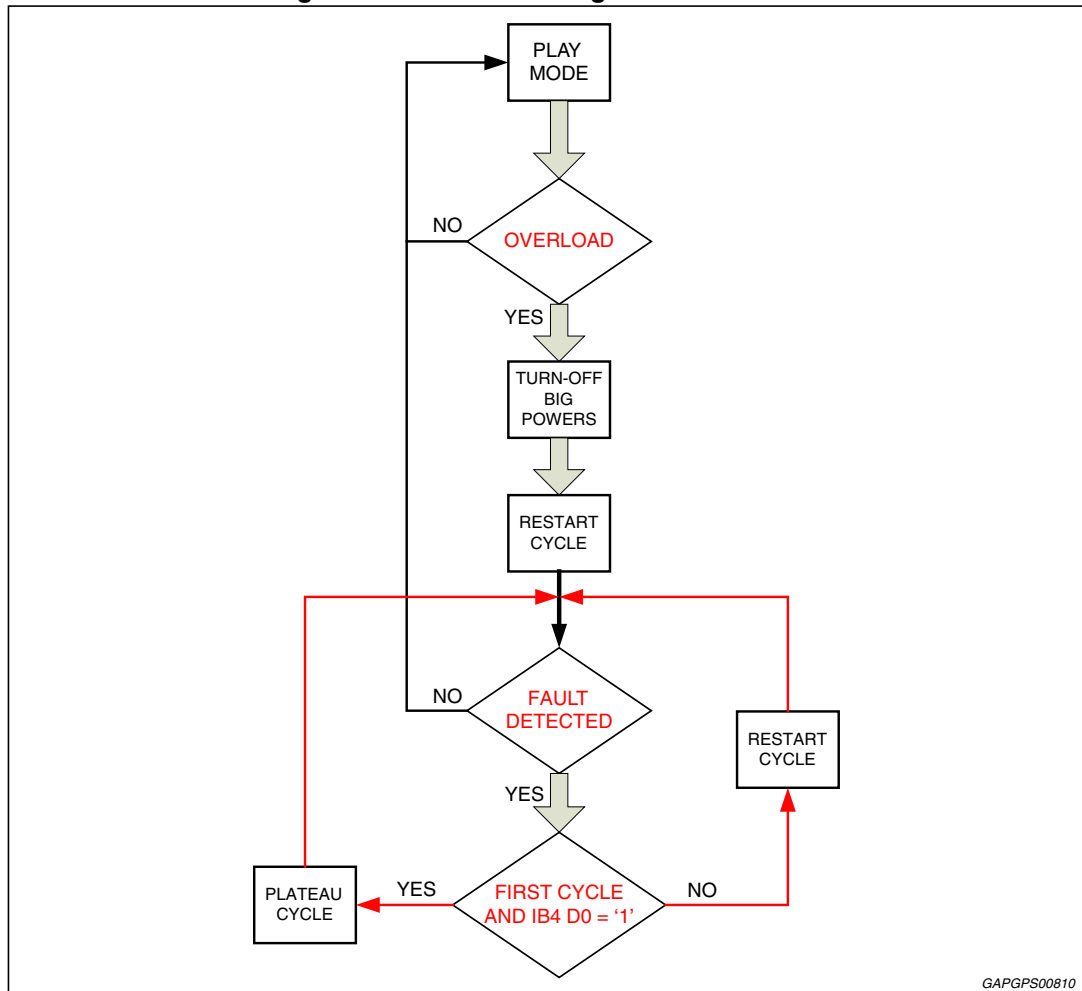
- Restart mode, (IB4 D0 = "0"). The diagnostic is not enabled. Each audio channel operates independently from each other. If any of the above mentioned faults occurs, only the channel(s) where the fault happened is shut down. The diagnostic performs restart cycles every 2 ms until the fault condition is present. The amplifier restarts in play only once the overload is removed. In Restart mode reporting diagnostic results are turned off and the corresponding bits in the channels' data byte registers will be reset accordingly.
- Diagnostic mode, (IB4 D0 = "1"). It is enabled via I<sup>2</sup>C and self activated if an output overload occurs to the speaker outputs. If any of the above mentioned faults occurs,

only the channel(s) where the fault happened is shut down. Once activated, the diagnostic procedure develops as below:

- The diagnostic performs one restart cycle in order to avoid momentary re-circulation spikes which could give erroneous results. If a normal state (no overloads) is detected, the channel returns back active.
- Instead, if after the restart cycle, the overload is still detected, then the diagnostic performs a plateau cycle.
- After the plateau cycle, a restart cycle is going to be performed every 2 ms until the fault condition is removed. The data acquired from the plateau cycle are stored and can be read from the microprocessor. If the fault condition persists, a new plateau cycle can be programmed from I<sup>2</sup>C simply by reading. This ensures continuous diagnostic throughout the car-radio operating time.

For a more immediate understanding, the permanent diagnostic's flowchart is as in *Figure 38*.

**Figure 38. Permanent diagnostic flow-chart**



When a plateau cycle is done during the permanent diagnostic the bit D5 of byte connected to the channel where the overload occurred is set to "1". If all the bits related to the diagnostic are "0", then the fault has possibly been removed or not detected. Eventually, an

over current event could have been occurred on a loudspeaker with a very high inductance and it took more than 2 ms to get the current reduced.

A plateau cycle can be recalled by means of a reading procedure of bytes DB1/2/3/4 when the amplifier is performing the restart cycle. As for the turn-on diagnostic, when DB4 is read DB1/2/3/4 are reset, therefore the incremental reading is suggested in order not to miss any data.

Please note that if the over-current cause was removed before the reading the plateau cycle cannot restart.

## 6.4 AC diagnostic

The goal of this feature is to detect accidental disconnection of tweeters in 2-way speaker and, more in general, the presence of capacitive (AC) coupled load. This diagnostic is based on the notion that the overall speaker's impedance (woofer + parallel tweeter) tends to increase towards high frequencies if the tweeter gets disconnected. This happens because the remaining speaker (woofer) would be out of its operating frequency's range (high impedance).

To determine the load impedance, a sine wave tone of a suitable frequency should be provided to the output pins and the AC diagnostic is able to determine if the tweeter is connected or not. The tweeter is not connected if for four consecutive sine waves the current threshold on the load is not crossed.

AC diagnostic is managed by I<sup>2</sup>C commands. When IB4 D3 = "1", the AC diagnostic is enabled; IB4 D4 is used to choose the current level threshold to be used as a reference for the test.

The results of the AC diagnostic test are stored in DB5 D3..6. It is written "1" if the tweeter for that channel is present.

The AC diagnostic is able to give the correct results only if the input signal  $V_{out} < V_s - 4V$ . User knows that this condition is verified by reading "0" in DB5 D7. When DB5 D7 = "0", it means that the test's signal was too high.

## 6.5 Input offset detector

Input offset detector aim is to avoid any possible offset that could come from the audio signal source through I2S/TDM input stream.

For this purpose the TDA7803A input offset detector performs an evaluation of the input signal and calculates if an offset with values higher than -19.5 dBFS is present.

Moreover, if high pass filter function is selected by means of IB3-d0, the TDA7803A will eliminate the input offset giving a complete robustness to any disturbance or malfunction coming from external audio chain blocks.

The input offset detector and high-pass filtering can be used during PLAY mode.

## 6.6 Double faults

Faults can occur simultaneously. When this happens, faults are read out in accordance with the priority table ([Table 7](#)).

Please note that a "short to GND" and a "short to  $V_S$ " can be simultaneously read only when an open load is present; however it would mean three faults at the same time, which is not covered by TDA7803A.

**Table 7. Double faults priority**

| -                                     | Soft short to GND <sup>(1)</sup> | Soft short to $V_S$ <sup>(1)</sup> | Short to GND | Short to $V_S$ | Short across load   | Open load <sup>(1)</sup> |
|---------------------------------------|----------------------------------|------------------------------------|--------------|----------------|---------------------|--------------------------|
| <b>Soft short to GND</b>              | Soft Short to GND                | /                                  | Short to GND | /              | Soft Short to GND   | Soft Short to GND        |
| <b>Soft short to <math>V_S</math></b> | /                                | Soft Short to $V_S$                | /            | Short to $V_S$ | Soft Short to $V_S$ | Soft Short to $V_S$      |
| <b>Short to GND</b>                   | Short to GND                     | /                                  | Short to GND | /              | Short to GND        | Short to GND             |
| <b>Short to <math>V_S</math></b>      | /                                | Short to $V_S$                     | /            | Short to $V_S$ | Short to $V_S$      | Short to $V_S$           |
| <b>Short across load</b>              | /                                | /                                  | /            | /              | Short across load   | N.A.                     |
| <b>Open load</b>                      | /                                | /                                  | /            | /              | /                   | Open Load                |

1. Open load, soft short to GND and soft short to  $V_S$  are only available for the turn-on diagnostic; in fact the permanent diagnostic can be triggered from an over current event, and none of these events can be the cause of an over current.

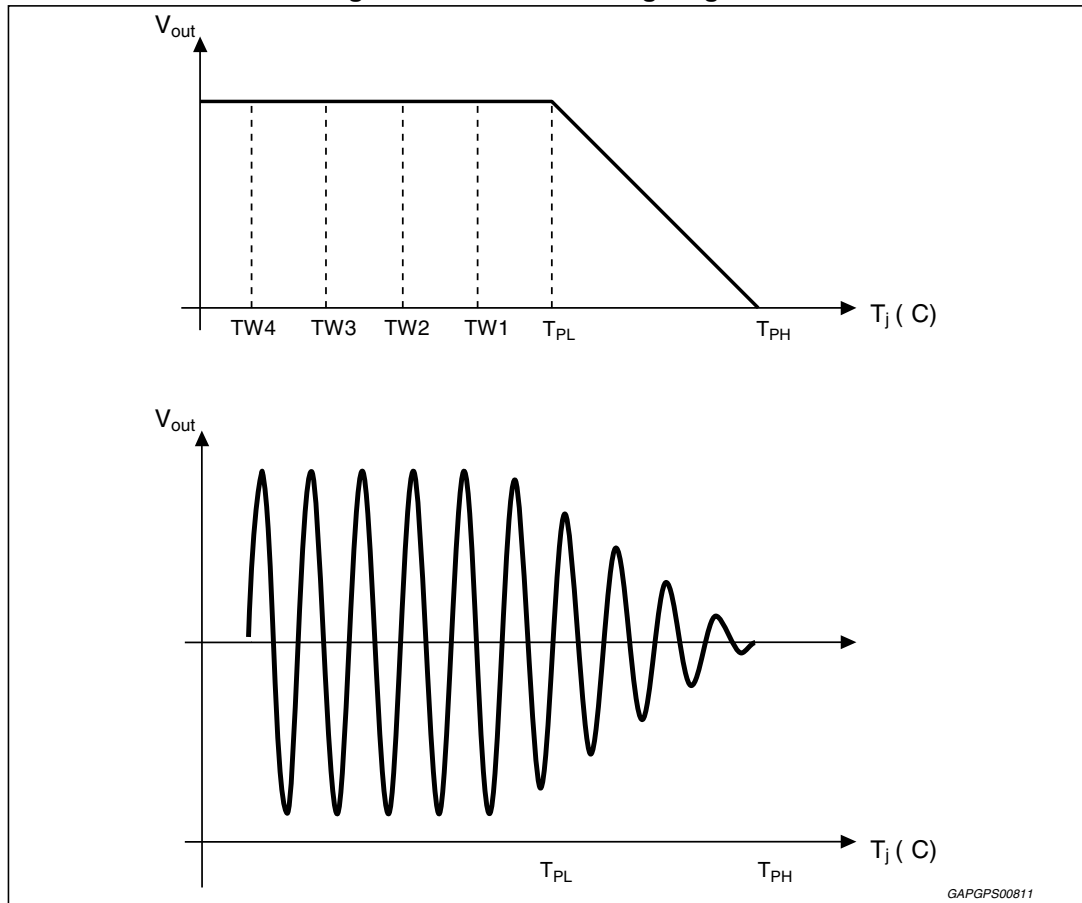
## 6.7 Thermal protection

The TDA7803A has four thermal warning thresholds ( $T_{w1}$ ,  $T_{w2}$ ,  $T_{w3}$ ,  $T_{w4}$ ) which are stored in I<sup>2</sup>C data bytes. Only one of the thermal warnings can be sent to the pin CDdiag and it is selectable via I<sup>2</sup>C bus.

A temperature dependent mute function is implemented in order to protect the junction against over temperature events and prevent the IC from sound quality degradation. For temperatures higher than  $T_{pl}$ , the device is gradually forced to the mute state. When the temperature is  $T_{pl}$  the output signal is attenuated by 0.5 dB, while at the  $T_{ph}$  the attenuation is >60 dB. The distortion is kept low throughout the whole muting transition. The thermal protection's behaviour is shown in [Figure 39](#).



Figure 39. Thermal muting diagram



### 6.8 Voltage monitoring feature and ADC characteristics

Through this feature it is possible to monitor the  $V_{CC}$  value on I<sup>2</sup>C data line; below a short description of the limits, granularity, frequency of operation of this function.

The result of  $V_{CC}$  sensing voltage range is 5 V - 19 V; the  $V_{CC}$  - ADC value conversion is expressed in the table below. The  $V_{CC}$  sensing voltage range is 5 V - 19 V (with a typical reset intervention at 4.8 V), with a precision of 200 mV effective (considering 1 bit of noise). The output update frequency is 2 MHz.

So, in order to exploit this function, the user should address only the DB7 with the following subaddress: '10011010' (\*) and then read the data contained in DB7.

(\*) '1' is the auto increment bit.

The  $V_{CC}$  value is expressed by 8 bits binary code:

Table 8.  $V_{CC}$  value express by 8 bit with thermometric code

| $V_{CC}$ | ADC value |
|----------|-----------|
| 5 V      | 01000001  |
| 6 V      | 01010000  |
| 7 V      | 01011101  |

**Table 8. V<sub>CC</sub> value express by 8 bit with thermometric code (continued)**

| V <sub>CC</sub> | ADC value |
|-----------------|-----------|
| 8 V             | 01101011  |
| 9 V             | 01111001  |
| 10 V            | 10000110  |
| 11 V            | 10010100  |
| 12 V            | 10100010  |
| 13 V            | 10101111  |
| 14 V            | 10111101  |
| 14.4 V          | 11000010  |
| 15 V            | 11001011  |
| 16 V            | 11011001  |
| 17 V            | 11100110  |
| 18 V            | 11110100  |
| 19 V            | 11111111  |

## 6.9 Mute management

The transition Mute → Play can happen once the device is in amplifier mode and IB2-D3/D4 = "1" or after it has been put in mute for one of the causes listed in [Table 9](#). It is done by means of a digital ramp whose time constant is programmable by IB2 D7, D6 and D5 bits.

The transition Play → Mute occurs when certain conditions are verified and it can be Digital or Analog. An overview of all the events that might happen is reported in the [Table 9](#).

**Table 9. Transition play to mute strategy**

| Cause of transition<br>Play → Mute | When it happens  | Analog | Digital  |
|------------------------------------|--|--------|--|
| I <sup>2</sup> C instruction       | When bit IB2 D4,D3 = "0" (Mute command)  | No     | Yes<br>Timing for transition is fixed by IB2 D7, D6, D5  |
| Low battery mute                   | When there is a battery dip and the Vs goes below the auto mute threshold (selectable by IB2 D1) | Yes    | IB2-D2 = 0: Yes<br>IB2-D2 = 1: Disable<br><br>If digital mute is enabled, timing for transition is fixed by IB2 D7-D6-D5 |
| High battery mute                  | When Vs ramp up above 19V  | Yes    | No   |
| PLL un-lock                        | The PLL lock detector goes down for some reason  | Yes    | Not possible because in case of un-lock, digital core is reset so not working  |
| Thermal mute                       | When Tw1 is "1"  | Yes    | Disabled   |
| Tristate command                   | No   | Yes    | Timing for transition is fixed by IB2-D7, D6, D5   |

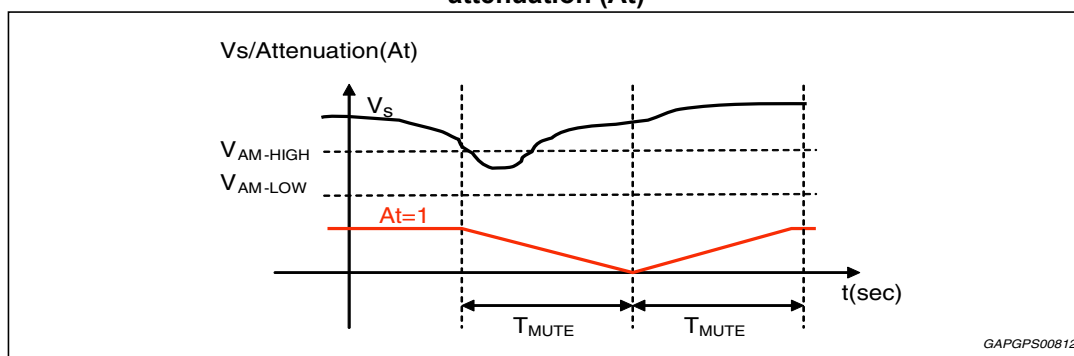
### 6.9.1 Auto-mute threshold

The device in play mode is put in mute when the supply voltage gets below the  $V_{lowM}$  threshold.

The muting strategy for this kind of event is reported in *Figure 40*. Both analog and digital mute start when the supply voltage is below  $V_{lowM\_HIGH}$ . The digital mute transition lasts a period  $T_{MUTE}$ . The analog mute attenuation is proportional to  $V_s$ ; when  $V_s$  is at  $V_{lowM\_LOW}$  the mute attenuation is  $A_M$ .

Note that, once it is engaged, the digital mute procedure will apply the  $A_M$  attenuation. It is not possible to stop it and move the device to play mode in advance. The concept of this procedure is to avoid that fast oscillation on  $V_s$  can generate fast oscillation on the output.

**Figure 40. Low voltage mute attenuation, supply voltage variation ( $V_s$ ); result digital attenuation ( $A_t$ )**



When the battery goes below the auto-mute low threshold, it is possible to disable the digital muting if IB2 D2 = "1". In this case the mute will be only analog.

The digital mute is also disabled during the turn-on diagnostic.

### 6.9.2 Mute and unmute commutation time

**Table 10. Mute and unmute commutation time**

| Parameter                        | Test condition   | Typ. | Unit |
|----------------------------------|--|------|------|
| Mute and unmute commutation time | Programmable by I <sup>2</sup> C bus register<br>IB2(7:5) $F_s = 44.1$ kHz | 1.45 | ms   |
|                                  |  | 6    |      |
|                                  |  | 12   |      |
|                                  |  | 25   |      |
|                                  |  | 45   |      |
|                                  |  | 90   |      |
|                                  |  | 180  |      |
|                                  |  | 370  |      |

### 6.10 Class SBI - Improved high efficiency principle

TDA7803A embeds an improved high efficiency feature that minimizes the power dissipated through the heat sink basing on the musical signal characteristic. All channels are connected to a common bar by means of four power switches. When an input signal goes

under a threshold that depends on the  $V_s$  level, the switch will short the corresponding output to the common bar in such a way that it can exchange current with the other channel. The dissipation reduction can be up to 50% compared to standard AB class.

The TDA7803A sets the high efficiency mode by default, but it can be changed through the bits IB0 D3, D2, D1 and D0.

## 6.11 High power and parallel mode configuration

The TDA7803A is able to support high power applications thanks to its characteristics. Whenever a higher output power with low impedance loads is needed (i.e. 2ohm load), it is recommended to enable the current capability enhancer through the IB5[4:1] register.

When needed, the TDA7803A can also support the parallel mode configuration. The functionality is allowed since the two output powers gates (master and slave) are shorted together and only one of the two drivers is effectively working (the master). At the same time the outputs are shorted on the application in such a way to minimize the resistive path.

The I2C bits IB6-d2,d3 are reserved for this function, as it follows:

Bits (D3, D2):

- "00" single channel mode configuration for all channels;
- "01" (ch1 and ch2): parallel mode configuration, (ch3 and ch4): single channel mode configuration;
- "10" (ch1 and ch2): single channel mode configuration, (ch3 and ch4): parallel mode configuration;
- "11" all channels set in parallel mode configuration.

The master channels are channel 1 when ch1 and ch2 are configured in parallel mode, and channel 3 when ch3 and ch4 are configured in parallel mode.

## 6.12 Power on reset threshold

When  $V_{CC}$  is lower than 4 V the integrity of I2C registers content is not guaranteed. In this case the I2C registers are reset and the TDA7803A is put in Eco-mode state. This event is communicated with a "0" on DB0-d7 I2C bit.

## 7 Additional features

### 7.1 Noise gating

Noise gating is an automatic noise reduction feature that activates when output signal reaches inaudible levels.

When input signal level falls below -102dBFs the system activity is automatically optimized in order to limit the output noise level as much as possible and permits the full audio chain to bring very low noise level on the output speakers.

The noise gating process has a 100ms observation time before turning on, in order to avoid spurious activations.

The feature is enabled by default and can be disabled selecting IB3-d2.

### 7.2 Tri-state mode

It can be activated by IB0-4..7= 1. It allows to turn-off one or more channels by individually disabling it or them by turning to a safety mode status (high impedance) whenever an overload is detected by the diagnostics, in order to prevent any other inconveniences. All the other sections not interested by a fault will remain completely operational. The tri-state mode has to be used with the IC preventively set to Standard Class-AB mode (IB0-D0..3 = 1). Not to be used as an alternative to "IB7-D0" command (amp on/off during normal operation)

## 8 I<sup>2</sup>S and TDM bus interface

The audio input port is a three/four-wire synchronous serial interface that can operate only as Slave. Pins SD13 and SD24 are the serial data inputs. The audio data format accepted from TDA7803A is the I<sup>2</sup>S standard.

Input data can also be sent in time division multiplexed (TDM). Pins SCK (bit clock) and WS (frame select) complete the I<sup>2</sup>S interface.

When I2S-clk is lost during amplifier operations a protection circuit acts and puts the amplifier in a safe condition: amplifier short circuit protections are guaranteed, dump protection is guaranteed, signal is muted and outputs bias is under control.

In order to avoid other side effects user should put the amplifier in standby moving STBY pin to 0 V.

### 8.1 I<sup>2</sup>S and TDM input data frame format

The audio data word length for each channel may be up to 24 bit. Either for I2S or TDM mode, the frame for each channel has 32 bit length.

The following table summarizes the frequencies configurations.

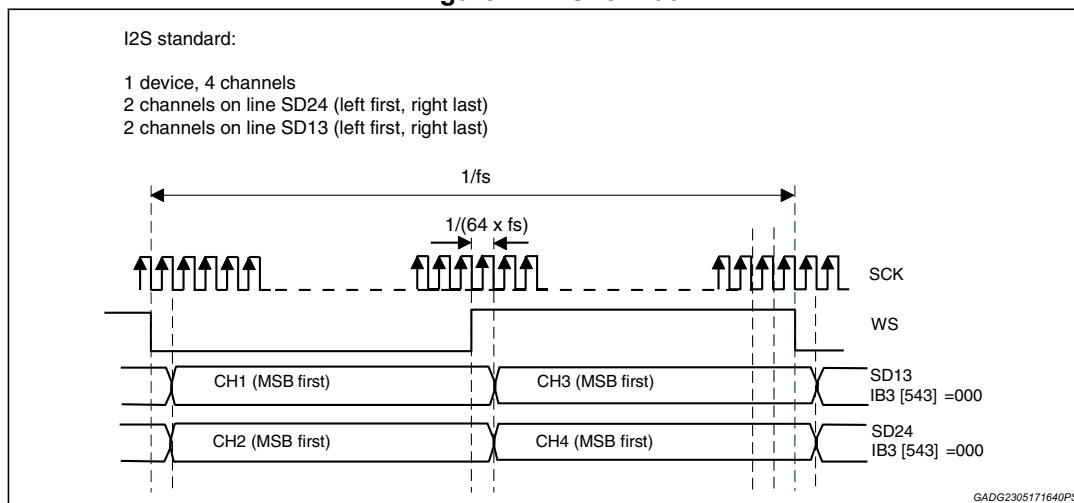
**Table 11. System input frequencies**

| Frequency sampling<br>(Fs) | System clock frequency (f <sub>SCK</sub> ), (MHz) |         |               |
|----------------------------|---|---------|---------------|
|                            | I <sup>2</sup> S standard                         | TDM 4ch | TDM 8ch/8+8ch |
| 44.1 (kHz)                 | 2.8224  | 5.6448  | 11.2896       |
| 48 (kHz)                   | 3.072   | 6.144   | 12.288        |
| 96 (kHz)                   | 6.144   | 12.288  | 24.576        |
| 192 (kHz)                  | 12.288  | 24.576  | N.A.          |

## 8.2 I<sup>2</sup>S input data format

The TDA7803A accepts I<sup>2</sup>S standard interface format as in *Figure 41* and the I<sup>2</sup>C bit configuration is IB3 [D5,D4,D3] = "000".

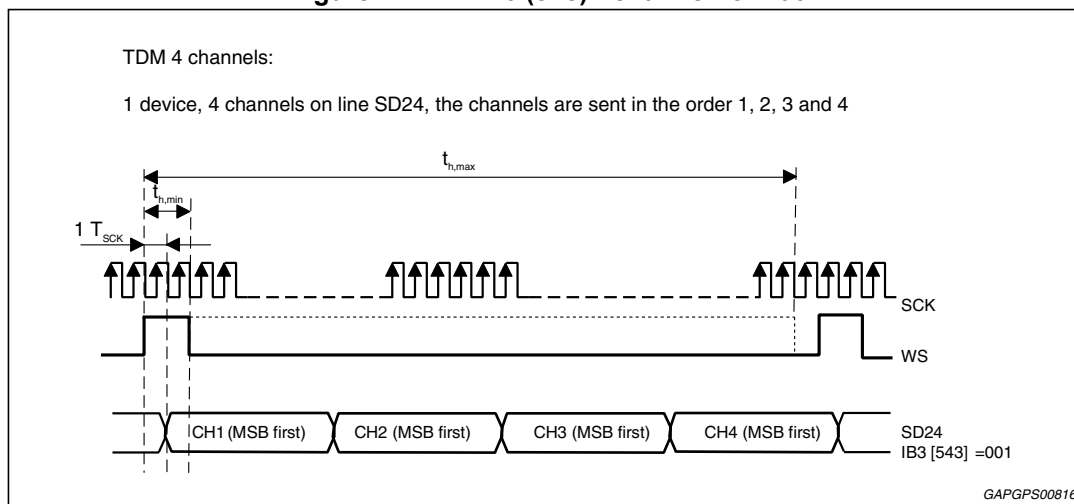
Figure 41. I<sup>2</sup>S format



## 8.3 TDM input data format

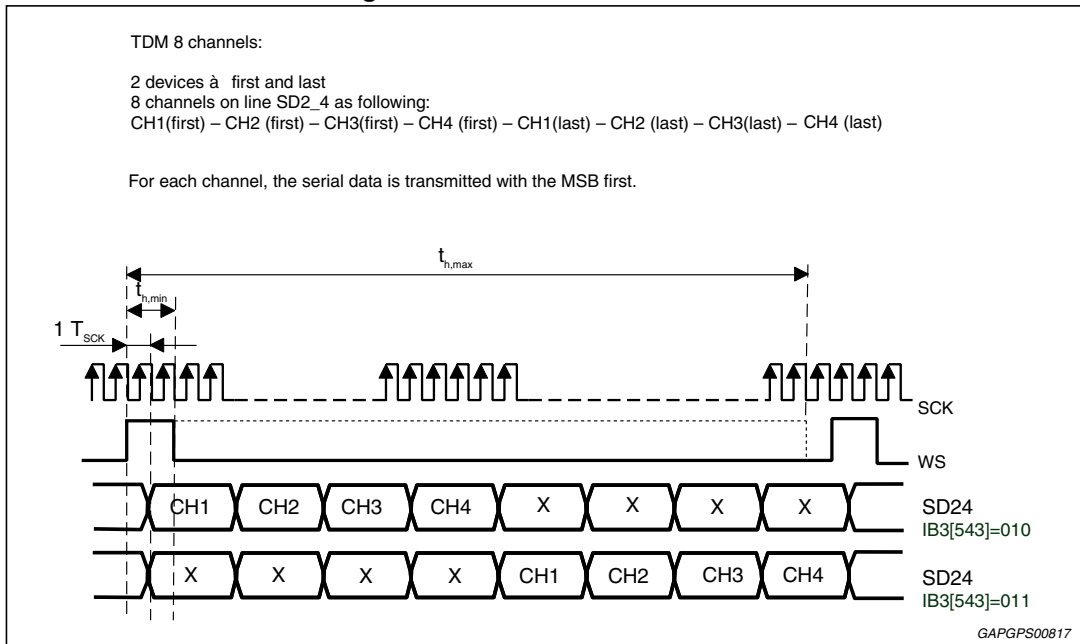
TDM 4-channel is allowed for TDA7803A and it is as in *Figure 42*. All the channels are sent on the audio data line SD24. The channel's order is 1, 2, 3 and 4. The I<sup>2</sup>C bit configuration is IB3 [D5, D4, D3] = "001".

Figure 42. TDM 16 (8+8) - channel format



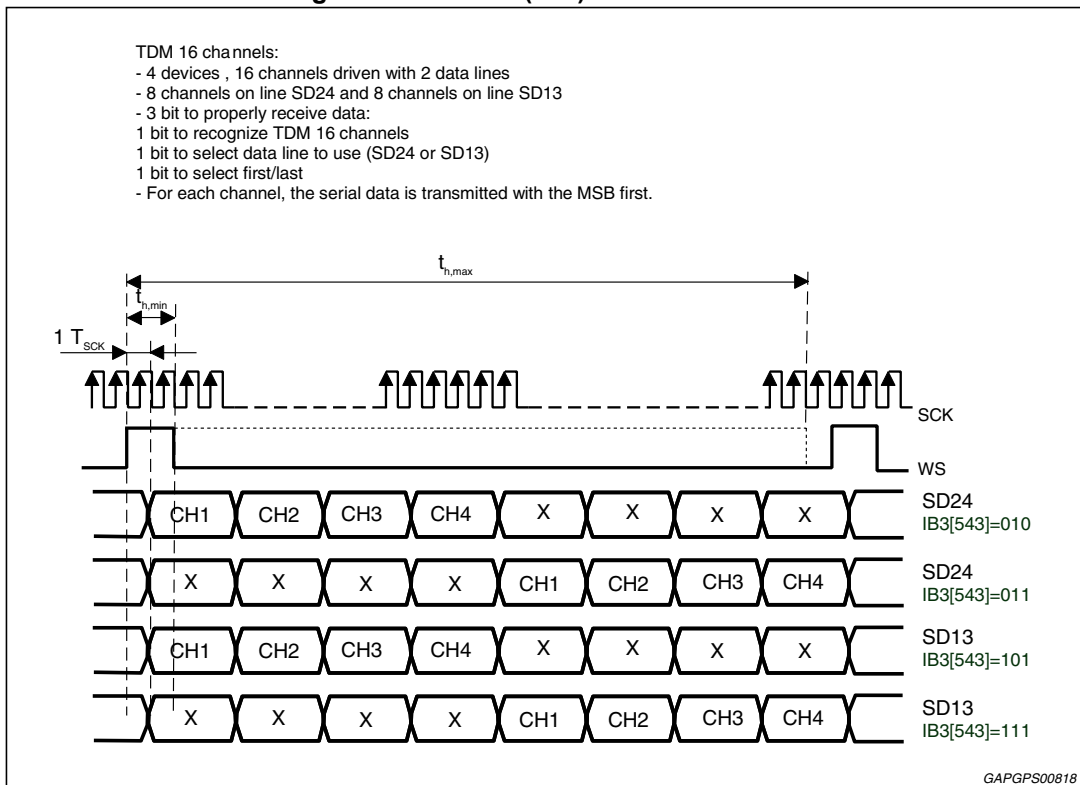
TDM 8-channel is also allowed and two devices (device 1 and device 2) can be driven by using just one serial data line SD24. There are two selectable options  
 When IB3 [D5,D4,D3] = "010" device 1 is first sent; when IB3 [D5,D4,D3] = "011" device 2 is first sent. In *Figure 43* TDM 8-channel format is showed.

**Figure 43. TDM 8-channel format**



The TDM 8 channel is expansible to TDM 16 channel (*Figure 44*) where both SD24 and SD13 data lines are used. All the configurations are selectable via I<sup>2</sup>C.

**Figure 44. TDM 16 (8+8) - channel format**





### 8.4 Timings requirements

Figure 45. Audio interface timing

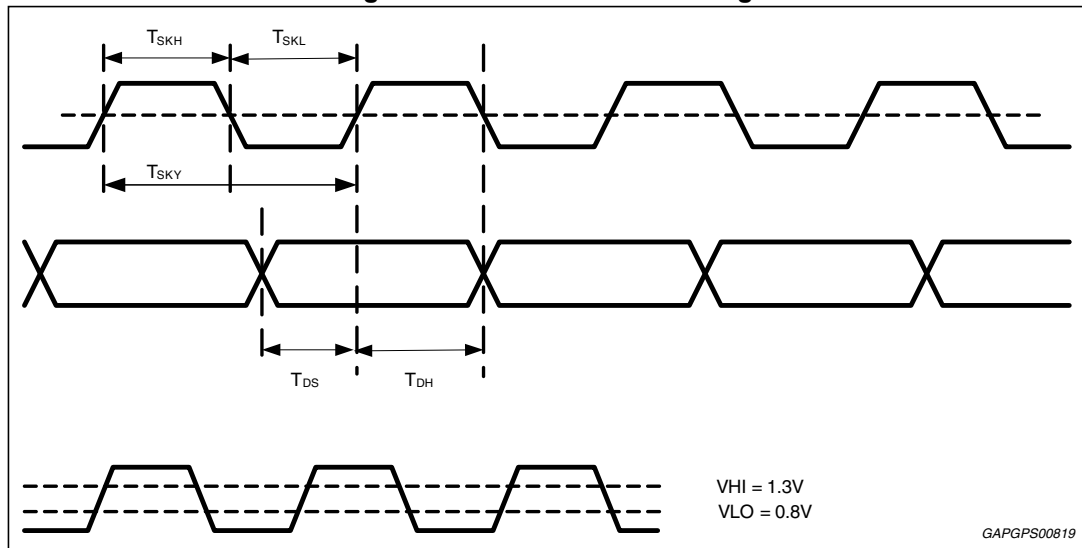


Table 12. I<sup>2</sup>S interface timing

| Symbol | Parameter   | note                         | min                            | max      | unit |
|--------|---|------------------------------|--------------------------------|----------|------|
| Fsck0  | SCK (bit clock) frequency                                 | -                            | -                              | 49.152   | MHz  |
| -      | SCK (bit clock) frequency tolerance                       | -                            | 0.9Fsck0                       | 1.1Fsck0 | MHz  |
| Tsck   | SCK period  | -                            | 20                             | -        | ns   |
| -      | SCK duty cycle  | -                            | 40                             | 60       | %    |
| Tsckh  | SCK high time   | -                            | 6                              | -        | ns   |
| Tsckl  | SCK low time  | -                            | 6                              | -        | ns   |
| -      | SCK transition time                                       | -                            | -                              | 4        | ns   |
| -      | WS (word select) frequency                                | -                            | -                              | 192      | kHz  |
| Twsh   | WS high time  | I2S standard                 | 25 or 32 Tsck (duty cycle=50%) |          | ns   |
| Twsh   | WS high time  | TDM 4-channel                | 1 Tsck                         | 127 Tsck | ns   |
| Twsh   | WS high time  | TDM 8 - TDM 16 (8+8) channel | 1 Tsck                         | 255 Tsck | ns   |
| Tws    | WS setup time   | -                            | 5                              | -        | ns   |
| Twh    | WS hold time  | -                            | 6                              | -        | ns   |
| Tds    | SD13 SD24 (data inputs) setup time before SCK rising edge | -                            | 5                              | -        | ns   |
| Tdh    | SD13 SD24 (data inputs) hold time after SCK rising edge   | -                            | 6                              | -        | ns   |

For TDM mode:

- WS changes at SCK falling edge, on clock period before the MSB is transmitted
- WS does not need to be symmetrical. It need to stay high for at least 2 SCK period clock. The maximum duration is:
  - $T_{h\_max} = 127 T_{SCK}$  in TDM 4-channel
  - $T_{h\_max} = 255 T_{SCK}$  in TDM 8-channel and TDM 16 (8+8) - channels
- The other timings are like in [Table 12](#).

## 8.5 Group delay

The group delay is due to the FIR filter first interpolator and it is  $T_{delay} = 32/F_s$ .

## 9 I<sup>2</sup>C bus interface

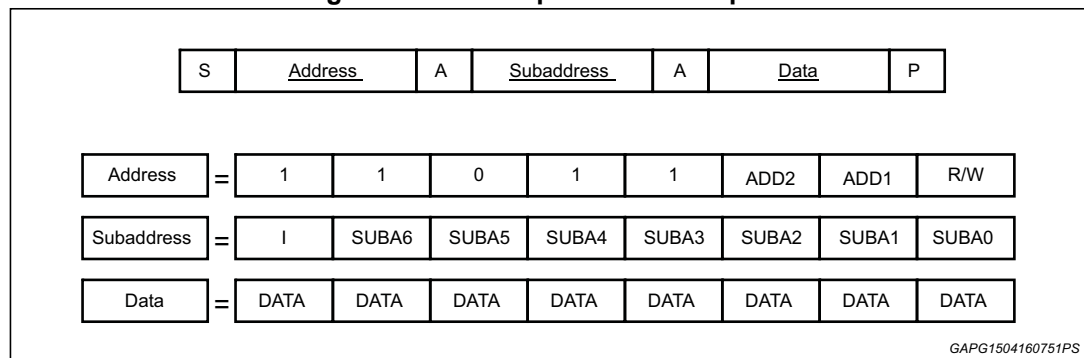
Data transmission from microprocessor to the TDA7803A and viceversa takes place through the 2 wires I<sup>2</sup>C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

When I<sup>2</sup>C bus is active, the user can select the IC's operating mode. The diagnostic cycle results are stored into the data byte, and read the instruction and data bytes back.

The protocol used for the bus is depicted in *Figure 46* and comprises:

- a start condition (S)
- a chip Address byte (the LSB bit determines read/write transmission)
- a Subaddress byte
- a sequence of Data (N-bytes + acknowledge)
- a stop condition (P)

**Figure 46. I<sup>2</sup>C bus protocol description**



**Description:**

- S = Start
- R/W = '0' => Receive-Mode (Chip could be programmed by uP)
- I = Auto increment; when 1, the address is automatically incremented for each byte transferred
- A = Acknowledge
- P = Stop
- MAX CLOCK SPEED 400kbit/sec

There are four I<sup>2</sup>C addresses (for PowerSO36 package): 1101100, 1101101, 1101110, 1101111.

For Flexiwatt package only the 1101100 is available.

## 9.1 Writing procedure

There are two possible procedures:

1. without increment: the I bit is set to 0 and the register to be written is addressed by the subaddress SUB A. Only this register is written by the DATA byte following the subaddress byte.
2. with increment: the I bit is set to 1 and the first register to be written is the one addressed by subaddress SUB A. Then all the registers from SUB A up to stop bit or the reaching of last register are written.

## 9.2 Reading procedure

There are two possible procedures:

1. without increment: the I bit is set to 0 and the only register to be read is addressed by the subaddress sent in the previous write procedure.
2. with increment: the I bit is set to 1 and the first register to be read is the one addressed by subaddress sent in the previous write procedure. Then all the registers from this subaddress up to stop bit or the reaching of last register are read.

## 9.3 Data validity

The data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

## 9.4 Start and stop conditions

A start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

## 9.5 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

## 9.6 Acknowledge

The transmitter\* puts a resistive HIGH level on the SDA line during the acknowledge clock pulse. The receiver\*\* has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

### \* Transmitter

- = master ( $\mu$ P) when it writes an address or instruction byte to the TDA7803A
- = slave (TDA7803A) when the  $\mu$ P reads a data byte from TDA7803A

### \*\* Receiver

- = slave (TDA7803A) when the  $\mu$ P writes an address or instruction byte to the TDA7803A
- = master ( $\mu$ P) when it reads a data byte from TDA7803A

## 9.7 Address selection

To select the proper I<sup>2</sup>C address a resistor must be connected to ADD pin as follows:

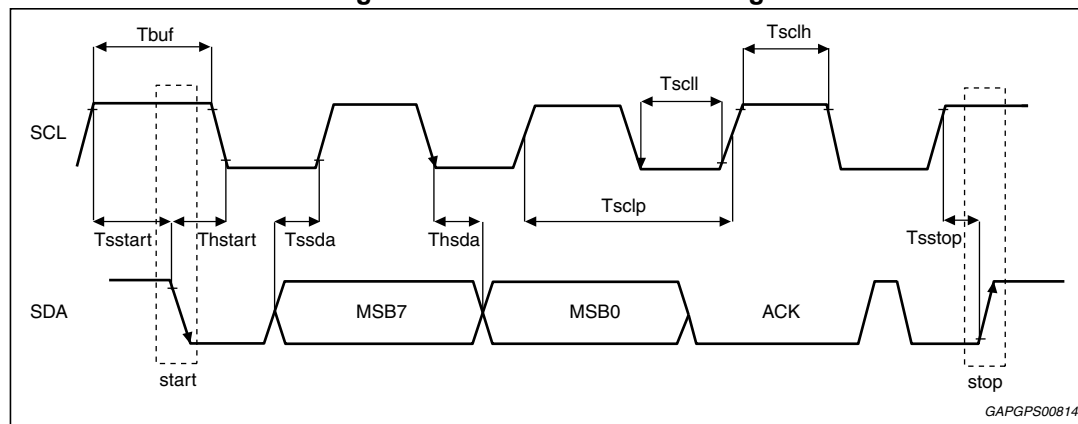
**Table 13. Address threshold**

| ADD2 | ADD1 | Rload         |
|------|------|---------------|
| 0    | 0    | 89K < R       |
| 0    | 1    | 52K < R < 65K |
| 1    | 0    | 30K < R < 39K |
| 1    | 1    | R < 23K       |

## 9.8 I<sup>2</sup>C bus timings

This paragraph describes more in detail the I<sup>2</sup>C bus protocol used and its timings. *Figure 47* and *Table 14* include the timings that have to be respected in order to correctly write into/read from the I<sup>2</sup>C registers.

**Figure 47. I<sup>2</sup>C bus interface timing**



**Table 14. I<sup>2</sup>C bus interface timing**

| Symbol  | Parameter  | Min              | Max | Unit |
|---------|--|------------------|-----|------|
| Fscl    | SCL (clock line) frequency                         | -                | 400 | kHz  |
| Tscl    | SCL period   | 2500             | -   | ns   |
| Tscelh  | SCL high time                                      | 0.6              | -   | µs   |
| Tscll   | SCL low time                                       | 1.3              | -   | µs   |
| Tsstart | Setup time for start condition                     | 0.6              | -   | µs   |
| Thstart | Hold time for start condition                      | 0.6              | -   | µs   |
| Tsstop  | Setup time for stop condition                      | 0.6              | -   | µs   |
| Tbuf    | Bus free time between a stop and a start condition | 1.3              | -   | µs   |
| Tssda   | Setup time for data line                           | 100              | -   | ns   |
| Thsda   | Hold time for data line                            | 0 <sup>(1)</sup> | -   | ns   |
| Tf      | Fall time for SCL and SDA                          | -                | 300 | ns   |

1. Device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

## 10 I<sup>2</sup>C registers

### 10.1 Instruction byte

#### 10.1.1 IB0 - Subaddress "I0000000h" - default = "00000000"

Table 15. IB0 - Subaddress "I0000000h" - default = "00000000"

| Bit | Instruction decoding bit  |
|-----|---|
| D7  | Channel 4 Tristate Mode<br><b>0: off</b><br>1: on   |
| D6  | Channel 3 Tristate Mode<br><b>0: off</b><br>1: on   |
| D5  | Channel 2 Tristate Mode<br><b>0: off</b><br>1: on   |
| D4  | Channel 1 Tristate Mode<br><b>0: off</b><br>1: on   |
| D3  | Channel 4 Amplifier Mode<br><b>0: High Efficiency SBI mode</b><br>1: Standard Class AB Mode |
| D2  | Channel 3 Amplifier Mode<br><b>0: High Efficiency SBI mode</b><br>1: Standard Class AB Mode |
| D1  | Channel 2 Amplifier Mode<br><b>0: High Efficiency SBI mode</b><br>1: Standard Class AB Mode |
| D0  | Channel 1 Amplifier Mode<br><b>0: High Efficiency SBI mode</b><br>1: Standard Class AB Mode |

## 10.1.2 IB1 - Subaddress "I0000001h" - default = "00000000"

Table 16. IB1 - Subaddress "I0000001h" - default = "00000000"

| Bit      | Instruction decoding bit   |
|----------|--|
| D7       | Impedance efficiency optimizer (front channels)<br><b>0: Efficiency optimized for 2 ohm</b><br>1: Efficiency optimized for 4 ohm |
| D6       | Impedance efficiency optimizer (rear channels)<br><b>0: Efficiency optimized for 2 ohm</b><br>1: Efficiency optimized for 4 ohm  |
| D5<br>D4 | Digital gain selection<br><b>D4 D5 Digital gain</b><br><b>0 0 No digital gain</b><br>0 1 +6 dB<br>1 0 +12 dB<br>1 1 Not used     |
| D3<br>D2 | Gain Channel 1 & 3<br><b>D3 D2 Gain</b><br><b>0 0 GV1</b><br>0 1 GV2<br>1 0 GV3<br>1 1 GV4                                       |
| D1<br>D0 | Gain Channel 2 & 4<br><b>D1 D0 Gain</b><br><b>0 0 GV1</b><br>0 1 GV2<br>1 0 GV3<br>1 1 GV4                                       |

10.1.3 IB2 - Subaddress "I0000010h" - default = "00000000"

Table 17. IB2 - Subaddress "I0000010h" - default = "00000000"

| Bit | Instruction decoding bit   |
|-----|--|
|     | Mute Time Setting<br><b>D7 D6 D5 mute timing (Fs = 44.1 kHz)</b><br><b>0 0 0 1.45 ms</b><br>0 0 1 5.8 ms<br>0 1 0 11.6 ms<br>0 1 1 23.2 ms<br>1 0 0 46.4 ms<br>1 0 1 92.8 ms<br>1 1 0 185.5 ms<br>1 1 1 371.1 ms |
| D4  | Mute 1&3<br><b>0: Channels 1 &amp; 3 Muted</b><br>1: Channels 1 & 3 un-Muted   |
| D3  | Mute 2&4<br><b>0: Channels 2 &amp; 4 Muted</b><br>1: Channels 2 & 4 un-Muted   |
| D2  | Disable digital mute<br><b>0: Digital mute ON</b><br>1: Digital mute OFF   |
| D1  | <b>Internal use – set "0"</b>  |
| D0  | Low Battery Mute threshold<br><b>0: 5.3 V (guaranteed play down to 6 V)</b><br>1: 7.3 V (guaranteed play down to 8 V)  |



### 10.1.4 IB3 - Subaddress "I0000011h" - default = "00000000"

Table 18. IB3 - Subaddress "I0000011h" - default = "00000000"

| Bit            | Instruction decoding bit                       |   |   |
|----------------|--|---|---|
| D7-D6          | Sample frequency range (Word select frequency) |   |   |
|                | <b>D7</b>                                      | <b>D6</b>                                     | <b>Sample frequency</b>                       |
|                | <b>0</b>                                       | <b>0</b>                                      | <b>44.1 kHz</b>                               |
|                | 0  | 1   | 48 kHz <sup>(1)</sup>                         |
|                | 1  | 0   | 96 kHz  |
|                | 1  | 1   | 192 kHz                                       |
| D5<br>D4<br>D3 | Digital Input Format                           |   |   |
|                | <b>D5</b>                                      | <b>D4</b>                                     | <b>D3</b>                                     |
|                | <b>0</b>                                       | <b>0</b>                                      | <b>0</b> <b>I2S standard</b>                  |
|                | 0  | 0   | 1 TDM – 4ch                                   |
|                | 0  | 1   | 0 TDM – 8ch (SD2_4 input, device 1)           |
|                | 0  | 1   | 1 TDM – 8ch (SD2_4 input device 2)            |
|                | 1  | 0   | 0 TDM – 16ch (8 + 8) (SD2_4 input - device 1) |
|                | 1  | 0   | 1 TDM – 16ch (8 + 8) (SD2_4 input - device 2) |
| 1              | 1  | 0 TDM – 16ch (8 + 8) (SD1_3 input - device 3) |   |
| 1              | 1  | 1 TDM – 16ch (8 + 8) (SD1_3 input - device 4) |   |
| D2             | Noise Gating Function enable/disable           |   |   |
|                | <b>0: enable</b>                               |   |   |
|                | 1: disable                                     |   |   |
| D1             | Input offset detection                         |   |   |
|                | <b>0: enable</b>                               |   |   |
|                | 1: disable                                     |   |   |
| D0             | Digital High pass filter enable/disable        |   |   |
|                | <b>0: disable</b>                              |   |   |
|                | 1: enable                                      |   |   |

1. Configurations IB3 [D7, D6] =00 and 01 are the same from a signal processing point of view. The distinction is needed in order to handle functions timings and duration.

**Note:** *Byte IB3 settings can be changed only if the amplifier is in ECO mode state, otherwise the command is ignored.*

## 10.1.5 IB4 - Subaddress "I0000100h" - default = "00000000"

Table 19. IB4 - Subaddress "I0000100h" - default = "00000000"

| Bit | Instruction decoding bit   |
|-----|--|
| D7  | Internal use – set "0"   |
| D6  | Short Fault information on CD/diag pin<br><b>0: yes</b><br>1: no                                     |
| D5  | Offset information on CD/diag pin. Selection possible only if IB3(0) = "0"<br><b>0: yes</b><br>1: no |
| D4  | AC diagnostic current threshold<br><b>0: high</b><br>1: low  |
| D3  | AC Diagnostic Enable/Disable<br><b>0: disable</b><br>1: enable                                       |
| D2  | Channel 1&3 Diagnostic Mode<br><b>0: Speaker mode</b><br>1: Line Driver mode                         |
| D1  | Channel 2&4 Diagnostic Mode<br><b>0: Speaker mode</b><br>1: Line Driver mode                         |
| D0  | Diagnostic Mode Enable/Disable<br><b>0: disable</b><br>1: enable                                     |

### 10.1.6 IB5 - Subaddress "I0000101h" - default = "00000000"

Table 20. IB5 - Subaddress "I0000101h" - default = "00000000"

| Bit               | Instruction decoding bit           |                               |                                  |
|-------------------|------------------------------------|-------------------------------|----------------------------------|
| D7, D6            | Thermal threshold programmability: |                               |                                  |
|                   | <b>D7</b>                          | <b>D6</b>                     | <b>Thermal threshold (TWs)</b>   |
|                   | <b>0</b>                           | <b>0</b>                      | <b>Default (datasheet value)</b> |
|                   | 0                                  | 1                             | TWs shifted -10°C                |
|                   | 1                                  | 0                             | TWs shifted -20°C                |
|                   | 1                                  | 1                             | Not used                         |
| D5                | Internal use – set "0"             |                               |                                  |
| D4, D3,<br>D2, D1 | <b>Current capability enhancer</b> |                               |                                  |
|                   | <b>D4 - D1</b>                     | 0000 disabled<br>1111 enabled |                                  |
| D0                | Internal use – set "0"             |                               |                                  |

10.1.7 IB6 - Subaddress "I0000110h" - default = "00000000"

Table 21. IB6 - Subaddress "I0000110h" - default = "00000000"

| Bit | Instruction decoding bit                                 |           |   |                              |
|-----|--|-----------|---|------------------------------|
|     | Diagnostic pulse stretch                                 |           |   |                              |
|     | <b>D7</b>  | <b>D6</b> | <b>D5</b>   | <b>Diagnostic timing set</b> |
|     | 0  | 0         | 0   | Default                      |
| D7  | 0  | 0         | 1   | Stretched*2                  |
| D6  | 0  | 1         | 0   | Stretched*4                  |
| D5  | 0  | 1         | 1   | Stretched*8                  |
|     | 1  | 0         | 0   | Stretched*16                 |
|     | Others   |           | Default   |                              |
| D4  | Internal use – set "0"                                   |           |   |                              |
|     | Parallel mode Configuration<br>D3 D2 (like LOADA,LOADB): |           |   |                              |
|     | <b>D3</b>  | <b>D2</b> | <b>Load configuration</b>                           |                              |
| D3  | <b>0</b>   | <b>0</b>  | <b>Single channel mode on 1,2,3 &amp; 4 channel</b> |                              |
| D2  | 0  | 1         | Parallel mode only on 1 & 2 channels                |                              |
|     | 1  | 0         | Parallel mode only on 3 & 4 channels                |                              |
|     | 1  | 1         | Parallel mode on both sides                         |                              |
| D1  | Internal use – set "0"                                   |           |   |                              |
| D0  | Internal use – set "0"                                   |           |   |                              |

10.1.8 IB7 - Subaddress "I0000111h" - default = "00000000"

Table 22. IB7 - Subaddress "I0000111h" - default = "00000000"

| Bit | Instruction decoding bit  |
|-----|---|
|     | Temperature warning information on CDdiag pin<br><b>D7 D6 D5    Temperature</b> |
| D7  | <b>0 0 0    TW1</b>   |
| D6  | 0 0 1    TW2  |
| D5  | 0 1 0    TW3  |
|     | 0 1 1    TW4  |
|     | 1 x x    no thermal warning information on diag pin                             |
|     | Clipping detection level for front channels<br><b>D4 D3</b>                     |
| D4  | <b>0 0    threshold 1 for all channel 1 and 3</b>                               |
| D3  | 0 1    threshold 2 for all channel 1 and 3                                      |
|     | 1 0    threshold 3 for all channel 1 and 3                                      |
|     | 1 1    no clipping for channel 1 and 3  |
|     | Clipping detection level for rear channels<br><b>D2 D1</b>                      |
| D2  | <b>0 0    threshold 1 for all channel 2 and 4</b>                               |
| D1  | 0 1    threshold 2 for all channel 2 and 4                                      |
|     | 1 0    threshold 3 for all channel 2 and 4                                      |
|     | 1 1    no clipping for channel 2 and 4  |
| D0  | Amplifier on/off<br><b>0: off</b><br>1: on                                      |

## 10.2 Data byte

### 10.2.1 DB0 - Subaddress: "I0010000h"

Table 23. DB0 - Subaddress: "I0010000h"

| Bit | Instruction decoding bit  |
|-----|---|
| D7  | Power on reset (POR)<br>0: the start-up phase to move from 'stand by' state to 'ECO - mode' state is running<br>1: the device is 'out of stand by'. |
| D6  | Start-up Diagnostic status<br>0: Turn-on Diag. cycle not activated or not terminated<br>1: Turn-on Diag. cycle terminated                           |
| D5  | Diagnostic Data Valid<br>1: diagnostic data not valid<br>0: diagnostic data valid   |
| D4  | Internal use  |
| D3  | Internal use  |
| D2  | Internal use  |
| D1  | Channel 2 & 4 in mute/play<br>0: Channel 2 & 4 in play<br>1: Channel 2 & 4 in mute  |
| D0  | Channel 1 & 3 in mute/play<br>0: Channel 1 & 3 in play<br>1: Channel 1 & 3 in mute  |

## 10.2.2 DB1 - Subaddress: "I0010001h" - Channel 1

Table 24. DB1 - Subaddress: "I0010001h" - Channel 1

| Bit | Instruction decoding bit   |
|-----|--|
| D7  | Overcurrent protection Channel 1:<br>0: Overcurrent protection NOT triggered on CH1<br>1: Overcurrent protection triggered on CH1                  |
| D6  | Channel 1 Soft Short present<br>0: No Soft short<br>1: Soft Short<br>(only during turn-on diagnostic)  |
| D5  | Channel 1 offset detection<br>0: No output offset<br>1: Output offset detected   |
| D4  | Channel 1 Permanent Diagnostic status<br>0: Permanent diagnostic cycle not activated or not terminated<br>1: Permanent diagnostic cycle terminated |
| D3  | Channel 1 Normal/Short Load<br>0: Normal load<br>1: Short load   |
| D2  | Channel 1 Open load<br>0: No open load<br>1: Open load detection<br>(only during turn-on diagnostic)   |
| D1  | Channel 1 Short to Vcc<br>0: No Hard short to Vcc<br>1: Hard short to Vcc  |
| D0  | Channel 1 Short to GND<br>0: No Hard short to GND<br>1: Hard Short to GND  |

## 10.2.3 DB2 - Subaddress: "I0010010h" - Channel 2

Table 25. DB2 - Subaddress: "I0010010h" - Channel 2

| Bit | Instruction decoding bit   |
|-----|--|
| D7  | Overcurrent protection Channel 2:<br>0: Overcurrent protection NOT triggered on CH2<br>1: Overcurrent protection triggered on CH2                  |
| D6  | Channel 2 Soft Short present<br>0: No Soft short<br>1: Soft Short<br>(only during turn-on diagnostic)  |
| D5  | Channel 2 offset detection<br>0: No output offset<br>1: Output offset detected   |
| D4  | Channel 2 Permanent Diagnostic status<br>0: Permanent diagnostic cycle not activated or not terminated<br>1: Permanent diagnostic cycle terminated |
| D3  | Channel 2 Normal/Short Load<br>0: Normal load<br>1: Short load   |
| D2  | Channel 2 Open load<br>0: No open load<br>1: Open load detection<br>(only during turn-on diagnostic)   |
| D1  | Channel 2 Short to Vcc<br>0: No Hard short to Vcc<br>1: Hard short to Vcc  |
| D0  | Channel 2 Short to GND<br>0: No short to GND<br>1: Short to GND  |



### 10.2.4 DB3 - Subaddress: "I0010011h" - Channel 3

**Table 26. DB3 - Subaddress: "I0010011h" - Channel 3**

| Bit | Instruction decoding bit   |
|-----|--|
| D7  | Overcurrent protection Channel 3:<br>0: Overcurrent protection NOT triggered on CH3<br>1: Overcurrent protection triggered on CH3                  |
| D6  | Channel 3 Soft Short present<br>0: No Soft short<br>1: Soft Short<br>(only during turn-on diagnostic)  |
| D5  | Channel 3 offset detection<br>0: No output offset<br>1: Output offset detected   |
| D4  | Channel 3 Permanent Diagnostic status<br>0: Permanent diagnostic cycle not activated or not terminated<br>1: Permanent diagnostic cycle terminated |
| D3  | Channel 3 Normal/Short Load<br>0: Normal load<br>1: Short load   |
| D2  | Channel 3 Open load<br>0: No open load<br>1: Open load detection<br>(only during turn-on diagnostic)   |
| D1  | Channel 3 Short to Vcc<br>0: No Hard short to Vcc<br>1: Hard short to Vcc  |
| D0  | Channel 3 Short to GND<br>0: No short to GND<br>1: Short to GND  |

## 10.2.5 DB4 - Subaddress: "I0010100h" - Channel 4

Table 27. DB4 - Subaddress: "I0010100h" - Channel 4

| Bit | Instruction decoding bit   |
|-----|--|
| D7  | Overcurrent protection Channel 4:<br>0: Overcurrent protection NOT triggered on CH4<br>1: Overcurrent protection triggered on CH4                  |
| D6  | Channel 4 Soft Short present<br>0: No Soft short<br>1: Soft Short<br>(only during turn-on diagnostic)  |
| D5  | Channel 4 offset detection<br>0: No output offset<br>1: Output offset detected   |
| D4  | Channel 4 Permanent Diagnostic status<br>0: Permanent diagnostic cycle not activated or not terminated<br>1: Permanent diagnostic cycle terminated |
| D3  | Channel 4 Normal/Short Load<br>0: Normal load<br>1: Short load   |
| D2  | Channel 4 Open load<br>0: No open load<br>1: Open load detection<br>(only during turn-on diagnostic)   |
| D1  | Channel 4 Short to Vcc<br>0: No Hard short to Vcc<br>1: Hard short to Vcc  |
| D0  | Channel 4 Short to GND<br>0: No short to GND<br>1: Short to GND  |

## 10.2.6 DB5 - Subaddress: "I0010101h"

Table 28. DB5 - Subaddress: "I0010101h"

| Bit | Instruction decoding bit  |
|-----|---|
| D7  | AC DIAG – Signal level compatible with AC diag detection<br>0: Signal ok<br>1: Signal too high  |
| D6  | AC DIAG – Channel 4 tweeter detection<br>0: Ch4 tweeter not present<br>1: Ch4 tweeter present   |
| D5  | AC DIAG – Channel 3 tweeter detection<br>0: Ch3 tweeter not present<br>1: Ch3 tweeter present   |
| D4  | AC DIAG – Channel 2 tweeter detection<br>0: Ch2 tweeter not present<br>1: Ch2 tweeter present   |
| D3  | AC DIAG – Channel 1 tweeter detection<br>0: Ch1 tweeter not present<br>1: Ch1 tweeter present   |
| D2  | Front channel clip detection<br>0: No clipping on front channel<br>1: Clipping on front channel |
| D1  | Rear channel clip detection<br>0: No clipping on rear channel<br>1: Clipping on rear channel    |
| D0  | PLL lock detector<br>0: PLL no locked<br>1: PLL locked  |

**10.2.7 DB6 - Subaddress: "I0010110h"****Table 29. DB6 - Subaddress: "I0010110h"**

| Bit | Instruction decoding bit  |
|-----|---|
| D7  | TW1<br>0: TW1 threshold not trespassed<br>1: TW1 threshold trespassed |
| D6  | TW2<br>0: TW2 threshold not trespassed<br>1: TW2 threshold trespassed |
| D5  | TW3<br>0: TW3 threshold not trespassed<br>1: TW3 threshold trespassed |
| D4  | TW4<br>0: TW4 threshold not trespassed<br>1: TW4 threshold trespassed |
| D3  | Internal use  |
| D2  | Internal use  |
| D1  | Internal use  |
| D0  | Internal use  |

**10.2.8 DB7 - Subaddress: "I0010111h" - Vcc level ADC conversion****Table 30. DB7 - Subaddress: "I0010111h" - Vcc level ADC conversion**

| Bit | Instruction decoding bit |
|-----|--------------------------|
| D7  | Battery Level (7)        |
| D6  | Battery Level (6)        |
| D5  | Battery Level (5)        |
| D4  | Battery Level (4)        |
| D3  | Battery Level (3)        |
| D2  | Battery Level (2)        |
| D1  | Battery Level (1)        |
| D0  | Battery Level (0)        |

# 11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

ECOPACK® is an ST trademark.

## 11.1 PowerSO-36 (slug up) package information

Figure 48. PowerSO-36 (slug up) package outline

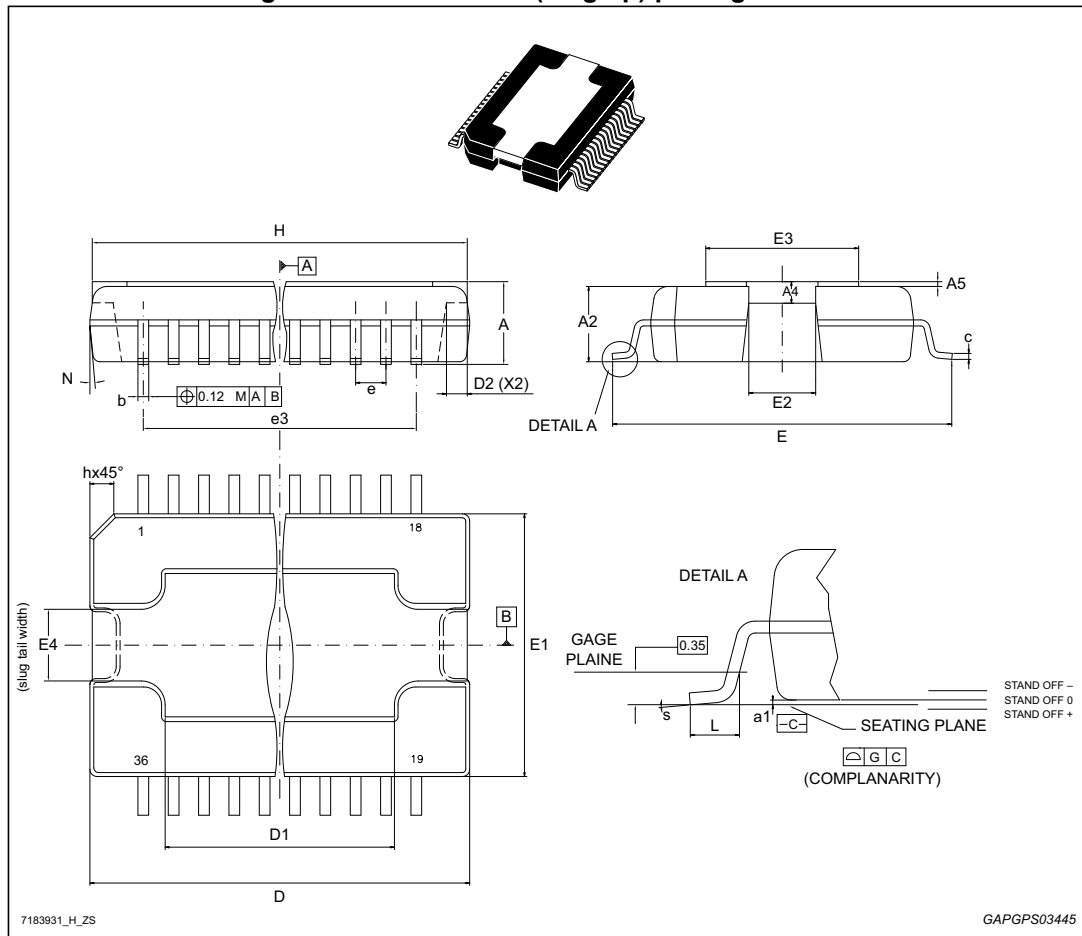


Table 31. PowerSO-36 (slug up) package mechanical data

| Ref | Dimensions  |      |      |                       |      |        |
|-----|-------------|------|------|-----------------------|------|--------|
|     | Millimeters |      |      | Inches <sup>(1)</sup> |      |        |
|     | Min.        | Typ. | Max. | Min.                  | Typ. | Max.   |
| A   | 3.27        | -    | 3.41 | 0.1287                | -    | 0.1343 |
| A2  | 3.1         | -    | 3.18 | 0.1220                | -    | 0.1252 |

**Table 31. PowerSO-36 (slug up) package mechanical data (continued)**

| Ref               | Dimensions  |       |        |                       |        |         |
|-------------------|-------------|-------|--------|-----------------------|--------|---------|
|                   | Millimeters |       |        | Inches <sup>(1)</sup> |        |         |
|                   | Min.        | Typ.  | Max.   | Min.                  | Typ.   | Max.    |
| A4                | 0.8         | -     | 1.0    | 0.0315                | -      | 0.0394  |
| A5                | -           | 0.2   | -      | -                     | 0.0079 | -       |
| a1                | 0.03        | -     | -0.04  | 0.0012                | -      | -0.0016 |
| b                 | 0.22        | -     | 0.38   | 0.0087                | -      | 0.0150  |
| c                 | 0.23        | -     | 0.32   | 0.0091                | -      | 0.0126  |
| D <sup>(2)</sup>  | 15.8        | -     | 16.0   | 0.6220                | -      | 0.6299  |
| D1                | 9.4         | -     | 9.8    | 0.3701                | -      | 0.3858  |
| D2                | -           | 1.0   | -      | -                     | 0.0394 | -       |
| E                 | 13.9        | -     | 14.5   | 0.5472                | -      | 0.5709  |
| E1 <sup>(2)</sup> | 10.9        | -     | 11.1   | 0.4291                | -      | 0.4370  |
| E2                | -           | -     | 2.9    | -                     | -      | 0.1142  |
| E3                | 5.8         | -     | 6.2    | 0.2283                | -      | 0.2441  |
| E4                | 2.9         | -     | 3.2    | 0.1142                | -      | 0.1260  |
| e                 | -           | 0.65  | -      | -                     | 0.0256 | -       |
| e3                | -           | 11.05 | -      | -                     | 0.4350 | -       |
| G                 | 0           | -     | 0.075  | 0                     | -      | 0.0031  |
| H                 | 15.5        | -     | 15.900 | 0.6102                | -      | 0.6260  |
| h                 | -           | -     | 1.1    | -                     | -      | 0.0433  |
| L                 | 0.8         | -     | 1.1    | 0.0315                | -      | 0.0433  |
| N                 | -           | -     | 10°    | -                     | -      | 10°     |
| s                 | -           | -     | 8°     | -                     | -      | 8°      |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. 'D' and 'E1' do not include mold flash or protusions.  
Mold flash or protusions shall not exceed 0.15mm (0.006").

## 11.2 Flexiwatt 27 (vertical) package information

Figure 49. Flexiwatt 27 (vertical) package outline

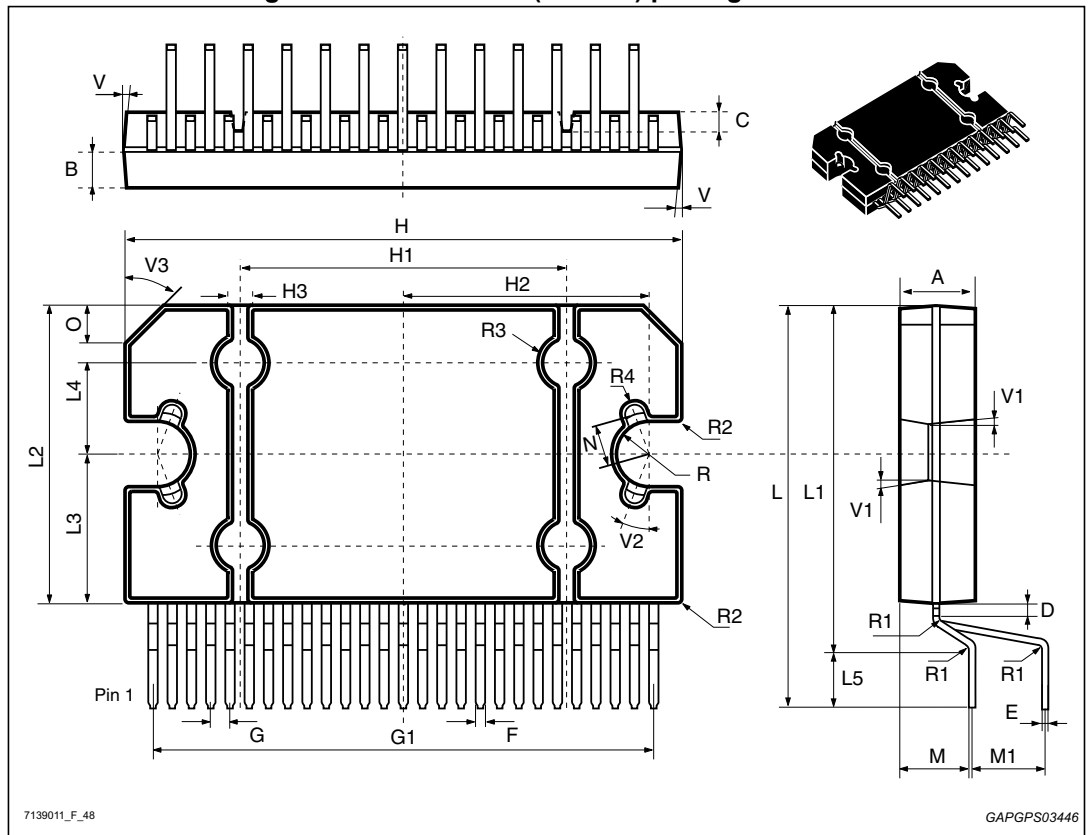


Table 32. Flexiwatt 27 (vertical) package mechanical data

| Ref              | Dimensions  |       |       |                       |        |        |
|------------------|-------------|-------|-------|-----------------------|--------|--------|
|                  | Millimeters |       |       | Inches <sup>(1)</sup> |        |        |
|                  | Min.        | Typ.  | Max.  | Min.                  | Typ.   | Max.   |
| A                | 4.45        | 4.50  | 4.65  | 0.1752                | 0.1772 | 0.1831 |
| B                | 1.80        | 1.90  | 2.00  | 0.0709                | 0.0748 | 0.0787 |
| C                | -           | 1.40  | -     | -                     | 0.0551 | -      |
| D                | 0.75        | 0.90  | 1.05  | 0.0295                | 0.0354 | 0.0413 |
| E                | 0.37        | 0.39  | 0.42  | 0.0146                | 0.0154 | 0.0165 |
| F <sup>(2)</sup> | -           | -     | 0.57  | -                     | -      | 0.0224 |
| G                | 0.80        | 1.00  | 1.20  | 0.0315                | 0.0394 | 0.0472 |
| G1               | 25.75       | 26.00 | 26.25 | 1.0138                | 1.0236 | 1.0335 |
| H <sup>(3)</sup> | 28.90       | 29.23 | 29.30 | 1.1378                | 1.1508 | 1.1535 |
| H1               | -           | 17.00 | -     | -                     | 0.6693 | -      |
| H2               | -           | 12.80 | -     | -                     | 0.5039 | -      |

Table 32. Flexiwatt 27 (vertical) package mechanical data (continued)

| Ref               | Dimensions  |       |       |                       |        |        |
|-------------------|-------------|-------|-------|-----------------------|--------|--------|
|                   | Millimeters |       |       | Inches <sup>(1)</sup> |        |        |
|                   | Min.        | Typ.  | Max.  | Min.                  | Typ.   | Max.   |
| H3                | -           | 0.80  | -     | -                     | 0.0315 | -      |
| L <sup>(3)</sup>  | 22.07       | 22.47 | 22.87 | 0.8689                | 0.8846 | 0.9004 |
| L1                | 18.57       | 18.97 | 19.37 | 0.7311                | 0.7469 | 0.7626 |
| L2 <sup>(3)</sup> | 15.50       | 15.70 | 15.90 | 0.6102                | 0.6181 | 0.6260 |
| L3                | 7.70        | 7.85  | 7.95  | 0.3031                | 0.3091 | 0.3130 |
| L4                | -           | 5     | -     | -                     | 0.1969 | -      |
| L5                | 3.35        | 3.5   | 3.65  | 0.1319                | 0.1378 | 0.1437 |
| M                 | 3.70        | 4.00  | 4.30  | 0.1457                | 0.1575 | 0.1693 |
| M1                | 3.60        | 4.00  | 4.40  | 0.1417                | 0.1575 | 0.1732 |
| N                 | -           | 2.20  | -     | -                     | 0.0866 | -      |
| O                 | -           | 2     | -     | -                     | 0.0787 | -      |
| R                 | -           | 1.70  | -     | -                     | 0.0669 | -      |
| R1                | -           | 0.5   | -     | -                     | 0.0197 | -      |
| R2                | -           | 0.3   | -     | -                     | 0.0118 | -      |
| R3                | -           | 1.25  | -     | -                     | 0.0492 | -      |
| R4                | -           | 0.50  | -     | -                     | 0.0197 | -      |
| V                 | 5°          |       |       | 5°                    |        |        |
| V1                | 3°          |       |       | 3°                    |        |        |
| V2                | 20°         |       |       | 20°                   |        |        |
| V3                | 45°         |       |       | 45°                   |        |        |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. dam-bar protusion not included.
3. molding protusion included.



### 11.3 Flexiwatt 27 (SMD) package information

Figure 50. Flexiwatt 27 (SMD) package outline

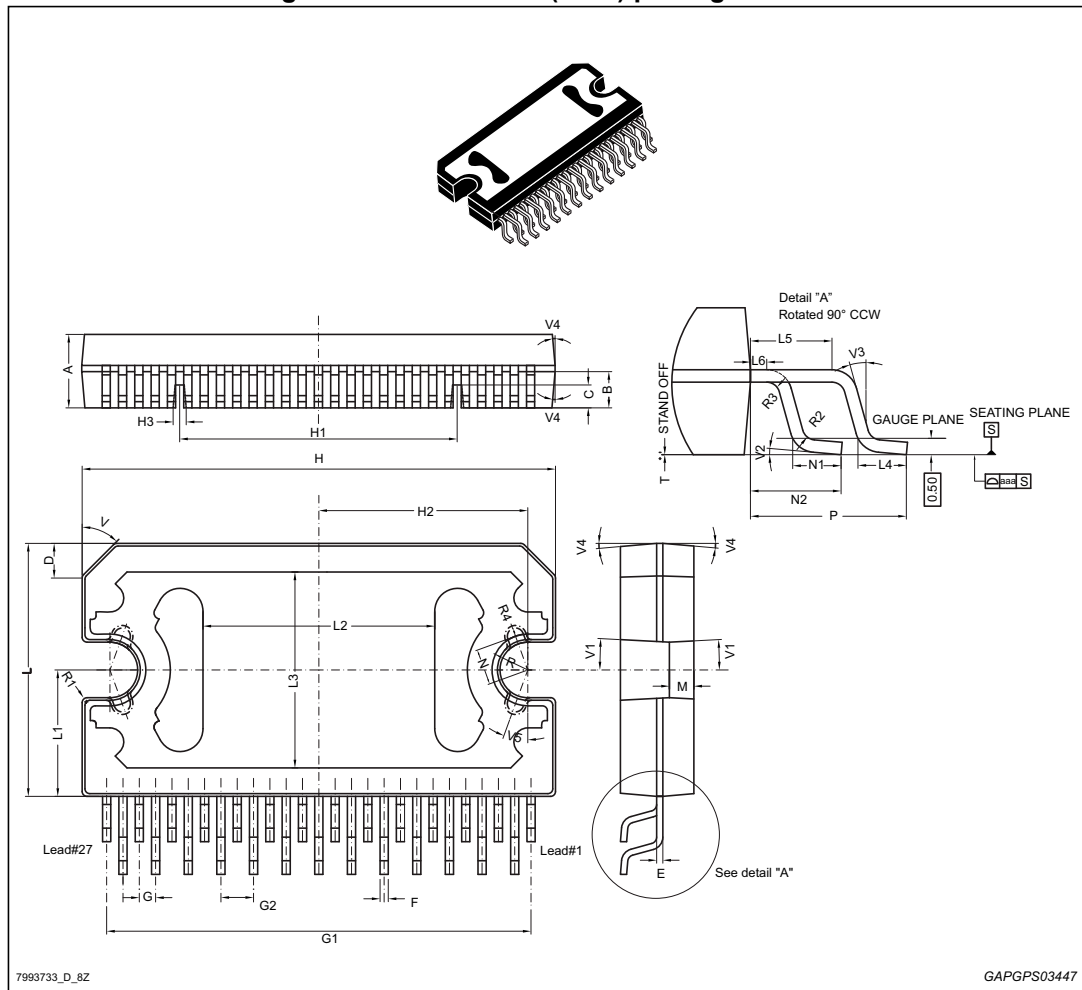


Table 33. Flexiwatt 27 (SMD) package mechanical data

| Ref              | Dimensions  |      |      |                       |        |        |
|------------------|-------------|------|------|-----------------------|--------|--------|
|                  | Millimeters |      |      | Inches <sup>(1)</sup> |        |        |
|                  | Min.        | Typ. | Max. | Min.                  | Typ.   | Max.   |
| A                | 4.45        | 4.50 | 4.65 | 0.1752                | 0.1772 | 0.1831 |
| B                | 2.12        | 2.22 | 2.32 | 0.0835                | 0.0874 | 0.0913 |
| C                | -           | 1.40 | -    | -                     | 0.0551 | -      |
| D                | -           | 2.00 | -    | -                     | 0.0787 | -      |
| E                | 0.36        | 0.40 | 0.44 | 0.0142                | 0.0157 | 0.0173 |
| F <sup>(2)</sup> | 0.47        | 0.51 | 0.57 | 0.0185                | 0.0201 | 0.0224 |
| G <sup>(3)</sup> | 0.75        | 1.00 | 1.25 | 0.0295                | 0.0394 | 0.0492 |

**Table 33. Flexiwatt 27 (SMD) package mechanical data (continued)**

| Ref                | Dimensions          |       |       |                       |        |        |
|--------------------|---------------------|-------|-------|-----------------------|--------|--------|
|                    | Millimeters         |       |       | Inches <sup>(1)</sup> |        |        |
|                    | Min.                | Typ.  | Max.  | Min.                  | Typ.   | Max.   |
| G1                 | 25.70               | 26.00 | 26.30 | 1.0118                | 1.0236 | 1.0354 |
| G2 <sup>(3)</sup>  | 1.75                | 2.00  | 2.25  | 0.0689                | 0.0787 | 0.0886 |
| H <sup>(2)</sup>   | 28.85               | 29.23 | 29.40 | 1.1358                | 1.1508 | 1.1575 |
| H1                 | -                   | 17.00 | -     | -                     | 0.6693 | -      |
| H2                 | -                   | 12.80 | -     | -                     | 0.5039 | -      |
| H3                 | -                   | 0.80  | -     | -                     | 0.0315 | -      |
| L <sup>(2)</sup>   | 15.50               | 15.70 | 15.90 | 0.6102                | 0.6181 | 0.6260 |
| L1                 | 7.70                | 7.85  | 7.95  | 0.3031                | 0.3091 | 0.3130 |
| L2                 | 14.00               | 14.20 | 14.40 | 0.5512                | 0.5591 | 0.5669 |
| L3                 | 11.80               | 12.00 | 12.20 | 0.4646                | 0.4724 | 0.4803 |
| L4                 | 1.30                | 1.48  | 1.66  | 0.0512                | 0.0583 | 0.0654 |
| L5                 | 2.42                | 2.50  | 2.58  | 0.0953                | 0.0984 | 0.1016 |
| L6                 | 0.42                | 0.50  | 0.58  | 0.0165                | 0.0197 | 0.0228 |
| M                  | -                   | 1.50  | -     | -                     | 0.0591 | -      |
| N                  | -                   | 2.20  | -     | -                     | 0.0866 | -      |
| N1                 | 1.30                | 1.48  | 1.66  | 0.0512                | 0.0583 | 0.0654 |
| N2 <sup>(3)</sup>  | 2.73 <sup>(3)</sup> | 2.83  | 2.93  | 0.1075                | 0.1114 | 0.1154 |
| P <sup>(3)</sup>   | 4.73                | 4.83  | 4.93  | 0.1862                | 0.1902 | 0.1941 |
| R                  | -                   | 1.70  | -     | -                     | 0.0669 | -      |
| R1                 | -                   | 0.30  | -     | -                     | 0.0118 | -      |
| R2                 | 0.35                | 0.40  | 0.45  | 0.0138                | 0.0157 | 0.0177 |
| R3                 | 0.35                | 0.40  | 0.45  | 0.0138                | 0.0157 | 0.0177 |
| R4                 | -                   | 0.50  | -     | -                     | 0.0197 | -      |
| T <sup>(3)</sup>   | -0.08               | -     | 0.10  | -0.0031               | -      | 0.0039 |
| aaa <sup>(3)</sup> | -                   | 0.1   | -     | -                     | 0.0039 | -      |
| V                  | -                   | 45°   | -     | -                     | 45°    | -      |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension "F" doesn't include dam-bar protrusion.  
Dimensions "H" and "L" include mold flash or protrusions.
3. Golden parameters.

### 11.4 Flexiwatt 27 (horizontal) package information

Figure 51. Flexiwatt 27 (horizontal) package outline

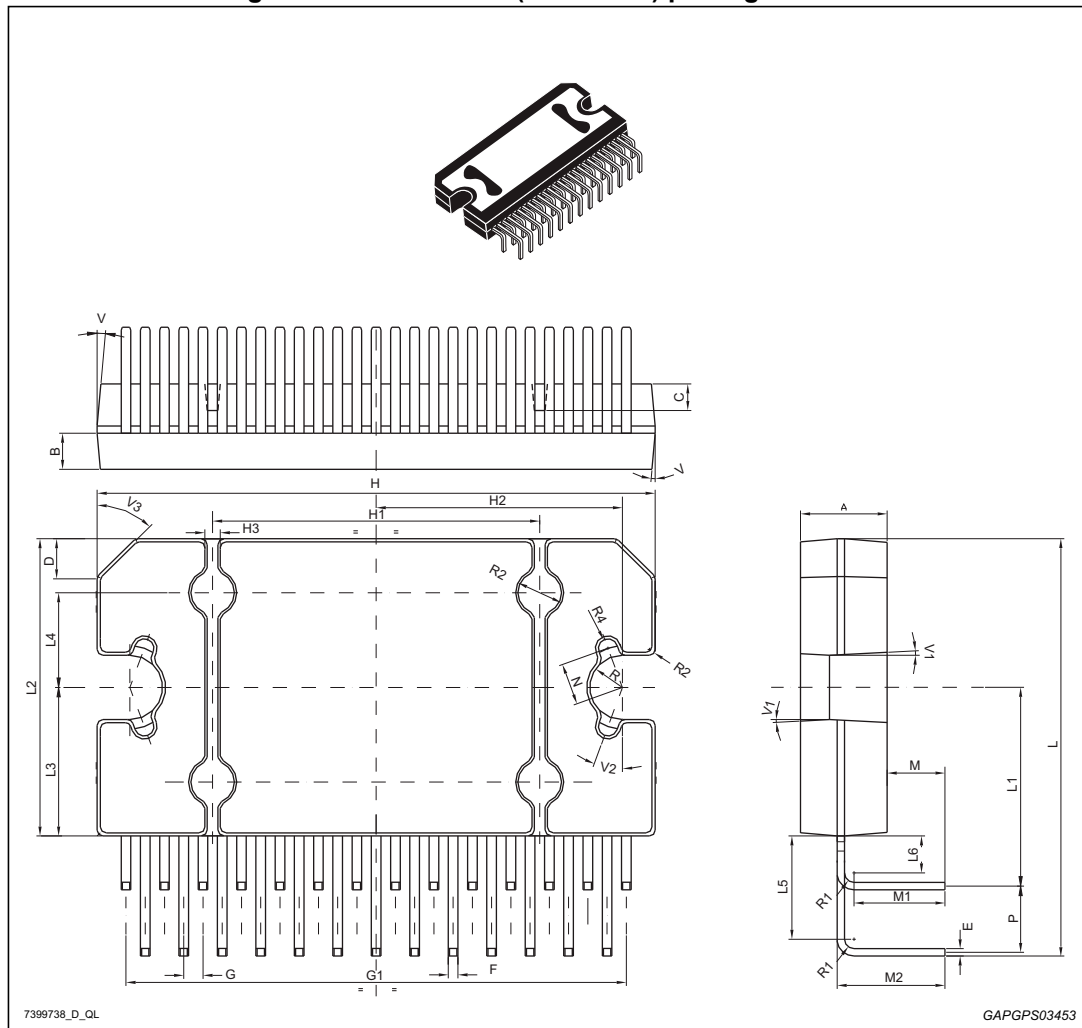


Table 34. Flexiwatt 27 (horizontal) package mechanical data

| Ref              | Dimensions  |      |      |                       |        |        |
|------------------|-------------|------|------|-----------------------|--------|--------|
|                  | Millimeters |      |      | Inches <sup>(1)</sup> |        |        |
|                  | Min.        | Typ. | Max. | Min.                  | Typ.   | Max.   |
| A                | 4.45        | 4.50 | 4.65 | 0.1752                | 0.1772 | 0.1831 |
| B                | 1.80        | 1.90 | 2.00 | 0.0709                | 0.0748 | 0.0787 |
| C                | -           | 1.40 | -    | -                     | 0.0551 | -      |
| D                | -           | 2.00 | -    | -                     | 0.0787 | -      |
| E                | 0.37        | 0.39 | 0.42 | 0.0146                | 0.0154 | 0.0165 |
| F <sup>(2)</sup> | -           | -    | 0.57 | -                     | -      | 0.0224 |
| G                | 0.75        | 1.00 | 1.25 | 0.0295                | 0.0394 | 0.0492 |

**Table 34. Flexiwatt 27 (horizontal) package mechanical data (continued)**

| Ref               | Dimensions  |       |       |                       |        |        |
|-------------------|-------------|-------|-------|-----------------------|--------|--------|
|                   | Millimeters |       |       | Inches <sup>(1)</sup> |        |        |
|                   | Min.        | Typ.  | Max.  | Min.                  | Typ.   | Max.   |
| G1                | 25.70       | 26.00 | 26.30 | 1.0118                | 1.0236 | 1.0354 |
| H <sup>(3)</sup>  | 28.90       | 29.23 | 29.30 | 1.1378                | 1.1508 | 1.1535 |
| H1                | -           | 17.00 | -     | -                     | 0.6693 | -      |
| H2                | -           | 12.80 | -     | -                     | 0.5039 | -      |
| H3                | -           | 0.80  | -     | -                     | 0.0315 | -      |
| L <sup>(3)</sup>  | 21.64       | 22.04 | 22.44 | 0.8520                | 0.8677 | 0.8835 |
| L1                | 10.15       | 10.50 | 10.85 | 0.3996                | 0.4134 | 0.4272 |
| L2 <sup>(3)</sup> | 15.50       | 15.70 | 15.90 | 0.6102                | 0.6181 | 0.6260 |
| L3                | 7.70        | 7.85  | 7.95  | 0.3031                | 0.3091 | 0.3130 |
| L4                | -           | 5     | -     | -                     | 0.1969 | -      |
| L5                | 5.15        | 5.45  | 5.85  | 0.2028                | 0.2146 | 0.2303 |
| M                 | 2.75        | 3.00  | 3.50  | 0.1083                | 0.1181 | 0.1378 |
| M1                | -           | 4.73  | -     | -                     | 0.1862 | -      |
| M2                | -           | 5.61  | -     | -                     | 0.2209 | -      |
| N                 | -           | 2.20  | -     | -                     | 0.0866 | -      |
| P                 | 3.20        | 3.50  | 3.80  | 0.1260                | 0.1378 | 0.1496 |
| R                 | -           | 1.70  | -     | -                     | 0.0669 | -      |
| R1                | -           | 0.5   | -     | -                     | 0.0197 | -      |
| R2                | -           | 0.3   | -     | -                     | 0.0118 | -      |
| R3                | -           | 1.25  | -     | -                     | 0.0492 | -      |
| R4                | -           | 0.50  | -     | -                     | 0.0197 | -      |
| V                 | 5°          |       |       | 5°                    |        |        |
| V1                | 3°          |       |       | 3°                    |        |        |
| V2                | 20°         |       |       | 20°                   |        |        |
| V3                | 45°         |       |       | 45°                   |        |        |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. dam-bar protusion not included.
3. molding protusion included.

### 11.5 Package marking information

Figure 52. PowerSO-36 marking information

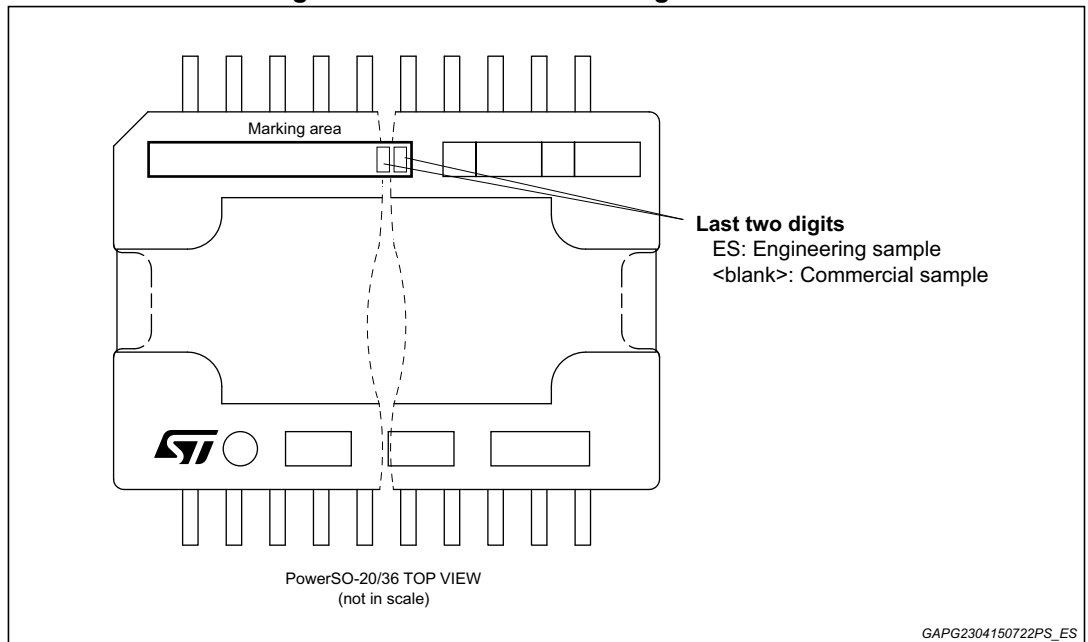
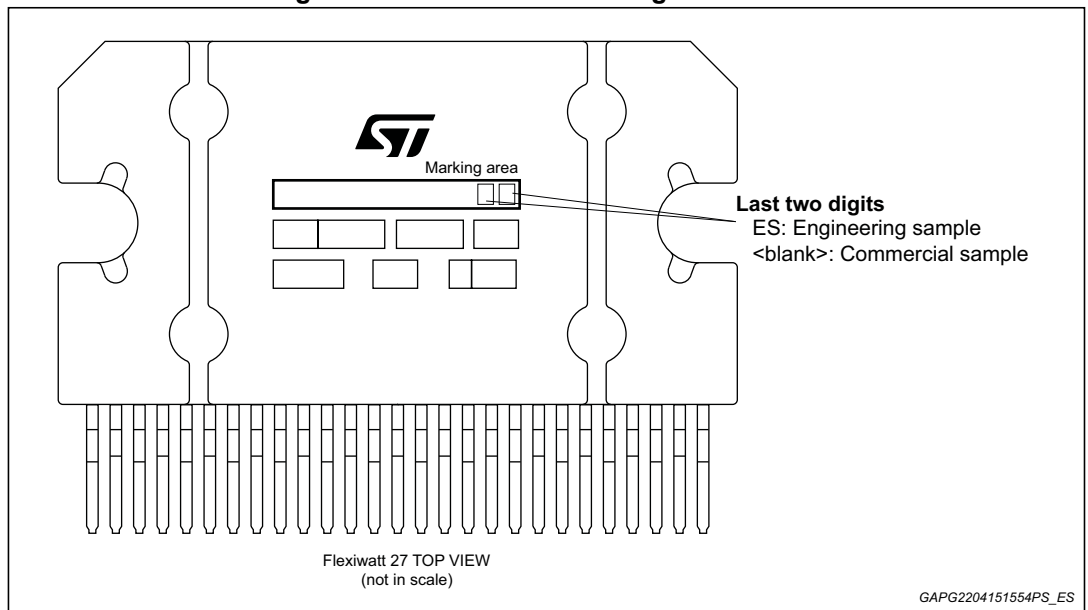


Figure 53. Flexiwatt 27 marking information



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## 12 Order codes

**Table 35. Ordering information**

| Order code   | Package                  | Packing     |
|--------------|--------------------------|-------------|
| TDA7803A-48X | Flexiwatt27 (Vertical)   | Tube        |
| TDA7803A-QLX | Flexiwatt27 (Horizontal) | Tube        |
| TDA7803A-8ZX | Flexiwatt27 (SMD)        | Tube        |
| TDA7803A-8ZT |                          | Tape & reel |
| TDA7803A-ZSX | PowerSO36                | Tube        |
| TDA7803A-ZST |                          | Tape & reel |

## 13 Revision history

**Table 36. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 16-Jun-2017 | 1        | Initial release.   |
| 19-Oct-2017 | 2        | Removed note 1 (Part number not yet released for production.) on <a href="#">Table 35: Ordering information on page 70</a> . |
| 15-Dec-2017 | 3        | Update column note for "T <sub>PLS</sub> and X" parameters in <a href="#">Table 6</a> .                                      |
| 18-Jan-2018 | 4        | Document changed from "Confidential" to "Public", no content change.   |

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## Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

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