

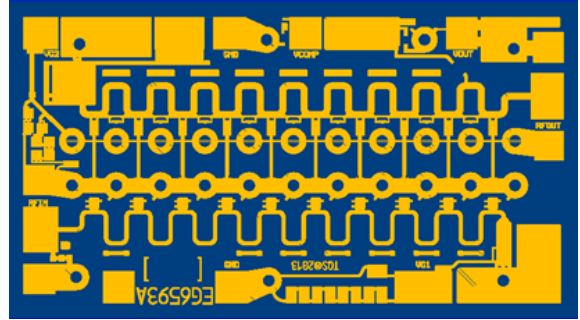
Product Description

The TriQuint TGA4852 is a medium power wideband AGC MMIC. Drain bias may be applied through the output port for best efficiency or through the on-chip drain termination. RF ports are DC coupled enabling the user to customize system corner frequencies. The TGA4852 requires off-chip decoupling and blocking components.

The TGA4852 is an excellent choice for 40Gb/s and 100Gb/s applications. The TGA4852 is capable of driving a modulator with an adjustable output voltage of 3-10 Vpp.

Bond pad and backside metallization is gold plated for compatibility with eutectic alloy attachment methods as well as the thermocompression and thermosonic wire bonding processes. Each device is 100% DC and RF tested on-wafer to ensure performance compliance. The device is available in die form.

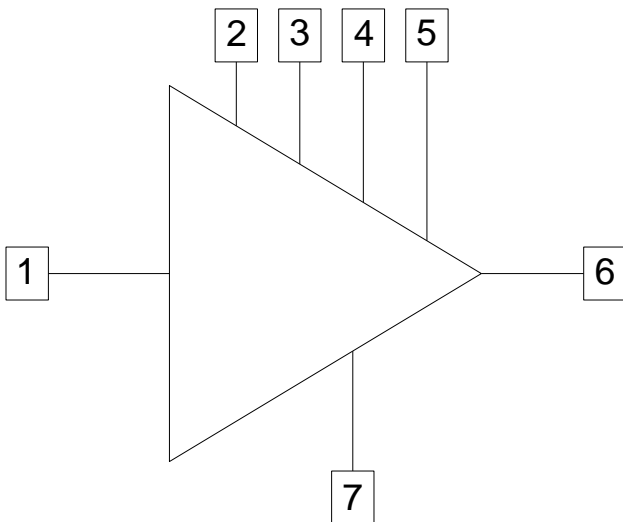
Lead Free & RoHS Compliant.



Product Features

- 40 & 100Gb/s Optical Modulator Driver
- 0.15um Power pHEMT Technology
- On-chip Power Detector
- Bias: $V_d = 6\text{ V}$, $I_d = 215\text{ mA}$ (7 Vpp out)
- Chip Size: 1.80 x 1.00 x 0.1 mm

Functional Block Diagram



Applications

- 40Gb/s DPSK / DQPSK Driver
- 100Gb/s DP-QPSK Driver
- 40Gb/s Predriver or Gain Block
- Test Equipment

Ordering Information

| Part No. | ECCN | Description |
|----------|-------------|----------------------|
| TGA4852 | 3A001.b.2.d | DC – 35GHz Amplifier |

Absolute Maximum Ratings

| Parameter | Value / Range |
|--------------------------------|---------------------------------|
| Drain Voltage, Vd | 9 V |
| Drain Voltage Termination, VdT | $(VdT - IdT \cdot 50) \leq 9$ V |
| Gate Voltage, Vg | -5 to 0 V |
| Control Voltage, Vc | MAX [(Vd-7), -1.3 V] to +3.9 V |
| Drain to Gate Voltage | 13 V |
| Drain Current, Id | 270 mA |
| Drain Current Termination, IdT | 135 mA |
| Ig | -30 to + 16 mA |
| RF CW Input Power | 10 Vpp (24 dBm) |
| Channel Temperature, Tch | 200 °C |
| Mounting Temperature (30 sec) | 320 °C |
| Storage Temperature | -40 to 150 °C |

Notes:

1. Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.
2. If VdT pin is being used:
assure $(VdT - IdT \cdot 50) - Vc \geq -0.5$ V.
3. If RFout / Vd pin is being used:
assure $Vd - Vc \geq -0.5$ V.

Recommended Operating Conditions

| Parameter | Min | Typ | Max | Units |
|-----------|-----|------|-----|-------|
| Vd | | 6 | | V |
| Id | | 215 | | mA |
| Vg | | -1.8 | | V |
| Vc | | 0.7 | | V |
| Ig | | <1 | | mA |
| Ic | | <2 | | mA |

Note:

1. Recommended operating conditions are measured at specified test conditions of Vout = 7 Vpp when Vin = 3.6 Vpp, 21.5 Gb/s.

Electrical Specifications

Test conditions unless otherwise noted: 25 °C, Vd = 7 V, Vc = 0.8 V, Id = 190 mA, Vg ~ -1.8 V typical.

| Parameter | Min | Typ | Max | Units |
|-----------------------|-----|------|-----|-------|
| Operational Data rate | | 21.5 | | Gb/s |
| Small Signal Gain | | | | dB |
| f = 0.1 - 20 GHz | | 11 | | |
| f = 20.1 - 30 GHz | | 10 | | |
| f = 30.1 - 35 GHz | | 9 | | |
| f = 35.1 - 40 GHz | | 6 | | |
| f = 40.1 - 50 GHz | | 4 | | |
| Input Return Loss | | | | dB |
| f = 0.1 – 25 GHz | | 15 | | |
| f = 25.1 – 30 GHz | | 15 | | |
| f = 30.1 – 35 GHz | | 15 | | |
| f = 35.1 - 38 GHz | | 10 | | |
| f = 38.1 – 50 GHz | | 6 | | |
| Output Return Loss | | | | dB |
| f = 0.1 - 20 GHz | | 15 | | |
| f = 20.1 - 30 GHz | | 12 | | |
| f = 30.1 - 35 GHz | | 10 | | |
| f = 35.1 - 50 GHz | | - | | |
| 3 dB Bandwidth | | 37 | | GHz |

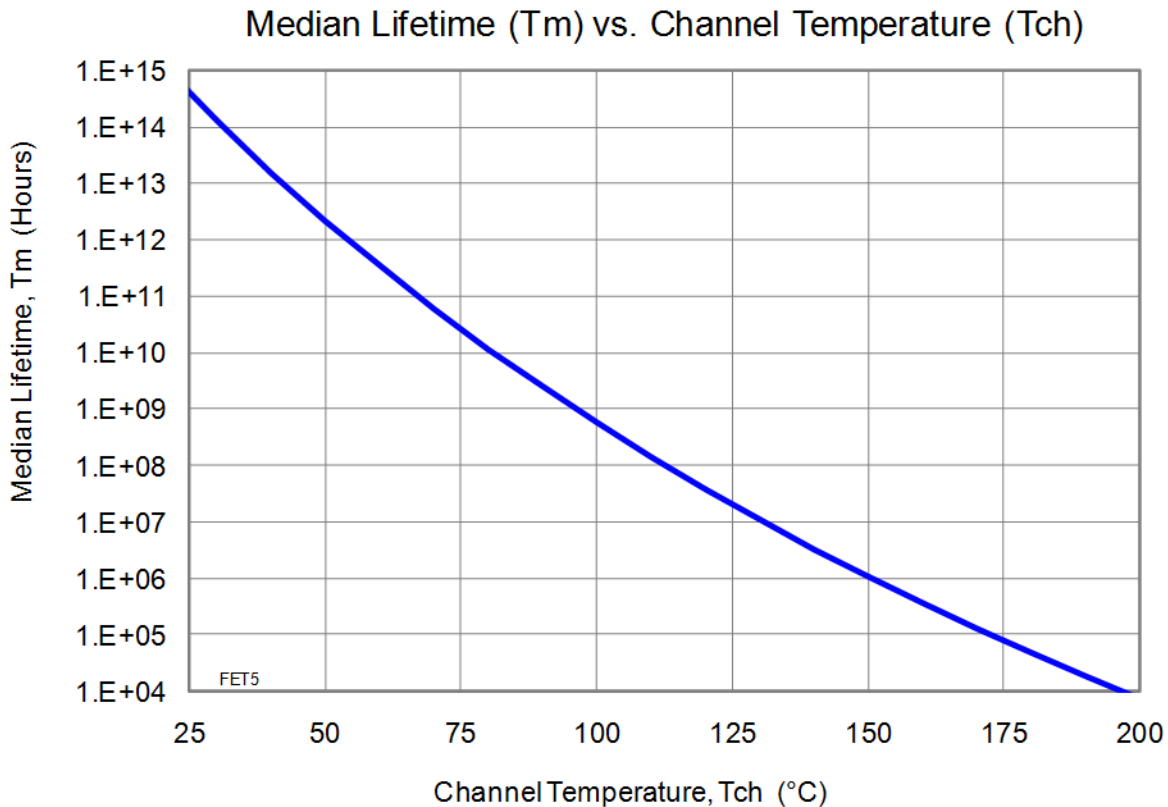
Thermal and Reliability Information

| Parameter | Test Conditions | Value |
|--------------------------------------------------------------------|--------------------------------------------------------------------------|-----------------------------------------------|
| Thermal Resistance, θ_{JC} , measured to back of package | Tbase = 70 °C | $\theta_{JC} = 43.1 \text{ }^\circ\text{C/W}$ |
| Channel Temperature (Tch), and Median Lifetime (Tm) | Tbase = 70 °C Vd = 6 V, Id = 200 mA Pdiss = 1.2 W | Tch = 122 °C Tm = 3E+7 Hours |
| Channel Temperature (Tch), and Median Lifetime (Tm) Under RF Drive | Tbase = 70 °C Vd = 6 V, Id = 215 mA Vout = 7 Vpp Pdiss = 1.17 W | Tch = 120 °C Tm = 3.7E+7 Hours |

Notes

1. Channel operating temperature will directly affect the device median lifetime (Tm). For maximum life, it is recommended that channel temperatures be maintained at the lowest possible levels.
2. θ_{jc} is the thermal resistance of the die mounted to a 0.020" thick Cu-Mo block using 0.8 mil conductive epoxy.

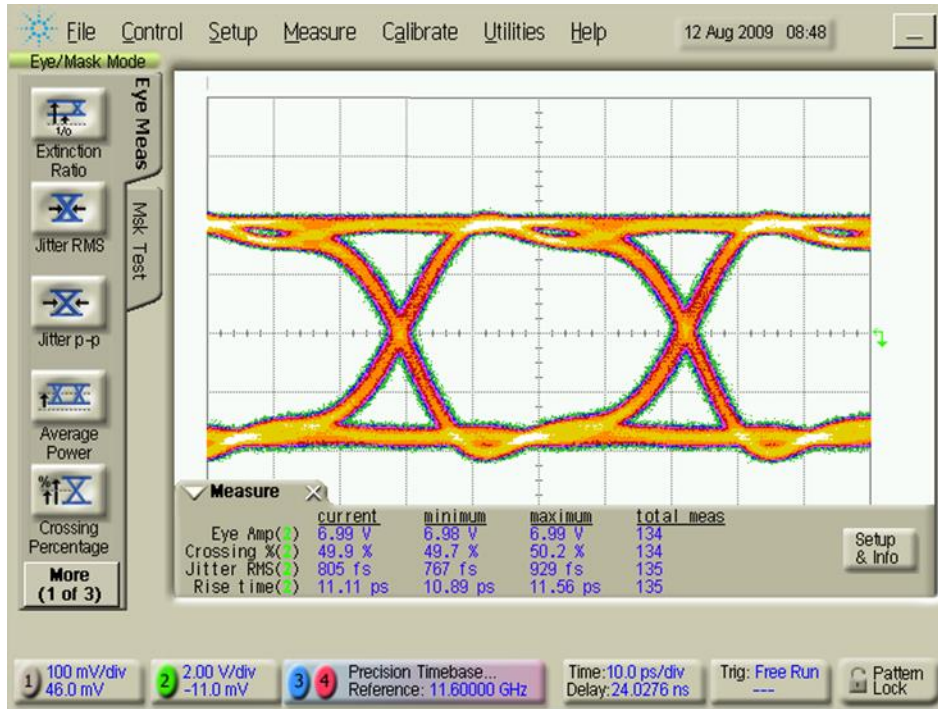
Median Lifetime



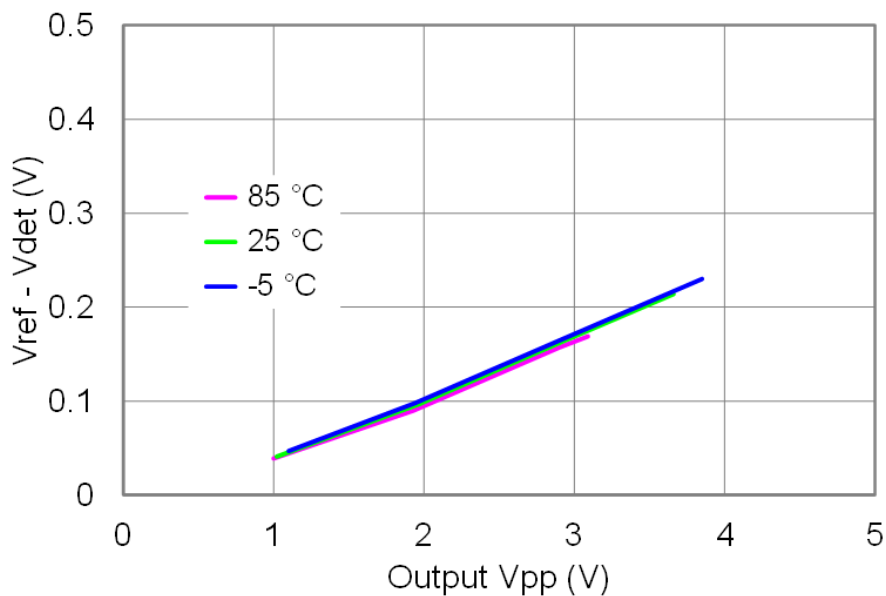
Typical Performance Electrical Eye Diagram

$V_{in} = 3.6 \text{ Vpp}$, 21.5 Gb/s, PRBS signal $2^{31} - 1$, V_g adjusted to attain desired V_{out} ., $T = 25 \text{ }^\circ\text{C}$

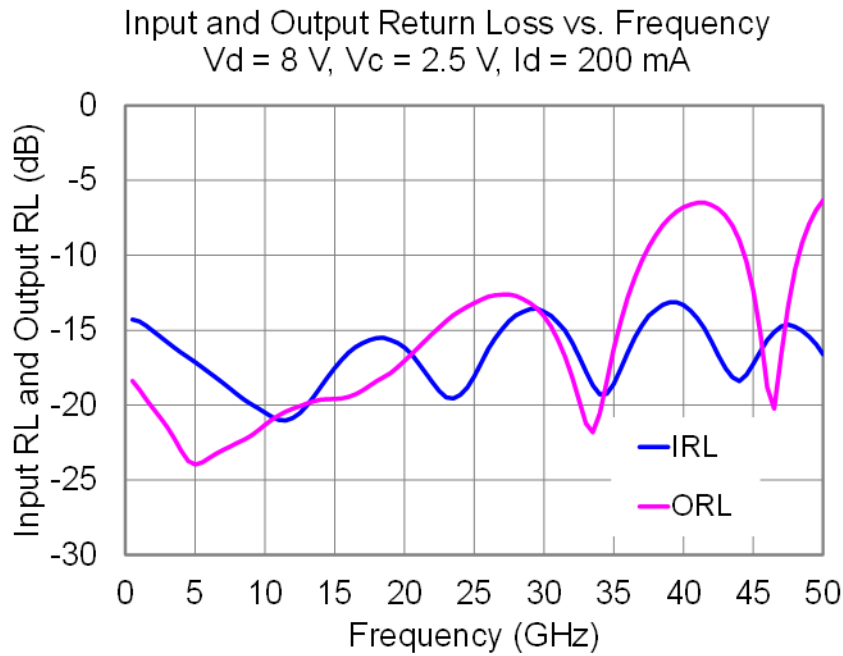
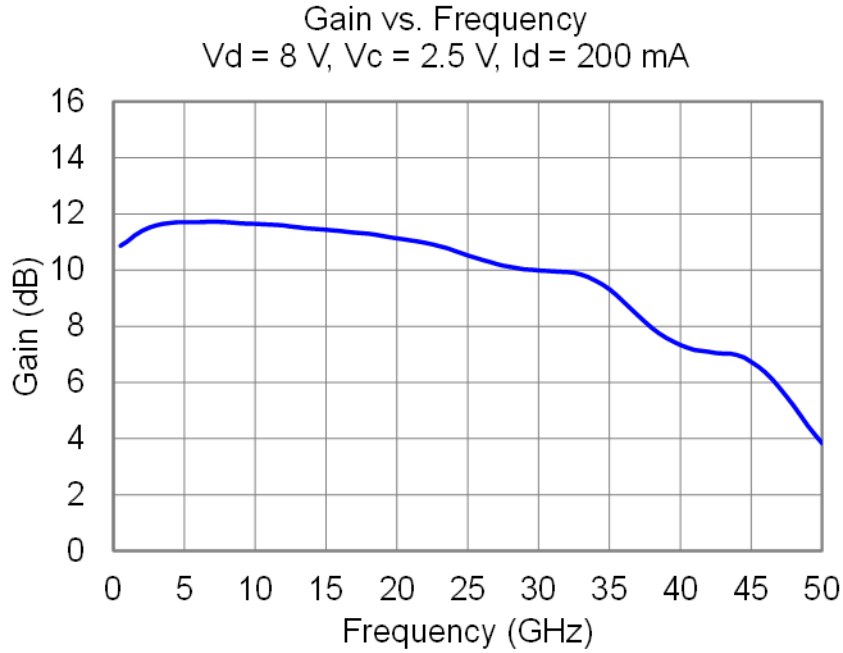
$V_d = 6 \text{ V}$, $V_c = 0.7 \text{ V}$, $I_d = 220 \text{ mA}$



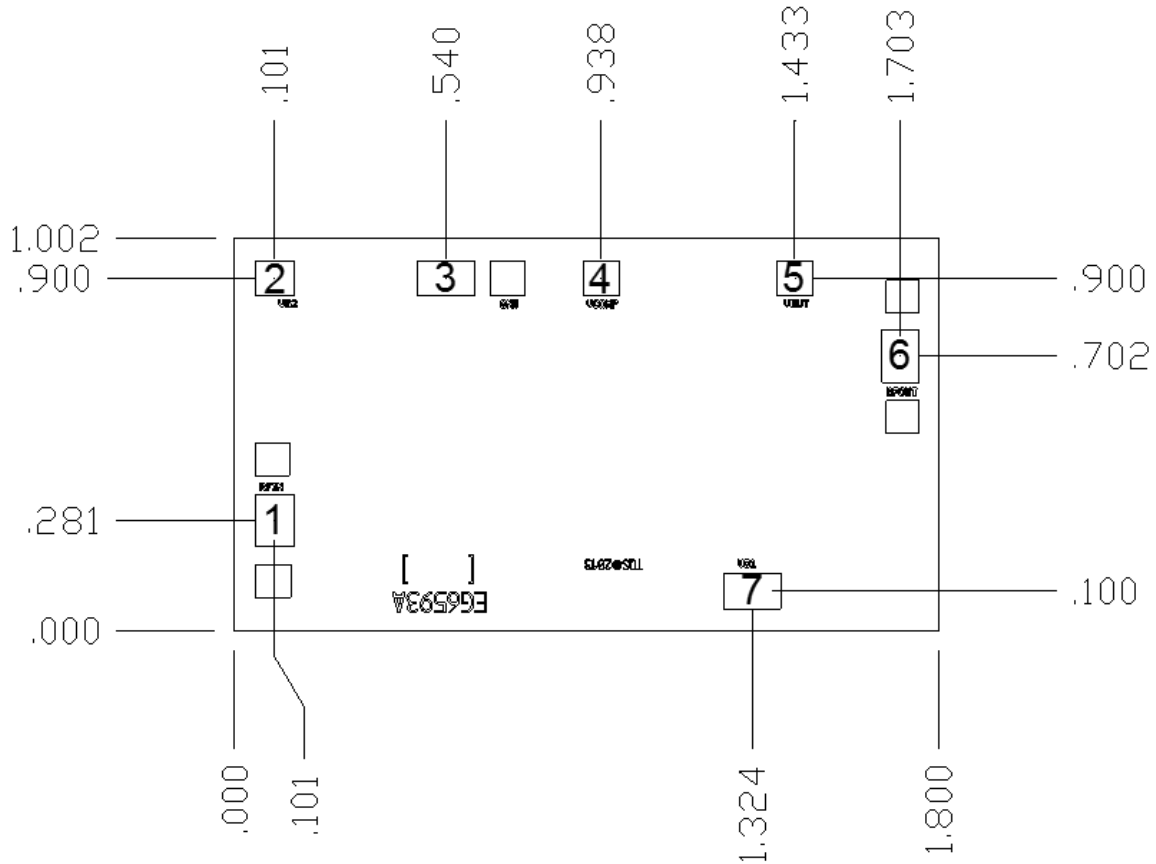
Vdet-Vref vs. Vout vs. Temperature



Typical Performance



Pin Configuration



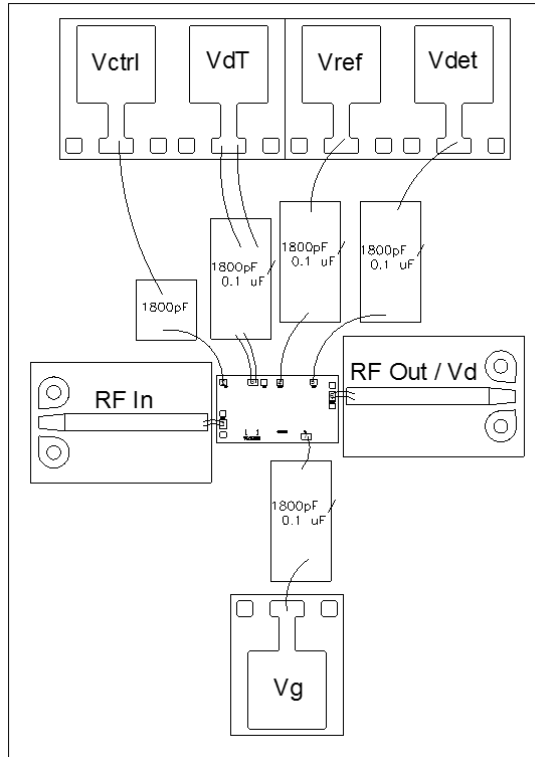
Units: millimeters
 Chip edge to bond pad dimensions are shown to center of pad
 Chip size tolerance: ± 0.051
 Thickness: 0.100 (reference only)

Pin Description

| Pin No. | Label | Description | Pad Size |
|---------|--------------------|--------------------------------------------------------------------------------|---------------|
| 1 | RFin | RF Input | 0.099 x 0.133 |
| 2 | Vc | Control voltage pin | 0.090 x 0.090 |
| 3 | VdT | Vd pin for biasing through the termination resistor | 0.146 x 0.090 |
| 4 | Vref | Diode reference voltage | 0.090 x 0.090 |
| 5 | Vdet | Diode detector output voltage | 0.090 x 0.090 |
| 6 | RFout / Vd (RFout) | RF Output and/or Vd bias pin (avoids voltage drop across termination resistor) | 0.094 x 0.136 |
| 7 | Vg | Gate voltage pin | 0.146 x 0.090 |

Application Circuit

Recommended Chip Assembly Diagram



Note: Input and Output ports are DC coupled.
If biasing Vd through the RFOut side, a bias tee is required.

Evaluation Board Bias Procedures

| Laboratory Bias-up Procedure: see Note 1 | Laboratory Bias-down Procedure |
|-----------------------------------------------------|--------------------------------|
| Set Vg to -3 V | Turn off RF supply. See note 2 |
| Set Vd or VdT to 6 V | Vg set to -3 V |
| Vc set to desired value | Vc set to 0 V |
| Adjust Vg more positive until target Id is reached. | Turn Vd to 0 V |
| Adjust Vc for desired Vout signal | Turn Vg to 0 V |
| Adjust Vg for 50% crossing | |
| Re-adjust Vc and Vg, if necessary | |
| Apply RF signal to RF Input. See note 2 | |

Notes:

- Any bias procedure will not harm the device as long as the guidelines explicitly stated in the Max Ratings Table and corresponding notes section on page 2 of the Datasheet are followed. For laboratory evaluation, the following is provided as a bias procedure that will allow user to observe and set each stage's quiescent point individually.
- RF supply can be on during power up and power down sequences.

Assembly Notes

Reflow Attachment:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C
- Use alloy station or conveyor furnace with reducing atmosphere
- No fluxes should be utilized
- Coefficient of thermal expansion matching is critical for long-term reliability
- Storage in dry nitrogen atmosphere

Adhesive Attachment:

- Organic attachment can be used in low-power applications
- Curing should be done in a convection oven; proper exhaust is a safety concern
- Microwave or radiant curing should not be used because of differential heating
- Coefficient of thermal expansion matching is critical


Component Pickup and Placement:

- Vacuum pencil and/or vacuum collet preferred method of pick up
- Avoidance of air bridges during placement
- Force impact critical during auto placement

Interconnect:

- Thermosonic ball bonding is the preferred interconnect technique
- Force, time, and ultrasonics are critical parameters
- Aluminum wire should not be used
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire
- Maximum stage temperature: 200°C

Handling Precautions

| Parameter | Rating | Standard |  Caution! ESD-Sensitive Device |
|------------------------------|--------|----------------------------|----------------------------------------------------------------------------------------------------------------------|
| ESD – Human Body Model (HBM) | TBD | JEDEC Standard JESD22 A114 | |

Solderability

Compatible with AuSn eutectic solder

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Qorvo:

Web: www.qorvo.com **Tel:** +1.972.994.8465
Email: info-sales@qorvo.com **Fax:** +1.972.994.8504

For technical questions and application information:

Email: info-products@qorvo.com

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Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331