

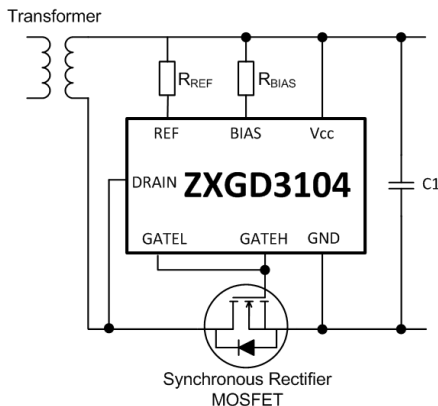
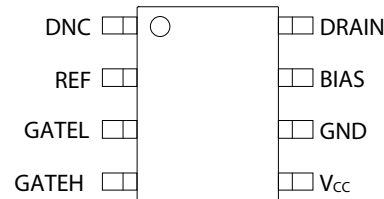
ZXGD3104N8
SYNCHRONOUS MOSFET CONTROLLER IN SO8
Description

The ZXGD3104 is intended to drive MOSFETS configured as ideal diode replacements. The device is comprised of a differential amplifier detector stage and high current driver. The detector monitors the reverse voltage of the MOSFET such that if body diode conduction occurs a positive voltage is applied to the MOSFET's Gate pin.

Once the positive voltage is applied to the Gate the MOSFET switches on. The detectors' output voltage is then proportional to the MOSFET Drain-Source voltage and this is applied to the Gate via the driver. This action provides a rapid MOSFET turn off at zero Drain current.

Applications

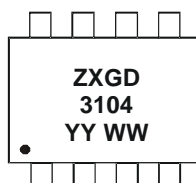
- Flyback Converters in:
 - ≥90W Laptop Adaptors

Typical Configuration

SO-8

 Top View
 Pin-Out

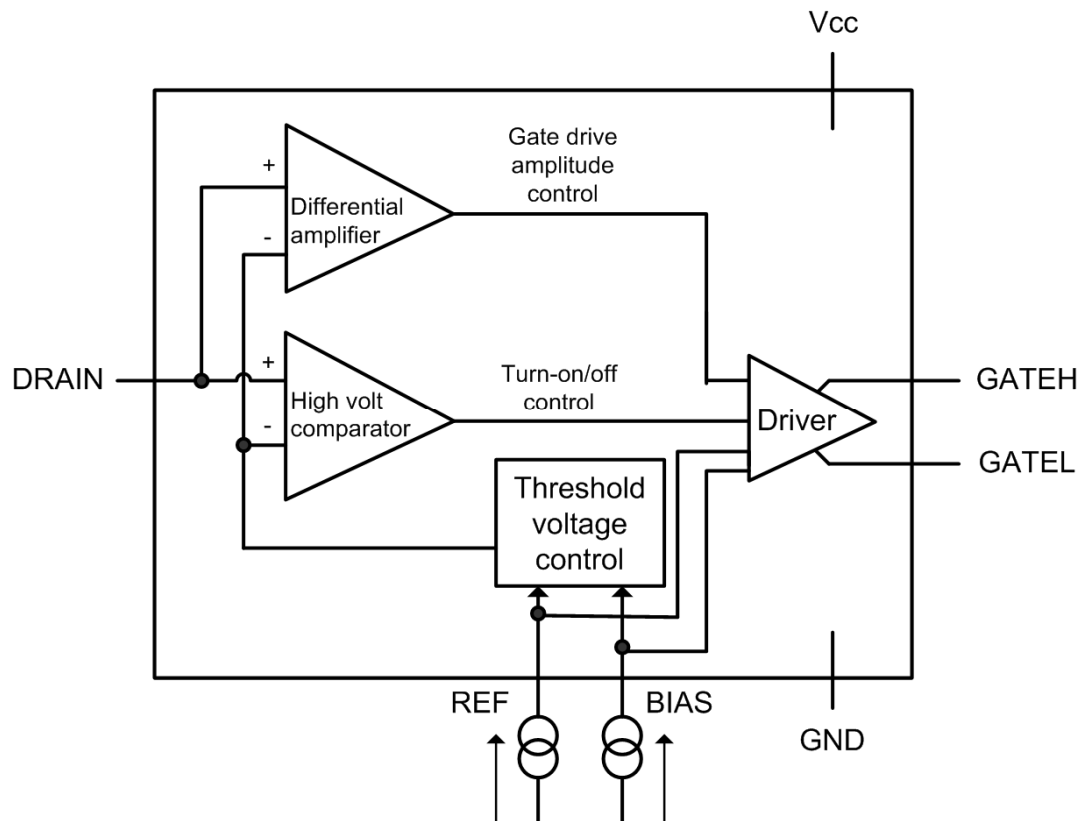
Ordering Information (Note 3)

| Product | Marking | Reel size (inches) | Tape width (mm) | Quantity per reel |
|--------------|----------|--------------------|-----------------|-------------------|
| ZXGD3104N8TC | ZXGD3104 | 13 | 12 | 2,500 |

- Notes:
1. No purposefully added lead
 2. Diodes Inc's "Green" Policy can be found on our website at <http://www.diodes.com>
 3. For packaging details, go to our website at <http://www.diodes.com>

Marking Information


- ZXGD = Product Type Marking Code, Line 1
 3104 = Product Type Marking Code, Line 2
 YY = Year (ex: 11 = 2011)
 WW = Week (01 - 53)

Functional Block Diagram


| Pin No. | Name | Description and function |
|---------|----------|--|
| 1 | DNC | Do not connect Leave pin floating. |
| 2 | REF | Reference This pin is connected to V_{CC} via resistor, R_{REF} . Select R_{REF} to source 2.16mA into this pin. Refer to Table 1, in Application Information section. |
| 3 | GATEL | Gate turn off This pin sinks current, I_{SINK} , from the synchronous MOSFET Gate. |
| 4 | GATEH | Gate turn on This pin sources current, I_{SOURCE} , to the synchronous MOSFET Gate. |
| 5 | V_{CC} | Power Supply This is the supply pin. It is recommended to decouple this point to ground closely with a ceramic capacitor. |
| 6 | GND | Ground This is the ground reference point. Connect to the synchronous MOSFET Source terminal. |
| 7 | BIAS | Bias This pin is connected to V_{CC} via resistor, R_{BIAS} . Select R_{BIAS} to source 3mA into this pin. Refer to Table 1, in Application Information section. |
| 8 | DRAIN | Drain connection This pin connects directly to the synchronous MOSFET Drain terminal. |

ZXGD3104N8
Maximum Ratings @T_A = 25°C unless otherwise specified

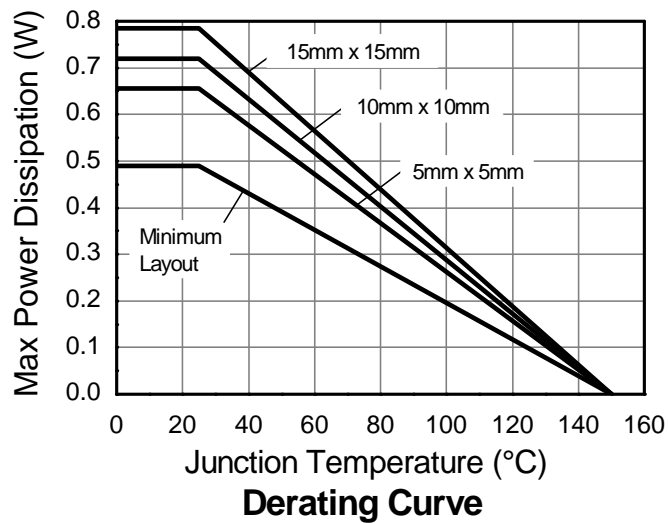
| Characteristic | Symbol | Value | Unit |
|---------------------------------|---------------------|---------------------------|------|
| Supply voltage, relative to GND | V _{CC} | 25 | V |
| Drain pin voltage | V _D | -3 to 180 | V |
| Gate output voltage | V _G | -3 to V _{CC} + 3 | V |
| Gate Driver peak source current | I _{SOURCE} | 2.5 | A |
| Gate Driver peak sink current | I _{SINK} | 7 | A |
| Reference voltage | V _{REF} | V _{CC} | V |
| Reference current | I _{REF} | 25 | mA |
| Bias voltage | V _{BIAS} | V _{CC} | V |
| Bias current | I _{BIAS} | 100 | mA |

Thermal Characteristics @T_A = 25°C unless otherwise specified

| Characteristic | Symbol | Value | Unit |
|---|------------------|-------------|-------------|
| Power Dissipation Linear derating factor | P _D | 490 | mW mW/°C |
| | | 3.92 | |
| | | 655 | |
| | | 5.24 | |
| | | 720 | |
| Thermal Resistance, Junction to Ambient | R _{θJA} | 5.76 | °C/W |
| | | 785 | |
| | | 6.28 | |
| | | 255 | |
| | | 191 | |
| Thermal Resistance, Junction to Lead | R _{θJL} | 173 | °C/W |
| | | 159 | |
| | | 135 | |
| Operating Temperature Range | T _J | -40 to +150 | °C |
| Storage Temperature Range | T _{STG} | -50 to +150 | |

- Notes:
4. For a device surface mounted on minimum recommended pad layout FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
 5. Same as note (4), except pin 5 (V_{CC}) and pin 6 (GND) are both connected to separate 5mm x 5mm 1oz copper heatsinks.
 6. Same as note (5), except both heatsinks are 10mm x 10mm.
 7. Same as note (5), except both heatsinks are 15mm x 15mm.
 8. Thermal resistance from junction to solder-point at the end of each lead on pin 5 (V_{CC}) and pin 6 (GND).

Thermal Derating Curve



ESD Rating

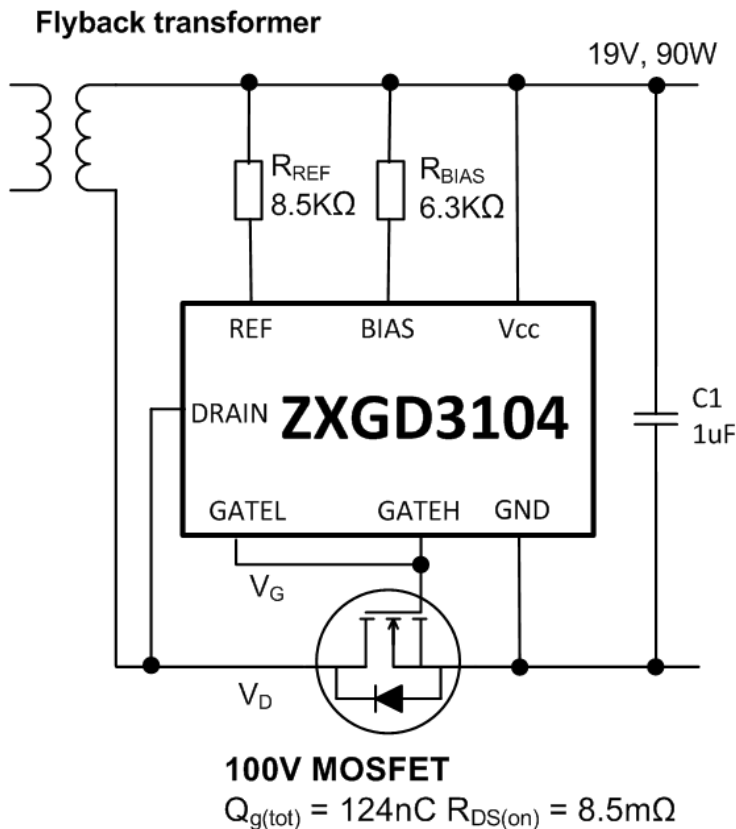
| Characteristic | Value | Unit |
|--------------------------|-------|------|
| ESD for Human Body Model | 2000 | V |
| ESD for Machine Model | 300 | |

Electrical Characteristics @T_A = 25°C unless otherwise specified

 V_{CC} = 19V; R_{BIAS} = 6.3kΩ; R_{REF} = 8.5kΩ

| Characteristic | | Symbol | Min | Typ | Max | Unit | Test Condition | |
|---|----------------|----------------------|------|------|-----------------|----------------------------|-------------------------|--|
| Input and Supply | | | | | | | | |
| Quiescent current | | I _Q | - | 5.16 | - | mA | V _D ≥ 0V | |
| Gate Driver | | | | | | | | |
| Turn-off Threshold Voltage (Note 9 & 10) | | V _T | -16 | -10 | 0 | mV | V _G = 1V | |
| Gate output voltage | (Note 9 & 10) | V _{G(off)} | 0 | 0.73 | 1.0 | V | V _D ≥ 1V | |
| | (Note 9 & 11) | V _G | 12.5 | 14 | V _{CC} | | V _D = -50mV | |
| | | | 17 | 18 | V _{CC} | | V _D = -100mV | |
| Switching Performance for Q _{G(tot)} = 124nC (Note 12) | | | | | | | | |
| Turn-on propagation delay | | t _{d(rise)} | 175 | 250 | 325 | ns | - | Refer to switching waveforms in Fig. 1 |
| Turn-off propagation delay | | t _{d(fall)} | 11 | 15 | 20 | | | |
| Gate rise time | t _r | 335 | 480 | 625 | | | | |
| | | 530 | 760 | 990 | | | | |
| Gate fall time | | t _f | 35 | 50 | 65 | Continuous Conduction Mode | | |

Notes: 9. GATEH connected to GATEL
 10. R_H = 100kΩ, R_L = O/C
 11. R_L = 100kΩ, R_H = O/C
 12. refer to test circuit below


Test conditions

Primary side input voltage = 400V
 Switching frequency = 65kHz
 Discontinuous conduction mode

Descriptions of the normal operation

The operation of the controller is described step-by-step with reference to the timing diagram in Figure 1.

1. The controller monitors the MOSFET Drain-Source voltage.
2. When, due to transformer action, the MOSFET body diode is forced to conduct there is approximately -0.8V on the Drain pin.
3. The detector outputs a positive voltage with respect to ground, this voltage is then fed to the MOSFET driver stage and current is sourced out of the GATE pin.
4. The controller goes into proportional gate drive control — the GATE output voltage is proportional to the on-resistance-induced Drain-Source voltage drop across the MOSFET. Proportional gate drive ensures that MOSFET conducts for majority of the conduction cycle and minimizes body diode conduction time.
5. As the Drain current decays linearly toward zero, proportional gate drive control reduces the Gate voltage so the MOSFET can be turned off rapidly at zero current crossing. The GATE voltage is removed when the Drain-Source voltage crosses the detection threshold voltage to minimize reverse current flow.
6. At zero Drain current, the controller GATE output voltage is pulled low to $V_{G(off)}$ to ensure that the MOSFET is off.

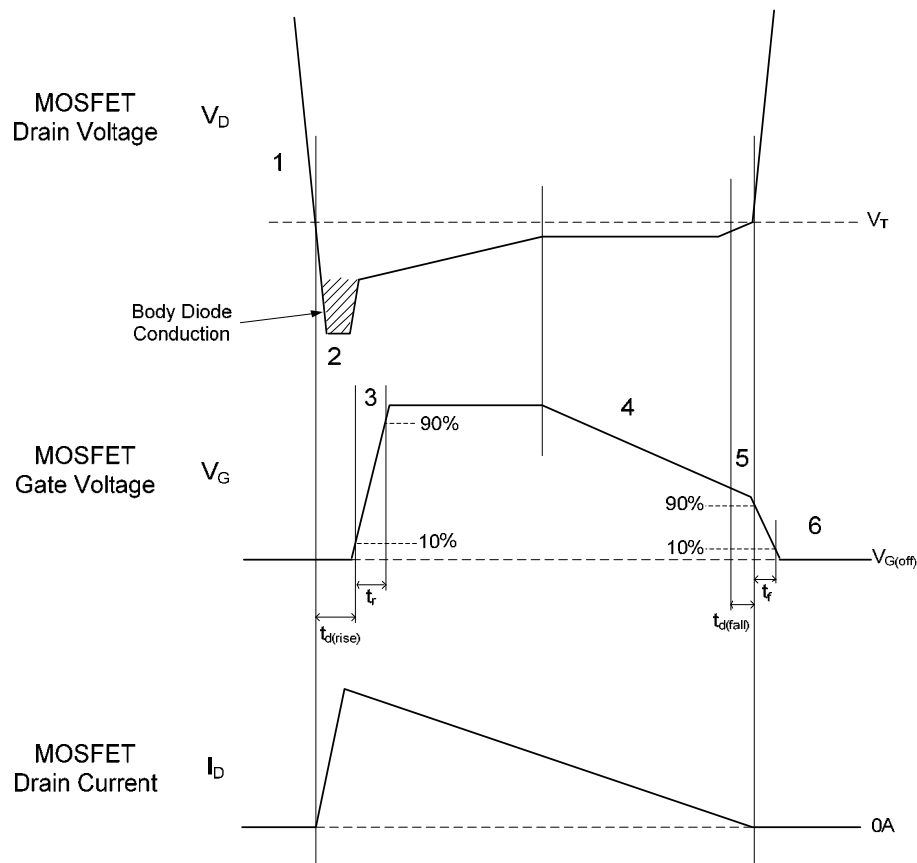
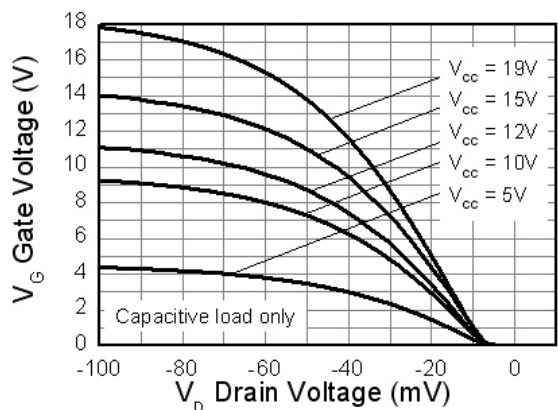
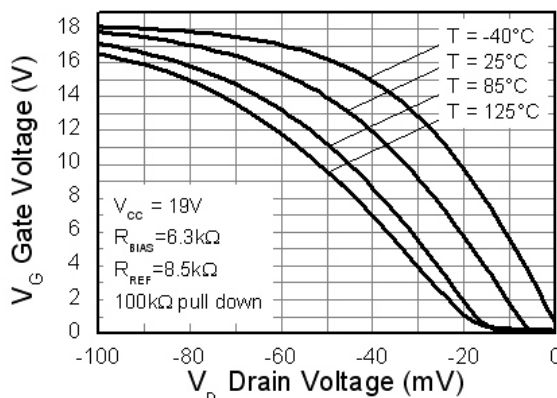


Figure 1. Timing diagram for a critical conduction mode Flyback converter

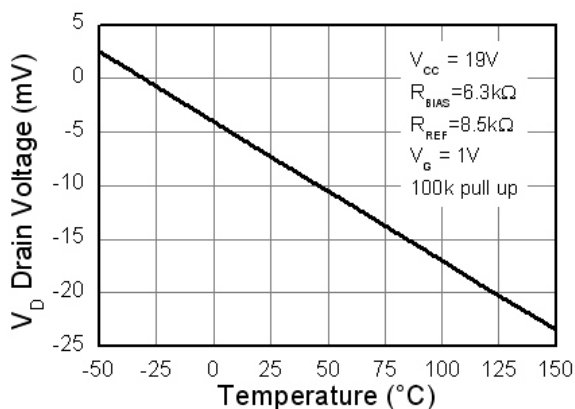
Typical Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified



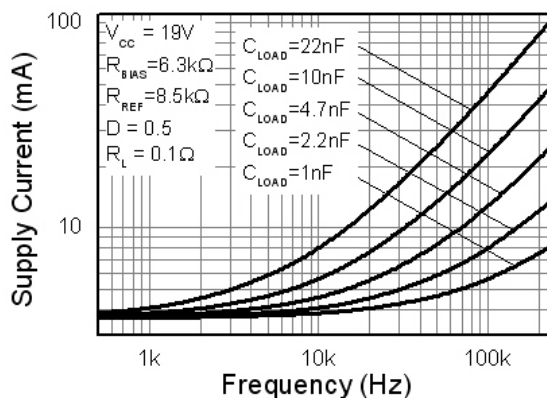
Transfer Characteristic



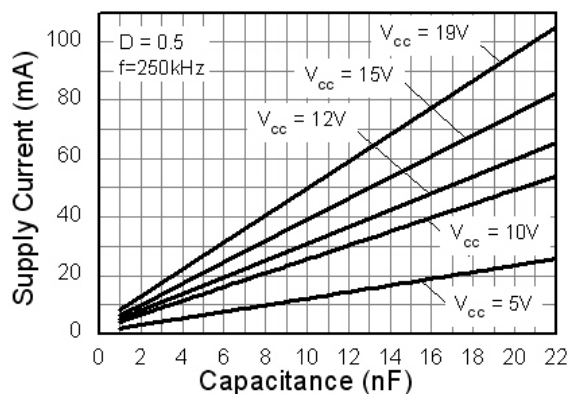
Transfer Characteristic



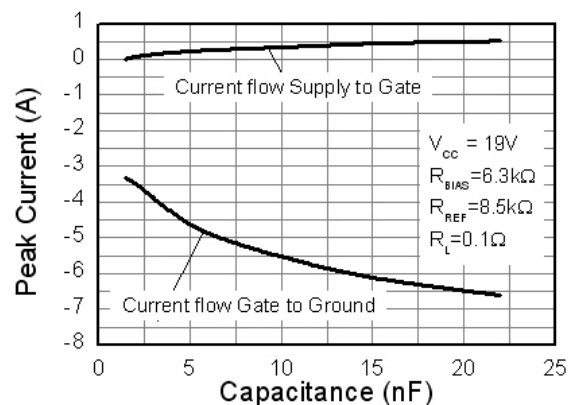
Drain Sense Voltage vs Temperature



Supply Current vs Frequency

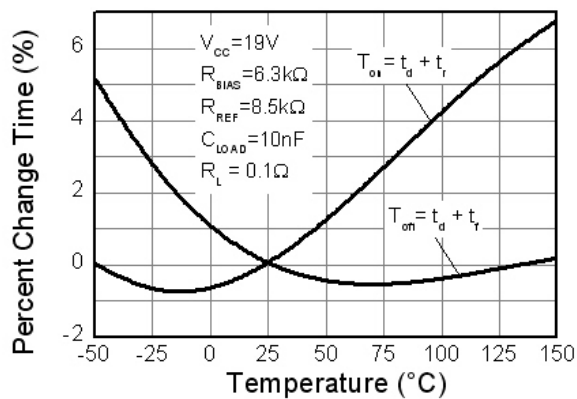
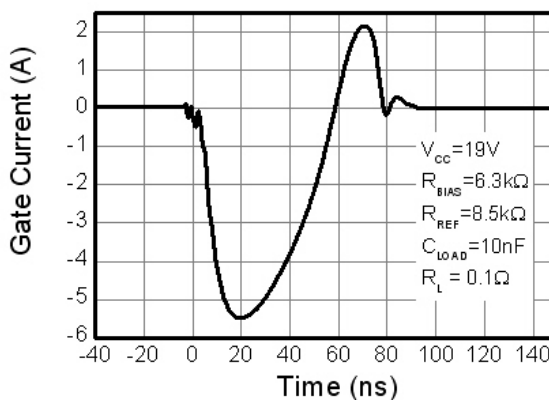
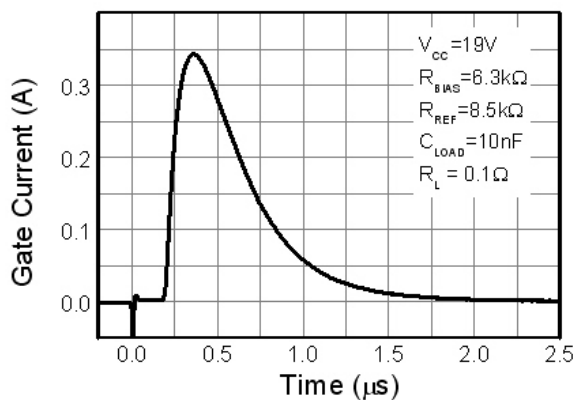
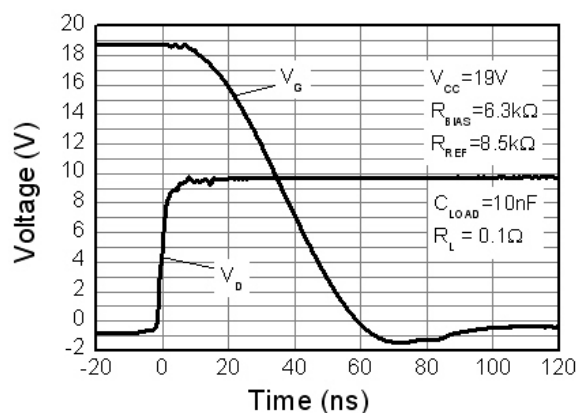
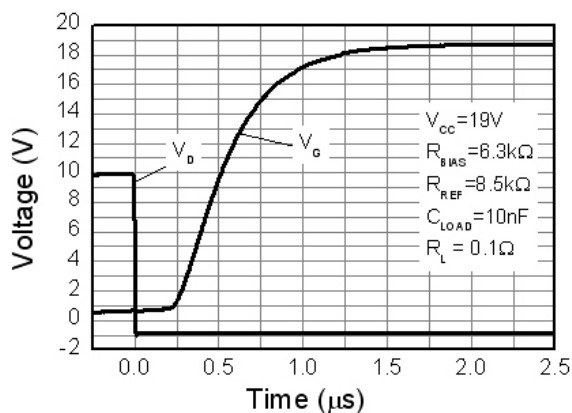


Supply Current vs Capacitive Load



Gate Current vs Capacitive Load

Continued - Typical Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified



Typical waveforms

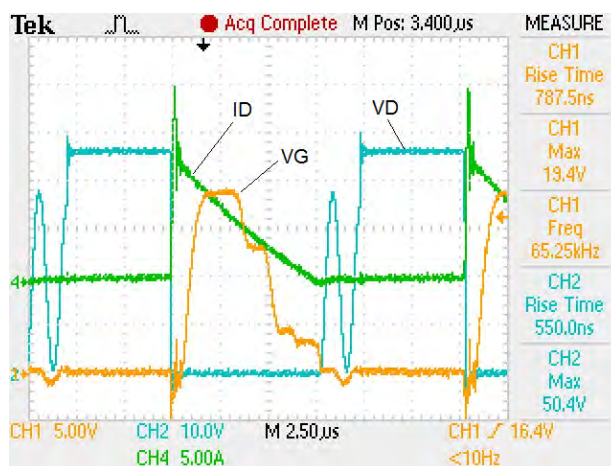


Fig 3a: Critical conduction mode, operating for MOSFET with $Q_{g(TOT)} = 124nC$

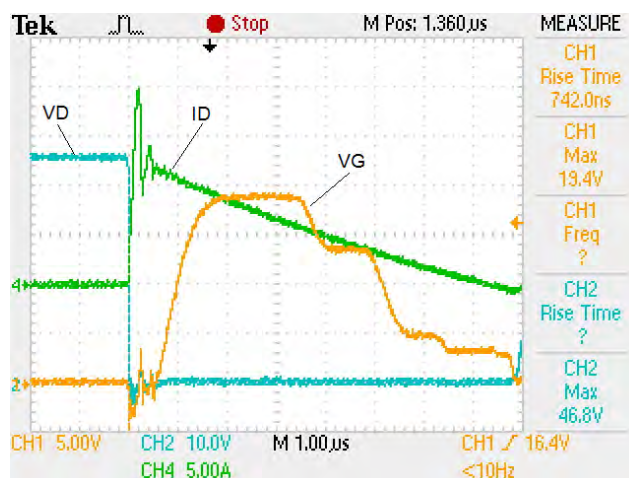


Fig 3b: Typical switching waveform

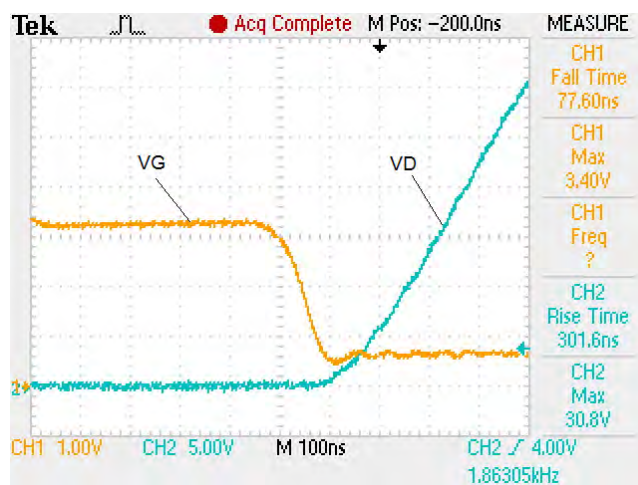


Fig 3c: Close up of typical turn off waveform

Design considerations

It is advisable to decouple the ZXGD3104 closely to V_{CC} and ground due to the possibility of high peak gate currents with a $1\mu\text{F}$ X7R type ceramic capacitor C1 as shown in Figure 2. Also the ground return loop should be as short as possible.

To minimize parasitic inductance-induced premature turn-off of the synchronous controller always keep the PCB track length between ZXGD3104's Drain input and MOSFET's Drain to less than 10mm. Low internal inductance SMD MOSFET packages are also recommended for high switching frequency power conversion to minimize MOSFET body diode conduction loss.

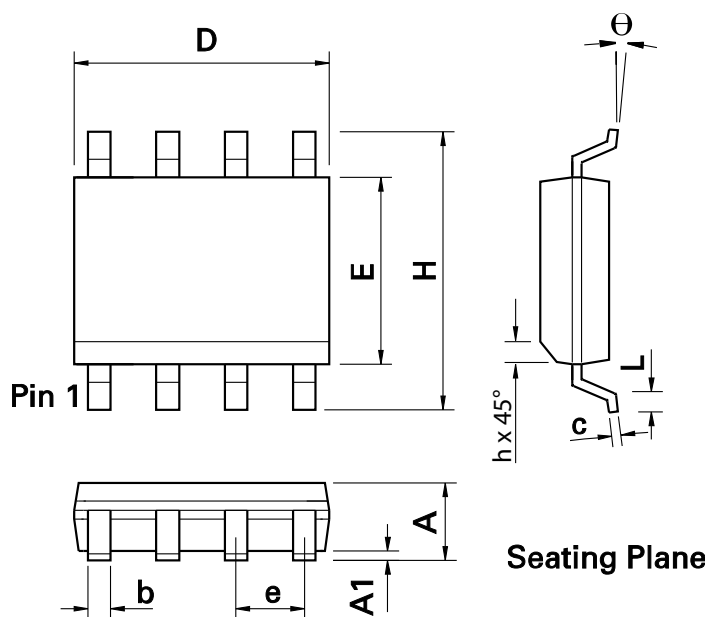
The Gate pins should be as close to the MOSFET's gate as possible. External gate resistors are optional. They can be inserted to control the rise and fall time which may help with EMI issues.

The careful selection of external resistors R_{REF} and R_{BIAS} is important to the optimum device operation. Select a value for resistor R_{REF} and R_{BIAS} from Table 1 based on the desired V_{CC} value. This provides the typical ZXGD3104's detection threshold voltage of -10mV.

Table 1. Recommended resistor values for various supply voltages

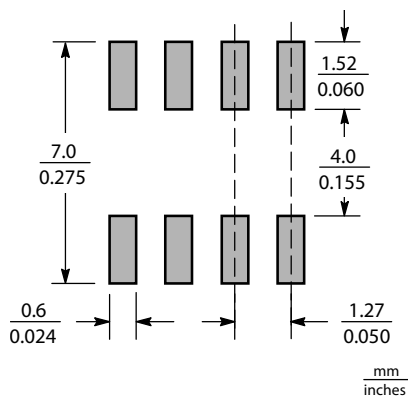
| V_{CC} | R_{BIAS} | R_{REF} |
|----------|----------------|----------------|
| 5V | 1.6 k Ω | 2 k Ω |
| 10V | 3.3 k Ω | 4.3 k Ω |
| 12V | 3.9 k Ω | 5.1 k Ω |
| 15V | 5.1 k Ω | 6.8 k Ω |
| 19V | 6.3 k Ω | 8.5 k Ω |

Package Outline Dimensions



| DIM | Inches | | Millimeters | | DIM | Inches | | Millimeters | |
|-----|--------|-------|-------------|------|-----|-----------|-------|-------------|------|
| | Min. | Max. | Min. | Max. | | Min. | Max. | Min. | Max. |
| A | 0.053 | 0.069 | 1.35 | 1.75 | e | 0.050 BSC | | 1.27 BSC | |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 | b | 0.013 | 0.020 | 0.33 | 0.51 |
| D | 0.189 | 0.197 | 4.80 | 5.00 | c | 0.008 | 0.010 | 0.19 | 0.25 |
| H | 0.228 | 0.244 | 5.80 | 6.20 | θ | 0° | 8° | 0° | 8° |
| E | 0.150 | 0.157 | 3.80 | 4.00 | h | 0.010 | 0.020 | 0.25 | 0.50 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | - | - | - | - | - |

Suggested Pad Layout



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