

LTM2889

Isolated CAN μ Module Transceiver Plus Power

DESCRIPTION

Demonstration circuit 1903A is an isolated CAN μ Module[®] transceiver plus power featuring the LTM[®]2889. The demo circuit features an EMI optimized circuit configuration and printed circuit board layout. All components are integrated into the μ Module isolator. The demo circuit operates from a single supply on V_{CC} . The part generates an isolated

output voltage on V_{CC2} and communicates all necessary signaling across the isolation barrier through LTC's isolator μ Module technology.

Design files for this circuit board are available at <http://www.linear.com/demo/DC1903A>

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PERFORMANCE SUMMARY

Specifications are at $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Input Supply Range	LTM2889-3	3.0	3.3	3.6	V
		LTM2889-5	4.5	5.0	5.5	V
V_{CC2}	Regulated Output Voltage	$I_{LOAD} = 100\text{mA}$, LTM2889-3 $I_{LOAD} = 150\text{mA}$, LTM2889-5	4.75	5	5.25	V
f_{MAX}	Maximum Data Rate				4	Mbps
V_{IORM}	Maximum Working Insulation Voltage	GND to GND2	560			V_{DC}
			400			V_{RMS}
	Common Mode Transient Immunity		30			kV/ μ s

OPERATING PRINCIPLES

The LTM2889 contains an isolated DC/DC converter that delivers power to V_{CC2} at 5V from the input supply V_{CC} . Isolation is maintained by the separation of GND and GND2 where significant operating voltages and transients can exist without affecting the operation of the LTM2889. The logic side ON pin enables or shuts down the LTM2889. All logic side signals are referenced to the logic supply pin V_L , connected to the input supply voltage V_{CC} . The LTM2889 is available with two input voltage ranges, 3V to 3.6V (LTM2889-3) or 4.5V to 5.5V (LTM2889-5). The isolated side and CAN interface is capable of operating at 3.3V. The V_{CC2} voltage is jumper selectable for either 5V or 3.3V operation.

CAN signaling is controlled by the logic input TXD and the silent pin S. \overline{RE} controls the RXD output. Connection to the transceiver pins (CANL and CANH) allows for half-duplex communication on the isolated side of the demo circuit. Termination resistors are included on the demo circuit, with support for split termination to reduce common mode perturbations.

Data on the TXD input is transmitted differentially on CANH-CANL when the silent pin (S) is low. Differential data received on CANH-CANL is delivered at the RXD output when \overline{RE} is low. The CAN driver features adjustable slew rate via RV1 connected to the RS pin. A jumper easily allows selection between a fixed fast slew rate and adjustable rate.

OPERATING PRINCIPLES

Demo circuit 1903A is available in two configurations, supporting both versions of the LTM2889. Table 1 details the demo circuit configurations.

Table 1

DEMO CIRCUIT	INPUT VOLTAGE	DEVICE
DC1903A-A	3V to 3.6V	LTM2889-3
DC1903A-B	4.5V to 5.5V	LTM2889-5

The demo circuit has been designed and optimized for low RF emissions. Some features of the LTM2889 are not available for evaluation on the demo circuit. The logic supply voltage V_L is tied to V_{CC} , and the ON and RE pins are not available on the input pin header, but may be controlled by jumpers JP1 and JP3 respectively. EMI mitigation techniques used include the following:

1. Four layer PCB, allowing for isolated side to logic side bridge capacitor. The bridge capacitor is formed between an inner layer of floating copper which overlaps the logic side and isolated side ground planes. This structure creates two series capacitors, each with approximately 0.008" of insulation, supporting the full dielectric withstand rating of 2500V_{RMS}. The bridge capacitor provides a low impedance return path for injected currents due to parasitic capacitances of the LTM2889's signal and power isolating elements.
2. Discrete bridge capacitors (C3, C4) mounted between GND2 and GND. The discrete capacitors provide additional attenuation at frequencies below 400MHz. Capacitors are safety rated type Y2, manufactured by Murata, part number GA342QR7GF471KW01L, rated for 250V_{RMS}.

3. Board/ground plane size has been minimized. This reduces the dipole antenna formed between the logic side and isolated side ground planes.
4. Top signal routing and ground floods have been optimized to reduce signal loops, minimizing differential mode radiation.
5. Common mode filtering is integrated into the input and output pin headers. Filtering helps to reduce emissions caused by conducted noise and minimizes the effects of cabling to common mode emissions.
6. A combination of low ESL and high ESR decoupling is used. A low ESL ceramic capacitor is located close to the module minimizing high frequency noise conduction. A high ESR tantalum capacitor is included to minimize board resonances and prevent voltage spikes due to hot plugging of the supply voltage.

EMI performance is shown in Figure 1, measured using a GHz transverse electromagnetic (GTEM) cell and method detailed in IEC 61000-4-20, testing and measurement techniques – emission and immunity testing in transverse electromagnetic waveguides.

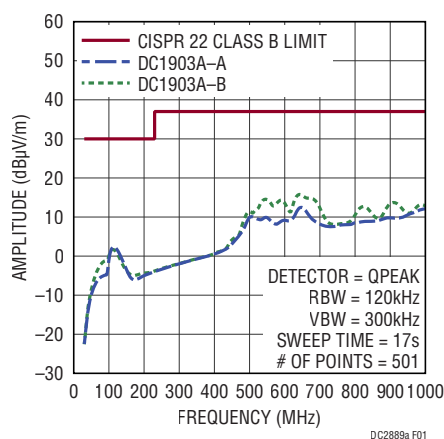


Figure 1. DC1903A Radiated Emissions

NOTE: When measuring the input or output voltage ripple or high speed signals, care must be taken to avoid a long ground lead on the oscilloscope probe.

1. Place jumpers in their default positions:

JP1 ON in the ON position

JP2 Silent in the OFF position

JP3 $\overline{\text{RE}}$ in the ON position

JP4 V_{CC2} in the 5V position

JP5 Slew in the FAST position

JP6 Split in the ON position

JP7 Termination in the ON position

2. With power off, connect the input power supply to V_{CC} and GND on pin header J1.

3. Turn on the power supply.

NOTE: Make sure that the input voltage does not exceed 6V.

4. Check for the proper output voltage. $V_{CC2} = 5V$ between test points V2 and G2.

5. Once the proper output voltages are established, connect a function generator to terminal TXD and set to square wave with a low of 0V, high = V_{CC} , termination is Hi-Z. Set frequency to 500kHz (1Mbps). Enable output of function generator.

6. Connect oscilloscope to terminal RXD and observe waveform at 500kHz. This demonstration shows data that is transmitted from TXD, loops back through CANH and CANL, and out of RXD.

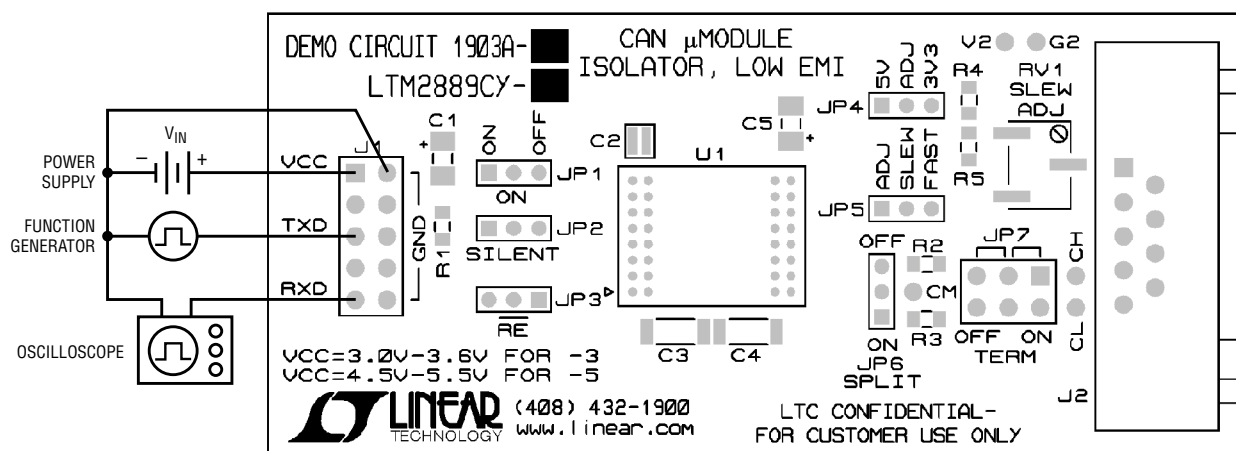
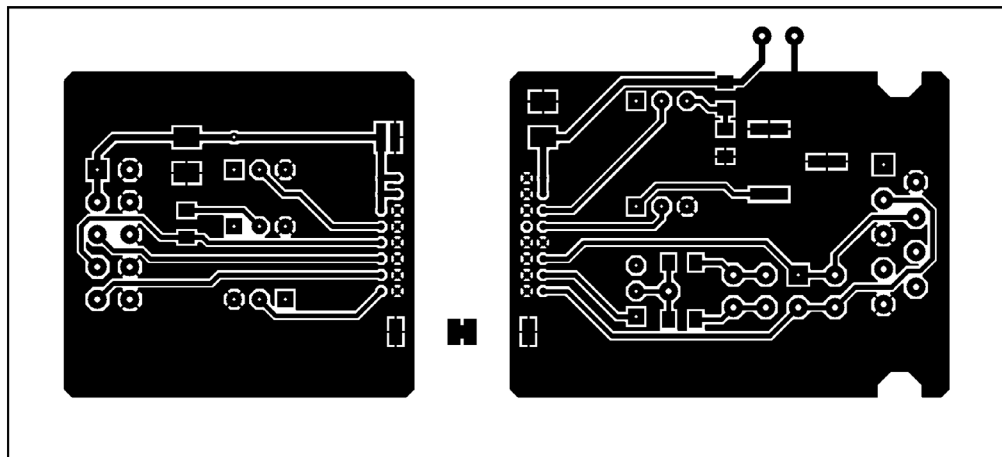
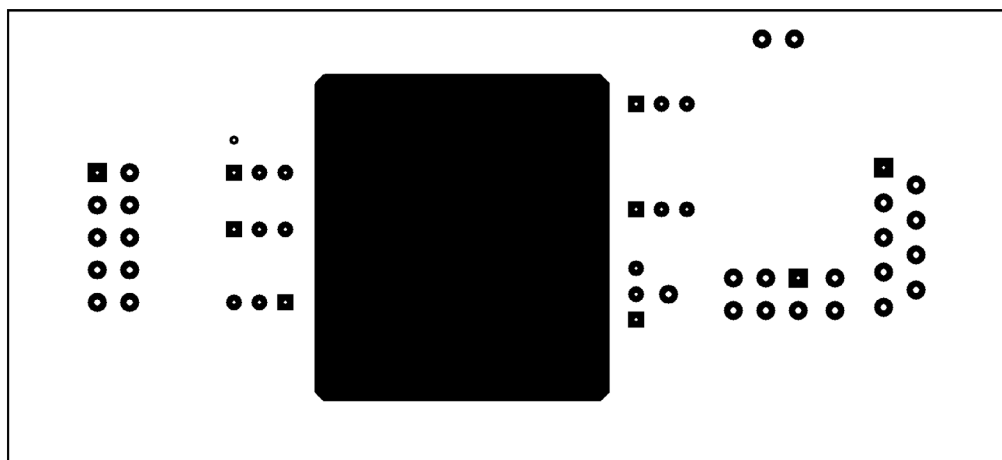


Figure 2. Demo Board Setup

PCB LAYOUT

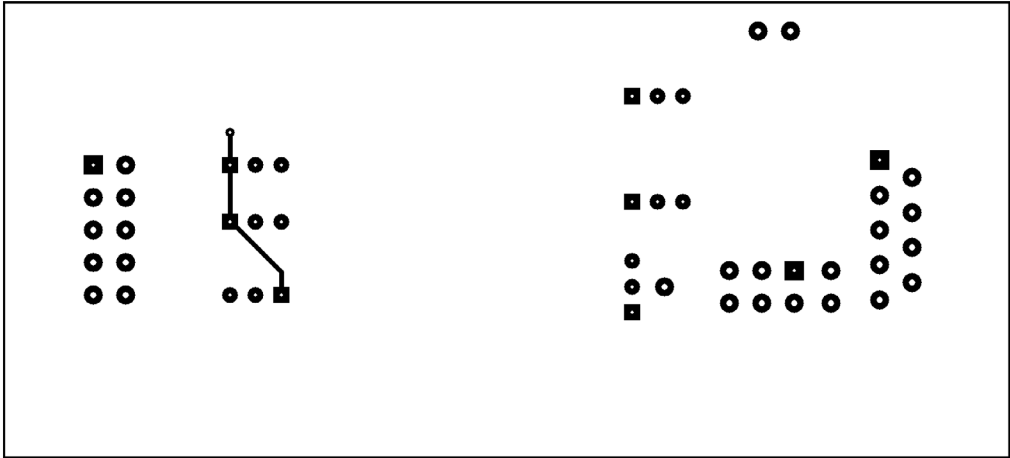


Layer 1. Top Layer

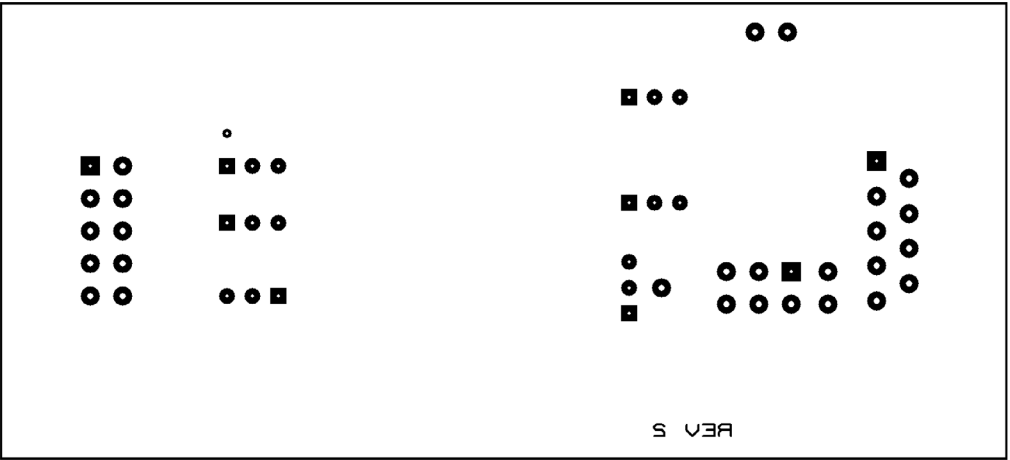


Layer 2. Ground Plane

PCB LAYOUT



Layer 3. Signal Layer



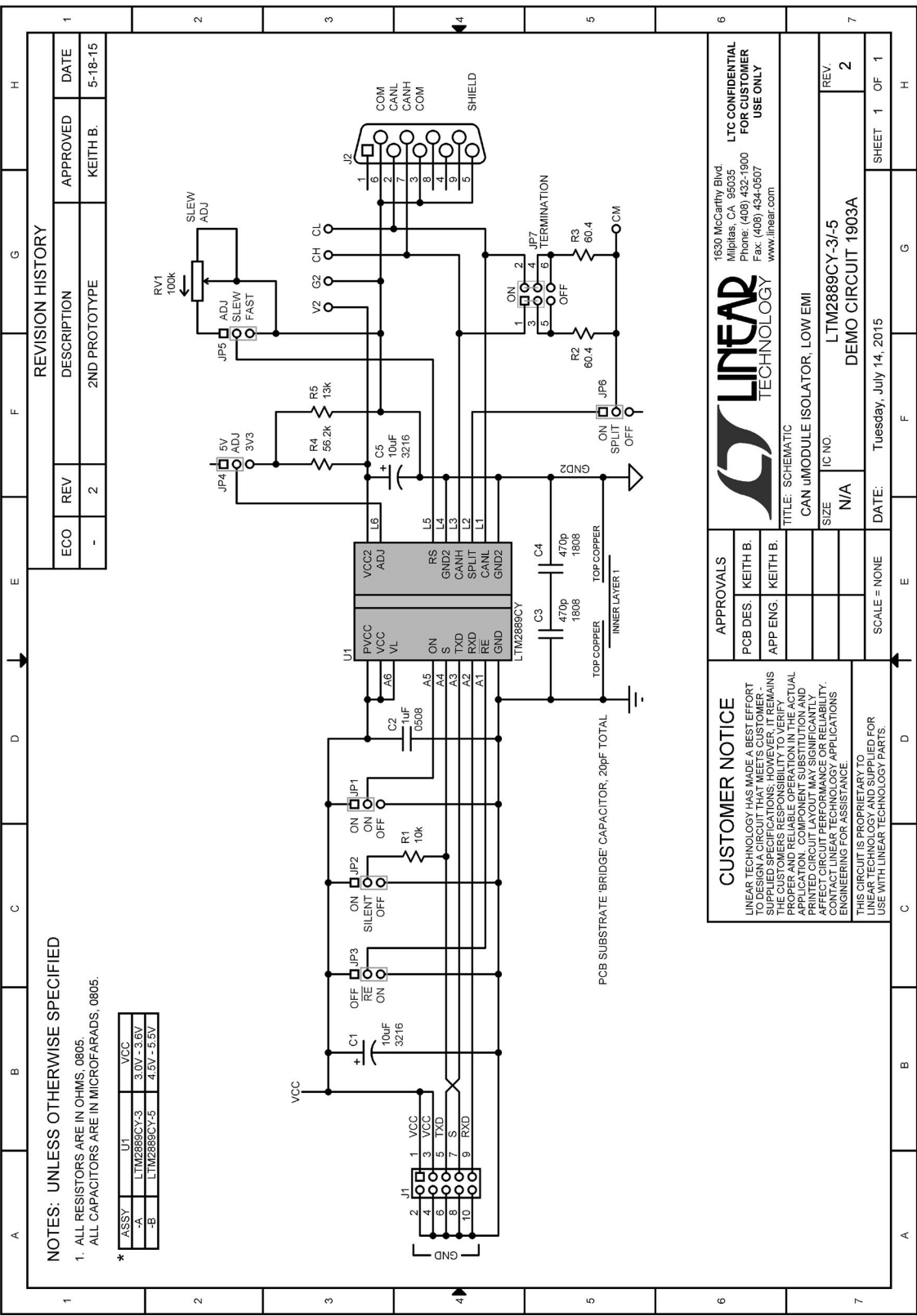
Layer 4. Bottom Layer

DEMO MANUAL DC1903A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	U1	-A IC, LTM2889CY-3 -B IC, LTM2889CY-5	LINEAR LTM2889CY-3#PBF LINEAR LTM2889CY-5#PBF
Hardware: For Demo Board Only				
1	1	C1, C5	CAP, TANT 10 μ F 10V 20% TAJA	AVX TAJA106M010RNJ
2	1	C2	CAP, CER 1 μ F 10V 20% 0508	MURATA LLL219R71A105MA01L
3	2	C3, C4	CAP, CER 470pF 250VAC 10% 1808	MURATA GA342QR7GF471KW01L
4	1	J1	0.1" DOUBLE ROW HEADER, 5 \times 2 PIN	SAMTEC TSW-105-22-G-D
5	1	J1	0.1" FERRITE PLATE, 5 \times 2 HOLE	FAIR RITE 2644247101
6	1	J2	CON, DSUB 9 PIN FEMALE	SINGATRON DR-E9SB-NJ000-S0007
7	6	JP1, JP2, JP3, JP4, JP5, JP6	HEADER, 2mm, 1 \times 3 PIN	WURTH 62000311121
8	1	JP7	HEADER, 0.1", 2 \times 3 PIN	WURTH 61300621121
9	6	JP1, JP2, JP3, JP4, JP5, JP6	SHUNT, 2mm	WURTH 60800213421
10	1	JP7	SHUNT, 0.1", 2 \times 2	WURTH 60910213421
11	1	R1	RESISTOR, 10k Ω 1% 0805 1/10W	VISHAY CRCW080510K0FKEA
12	2	R2, R3	RESISTOR, 60.4 Ω 1% 0805 1/10W	VISHAY CRCW080560R4FKEA
13	1	R4	RESISTOR, 56.2k Ω 1% 0805 1/10W	VISHAY CRCW080556K2FKEA
14	1	R5	RESISTOR, 13k Ω 1% 0805 1/10W	VISHAY CRCW080513K0FKEA
15	1	RV1	POTENTIOMETER, 100k Ω , SMT	VISHAY TS63Y104KR10

SCHEMATIC DIAGRAM



DEMO MANUAL DC1903A

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dc1903af



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