8-Channel, PDM to I²S/TDM Converter

Data Sheet

ADAU7118

FEATURES

8 channels of PDM audio inputs from digital microphones
16×, 32×, or 64× decimation ratio of PDM to PCM audio data
24-bit resolution to support high sound pressure level (SPL) microphones
126 dB A-weighted SNR
4 kHz to 192 kHz output sampling rate
Bit clock rates of 64×, 128×, 192×, 256×, 384×, or 512× the output sampling rate
Dual output PDM clocks
Automatic PDM clock generation
Automatic power-down when BCLK removed
Selectable I²C control or hardware mode operation
1.2 mA DVDD operating current for 8 channels at 48 kHz frequency sampling rate and 1.8 V supply
Slave I²S or TDM output interface
Up to TDM-16 supported
Configurable TDM slot routing and sizes
I/O supply voltage from 1.70 V to 3.63 V
DVDD supply voltage from 1.10 V to 1.98 V
<5 µA typical DVDD shutdown current
16-lead, 3 mm × 3 mm, 0.50 mm pitch LFCSP
Power-on reset

APPLICATIONS

Microphone arrays
Mobile computing
Portable electronics
Consumer electronics
Professional electronics

FUNCTIONAL BLOCK DIAGRAM

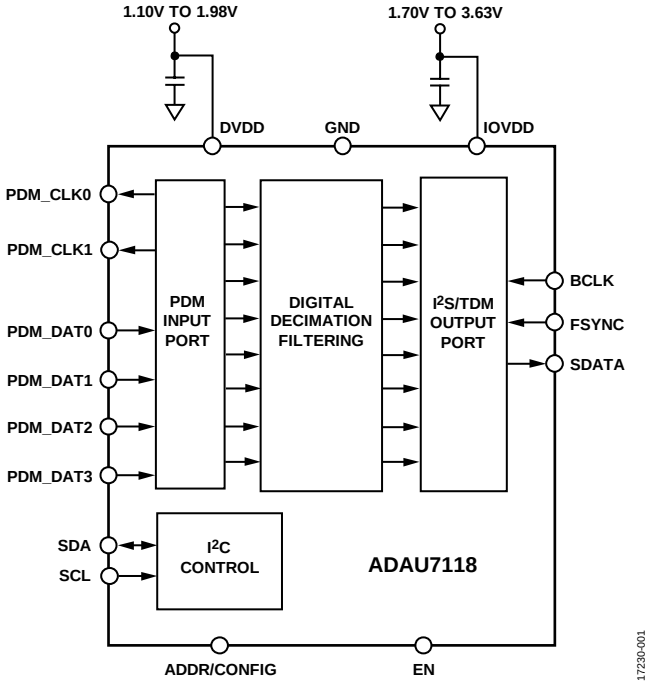

Figure 1.

GENERAL DESCRIPTION

The ADAU7118 converts four stereo pulse density modulation (PDM) bitstreams into one pulse code modulation (PCM) output stream. The source for the PDM data can be eight microphones or other PDM sources. The PCM audio data is output on a serial audio interface port in either inter-IC serial (I²S) or time domain multiplexed (TDM) format.

The ADAU7118 is specified over the commercial temperature range (−40°C to +85°C). The ADAU7118 is available in a 16-lead, 3 mm × 3 mm, 0.40 mm pitch, lead frame chip scale package (LFCSP).

Note that throughout this data sheet, multifunction pins, such as ADDR/CONFIG, are referred to either by the entire pin name or by a single function of the pin, for example, ADDR, when only that function is relevant.

Rev. A Document Feedback

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REVISION HISTORY

8/2019—Rev. 0 to Rev. A

Change to Features Section ... 1
Changes to Ordering Guide ... 34

5/2019—Revision 0: Initial Version

SPECIFICATIONS

DVDD = 1.10 V to 1.98 V, IOVDD = 1.70 V to 3.63 V, T_A = 25°C, and pins set to low drive setting, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUT					
Input Voltage					
High Level (V_{IH})	0.7 × IOVDD			V	
Low Level (V_{IL})			0.3 × IOVDD	V	
Input Leakage					
High Level (I_{IH})			2.5	µA	Digital input pins with pull-down resistor
Low Level (I_{IL}) at 0 V			1	µA	Digital input pins with pull-down resistor
Input Capacitance (C_I)		2		pF	Guaranteed by design
DIGITAL OUTPUT					
Output Voltage					
High Level (V_{OH})	0.85 × IOVDD			V	Source current when output is high (I_{OH}) = 1 mA
Low Level (V_{OL})			0.1 × IOVDD	V	Source current when output is low (I_{OL}) = 1 mA
Digital Output Pins, Output Drive					Digital output pins drive low impedance PCB traces to a high impedance digital input buffer
IOVDD = 1.8 V Nominal					
Drive Strength Setting					
2.5 mA	0.7			mA	
5 mA	1.4			mA	
10 mA	2.8			mA	
15 mA	4.2			mA	
IOVDD = 3.3 V Nominal					
Drive Strength Setting					
2.5 mA	2.5			mA	
5 mA	5			mA	
10 mA	10			mA	
15 mA	15			mA	
PERFORMANCE					
Dynamic Range		126		dB	20 Hz to 20 kHz, −60 dB input, A-weighted filter (rms), relative to 0 dBFS output
Signal-to-Noise-Ratio (SNR)		126		dB	A-weighted filter, fifth-order input, relative to 0 dBFS output
Decimation Ratio	16×	64×	64×		
Frequency Response	−0.1		+0.01	dB	DC to 0.45 × output sampling rate (f_S)
Stop Band		0.566 × f_S		Hz	
Stop Band Attenuation	75			dB	
Group Delay	4.47	4.47	4.47	FSYNC cycles	0.02 f_S input signal, 64× decimation
	5.02	5.02	5.02	FSYNC cycles	0.02 f_S input signal, 32× decimation
	5.83	5.83	5.83	FSYNC cycles	0.02 f_S input signal, 16× decimation

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Gain	0	0	0	dB	PDM to PCM
Start-Up Time	63	64	64	FSYNC cycles	After power-up reset and initialization code runs
Bit Resolution		24		Bits	Internal and output
Interchannel Phase	0	0	0	Degrees	
High-Pass Filter −3 dB Point	0.23328	0.9312	242.4	Hz	f_S = 48 kHz, cutoff frequency set using the HPF_FC bits located in the HPF_CONTROL register, typical value is default setting
CLOCKING					
Output Sampling Rate (f_S)	4	48	192	kHz	FSYNC pulse rate
Bit Clock Frequency (f_{BCLK})	0.256	12.288	24.576	MHz	
PDM_CLKx Frequency (f_{PDM_CLK})	0.256	3.072	6.144	MHz	
POWER					
Supply Voltage					
Digital Voltage (DVDD Pin)	1.10		1.98	V	Supply for digital circuitry
I/O Supply Voltage (IOVDD Pin)	1.70		3.63	V	Supply for input/output (I/O) circuitry, including pads and level shifters
Supply Current					
I/O Current (IOVDD Pin)					Dependent on the clock rates and characteristics of external loads
Operation State		2		mA	IOVDD = 3.3 V, 48 kHz f_S, TDM-8 format, all channels driven, default drive strength, 25 pF capacitance, only one PDM_CLKx pin used
		0.86		mA	IOVDD = 1.8 V, 48 kHz f_S, TDM-8 format, all channels driven, default drive strength, 25 pF capacitance, only one PDM_CLKx pin used
Shutdown Current		16		µA	Power applied, frame and bit clocks applied, and then device placed into power-down state using the procedure in Table 10
		3		µA	Power applied, frame and bit clocks applied, and then device placed into power-down state using the procedure in Table 9
Digital Current (DVDD Pin)					
Operation State		1.4		mA	Over all temperatures, full voltage range and silicon skews, 8 channels, 48 kHz f_S
		1.2		mA	DVDD = 1.8 V, 8 channels, 48 kHz f_S
		0.8		mA	DVDD = 1.2 V, 8 channels, 48 kHz f_S
		0.7		mA	DVDD = 1.8 V, 4 channels, 48 kHz f_S
		0.4		mA	DVDD = 1.2 V, 4 channels, 48 kHz f_S
		0.4		mA	DVDD = 1.8 V, 8 channels, 16 kHz f_S
		0.27		mA	DVDD = 1.2 V, 8 channels, 16 kHz f_S
		0.22		mA	DVDD = 1.8 V, 4 channels, 16 kHz f_S
		0.14		mA	DVDD = 1.2 V, 4 channels, 16 kHz f_S
Shutdown Current		4		µA	Power-down mode using either method in Table 9 or method in Table 10

Serial Ports

T_A = −40°C to +85°C, DVDD = 1.10 V to 1.98 V, and IOVDD = 1.70 V to 3.63 V, unless otherwise noted.

Table 2.

Parameter	Min	Max	Unit	Description
SERIAL PORT				
f_{FSYNC}		192	kHz	FSYNC frequency, $1/t_{FSYNC}$
t_{FSYNC}	5.21		µs	FSYNC period
f_{BCLK}		24.576	MHz	BCLK frequency, sample rate ranging from 4 kHz to 192 kHz, $1/t_{BCLK}$
t_{BCLK}	40.7		ns	BCLK period
t_{BIL}	18		ns	BCLK low pulse width, slave mode, BCLK frequency = 24.576 MHz, BCLK period = 40.6 ns
t_{BIH}	18		ns	BCLK high pulse width, slave mode, BCLK frequency = 24.576 MHz, BCLK period = 40.6 ns
t_{LIS}	10		ns	FSYNC setup to BCLK input rising edge, slave mode, FSYNC frequency = 192 kHz
t_{LIH}	10		ns	FSYNC hold from BCLK input rising edge, slave mode, FSYNC frequency = 192 kHz
t_{SOD}		20.63	ns	SDATA delay from BCLK output falling edge, 25 pf load over entire range of IOVDD, all temperatures and skews, default drive strength of 10 mA
		11.71	ns	IOVDD = 3.3 V ± 10%, drive strength set to 0b00, with 25 pf load
		10.37	ns	IOVDD = 3.3 V ± 10%, drive strength set to 0b01, with 25 pf load
		9.03	ns	IOVDD = 3.3 V ± 10%, drive strength set to 0b10, with 25 pf load
		8.72	ns	IOVDD = 3.3 V ± 10%, drive strength set to 0b11, with 25 pf load
		31.02	ns	IOVDD = 1.7 V to 1.89 V, drive strength set to 0b00, with 25 pf load
		25.83	ns	IOVDD = 1.7 V to 1.89 V, drive strength set to 0b01, with 25 pf load
		20.63	ns	IOVDD = 1.7 V to 1.89 V, drive strength set to 0b10, with 25 pf load
		20.33	ns	IOVDD = 1.7 V to 1.89 V, drive strength set to 0b11, with 25 pf load

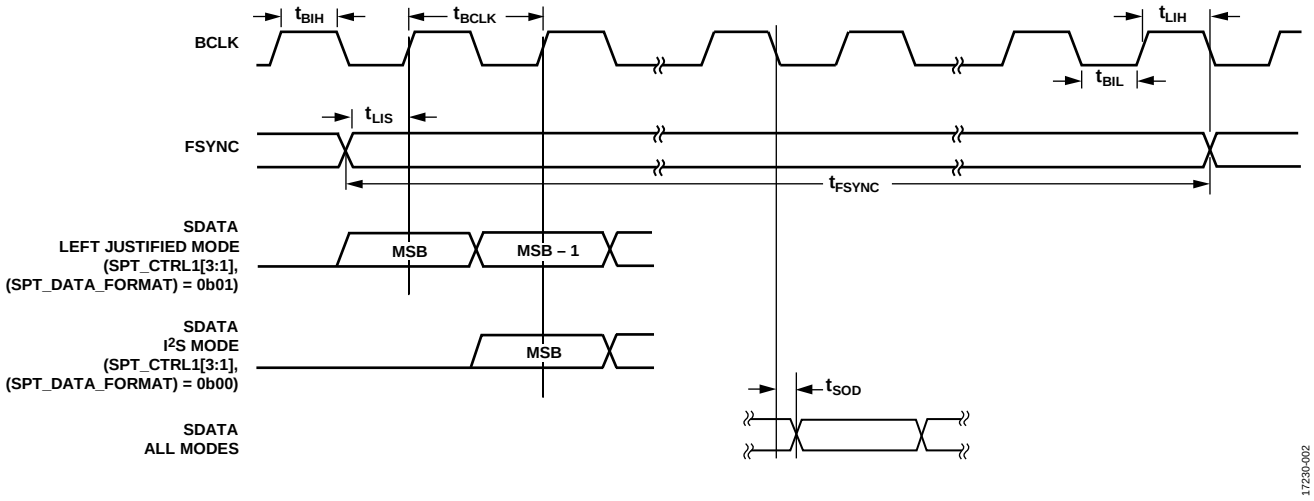


Figure 2. Serial Port Timing Specifications

I²C Interface—Slave

T_A = −40°C to +85°C, DVDD = 1.10 V to 1.98 V, and IOVDD = 1.70 V to 3.63 V, unless otherwise noted.

Table 3.

Parameter	Min	Max	Unit	Description
I²C SLAVE PORT				
f_{SCL}		1000	kHz	SCL clock frequency, not shown in Figure 3
t_{SCLH}	0.26		µs	SCL pulse width high
t_{SCLL}	0.5		µs	SCL pulse width low
t_{SCS}	0.26		µs	Start and repeated start condition setup time
t_{SCH}	0.26		µs	Start condition hold time
t_{DS}	50		ns	Data setup time
t_{DH}		0.45	µs	Data hold time
t_{SCLR}		120	ns	SCL rise time
t_{SCLF}		120	ns	SCL fall time
t_{SDR}		120	ns	SDA rise time
t_{SDF}		120	ns	SDA fall time
t_{BFT}	0.5		µs	Bus-free time between stop and start
t_{SUSTO}	0.26		µs	Stop condition setup time

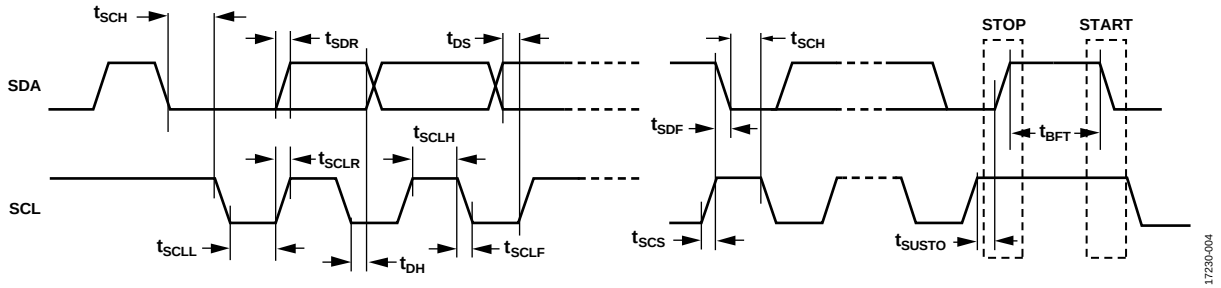


Figure 3. I²C Slave Port Timing Specifications

PDM Inputs

T_A = −40°C to +85°C, DVDD = 1.10 V to 1.98 V, IOVDD = 1.70 V to 3.63 V, and PDM data is latched on both edges of the clock (see Figure 4), unless otherwise noted.

Table 4.

Parameter	t_{MIN}	t_{MAX}	Unit	Description
Timing Requirements				
t_{SETUP}	9		ns	Data setup time
t_{HOLD}	3		ns	Data hold time

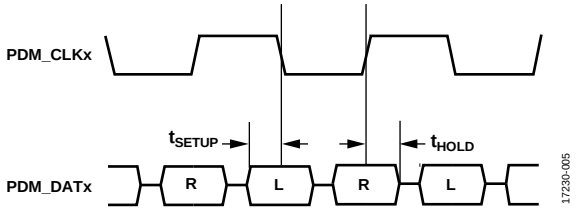


Figure 4. PDM Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
DVDD to Ground	1.98 V
IOVDD to Ground	3.63 V
Digital Inputs	GND − 0.3 V to IOVDD + 0.3 V
Maximum Operating Ambient Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Storage Temperature Range	−65°C to +150°C
Soldering (60 sec)	300°C
Electrostatic Discharge (ESD) Susceptibility	4.5 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 6. Thermal Resistance

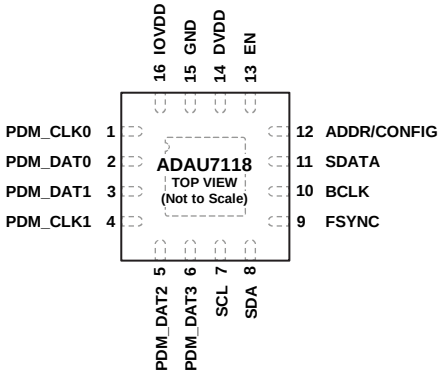
Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-16-22	57	15	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 1S0P thermal test board. See JEDEC JESD-51.
[2] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD-51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
EXPOSED PAD. THE EXPOSED PAD MUST BE GROUNDED BY SOLDERING IT TO A GROUNDED COPPER PAD OF EQUIVALENT SIZE ON THE PCB. THERMAL VIAS ARE NOT NECESSARY.

17230-006

Figure 5. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PDM_CLK0	PDM Output Clock 0.
2	PDM_DAT0	PDM Input Data 0.
3	PDM_DAT1	PDM Input Data 1.
4	PDM_CLK1	PDM Output Clock 1.
5	PDM_DAT2	PDM Input Data 2.
6	PDM_DAT3	PDM Input Data 3.
7	SCL	I^2C Serial Clock Input.
8	SDA	I^2C Data.
9	FSYNC	I^2S/TDM Frame Sync or Left/Right Clock.
10	BCLK	I^2S/TDM Bit Clock.
11	SDATA	I^2S/TDM Serial Data Output.
12	ADDR/CONFIG	I^2C Address or Standalone Configuration Selection.
13	EN	Chip Enable.
		Ground this pin to disable the device and put it in low power mode.
		Apply IOVDD to this pin to enable normal operation. All register settings are preserved when the device is disabled. However, the bit clock counters, and the audio data resets, which is the same as performing a soft reset.
14	DVDD	Internal Core Digital Power Supply.
15	GND	Ground.
16	IOVDD	Digital Input/Output Power Supply.
EP	EPAD	Exposed Pad. The exposed pad must be grounded by soldering it to a grounded copper pad of equivalent size on the PCB. Thermal vias are not necessary.

TYPICAL PERFORMANCE CHARACTERISTICS

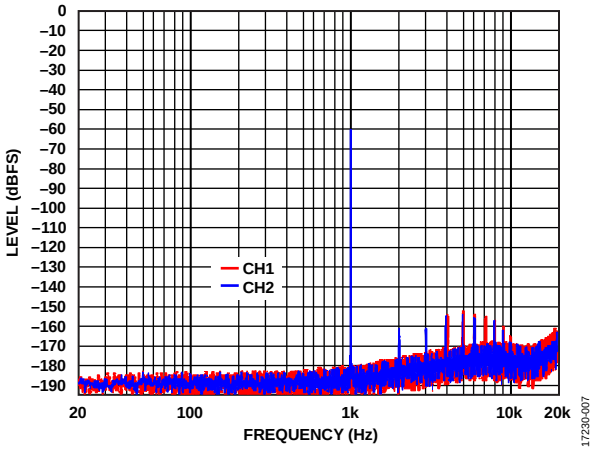


Figure 6. FFT, f_S = 48 kHz, −60 dBFS Input, 64× Decimation, Fifth Order

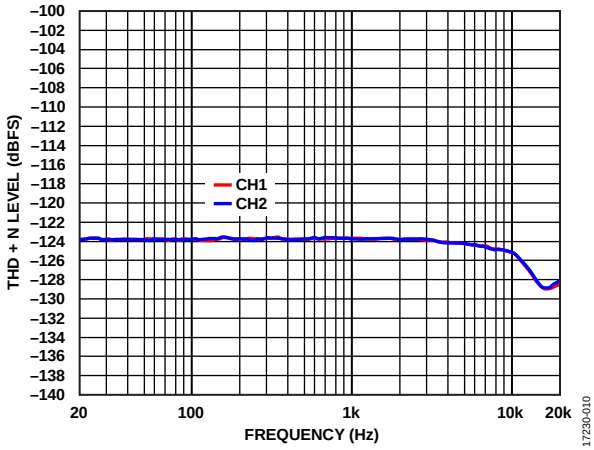


Figure 9. Total Harmonic Distortion + Noise (THD + N) vs. Frequency at −10 dBFS Unweighted, f_S = 48 kHz, 64× Decimation, Fifth Order

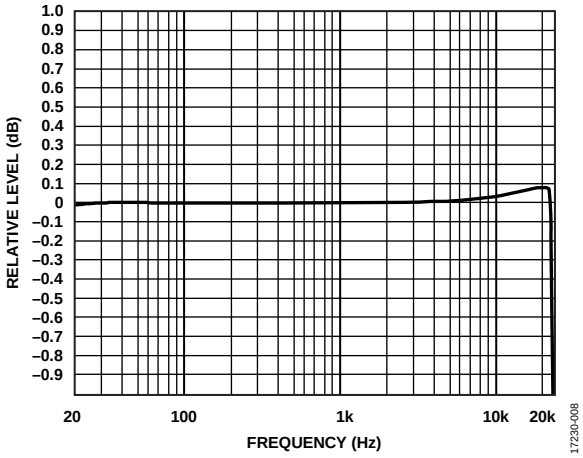


Figure 7. Relative Level vs. Frequency at −10 dBFS Normalized, 64× Decimation, f_S = 48 kHz

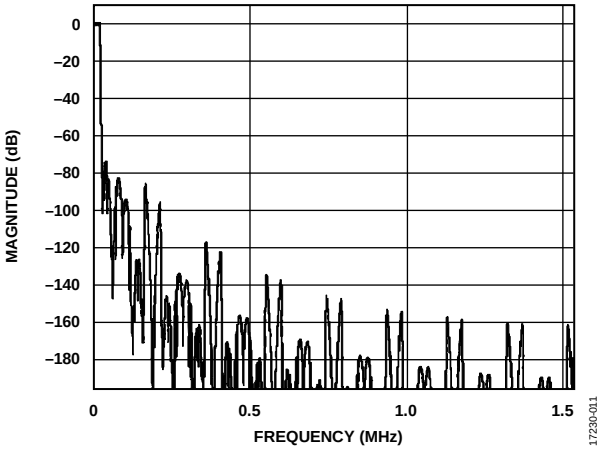


Figure 10. Magnitude vs. Frequency, 48 kHz Output, 64× Decimation

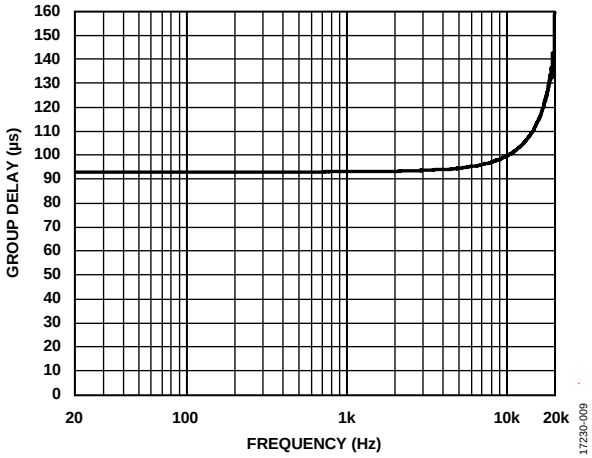


Figure 8. Group Delay vs. Frequency, f_S = 48 kHz, 64× Decimation

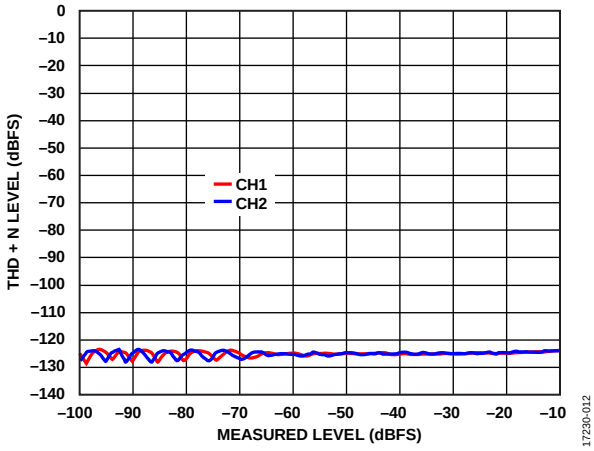


Figure 11. THD + N Level vs. Measured Level, 1 kHz, Unweighted, 64× Decimation, Fifth Order, f_S = 48 kHz

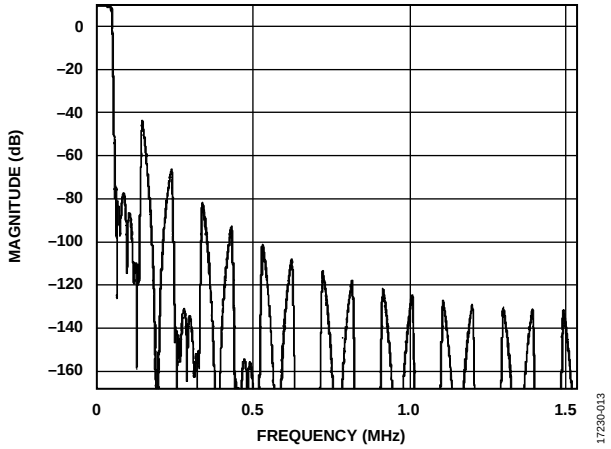


Figure 12. Magnitude vs. Frequency, 48 kHz Output, 32× Decimation

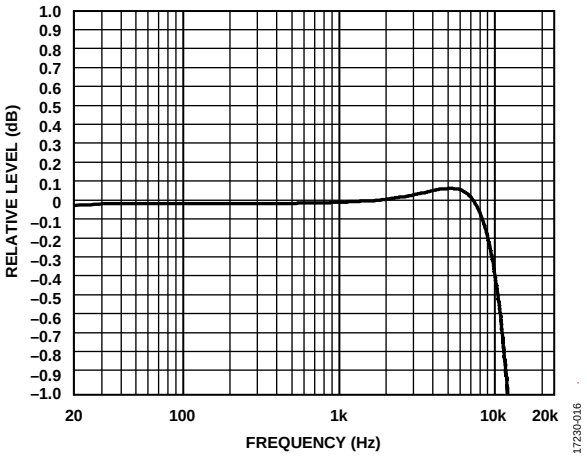


Figure 15. Relative Level vs. Frequency at −10 dBFS Normalized, 16× Decimation, f_S = 48 kHz

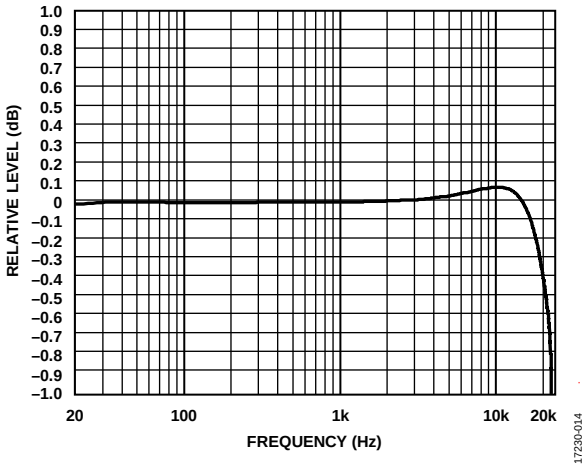


Figure 13. Relative Level vs. Frequency at −10 dBFS Normalized, 32× Decimation, f_S = 48 kHz

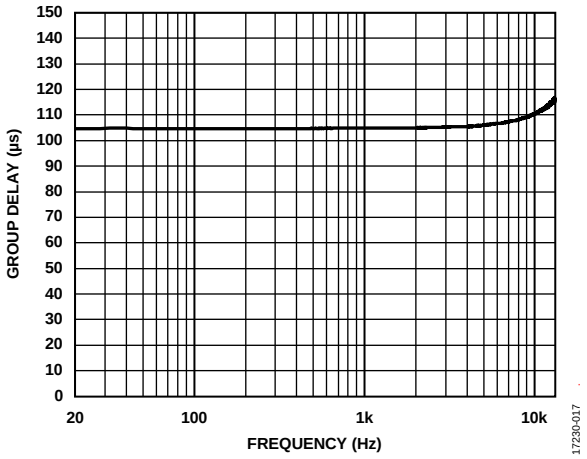


Figure 16. Group Delay vs. Frequency, f_S = 48 kHz, 32× Decimation

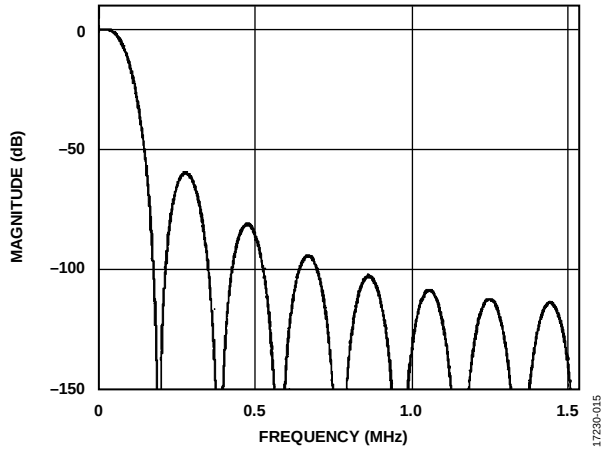


Figure 14. Magnitude vs. Frequency, 48 kHz Output, 16× Decimation

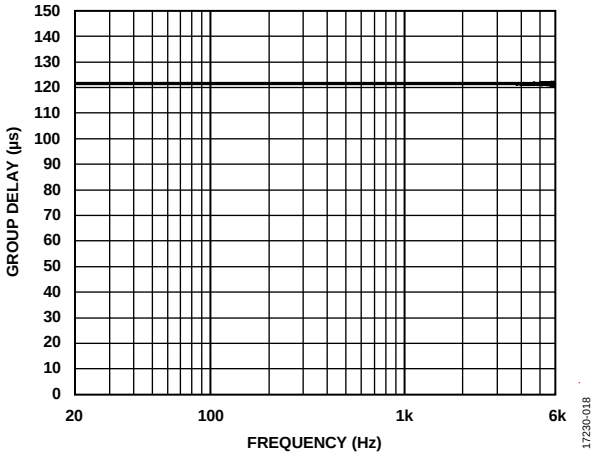


Figure 17. Group Delay vs. Frequency, f_S = 48 kHz, 16× Decimation

THEORY OF OPERATION

The ADAU7118 provides up to 8 channels of decimation from a 1-bit PDM source to a 24-bit PCM audio. The downsampling ratio is typically 64 × f_S, with f_S being the PCM output sampling rate, but the downsampling ratio can also be set at 32 × f_S or 16 × f_S to facilitate higher output sampling rates. All channels decimate at the same ratio. The 24-bit downsampled PCM audio is output via standard I²S or TDM format.

The input sources for the ADAU7118 can be any device that has a slave PDM output, such as a digital microphone. The output pins of these microphones can connect directly to the input pins of the ADAU7118. There are two separate PDM_CLKx outputs that are replications of the same signal to allow easier drive of multiple sources. Each PDM_CLKx can be disabled individually.

The PDM_DATx input pins are connected to the data output of the PDM sources. Internally, there are 8 channels, Channel 0 through Channel 7. The mapping of PDM_DATx inputs to the internal channels is detailed in Table 8.

Table 8. PDM_DATx to Internal Channel Mapping

Input Pin	PDM_CLK Edge	Internal Channel
PDM_DAT0	Falling	0
PDM_DAT0	Rising	1
PDM_DAT1	Falling	2
PDM_DAT1	Rising	3
PDM_DAT2	Falling	4
PDM_DAT2	Rising	5
PDM_DAT3	Falling	6
PDM_DAT3	Rising	7

Each internal channel pair associated with each PDM_DATx pin can be disabled to save power if those channels are not used.

Each PDM data pin must be assigned to either the PDM_CLK0 or PDM_CLK1 clock sources, using the decimation ratio and PDM clock mapping controls register (DEC_RATIO_CLK_MAP), to ensure compliance with timing specifications. The PDM_CLKx assignment must be the actual PDM clock that is driving the PDM microphone. By default, PDM_DAT0 and PDM_DAT1 are mapped to PDM_CLK0, and PDM_DAT2 and PDM_DAT3 are mapped to PDM_CLK1. This mapping of the two clock sources to the four data input pins can be modified by the PDM_DATx_CLK_MAP bits.

POWER-UP AND INITIALIZATION

The ADAU7118 requires two power supplies to function: the IOVDD and the DVDD. Both power supplies can be applied at the same time. If the power supplies are applied at different times, the IOVDD must be applied first and then the DVDD at any point after. There are no timing restrictions.

After the power supplies have stabilized, the device initializes and is ready to accept incoming I²S clocks or I²C commands based on the mode of operation.

After the initialization is complete, and I²S clocks are applied, it takes 16 full frame sync cycles to begin sending out PDM clocks. When the PDM clocks start, and after another 48 frame sync cycles, the PDM data shows up on the SDATA pin. These 64 frame sync cycles are listed in Table 1.

The ADAU7118 can operate in two modes of operation: standalone hardware and I²C. See the Standalone Hardware Mode section or the I²C Control Interface section for more details.

CLOCKING

After power is applied and the power-up initialization is complete, the device is ready to accept I²S clocks. At that point, it takes 16 full frame sync cycles for the device to fully initialize and start sending PDM clocks. If during normal operation the bit clock or frame sync is removed, the ADAU7118 PDM_CLKx outputs stop immediately, and the ADAU7118 goes into a lower power state automatically. See the Power-Down State section for more details. When the clocks resume, the ADAU7118 relocks to the bit clock and the frame sync signals and adjusts the PDM_CLKx outputs accordingly. The length of time before the PDM clock outputs resume is 4 frames ± 1 frame to lock to the incoming signal. If the format of the clock signals change, the ADAU7118 detects this change at the end of the frame and stops the PDM clock outputs. Then, the device reconfigures and resumes sending PDM clocks with no user intervention. Again, the length of time before the PDM clock outputs resume usually takes 4 frames ±1 frame to lock to the incoming signal.

The ADAU7118 requires a BCLK rate that is a minimum of 64× the frame sync (FSYNC) sample rate. BCLK rates of 128×, 192×, 256×, 384×, and 512× the FSYNC rate are also supported. The ADAU7118 automatically detects the ratio between BCLK and FSYNC and generates a PDM clock output at 64 × the FSYNC rate by default. If lower decimation ratios are selected in Register 0x05, DEC_RATIO_CLK_MAP, the PDM output clock rate corresponds with the DEC_RATIO bits setting. The minimum sampling rate is 4 kHz, and the maximum sampling rate is 192 kHz. The PDM clock range is 256 kHz to 6.144 MHz. Internally, all processing is done at the PDM_CLK rate.

The two PDM clock outputs, PDM_CLK0 and PDM_CLK1, are separate buffered outputs of the same clock. However, the incoming PDM data is clocked in using the signal present at the actual clock pin and not the internal clock going out to the pin. The reason for this is to allow the clock rise time to be slowed by the external capacitance in a similar manner to the PDM data signal. It is recommended to associate the incoming PDM data with the clock output that is actually connected to the PDM microphone. The DEC_RATIO_CLK_MAP register, Register 0x05, is used to assign one of the two clocks to each PDM data input.

POWER-DOWN STATE

The ADAU7118 can be placed into a power-down state by using one of two methods available. The preferred method is by using register writes to place the device into the lowest possible power-down state. However, for when the ADAU7118 operates in standalone mode, use the second method, which uses the enable pin (EN).

With a system controller and when entering the low power state, disable the PDM clocks and disable the channel outputs by writing a zero to Register 0x04 (ENABLES register). Then, the frame and bit clocks can be removed (stopped) to place the device in the power-down state. Allow enough time for the I²C write to complete before stopping the clocks. A minimum of one full frame after the I²C write completes is enough wait time. It is not necessary to lower the EN pin, it does not lower the power draw any further. See Table 9 for more details.

Table 9. Placing the ADAU7118 into the Power-Down State Using Register Writes

Step	Action
1	Write a zero into Register 0x04
2	Wait at least one frame period
3	Stop the frame and bit clocks

When the ADAU7118 is in standalone mode, the device can be placed into the power-down state by applying a low signal to the EN pin and then waiting a minimum of one full frame to place the device into the power-down state. See Table 10 for more details. Note that if a pull-up resistor is used on the EN pin, the additional current through this pull-up resistor must be added to the values in Table 1.

Table 10. Placing the ADAU7118 into the Power-Down State when Operating in Standalone Mode

Step	Action
1	Apply a low voltage to the EN pin
2	Wait at least one frame period
3	Stop the frame and bit clocks

To come out of the power-down mode, the order for restarting the clocks vs. enabling the device does not matter. Enabling the device refers to either raising the EN pin or enabling the device by writing to Register 0x04.

STANDALONE HARDWARE MODE

Because all channels default to enable and output, the device can be used with the default control settings without I²C and with any setting of the ADDR/CONFIG pin, except for hardware mode. If the ADDR/CONFIG pin is left open, the device is in standalone hardware mode and I²C communications are not possible. See Table 14 for details on the ADDR/CONFIG pin settings. In standalone hardware mode, the settings of the I²C SCL pin and SDA pin can select different functionality by changing the state of some registers from their default. See Table 11 for details of the differences from the default settings.

To achieve the lowest power in standalone hardware mode operation when a BCLK is present, the EN pin is still functional and can be pulled low, placing the device into a low power mode. The EN pin also performs a soft reset but does not reset any of the register settings. Stopping the bit clock and frame sync clocks also places the device into a low power state. See the Clocking section for more details.

Table 11. Standalone Hardware Mode Settings: Changes From Default Settings

SCL Pin Tied to	SDA Pin Tied to	Operation Settings	PDM Clock Settings: ENABLES, Register 0x04	Channel Enables: ENABLES, Register 0x04	Drive Strength
IOVDD	IOVDD	4-channel	PDM_CLK1_EN bit = 0, disabled	CHAN_45_EN bit = 0, CHAN_67_EN bit = 0	Default setting = 10
IOVDD	GND	8-channel high drive	Default settings	All channels enabled	SDATA_DS = 11, PDM_CLK0_DS = 11, PDM_CLK1_EN = 11
GND	IOVDD	6-channel	Default settings	CHAN_67_EN = 0	Default setting = 10
GND	GND	6-channel high drive	Default settings	CHAN_67_EN = 0	SDATA_DS = 11, PDM_CLK0_DS = 11, PDM_CLK1_EN = 11

SERIAL AUDIO OUTPUT INTERFACE

The ADAU7118 supports I²S and TDM serial output formats. Up to 16 TDM slots can be used. TDM slot widths of 16 bits, 24 bits, and 32 bits are supported. Any internal channel can be routed to any output slot via the SPT_Cx_SLOT bits. By default, each channel is routed to its same number slot. For example, Channel 1 goes to Slot 1 and Channel 6 goes to Slot 6. Each channel can be set to drive during their set slot or not drive (tristate high impedance mode) via their respective SPT_Cx_DRV bit. I²S mode or TDM mode selection is via the SPT_SAI_MODE bit (Bit 0) in the SPT_CTRL1 register. The SDATA pin is in tristate high impedance mode, except when the port is driving serial data by default. It is possible for two or more channels to be set to the same TDM slot. In that case, the lowest channel number wins and drives its data into the slot. The data of the other channel never appears anywhere. There is no cross-checking of register settings to prevent the user from doing this, but the device is not damaged, only the data is missing from the output.

The SPT_CTRL1 register, SPT_SAI_MODE bit (Bit 0) sets the serial port audio interface mode. The two modes are stereo and TDM. The primary difference between these two modes is the format of the frame sync clock that is expected and the polarity of the active edge of the clock.

With the SPT_SAI_MODE bit set to 0, and the SPT_LRCLK_POL bit (Bit 1, Register SPT_CTRL2) set to 0, the serial port is in stereo mode with the clock polarity set to normal. In this mode, only two channels of data are expected to be sent. The frame starts with the falling edge of the frame sync, and the expected duty cycle is 50% high and 50% low. Channel 0 sends out its data when the clock is low, and as soon as the frame sync goes high, the data from Channel 0 is stopped, and Channel 1 begins sending. Both edges of the frame sync clock are used. If the duty cycle is not 50/50, there may be errors in the resulting data. In this mode of operation, the ADAU7118 does not expect 32-bit clock transitions for each channel. All bit clock to frame sync ratios are supported.

With the SPT_SAI_MODE bit set to 1, and the SPT_LRCLK_POL bit set to 0, the serial port is in TDM mode with the clock polarity set to normal. In this mode, there can be as few as a single channel transmitted or as many as 8 channels spread out across 16 data slots of a TDM-16 format.

The ADAU7118 can support six different bit clock rates of 64×, 128×, 192×, 256×, 384×, or 512× the output sampling rate. These bit clock rates are combined with the three different TDM slot sizes of 16-bit, 24-bit, or 32-bit slots, selected in the SPT_CTRL1 register, Bits[5:4] (SPT_SLOT_WIDTH), to result in 18 combinations of TDM formats that are supported. Note that some of these formats do not have an even number of full width slots (see Table 12).

Note that as soon as the next frame sync edge is detected, the ADAU7118 restarts from Slot 0, and any data in the previous frame that was never reached is lost. This process is how to achieve unusual TDM formats like TDM-5 or TDM-10. In addition, only TDM-16 or less is supported for placing data into a TDM slot. Data cannot be placed into slots above 16. The ADAU7118 can be configured to tristate all unused TDM slots, which includes all the slots above the first 16 slots for modes that have more than 16 slots.

In TDM mode, the frame sync is expected to be a positive going pulse that is at least one bit clock period wide. The falling edge is not important and is not looked at as long as it is low long enough to meet the timing specification read as a low before going back high. The frame starts with the rising edge of this pulse. The data is clocked out according to the slot width and data format specified in the SPT_CTRL1 register, Register 0x07. The ADAU7118 continues to send data until all active channels are sent and then the device waits for the next frame sync clock edge to start sending the next set of frame samples. If TDM-16 is used and the ADAU7118 is set to output Channel 0 to Channel 7 into Slot 0 to Slot 7, the ADAU7118 can tristate for the remainder of the frame, allowing another ADAU7118 to output its 8 channels on to Slot 8 to Slot 15. These slots do not have to be consecutive. The two devices may interleave their respective data if properly set up to do this. The serial port can be set up to only drive when there is data to drive into a data slot. If one or more of the eight channels is not used, the channel can be assigned to drive a slot or tristate during that data slot in the TDM data stream, which is done using Bit 0 in the SPT_Cx registers.

The SPT_LRCLK_POL bit, left/right clock polarity, can be set to 1 and the bit inverts the expected frame clock. In stereo mode with the SPT_LRCLK_POL bit set to 1, Channel 0 is sent out when the frame sync is high so the start of the frame is a low to high transition.

In TDM mode, with the SPT_LRCLK_POL bit set to 1, the expected frame sync pulse is negative going so that the frame starts with the high to low transition.

The SPT_DATA_FORMAT bits (Bits[3:1]) in the SPT_CTRL1 register allow for the justification of the data within the 32-bit data slot. The left justified mode, delayed by one bit clock period, and the right justified modes for 24-bit, 20-bit, and 16-bit data word sizes are all supported.

Table 12. Number of Slots in Supported TDM Bit Clock Rates vs. Slot Size Setting

	SPT_CTRL1, Bits[5:4]		
Bit Clock Rate	**0b01, 16-Bit Slot**	**0b10, 24-Bit Slot**	**0b00, 32-Bit Slot**
$64 \times f_S$	4	2[1]	2
$128 \times f_S$	8	5[1]	4
$192 \times f_S$	12	8	6
$256 \times f_S$	16	10[1]	8
$384 \times f_S$	24	16	12
$512 \times f_S$	32	21[1]	16

[1] This combination produces a partial final TDM slot that is not included in the number of slots. The data in that final slot is invalid. The number of slots shown in the table are the full width slots.

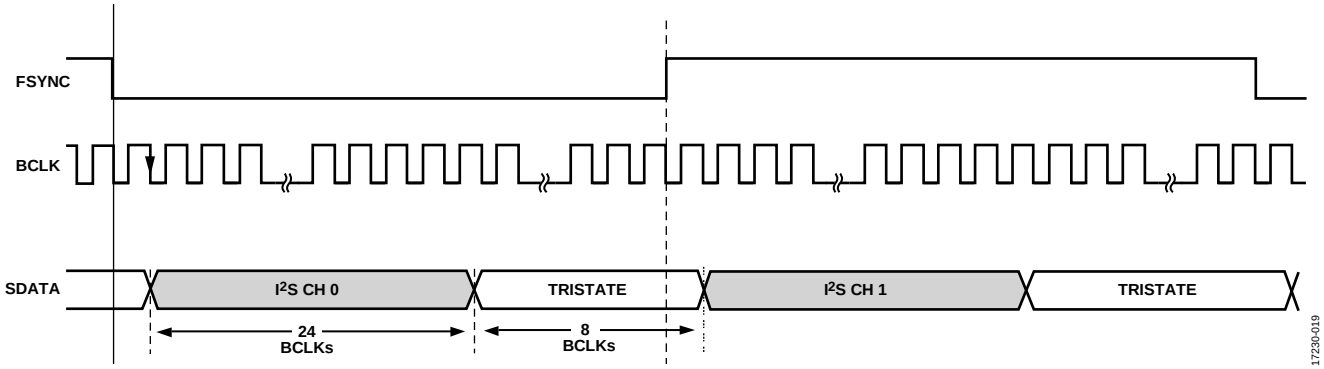


Figure 18. SPT_SIA_MODE = Stereo Mode (I²S), I²C Operation Only

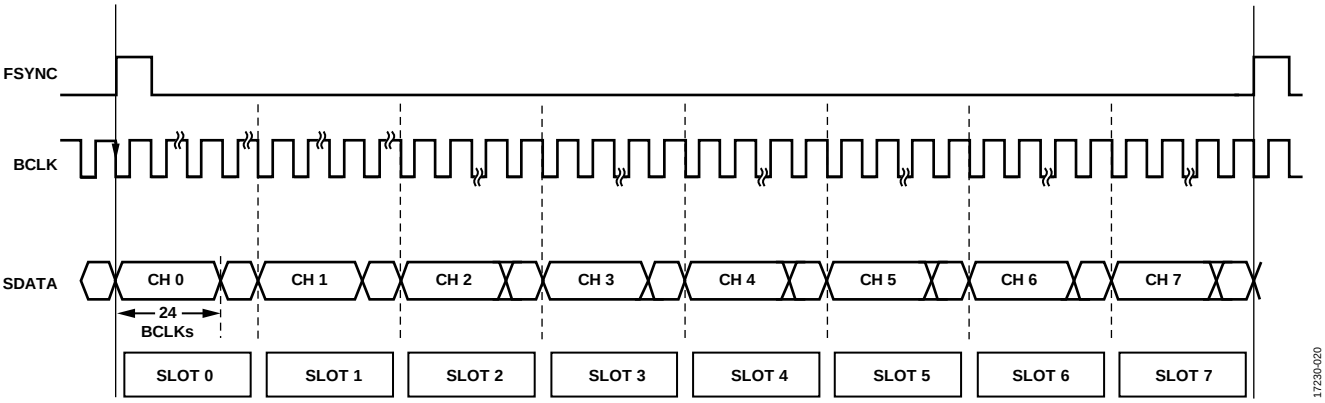


Figure 19. TDM-8, Default Channel Assignments, Left Justified Delayed by Zero, 24-Bit Data, 32-Bit Slots, Normal Polarity Clocks

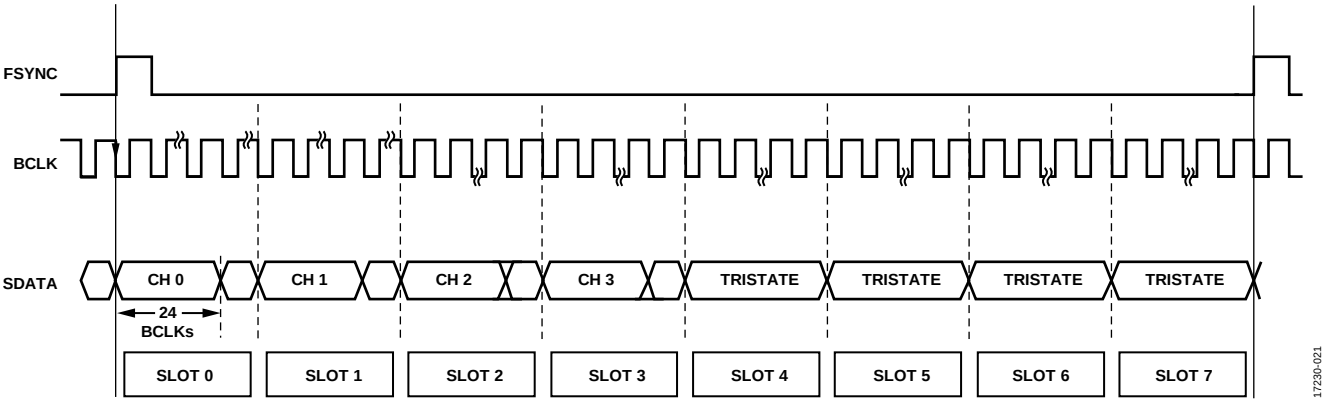


Figure 20. TDM-8, Left Justified Zero BCLK Delay, Only Channel 0 to Channel 3 Enabled

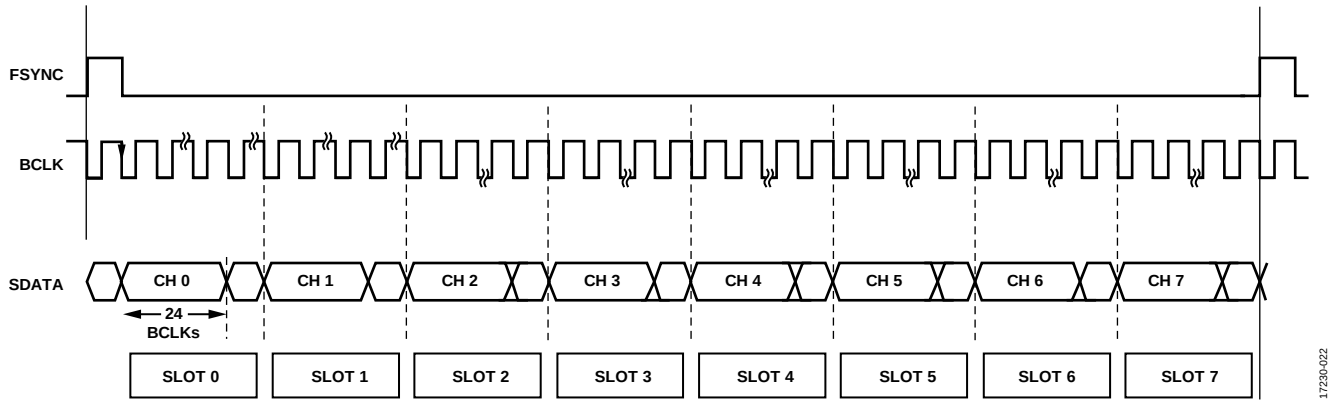


Figure 21. TDM-8 Hardware Mode, SCL = 1, SDA = 0, I²C Mode, One BCLK Delay, Normal Clock Polarity, Default Channel Assignments

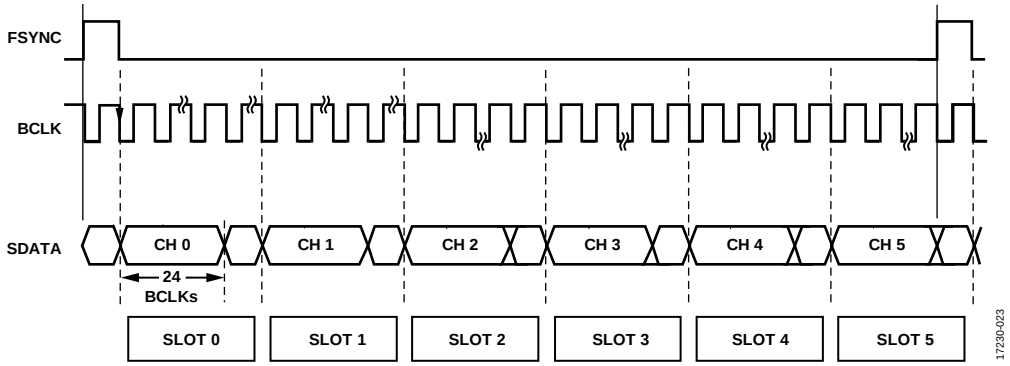


Figure 22. TDM-6, Hardware Mode, SCL = 0, SDA = x, I²C Mode, One BCLK Delay, Normal Clock Polarity, Default Channel Assignments

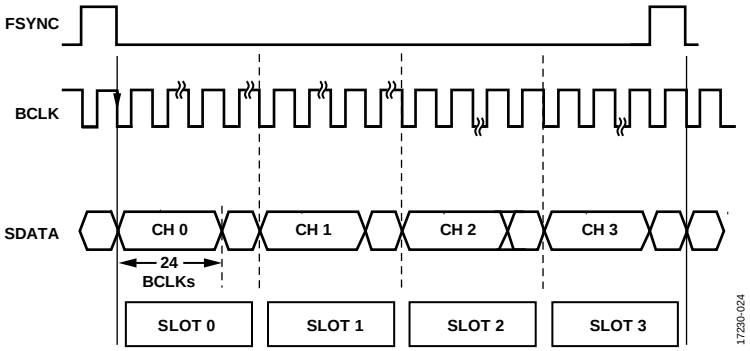


Figure 23. TDM-4, Hardware Mode, SCL = 1, SDA = 1, I²C Mode, One BCLK Delay, Normal Clock Polarity, Default Channel Assignments

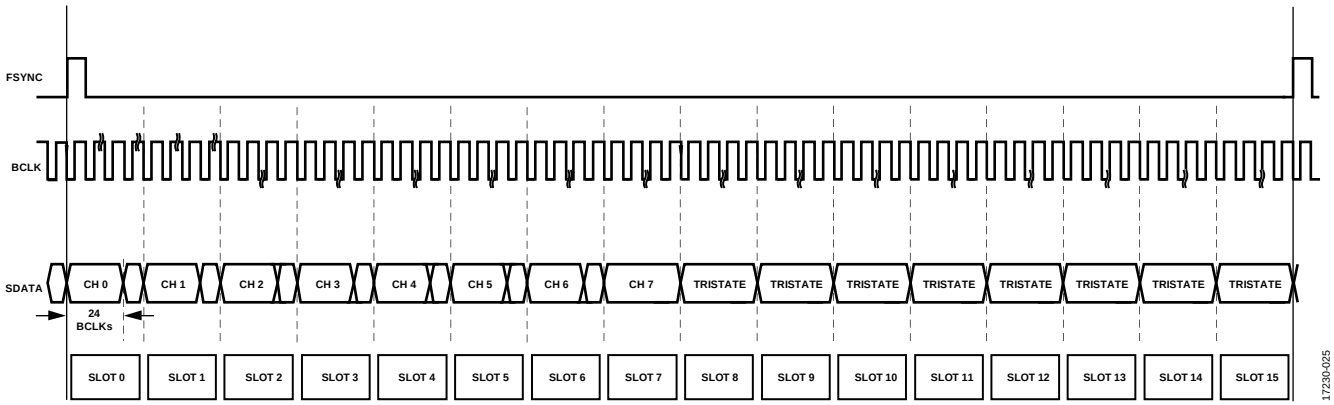


Figure 24. TDM-16, Default Channel Assignments, Left Justified Zero BCLK Delay, Normal Clock Polarity

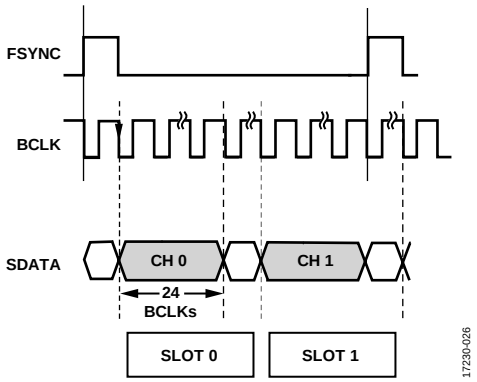


Figure 25. TDM-2, I²C Mode, One BCLK Delay, Normal Clock Polarity, Default Channel Assignments

I²C CONTROL INTERFACE

The ADAU7118 supports a 2-wire serial bus (I²C-compatible) shared across multiple peripherals. Two signals, serial data (SDA) and serial clock (SCL), carry information between the ADAU7118 and the system I²C master controller. The ADAU7118 is always a slave on the bus and cannot initiate a data transfer. Each slave device is identified by a unique address. The address byte format is shown in Table 13 with the LSBs of the address determined by the state of the ADDR/CONFIG pin (see Table 14). The address resides in the first 7 bits of the I²C write. The LSB of this byte sets either a read or write operation. Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation.

Both SDA and SCL are open-drain and require pull-up resistors to the IOVDD voltage. The ADAU7118 operates with I²C voltages over the full range of IOVDD

Table 13. I²C Device Address Byte Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	1	0	1	Bit 2	Bit 1	R/$\overline{W}$

Table 14. Standalone Hardware Mode: ADDR/CONFIG Pin Options

I²C Address Bit 2	I²C Address Bit 1	ADDR Pin Configuration
1	1	Tie to IOVDD
0	0	Tie to GND
Hardware Mode 1	Hardware Mode 1	Open
1	0	Tie to IOVDD through a 47 kΩ resistor
0	1	Tie to GND through a 47 kΩ resistor

OUTPUT PIN DRIVE STRENGTH

All output pins have configurable output drive strength that can be set via their respective control registers. Drive strengths of 2.5 mA, 5 mA, 10 mA, and 15 mA at 3.3 V IOVDD are possible. The serial data output pin functions in slave mode at all valid sample rates, provided that the external circuit design provides sufficient electrical signal integrity. When operating at IOVDD = 1.8 V nominal, take care to achieve sufficient timing margins at BCLK frequencies over 12.288 MHz. The capacitance of the bit clock and SDATA signal lines on the PCB, along with the length of the trace, enter into the calculation of this timing margin.

HIGH-PASS FILTER

There is a first order high-pass filter in the signal path that can be bypassed, if desired. The high-pass filter is disabled by default and can be enabled by setting HPF_EN (Bit 0, Register HPF_CONTROL) = 1. The cutoff frequency can be adjusted using the HPF_FC bits (Bits[7:4]) in the HPF_CONTROL register. The settings are relative to the output sampling rate. Table 15 shows the setting and the cutoff frequency for common sampling rates.

Table 15. HPF Cutoff Frequency Selections

		Cutoff Frequency in Hz	
HPF_FC (Bits[7:4]) Setting	**Multiplication Factor**	**For 48 kHz Sampling Rate**	**For 32 kHz Sampling Rate**
101	0.00505	242.4	161.6
110	0.00251	120.48	80.32
111	0.00125	60	40
1000	0.000623	29.904	19.936
1001	0.000311	14.928	9.952
1010	0.000155	7.44	4.96
1011	0.0000777	3.7296	2.4864
1100	0.0000389	1.8672	1.2448
1101	0.0000194	0.9312	0.6208
1110	0.00000971	0.46608	0.31072
1111	0.00000486	0.23328	0.15552

APPLICATIONS INFORMATION

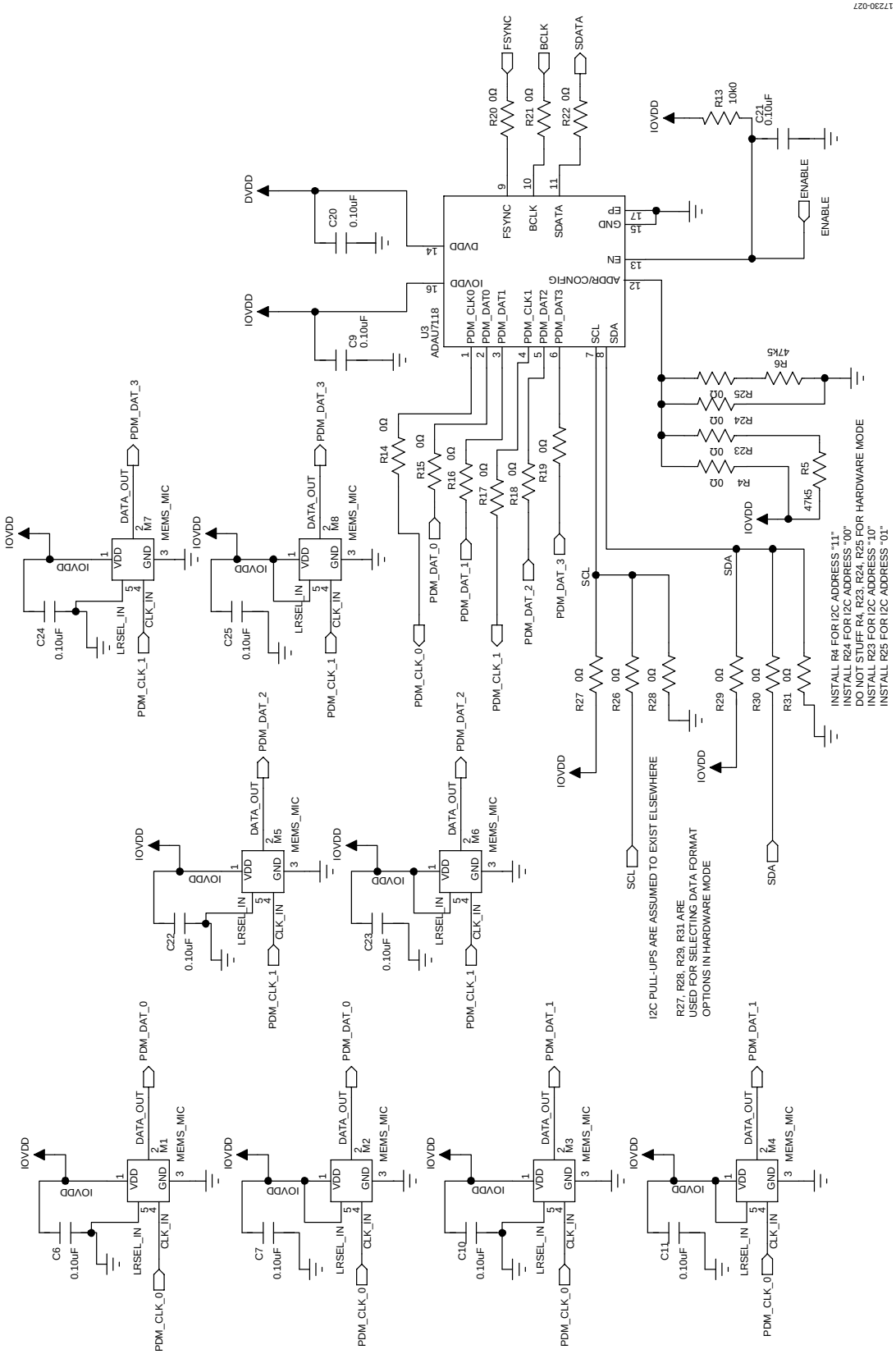


Figure 26. Example Application Circuit

REGISTER SUMMARY

Table 16. ADAU7118 Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x00	VENDOR_ID	[7:0]	VENDOR								0x41	R
0x01	DEVICE_ID1	[7:0]	DEVICE1								0x71	R
0x02	DEVICE_ID2	[7:0]	DEVICE2								0x18	R
0x03	REVISION_ID	[7:0]	REV								0x00	R
0x04	ENABLES	[7:0]	RESERVED		PDM_CLK1_EN	PDM_CLK0_EN	CHAN_67_EN	CHAN_45_EN	CHAN_23_EN	CHAN_01_EN	0x3F	R/W
0x05	DEC_RATIO_CLK_MAP	[7:0]	PDM_DAT3_CLK_MAP	PDM_DAT2_CLK_MAP	PDM_DAT1_CLK_MAP	PDM_DAT0_CLK_MAP	RESERVED		DEC_RATIO		0xC0	R/W
0x06	HPF_CONTROL	[7:0]	HPF_FC				RESERVED			HPF_EN	0xD0	R/W
0x07	SPT_CTRL1	[7:0]	RESERVED	SPT_TRI_STATE	SPT_SLOT_WIDTH		SPT_DATA_FORMAT			SPT_SAI_MODE	0x41	R/W
0x08	SPT_CTRL2	[7:0]	RESERVED						SPT_LRCLK_POL	SPT_BCLK_POL	0x00	R/W
0x09	SPT_C0	[7:0]	SPT_C0_SLOT				RESERVED			SPT_C0_DRV	0x01	R/W
0x0A	SPT_C1	[7:0]	SPT_C1_SLOT				RESERVED			SPT_C1_DRV	0x11	R/W
0x0B	SPT_C2	[7:0]	SPT_C2_SLOT				RESERVED			SPT_C2_DRV	0x21	R/W
0x0C	SPT_C3	[7:0]	SPT_C3_SLOT				RESERVED			SPT_C3_DRV	0x31	R/W
0x0D	SPT_C4	[7:0]	SPT_C4_SLOT				RESERVED			SPT_C4_DRV	0x41	R/W
0x0E	SPT_C5	[7:0]	SPT_C5_SLOT				RESERVED			SPT_C5_DRV	0x51	R/W
0x0F	SPT_C6	[7:0]	SPT_C6_SLOT				RESERVED			SPT_C6_DRV	0x61	R/W
0x10	SPT_C7	[7:0]	SPT_C7_SLOT				RESERVED			SPT_C7_DRV	0x71	R/W
0x11	DRIVE_STRENGTH	[7:0]	RESERVED		SDATA_DS		PDM_CLK1_DS		PDM_CLK0_DS		0x2A	R/W
0x12	RESETS	[7:0]	RESERVED						SOFT_FULL_RESET	SOFT_RESET	0x00	W

REGISTER DETAILS

ADI VENDOR ID REGISTER

Address: 0x00, Reset: 0x41, Name: VENDOR_ID

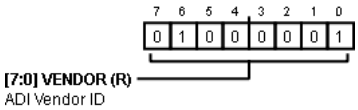


Table 17. Bit Descriptions for VENDOR_ID

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VENDOR	Not applicable	ADI Vendor ID	0x41	R

DEVICE ID 1 REGISTER

Address: 0x01, Reset: 0x71, Name: DEVICE_ID1

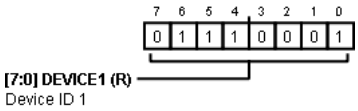


Table 18. Bit Descriptions for DEVICE_ID1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DEVICE1	Not applicable	Device ID 1	0x71	R

DEVICE ID 2 REGISTER

Address: 0x02, Reset: 0x18, Name: DEVICE_ID2

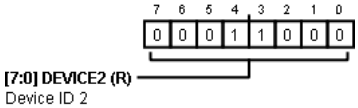


Table 19. Bit Descriptions for DEVICE_ID2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DEVICE2	Not applicable	Device ID 2	0x18	R

REVISION CODE REGISTER

Address: 0x03, Reset: 0x00, Name: REVISION_ID

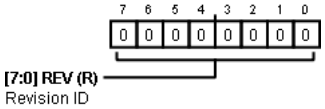


Table 20. Bit Descriptions for REVISION_ID

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	REV	Not applicable	Revision ID	0x0	R

CHANNEL PAIR AND CLOCK ENABLES REGISTER

Address: 0x04, Reset: 0x3F, Name: ENABLES

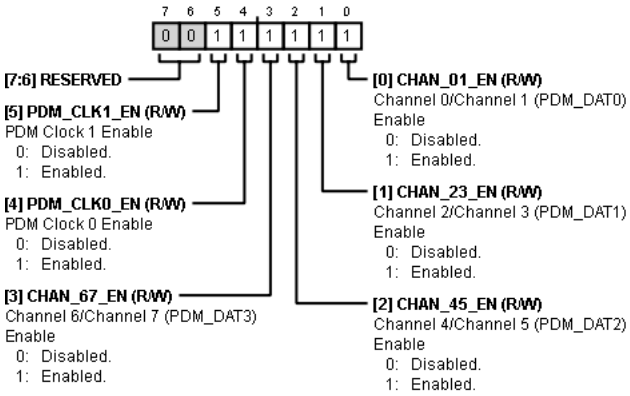


Table 21. Bit Descriptions for ENABLES

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R
5	PDM_CLK1_EN		PDM Clock 1 Enable.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
4	PDM_CLK0_EN		PDM Clock 0 Enable.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
3	CHAN_67_EN		Channel 6/Channel 7 (PDM_DAT3) Enable.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
2	CHAN_45_EN		Channel 4/Channel 5 (PDM_DAT2) Enable.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
1	CHAN_23_EN		Channel 2/Channel 3 (PDM_DAT1) Enable.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
0	CHAN_01_EN		Channel 0/Channel 1 (PDM_DAT0) Enable.	0x1	R/W
		0	Disabled.		
		1	Enabled.		

DECIMATION RATIO AND PDM CLOCK MAPPING CONTROLS REGISTER

Address: 0x05, Reset: 0xC0, Name: DEC_RATIO_CLK_MAP

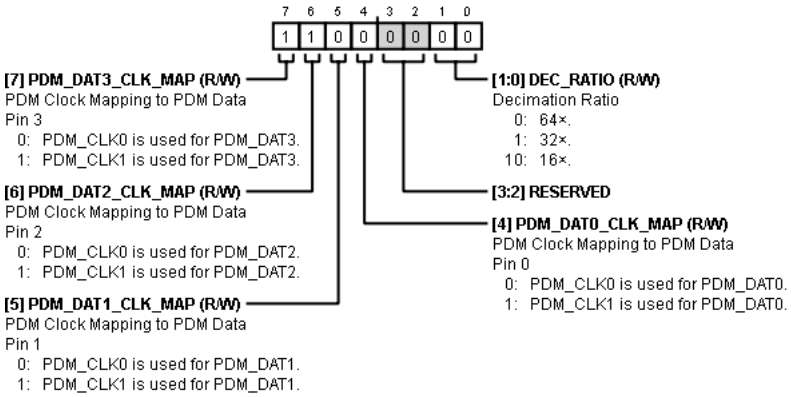


Table 22. Bit Descriptions for DEC_RATIO_CLK_MAP

Bits	Bit Name	Settings	Description	Reset	Access
7	PDM_DAT3_CLK_MAP		PDM Clock Mapping to PDM Data Pin 3.	0x1	R/W
		0	PDM_CLK0 is used for PDM_DAT3.		
		1	PDM_CLK1 is used for PDM_DAT3.		
6	PDM_DAT2_CLK_MAP		PDM Clock Mapping to PDM Data Pin 2.	0x1	R/W
		0	PDM_CLK0 is used for PDM_DAT2.		
		1	PDM_CLK1 is used for PDM_DAT2.		
5	PDM_DAT1_CLK_MAP		PDM Clock Mapping to PDM Data Pin 1.	0x0	R/W
		0	PDM_CLK0 is used for PDM_DAT1.		
		1	PDM_CLK1 is used for PDM_DAT1.		
4	PDM_DAT0_CLK_MAP		PDM Clock Mapping to PDM Data Pin 0.	0x0	R/W
		0	PDM_CLK0 is used for PDM_DAT0.		
		1	PDM_CLK1 is used for PDM_DAT0.		
[3:2]	RESERVED		Reserved.	0x0	R
[1:0]	DEC_RATIO		Decimation Ratio.	0x0	R/W
		0	64×.		
		1	32×.		
		10	16×.		

HIGH-PASS FILTER CONTROLS REGISTER

Address: 0x06, Reset: 0xD0, Name: HPF_CONTROL

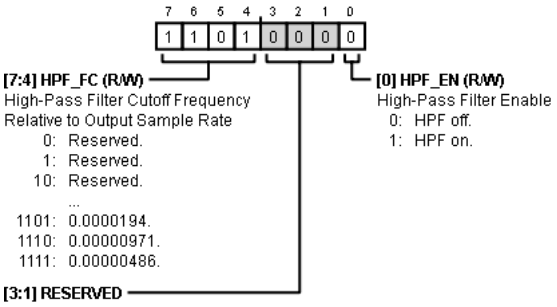


Table 23. Bit Descriptions for HPF_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	HPF_FC		High-Pass Filter Cutoff Frequency Relative to Output Sample Rate.	0xD	R/W
		0	Reserved.		
		1	Reserved.		
		10	Reserved.		
		11	Reserved.		
		100	Reserved.		
		101	0.00505.		
		110	0.00251.		
		111	0.00125.		
		1000	0.000623.		
		1001	0.000311.		
		1010	0.000155.		
		1011	0.0000777.		
		1100	0.0000389.		
		1101	0.0000194.		
		1110	0.00000971.		
		1111	0.00000486.		
[3:1]	RESERVED		Reserved.	0x0	R
0	HPF_EN		High-Pass Filter Enable.	0x0	R/W
		0	HPF off.		
		1	HPF on.		

SERIAL PORT CONTROLS 1 REGISTER

Address: 0x07, Reset: 0x41, Name: SPT_CTRL1

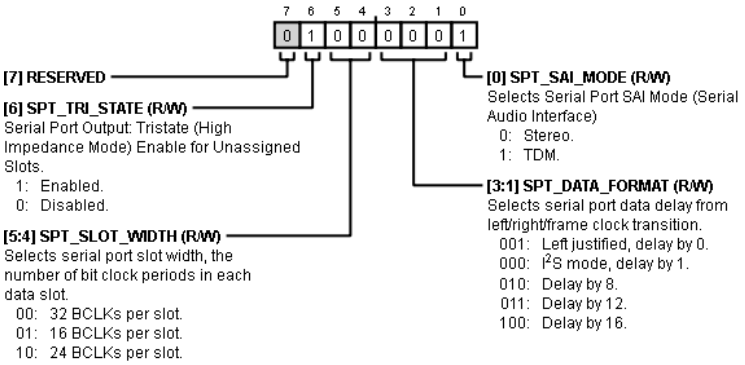


Table 24. Bit Descriptions for SPT_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
6	SPT_TRI_STATE		Serial Port Output: Tristate (High Impedance Mode) Enable for Unassigned Slots.	0x1	R/W
		1	Enabled.		
		0	Disabled.		
[5:4]	SPT_SLOT_WIDTH		Selects serial port slot width, the number of bit clock periods in each data slot.	0x0	R/W
		00	32 BCLKs per slot.		
		01	16 BCLKs per slot.		
		10	24 BCLKs per slot.		
[3:1]	SPT_DATA_FORMAT		Selects serial port data delay from left/right/frame clock transition.	0x0	R/W
		001	Left justified, delay by 0.		
		000	I^2S mode, delay by 1.		
		010	Delay by 8.		
		011	Delay by 12.		
		100	Delay by 16.		
0	SPT_SAI_MODE		Selects Serial Port SAI Mode (Serial Audio Interface).	0x1	R/W
		0	Stereo.		
		1	TDM.		

SERIAL PORT CONTROLS 2 REGISTER

Address: 0x08, Reset: 0x00, Name: SPT_CTRL2

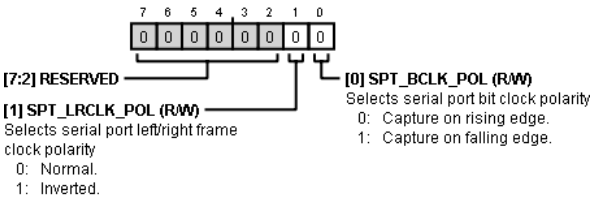


Table 25. Bit Descriptions for SPT_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	RESERVED		Reserved.	0x0	R
1	SPT_LRCLK_POL		Selects serial port left/right frame clock polarity.	0x0	R/W
		0	Normal.		
		1	Inverted.		
0	SPT_BCLK_POL		Selects serial port bit clock polarity.	0x0	R/W
		0	Capture on rising edge.		
		1	Capture on falling edge.		

SERIAL PORT ROUTING AND DRIVE ENABLE CHANNEL 0 REGISTER

Address: 0x09, Reset: 0x01, Name: SPT_C0

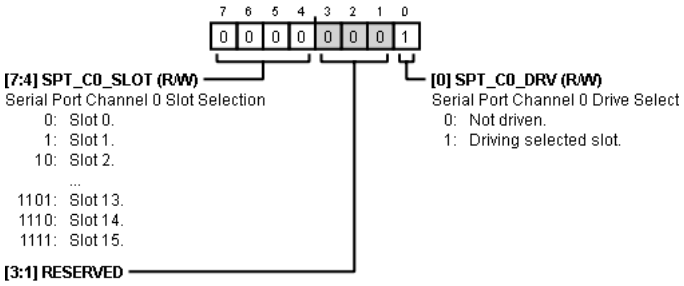


Table 26. Bit Descriptions for SPT_C0

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	SPT_C0_SLOT		Serial Port Channel 0 Slot Selection.	0x0	R/W
		0	Slot 0.		
		1	Slot 1.		
		10	Slot 2.		
		11	Slot 3.		
		100	Slot 4.		
		101	Slot 5.		
		110	Slot 6.		
		111	Slot 7.		
		1000	Slot 8.		
		1001	Slot 9.		
		1010	Slot 10.		
		1011	Slot 11.		
		1100	Slot 12.		
		1101	Slot 13.		
		1110	Slot 14.		
		1111	Slot 15.		
[3:1]	RESERVED		Reserved.	0x0	R
0	SPT_C0_DRV		Serial Port Channel 0 Drive Select. This bit determines whether the associated channel is driven in its assigned slot or if it is in a high impedance state floating during the assigned slot.	0x1	R/W
		0	Not driven.		
		1	Driving selected slot.		

SERIAL PORT ROUTING AND DRIVE ENABLE CHANNEL 1 REGISTER

Address: 0x0A, Reset: 0x11, Name: SPT_C1

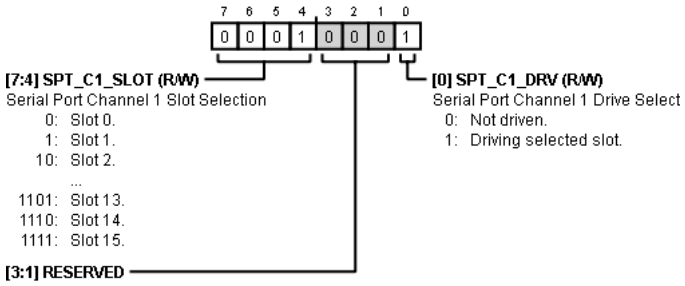


Table 27. Bit Descriptions for SPT_C1

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	SPT_C1_SLOT		Serial Port Channel 1 Slot Selection.	0x1	R/W
		0	Slot 0.		
		1	Slot 1.		
		10	Slot 2.		
		11	Slot 3.		
		100	Slot 4.		
		101	Slot 5.		
		110	Slot 6.		
		111	Slot 7.		
		1000	Slot 8.		
		1001	Slot 9.		
		1010	Slot 10.		
		1011	Slot 11.		
		1100	Slot 12.		
		1101	Slot 13.		
		1110	Slot 14.		
		1111	Slot 15.		
[3:1]	RESERVED		Reserved.	0x0	R
0	SPT_C1_DRV		Serial Port Channel 1 Drive Select. This bit determines whether the associated channel is driven in its assigned slot or if it is in a high impedance state floating during the assigned slot.	0x1	R/W
		0	Not driven.		
		1	Driving selected slot.		

SERIAL PORT ROUTING AND DRIVE ENABLE CHANNEL 2 REGISTER

Address: 0x0B, Reset: 0x21, Name: SPT_C2

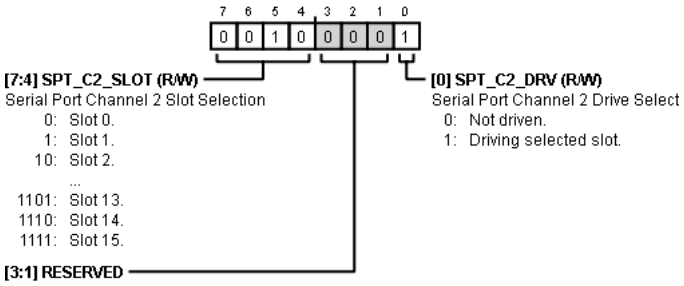


Table 28. Bit Descriptions for SPT_C2

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	SPT_C2_SLOT		Serial Port Channel 2 Slot Selection.	0x2	R/W
		0	Slot 0.		
		1	Slot 1.		
		10	Slot 2.		
		11	Slot 3.		
		100	Slot 4.		
		101	Slot 5.		
		110	Slot 6.		
		111	Slot 7.		
		1000	Slot 8.		
		1001	Slot 9.		
		1010	Slot 10.		
		1011	Slot 11.		
		1100	Slot 12.		
		1101	Slot 13.		
		1110	Slot 14.		
		1111	Slot 15.		
[3:1]	RESERVED		Reserved.	0x0	R
0	SPT_C2_DRV		Serial Port Channel 2 Drive Select. This bit determines whether the associated channel is driven in its assigned slot or if it is in a high impedance state floating during the assigned slot.	0x1	R/W
		0	Not driven.		
		1	Driving selected slot.		

SERIAL PORT ROUTING AND DRIVE ENABLE CHANNEL 3 REGISTER

Address: 0x0C, Reset: 0x31, Name: SPT_C3

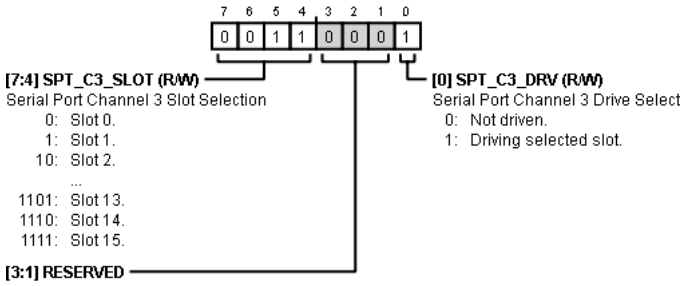


Table 29. Bit Descriptions for SPT_C3

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	SPT_C3_SLOT		Serial Port Channel 3 Slot Selection.	0x3	R/W
		0	Slot 0.		
		1	Slot 1.		
		10	Slot 2.		
		11	Slot 3.		
		100	Slot 4.		
		101	Slot 5.		
		110	Slot 6.		
		111	Slot 7.		
		1000	Slot 8.		
		1001	Slot 9.		
		1010	Slot 10.		
		1011	Slot 11.		
		1100	Slot 12.		
		1101	Slot 13.		
		1110	Slot 14.		
		1111	Slot 15.		
[3:1]	RESERVED		Reserved.	0x0	R
0	SPT_C3_DRV		Serial Port Channel 3 Drive Select. This bit determines whether the associated channel is driven in its assigned slot or if it is in a high impedance state floating during the assigned slot.	0x1	R/W
		0	Not driven.		
		1	Driving selected slot.		

SERIAL PORT ROUTING AND DRIVE ENABLE CHANNEL 4 REGISTER

Address: 0x0D, Reset: 0x41, Name: SPT_C4

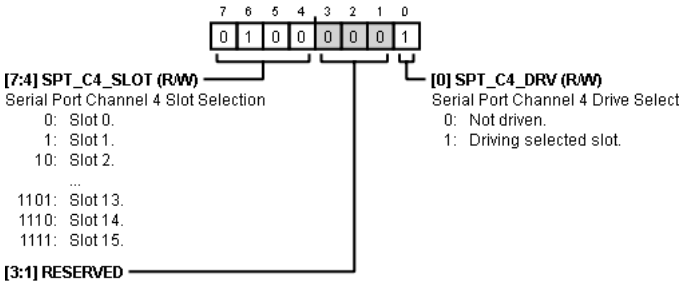


Table 30. Bit Descriptions for SPT_C4

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	SPT_C4_SLOT		Serial Port Channel 4 Slot Selection.	0x4	R/W
		0	Slot 0.		
		1	Slot 1.		
		10	Slot 2.		
		11	Slot 3.		
		100	Slot 4.		
		101	Slot 5.		
		110	Slot 6.		
		111	Slot 7.		
		1000	Slot 8.		
		1001	Slot 9.		
		1010	Slot 10.		
		1011	Slot 11.		
		1100	Slot 12.		
		1101	Slot 13.		
		1110	Slot 14.		
		1111	Slot 15.		
[3:1]	RESERVED		Reserved.	0x0	R
0	SPT_C4_DRV		Serial Port Channel 4 Drive Select. This bit determines whether the associated channel is driven in its assigned slot or if it is in a high impedance state floating during the assigned slot.	0x1	R/W
		0	Not driven.		
		1	Driving selected slot.		

SERIAL PORT ROUTING AND DRIVE ENABLE CHANNEL 5 REGISTER

Address: 0x0E, Reset: 0x51, Name: SPT_C5

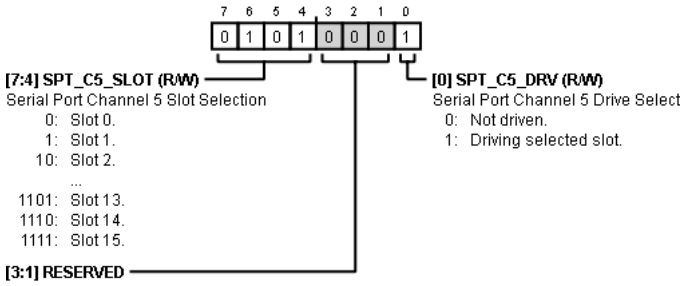


Table 31. Bit Descriptions for SPT_C5

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	SPT_C5_SLOT		Serial Port Channel 5 Slot Selection.	0x5	R/W
		0	Slot 0.		
		1	Slot 1.		
		10	Slot 2.		
		11	Slot 3.		
		100	Slot 4.		
		101	Slot 5.		
		110	Slot 6.		
		111	Slot 7.		
		1000	Slot 8.		
		1001	Slot 9.		
		1010	Slot 10.		
		1011	Slot 11.		
		1100	Slot 12.		
		1101	Slot 13.		
		1110	Slot 14.		
		1111	Slot 15.		
[3:1]	RESERVED		Reserved.	0x0	R
0	SPT_C5_DRV		Serial Port Channel 5 Drive Select. This bit determines whether the associated channel is driven in its assigned slot or if it is in a high impedance state floating during the assigned slot.	0x1	R/W
		0	Not driven.		
		1	Driving selected slot.		

SERIAL PORT ROUTING AND DRIVE ENABLE CHANNEL 6 REGISTER

Address: 0x0F, Reset: 0x61, Name: SPT_C6

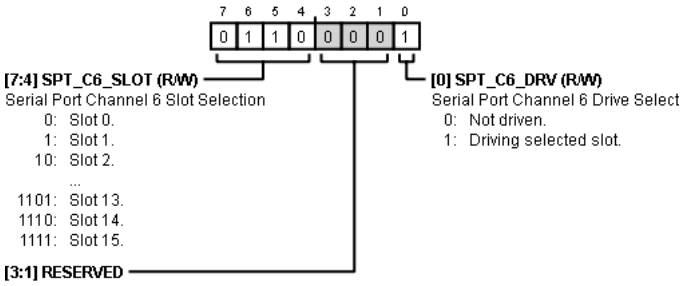


Table 32. Bit Descriptions for SPT_C6

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	SPT_C6_SLOT		Serial Port Channel 6 Slot Selection.	0x6	R/W
		0	Slot 0.		
		1	Slot 1.		
		10	Slot 2.		
		11	Slot 3.		
		100	Slot 4.		
		101	Slot 5.		
		110	Slot 6.		
		111	Slot 7.		
		1000	Slot 8.		
		1001	Slot 9.		
		1010	Slot 10.		
		1011	Slot 11.		
		1100	Slot 12.		
		1101	Slot 13.		
		1110	Slot 14.		
		1111	Slot 15.		
[3:1]	RESERVED		Reserved.	0x0	R
0	SPT_C6_DRV		Serial Port Channel 6 Drive Select. This bit determines whether the associated channel is driven in its assigned slot or if it is in a high impedance state floating during the assigned slot.	0x1	R/W
		0	Not driven.		
		1	Driving selected slot.		

SERIAL PORT ROUTING AND DRIVE ENABLE CHANNEL 7 REGISTER

Address: 0x10, Reset: 0x71, Name: SPT_C7

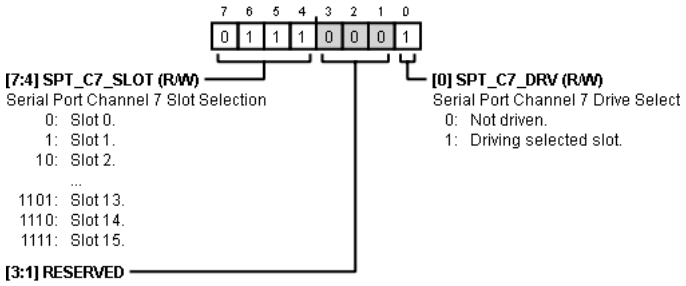


Table 33. Bit Descriptions for SPT_C7

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	SPT_C7_SLOT		Serial Port Channel 7 Slot Selection.	0x7	R/W
		0	Slot 0.		
		1	Slot 1.		
		10	Slot 2.		
		11	Slot 3.		
		100	Slot 4.		
		101	Slot 5.		
		110	Slot 6.		
		111	Slot 7.		
		1000	Slot 8.		
		1001	Slot 9.		
		1010	Slot 10.		
		1011	Slot 11.		
		1100	Slot 12.		
		1101	Slot 13.		
		1110	Slot 14.		
		1111	Slot 15.		
[3:1]	RESERVED		Reserved.	0x0	R
0	SPT_C7_DRV		Serial Port Channel 7 Drive Select. This bit determines whether the associated channel is driven in its assigned slot or if it is in a high impedance state floating during the assigned slot.	0x1	R/W
		0	Not driven.		
		1	Driving selected slot.		

OUTPUT PAD DRIVE STRENGTH CONTROLS REGISTER

Address: 0x11, Reset: 0x2A, Name: DRIVE_STRENGTH

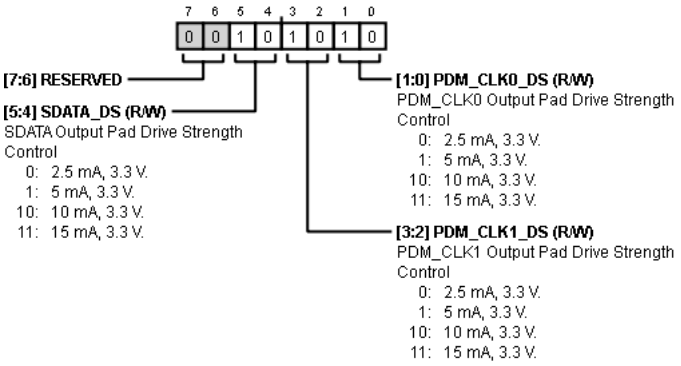


Table 34. Bit Descriptions for DRIVE_STRENGTH

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R
[5:4]	SDATA_DS		SDATA Output Pad Drive Strength Control.	0x2	R/W
		0	2.5 mA, 3.3 V.		
		1	5 mA, 3.3 V.		
		10	10 mA, 3.3 V.		
		11	15 mA, 3.3 V.		
[3:2]	PDM_CLK1_DS		PDM_CLK1 Output Pad Drive Strength Control.	0x2	R/W
		0	2.5 mA, 3.3 V.		
		1	5 mA, 3.3 V.		
		10	10 mA, 3.3 V.		
		11	15 mA, 3.3 V.		
[1:0]	PDM_CLK0_DS		PDM_CLK0 Output Pad Drive Strength Control.	0x2	R/W
		0	2.5 mA, 3.3 V.		
		1	5 mA, 3.3 V.		
		10	10 mA, 3.3 V.		
		11	15 mA, 3.3 V.		

SOFTWARE RESET REGISTER

Address: 0x12, Reset: 0x00, Name: RESETS

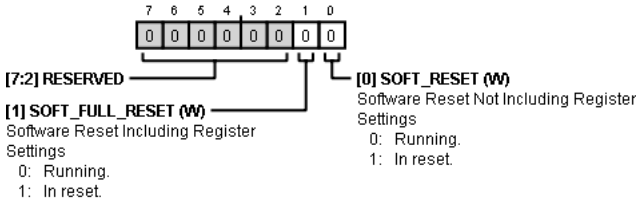
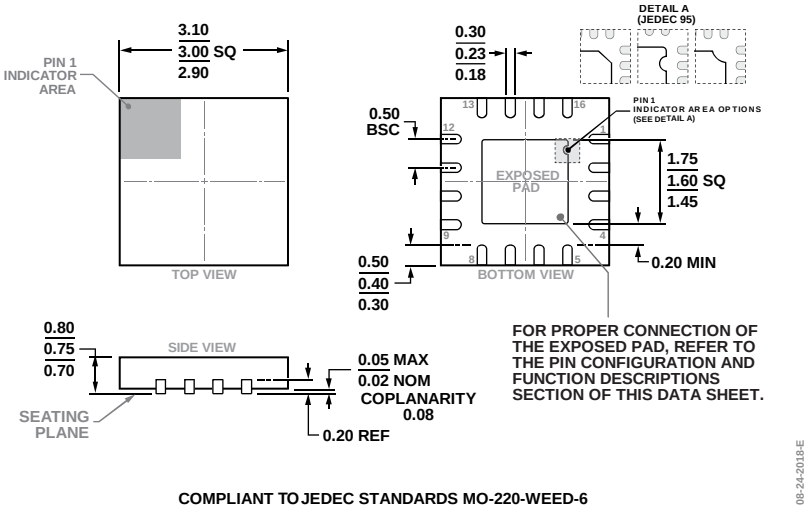


Table 35. Bit Descriptions for RESETS

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	RESERVED		Reserved.	0x0	R
1	SOFT_FULL_RESET		Software Reset Including Register Settings.	0x0	W
		0	Running.		
		1	In reset.		
0	SOFT_RESET		Software Reset Not Including Register Settings.	0x0	W
		0	Running.		
		1	In reset.		

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6

Figure 27. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Height
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Marking Code	Package Option
ADAU7118ACPZRL	−40°C to +85°C	16-Lead LFCSP, 13″ Tape and Reel	Y70	CP-16-22
ADAU7118ACPZRL7	−40°C to +85°C	16-Lead LFCSP, 7″ Tape and Reel	Y70	CP-16-22
EVAL-ADAU7118Z		Evaluation Board		

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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D17230-0-8/19(A)

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