Enpirion EN5364QI 6A DCDC Converter w/Integrated Inductor Evaluation Board

Introduction

Thank you for choosing Altera Enpirion power products!

This user guide should be used together with the latest device datasheet.

- The EN5364QI features integrated inductor, power MOSFETS, Controller, bulk of the compensation Network, and protection circuitry against system faults. This level of integration delivers a substantial reduction in footprint and part count over competing solutions. However, the evaluation board is not optimized for minimum footprint; rather for engineering ease of evaluation through programming options, clip leads, test points etc.
- The EN5364QI device is feature rich and supports the following additional functions:
  - **Margining** – The output voltage can be changed by ±2.5%, ±5% or ±10% about the nominal, under digital control using ternary pins MAR[1:2] Margining is highly valued for system robustness verification and reliability studies. Note: POK automatically scales with margining.
  - **Phase Lock** - The internal switching frequency can be phase locked to an external clock source (or another EN5364QI) by connecting such a clock source to pin S_IN. This feature is highly valued to keep beat frequencies (between a system sampling clock and the DC/DC converter switching frequency) out of the desired signal band.
  - **Delay** - A delayed version of the internal switching clock (or the PWM signal) is available at pin S_OUT. This may be input to another EN5364QI device.
  - The delay is programmable by means of a single resistor connected between pin S_delay and AGND. This feature allows the control of input ripple when multiple EN5364QI devices are used on a system board.
  - **Pre-bias operation** – When the device pre-bias is enabled (jumper provided), the device will monotonically ramp-up its output voltage from a pre-bias voltage level to the programmed output voltage level under control of Enable signal. The pre-bias (Back-feed) voltage may be coupled to the output via a diode. This diode (D2) is populated on the board. Back-feed voltage may be applied at BF_IN (TP18)

- **Parallel Mode operation** – Up to 4 EN5364QI devices may be operated in parallel when load currents greater than 6A is desired. In parallel mode, one device is designated the Master and up to 3 devices operate in slave mode, controlled by the Master. The PWM output of the Master is routed to slave devices. By daisy chaining the Slave devices even more devices can be operated in parallel but practical considerations, such as board layout would limit the number of slave devices to three.
- **Soft-Start** – A 15nF (C11) soft-start capacitor is populated on the evaluation board for an output voltage ramp time of ~1ms. This may be swapped for a different value capacitor if a different ramp time is desired. To limit the inrush current this capacitor value should be greater than 4.7nF. The output voltage rise time is ~65k*C_{SS}.

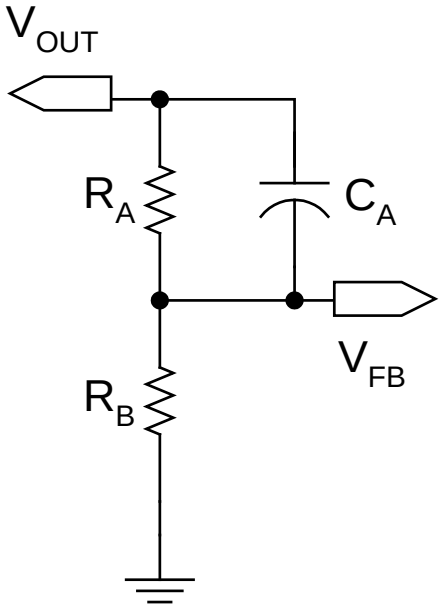
- The EN5364QI features a customer programmable output voltage by means of a resistor divider. The resistor divider allows the user to set the V_{OUT} to any value within the range 0.6V to approximately (V_{IN}-0.5V). `Referring to Figure 1, the evaluation board, as shipped is populated with a single R_A, a single C_A, and four possible R_B resistors. A jumper selects one of the 4 R_B resistors to produce a voltage of 0.804, 0.998, 1.2 or 1.8Volts. You can populate more than one R_B jumper position to get even higher output voltages. See "VOUT Programming" section in the evaluation board schematic (Figure 7).
- The EN5364QI includes the bulk of the compensation network internally. However, an external phase-lead (zero) capacitor is required as part of the feedback. This network is shown in Figure -1. Appropriate component values allow for optimum compensation for a given Input voltage and choice of loop bandwidth. The equations in Figure 1 provide the details to calculate component values.
- MAR1 and MAR2 are ternary input signals. The pins are allowed to be in a low state (tied to GND), a high state (tied to V_{IN}), or a float state. Table-1 shows the margining truth table. Accordingly, the output voltage can be nominal or ±2.5%, ±5% or ±10% about the nominal. 7 out of 9 possible states of MAR[1:2] are used for margining. The other two states are reserved for diagnostics. If tying MAR[1,2] to V_{IN}, a series resistor is recommended to reduce the pin input current (see Figure 2).
- A footprint is provided for a SMC connector (not populated) for S_IN. A clock source (3.6 to 4.4MHz) may be applied to S_IN to synchronize the device switching frequency to the external source. S_OUT will output a clock signal synchronous with the switching frequency, with a phase delay. S_OUT of one EN5364QI may be connected to S_IN of another EN5364QI device in different modes of operation.
- The phase delay is set by connecting a resistor from S_delay to AGND. The delay is approximately:

Delay (nsec) = 2*[S_delay resistance in kΩ.]

A 49.9kΩ (populated on Evaluation board) resistor value delays the clock signal by ~100nsec.

- EN5364QI supports pre-bias mode operation. To use this option set the EN_PB jumper to pre-bias enable position with device powered down. When the device is subsequently powered and enabled, the output voltage will ramp monotonically from its pre-bias value to the programmed value. Pre-bias voltage may be applied to clip lead BF_IN on the evaluation board. A diode D2 is populated on the board between BF_IN and VOUT.
- Jumpers are provided for ease of logical high/low programming of the following signals:
  - Enable
  - Pre-bias Enable
  - MAR1 and MAR2 Margining ternary inputs
  - Master/Slave ternary input

  Enable may also be controlled using an external switching source by removing the jumper and applying the enable signal to the middle pin and ground.
  - Jumpers are also provided for selecting one of 4 possible output voltages.
- The board comes with input decoupling and reverse polarity protection to guard the device against common setup mishaps.



$$R_A = 30{,}000 \times Vin \quad (value\ in\ \Omega)$$

$$C_A = \frac{4.72 \times 10^{-6}}{R_A} \quad (C_A\ in\ Farads,\ R_A\ in\ \Omega)$$

$$R_B = \frac{V_{FB} \times RA}{(V_{OUT} - V_{FB})}$$

Figure - 1 : Output voltage programming and loop compensation. R_A and C_A correspond R17 & C20 on the board. R_B corresponds to a combination of R13, R14, R16, or R18 on the board, depending on which jumpers are populated on J13.

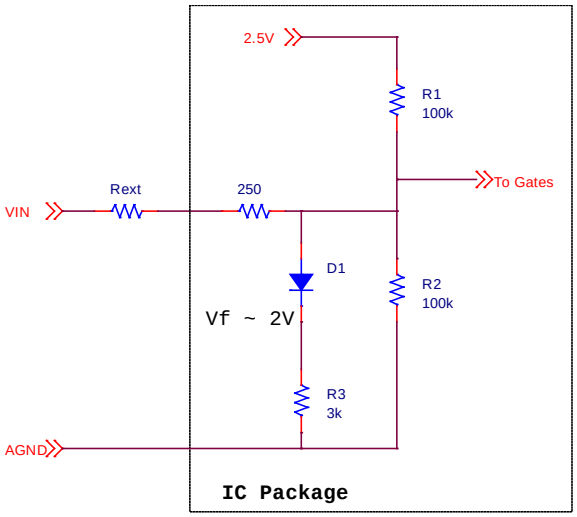


Figure 2: Equivalent circuit of a ternary pin (MAR1, MAR2, or M/S) input buffer. To get a logic High on a ternary input, pull the pin to V_{IN} through an external resistor R_{EXT}. The board is populated with a 10kΩ REXT for all three ternary pins.

Quick Start Guide

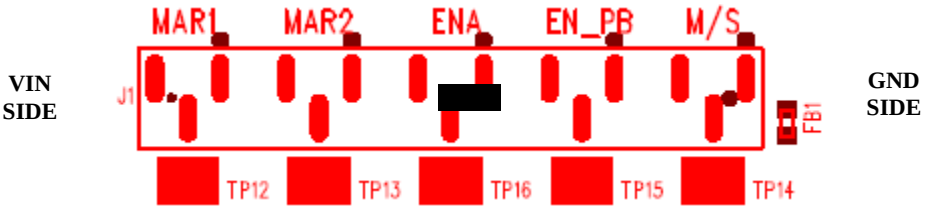


Figure – 3 : J1 Mode Selection Jumpers

In Figure 3, the jumper on ENA pin as shown is in disable mode. For all the J1 positions, when the jumper is between the middle and right pins the signal pin is connected to ground or logic low. When the jumper is between the left and middle pins, the signal pin is connected to VIN or logic High. When there is no jumper, MAR1, MAR2 and M_S pins will be in Float mode, however ENA and EN_PB are internally pulled low.

WARNING: complete steps 1 through 4 before applying power to the EN5364QI evaluation board.

STEP 1: Set the "ENA" and "ENA_PB" jumper to the Disable Position. Select MAR1, MAR2, and M/S to float (no jumper).

STEP 2: Set the output voltage select jumper for the desired setting as shown below:

Figure – 4 : J13 Voltage Selection Jumpers

In Figure 4, output Voltages, from left to right, are 0.804V, 0.998V, 1.2V and 1.0V.Jumper as shown, selects 1.2V output. Higher output voltages can be achieved by populating multiple J13 jumper positions. See Figures 1 and 7.

CAUTION: Except for ENA, NONE of the J1 & J13 jumpers can be changed while the EN5364QI is enabled. Doing so could damage the part.

STEP 3: Connect Power Supply to the input power connectors, VIN (+) and GND (–) as indicated in Figure - 5 and set the power supply to the desired voltage. The compensation components for the board have been optimized for an input voltage of 5V (see Figures 1 & 7). To optimize the board for another input voltage, calculate new values R_A, C_A, and R_B using the equations in Figure 1. The caption in Figure 1, states which components on the PCB correspond to R_A, C_A, & R_B.

CAUTION: be mindful of the polarity. Even though the evaluation board comes with reverse polarity protection diodes, it is rarely a good idea to reverse the input polarity.

STEP 4: Connect the load to the output connectors VOUT (+) and GND (–), as indicated in Figure -5.

STEP 5: Power up the board and move the ENA jumper to the enabled position. The EN5364QI is now powered up and generating the desired output. You are free to make Efficiency, Ripple, Line/Load Regulation, Load transient, Power OK, over current limit and temperature related measurements. You may also view the delayed switching clock at S_OUT. However, you do not have a reference to measure the delay against!

STEP 5A: Power Up/Down Behavior – Remove ENA jumper and connect a pulse generator (output disabled) signal to the middle pin of ENA and Ground. Set the pulse amplitude to swing from 0 to 2.5 volts. Set the pulse period to 10msec., duty cycle to 50% and fast transition (<1usec.) Hook up oscilloscope probes to ENA, SS, POK and VOUT with clean ground returns. Enable pulse generator output. Observe the SS capacitor and VOUT voltage ramps as ENA goes high and again as ENA goes low.

STEP 6: Margining – Disable device by moving the ENA jumper. Set MAR-1 and MAR-2 jumpers to the desired amount (percentage) voltage shift according to Table 1. Re-Enable device and continue as in Step 5.

MAR-1	MAR-2	Output Modulation
Float	Float	0%
Low	Low	-2.5%
High	Low	+2.5%
Low	High	-5%
High	High	+5%
Low	Float	-10%
High	Float	+10%
Float	High	0%, Delay Bypass
Float	Low	Reserved

Table-1 : Margin Block Truth Table

STEP 7: Phase Lock – Disable device by moving ENA jumper. Power down the device. Connect a pulse generator (properly terminated and output disabled) signal between S_IN and GND. Set the pulse amplitude to swing from 0 to 2.5 volts. Set the pulse frequency to 4MHz. Connect oscilloscope probes to S_IN & S_OUT. Power up device. Enable device. Note S_OUT – it is the free running switching frequency. Now enable the pulse generator output. S_OUT should be locked to S_IN with a fixed delay (depending on the value of the S_Delay resistor.) Sweep the clock frequency between 3.6 and 4.4 MHz and note the lock range at both extremes.
You may next wish to observe the delay as a function of S_Delay resistor.
ALWAYS power down device before changing board level components!

STEP 8: Pre-Bias Operation – Disable device by removing Enable jumper. Power down device. Set EN_PB jumper to logical "1." Connect a pulse generator (output disabled) signal to the middle pin of ENA and Ground. Set the pulse amplitude to swing from 0 to 2.5 volts. Set the pulse period to 10msec., duty cycle to 50% and fast transition (<1usec.) Hook up oscilloscope probes to ENA, SS, POK and VOUT with clean ground returns. Connect a power supply (set desired voltage but output disabled) to TP18 (BF_IN.) D2 is a diode connecting BF_IN to VOUT. Turn the back feed supply on. VOUT will charge to BF_IN minus a diode drop. Set the output voltage to a level greater than the back feed voltage. Enable pulse generator output. Observe the output voltage and SS voltage in relation to the Enable pulse. Sweep the back feed voltage up and down but always less than VOUT and note device operation.

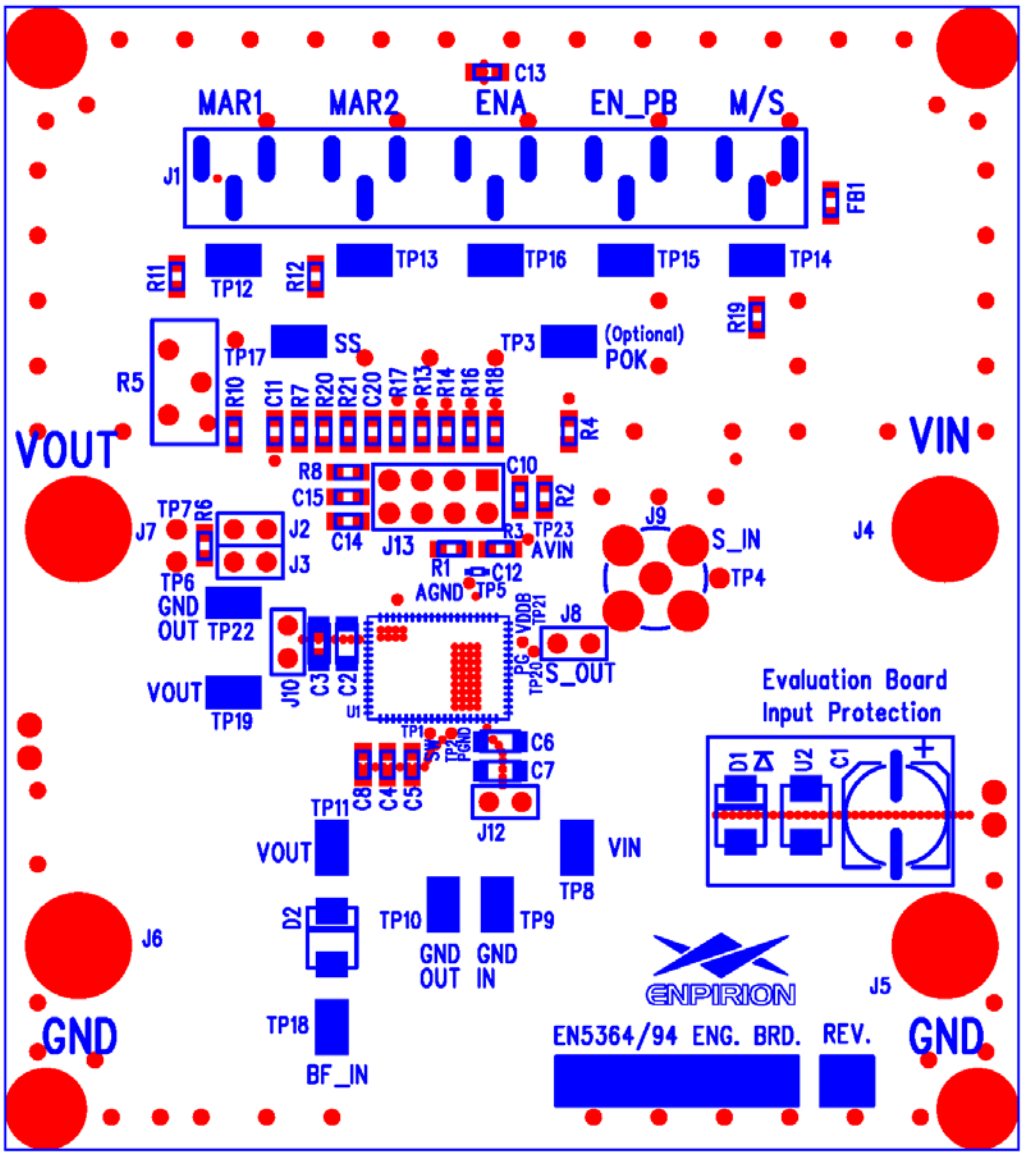


Figure – 5 : Evaluation Board Layout.

Test Recommendations

To guarantee measurement accuracy, the following precautions should be observed:

1. Make all input and output voltage measurements at the board using the test points provided. This will eliminate voltage drop across the line and load cables that can produce false readings.
2. Measure input and output current with series ammeters or accurate shunt resistors. This is especially important when measuring efficiency.
3. Use a low-loop-inductance probe shown here to measure switching signals to avoid noise coupling into the probe ground lead. J10 is a convenient point to measure output ripple and load transient deviation. Please refer to Enpirion's Output Ripple Measurement application note for more accurate ripple measurements (www.altera.com/enpirion).

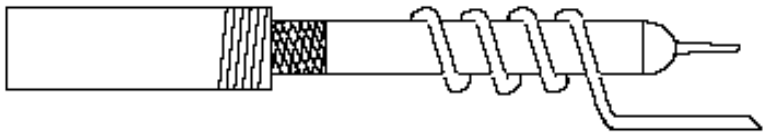


Figure – 6 : Low-loop-inductance Oscilloscope Probe

4. The board includes a 10k pull-up for the POK signal and ready to monitor the power OK status.
5. A 15nF soft-start capacitor is populated on the board for ~1msec soft-start time.
6. Please consult Altera Power Applications support if you are planning to perform any special EMI or noise measurements on this evaluation board.

Input and Output Capacitors

The **input** capacitance requirement is between 20-50uF for the EN5364QI. The voltage rating should be high enough to provide adequate margin for your application. This evaluation board is populated with 2x22uF, 1206, X5R capacitors.

The **output** capacitance requirement is approximately 50uF at the voltage sensing point. The board is populated with a 47uF, 1206, X5R and a 10uF, 0805, X7R capacitor.

NOTE: Capacitors must be X5R or X7R dielectric formulations to ensure adequate capacitance over operating voltage and temperature ranges.

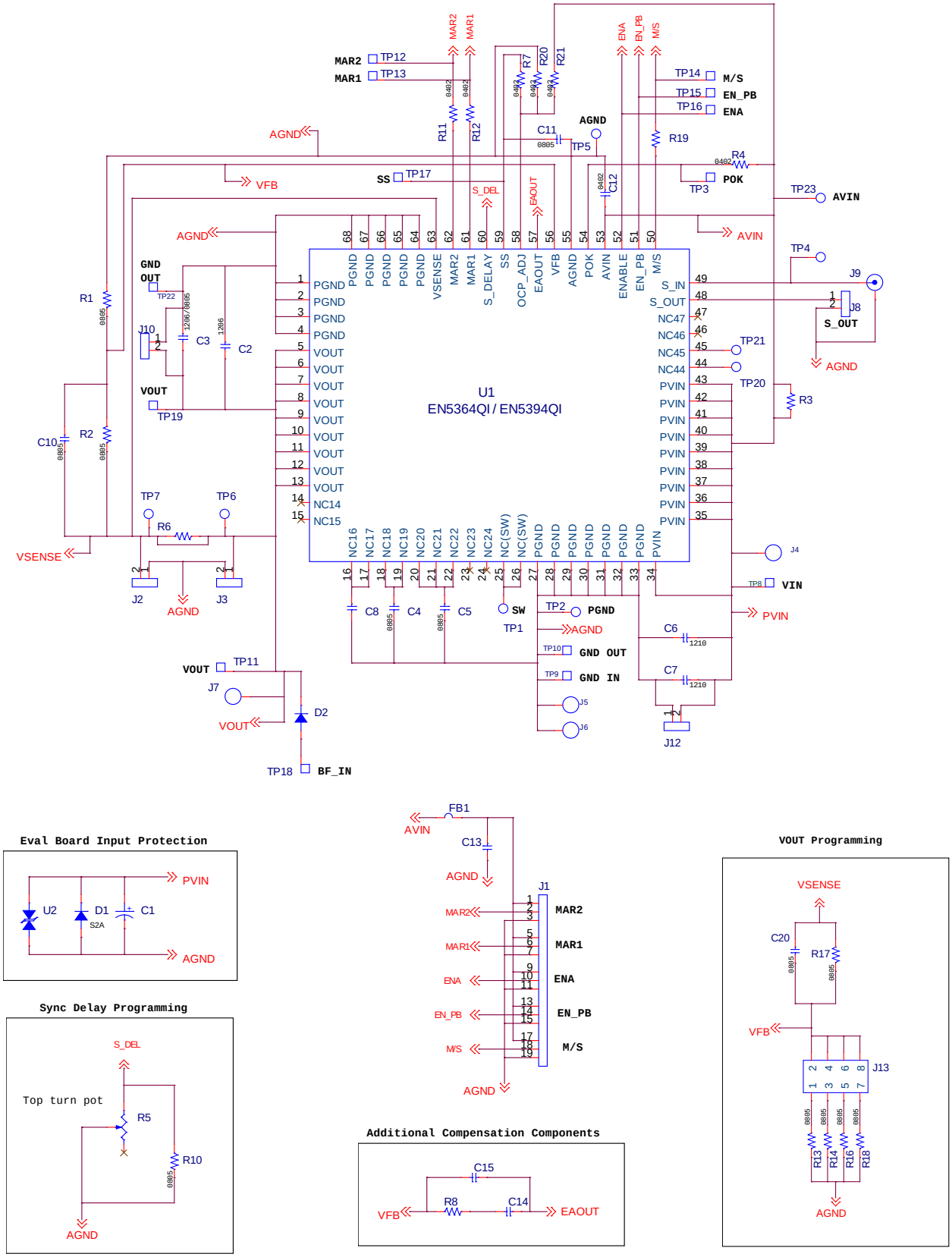


Figure – 7 : Evaluation Board Schematic

Bill of Materials

Designator	Qty	Description
C1	1	CAP, SMT ELECTROLYTIC, 150UF, 20%, 10V
C2	1	CAP, CER 47UF 10V X5R 1206
C3, C13	2	CAP, 10UF 0805 X7R 10% 10V CERAMIC
C6, C7	2	CAP, CER 22UF 10V X5R 1206
C20	1	CAP, CERAMIC 33PF 50V NP0 0805
C11	1	CAP, 15000PF 10% 50V SMD 0805 X7R CERAMIC
C4, C5, C8, C10, C12, C14, C15, J9 R1-R3, R5-R8, R20, R21	17	NOT USED
D1, D2	2	S2A DIODE
FB1	1	MULTILAYER SMD FERRITE BEAD 4000MA 0805 L=TYPICAL (NOT GUARANTED)
J1	1	CONNECTOR, CUSTOM, VERTICAL HEADER, SMT
J4-J7	4	BANANA JACK
J13	1	CONNECTOR HEADER 8 POS .100" STR TIN
R10	1	RES 49.9K OHM 1/8W 1% 0805 SMD
R13	1	RES 442K OHM 1/8W 0.1% 0805
R14	1	RES 226K OHM 1/8W 0.1% 0805
R16, R17	2	RES 150K OHM 1/8W 0.1% 0805 SMD
R18	1	RES 75.0K OHM 1/8W 0.1% 0805 SMD
R4, R11, R12. R19	4	10K 1% 1/8W 1% 0805 CHIP RESISTOR
TP3, TP8-TP19, TP22	14	TEST POINT SURFACE MOUNT
U1	1	EN5364 6A QFN
U2	1	TRANSIENT VOLTAGE SUPPRESSOR, 6.5V, BIDIRECTIONAL, SMT

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